DESIGNING OF SPI(SERIAL PERIPHERAL INTERFACE) MASTER

TANYA TYAGI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INDIRA GANDHI DELHI TECHNICAL UNIVERSITY FOR WOMEN

DELHI, INDIA

tanyatyagi35@gmail.com

***Abstract*— This paper presents the designing of SPI(serial peripheral interface) master of master-slave interface which basically provides a full duplex and synchronous communication between master and slave. Data transmitted/ received by master/slave is synchronized on rising or falling edge of the clock.**

Keywords—clock polarity, clock phase, MISO, MOSI, full duplex, chip select signal, Modes of SPI communication and SPI clock

I. DESCRIPTION

A) SPI INTERFACE

The master-slave interface communication occur using four signals :

1. SCLK (SPI serial Clock)
2. CS (Chip Select)
3. MOSI (Master Out Slave In)
4. MISO (Master In Slave Out)

SPI serial clock generating device is known as master. This clock is used to synchronize the data transmission between master and slave. Multiple slaves can be connected to single master node. The CS signal (active low signal) generated by master is used to select a particular slave node. This signal is made high to unselect the particular slave.

B) DATA TRANSMISSION PROCEDURE

MOSI data line is used to transmit the data from master to slave and MISO data line is used to transmit the data form slave to master. SPI provides full duplex communication between master-slave I.e., both can send data at the same time using MOSI and MISO data lines. The simultaneous transmission and reception of data during SPI communication is being synchronized by serial clock (SCLK) edge which synchronizes the sampling and shifting of data. During transmission, data is shifted serially out onto the MOSI bus and during reception, the data is sampled from the data on MISO bus.

In our design, we have used a tx_buffer and rx_buffer for master which contains number of slots equal to that of the number of bits in transmitted/received data. Then in rx_buffer for each rising or falling clock edge, we will sample the data from MISO line and then store it in the rx_buffer and the whenever next new bit is sampled, we will first right/left shift the contents of buffer in order to accommodate new bit.

C) FOUR MODES OF SPI COMMUNICATION

MODE 0: CPOL=0 & CPHA=0

MODE 1: CPOL=0 & CPHA=1

MODE 2: CPOL=1 & CPOL=0

MODE 3: CPOL=1 & CPHA=1

Where CPOL denotes clock polarity and CPHA denotes clock phase.

CPOL=0 indicates that polarity of clock signal in idle state is logic low.

CPOL=1 indicates that polarity of clock signal in idle state is logic high.

CPHA=0 indicates that the rising edge of the clock is used to sample the data and falling edge of clock is used to shift out the data.

CPHA=1 indicates that the falling edge of the clock is used to sample the data and rising edge of clock is used to shift out the data.

II. WAVEFORMS

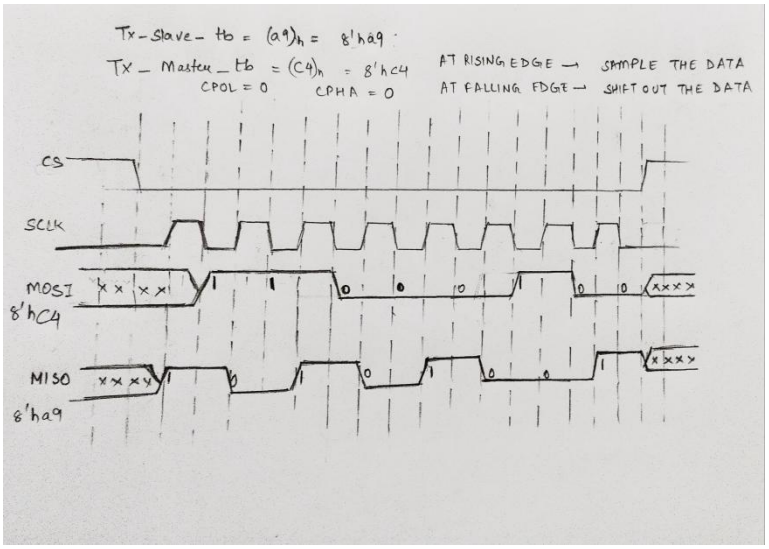

Figure1*:Waveforms obtained for master-slave SPI communication.*

REFERENCES

1. introduction to SPI interface by Analog Devices

(https://www.analog.com/media/en/analog-dialogue/volume-52/number-3/introduction-to-spi-interface.pdf)

2. https://github.com/nandland/spi-master