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11

Microelectronics Packaging

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11.1 Introduction

Packaging of electronic circuits is the science and the art of establishing interconnections and a suitable operating environment for predominantly electrical circuits. It supplies the chips with wires to distribute signals and power, remove the heat generated by the circuits, and provides them with physical support and environmental protection. It plays an important role in determining the performance, cost, and reliability of the system. With the decrease in feature size and increase in the scale of integration, the delay in on-chip circuitry is now smaller than that introduced by package. Thus, the ideal package would be one that is compact, and should supply the chips with a required number of signal and power connections, which have minute capacitance, inductance, and resistance. The package should remove the heat generated by the circuits. Its thermal properties should match well with semiconductor chip to avoid stress-induced cracks and failures. The package should be reliable, and it should cost much less than the chips it carries[1] (See Table 11.1).

TABLE 11.1 Electronic Packaging Requirements

Speed	Size
• Large bandwidth	• Compact size
• Short inter-chip propagation delay	
Thermal & Mechanical	Test & Reliability
• High heat removal rate	• Easy to test
• A good match between the thermal coefficients of the dice and the chip carrier	• Easy to modify • Highly reliable • Low cost
Pin Count & Wireability	Noise
• Large I/O count per chip	• Low noise coupling among wires
• Large I/O between the first and second level package	• Good-quality transmission line • Good power distribution

11.2 Packaging Hierarchy

The semiconductor chip is encapsulated into a package, which constitutes the first level of packaging. A printed circuit board is usually employed because the total circuit and bit count required might exceed that available on a single first-level package. Further, there may be components that cannot be readily integrated on a chip or first-level package, such as capacitors, high power resistors, inductors, etc. Therefore, as a general rule, several levels of packaging will be present. They are often referred to as a packaging hierarchy. The number of levels within a hierarchy may vary, depending on the degree of integration and the totality of packaging needs[2] (see Fig. 11.1).

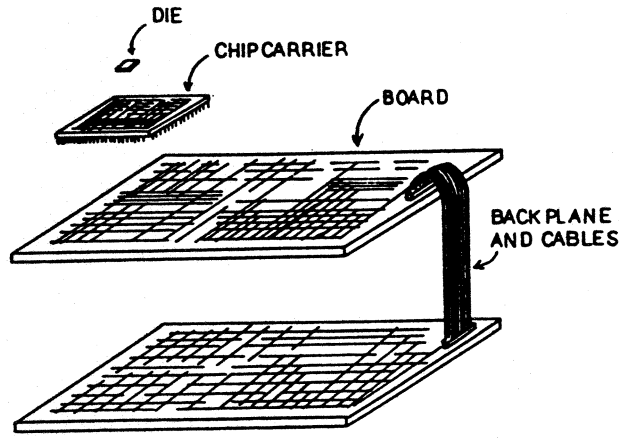


FIGURE 11.1 Packaging hierarchy of a hypothetical digital computer.

In the past, the packaging hierarchy contained more levels. Dies were mounted on individual chip carriers, which were placed on a printed circuit board. Cards then plugged into a larger board, and the boards were cabled into a gate. Finally, the gates were connected to assemble the computer. Today, higher levels of integration make many levels of packaging unnecessary, and this improves the performance, cost, and reliability of the computers. Ideally, all circuitry one day may be placed on a single piece of semiconductor. Thus, packaging evolution reflects the integrated circuits progress.[3,4]

11.3 Package Parameters

A successful package design will satisfy all given application requirements at an acceptable design, manufacturing, and operating expense. As a rule, application requirements prescribe the number of logic

circuits and/or bits of storage that must be packaged, interconnected, supplied with electric power, kept within a proper temperature range, mechanically supported, and protected against the environment. Thus. IC packages are designed to accomplish the following three basic functions[5]:

- Enclose the chip within a protective envelope to protect it from the external environment
- Provide electrical connection from chip to circuit board
- Dissipate heat generated by the chip by establishing a thermal path from a semiconductor junction to the external environment

To execute these functions, package designers start with a fundamental concept and, using principles of engineering, material science, and processing technology, create a design that encompasses:

1. Low lead capacitance and inductance
2. Safe stress levels
3. Material compatibility
4. Low thermal resistance
5. Seal integrity
6. High reliability
7. Ease of manufacture
8. Low cost

Success in performing the functions outlined depends on the package design configuration, the choice of encapsulating materials, and the operating conditions.[6,7] Package design is driven by performance, cost, reliability, and manufacturing considerations. Conflicts between these multiple criteria are common. The design process involves many tradeoff analyses and the optimization of conflicting requirements.

While designing the package for an application, the following parameters are considered.

Number of Terminals

The total number of terminals at packaging interfaces is a major cost factor. Signal interconnections and terminals constitute the majority of conducting elements. Other conductors supply power and provide ground or other reference voltages.

The number of terminals supporting a group of circuits is strongly dependent on the function of this group. The smallest pinout can be obtained with memory ICs because the stream of data can be limited to a single bit. Exactly the opposite is the case with groups of logic circuits which result from a random partitioning of a computer. The pinout requirement is one of the key driving parameters for all levels of packaging: chips, chip carriers, cards, modules, cables, and cable connectors.

Electrical Design Considerations

Electrical performance at the IC package level is of great importance for microwave designs and has gained considerable attention recently for silicon digital devices due to ever-increasing speed of today's circuits and their potentially reduced noise margins.[8] As a signal propagates through the package, it is degraded due to reflections and line resistance. Controlling the resistance and the inductance associated with the power and ground distribution paths to combat ground bounce and the simultaneous switching noise has now become essential. Controlling the impedance environment of the signal distribution path in the package to mitigate the reflection-related noise is becoming important. Reflections, in addition, cause an increase in the transition time, and may split the signal into two or more pulses with the potential of causing erroneous switching in the subsequent circuit and thus malfunction of the system. Controlling the capacitive coupling between signal traces in the signal distribution path to reduce crosstalk is gaining importance. Increased speed of the devices demands that package bandwidth be increased to reduce undue distortion of the signal. All these criteria are related through geometric variables, such as conductor cross-section and length, dielectric thickness, and the dielectric constant of the packaging body. These problems are usually handled with transmission line theory.[9]

Thermal Design Considerations

The thermal design objective is to keep the operating junction temperature of a silicon chip low enough to prevent triggering the temperature-activated failure mechanisms. Thus, the package should provide a good medium for heat transfer from junction to the ambient/heat sink. It is generally recommended to keep the junction temperature below 150°C to ensure proper electrical performance and to contain the propensity to fail.[10,11]

Thermal expansion caused by heating up the packaging structure is not uniform — it varies in accordance with the temperature gradient at any point in time and with the mismatches in the thermal coefficient of expansion. Mechanical stresses result from these differences and are one of the contributors to the finite lifetime and the failure rate of any packaging structure.[12]

In a simplistic heat transfer model of a packaged chip, the heat is transferred from the chip to the surface of the package by conduction, and from the package surface to the ambient by convection and radiation.[13,14] Typically, the temperature difference between the case and ambient is small, and hence radiation can be neglected. This model also neglects conduction heat transfer out of the package terminals, which can become significant. A multilayer example, which models the heat transfer from a region in the silicon device to the ambient, is shown in Fig. 11.2. The total thermal resistance from the junction to the ambient is given by:

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa} \tag{11.1}$$

The resulting junction temperature, assuming a power dissipation of P_d, is

$$T_j = P_d(R_{\theta jc} + R_{\theta cs} + R_{\theta sa}) + T_a \tag{11.2}$$

in analogy with electric circuits. If there are parallel paths for heat flow, the thermal resistances are combined in exactly the same manner as electrical resistors in parallel.

$R_{\theta cs}$, the conductive thermal resistance, is mainly a function of package materials and geometry. With the higher power requirements, one must consider the temperature dependence of materials selected in design. T_j depends on package geometry, package orientation in the application, and the conditions of the ambient in the operating environment. The heat sink is responsible for getting rid of the heat of the environment by convection and radiation. Because of all the many heat transfer modes occurring in a finned heat sink, the accurate way to obtain the exact thermal resistance of the heat sink would be to measure it. However, most heat sink manufactures today provide information about their extrusions concerning the thermal resistance per unit length.

Reliability

The package should have good thermomechanical performance for better reliability. A variety of materials of widely differing coefficients of thermal expansion (CTEs) are joined to create interfaces. These interfaces are subject to relatively high process temperatures and undergo many temperature cycles in their useful life as the device is powered on and off. As a result, residual stresses are created in the interfaces. These stresses cause reliability problems in the packages.[15,16]

Testability

Implicit in reliability considerations is the assumption of a flawless product function after its initial assembly — a zero defect manufacturing. Although feasible in principle, it is rarely practiced because of the high costs and possible loss of competitive edge due to conservative dimensions, tolerances, materials, and process choices. So, several tests are employed to assess the reliability of the packages.[17,18]

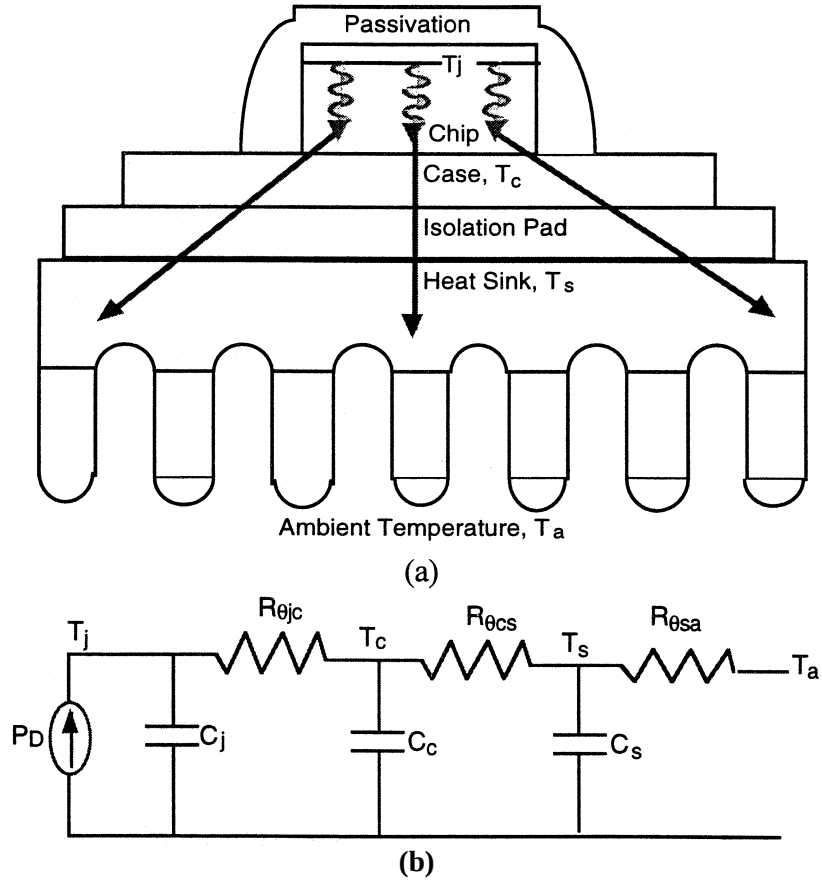


FIGURE 11.2 Steady-state heat flow and thermal resistance in a multilayer structure (a) path of heat flow; (b) equivalent electrical circuit based on thermal resistance.

11.4 Packaging Substrates

An IC package falls into two basic categories. In the first, a single-layer type, the package is constructed around the IC chip on a lead frame. In the second, a multilayer type, the IC chip is assembled into a prefabricated package.

In a single-layer technology, the IC chip is first mechanically bonded to a lead frame, and then electrically interconnected with fine wires from the chip bond pads to the corresponding lead-frame fingers. The final package is then constructed around the lead-frame subassembly. Two single-layer technologies are used in the industry: molded plastic and glass-sealed pressed ceramic.

Plastic Packaging

Plastic is a generic term for a host of man-made organic polymers. Polymer materials are relatively porous structures, which may allow absorption or transport of water molecules and ions.[19] The aluminum metallization is susceptible to rapid corrosion in the presence of moisture, contaminants, and electric fields. So, plastic packages are not very reliable. Impurities from the plastic or other materials in the construction of the package can cause threshold shifts or act as catalysts in metal corrosion. Fillers can also affect reliability and thermal performance of the plastic package.

Ceramic Packaging

Pressed ceramic technology packages are used mainly for economically encapsulating ICs and semiconductor devices requiring hermetic seals. Hermeticity means that the package must pass both gross and fine leak tests and also exclude environmental contaminants and moisture for a long period of time. Further, any contaminant present before sealing must be removed to an acceptable level before or during the sealing process.[20] Silicon carbide (SiC), aluminum nitride, beryllia (BeO), and alumina (Al_2O_3) are some of the ceramics used in electronic packaging. In comparison with other ceramics, SiC has a thermal expansion coefficient closer to silicon, and as a result less stress is generated between the *dice* and the substrate during temperature cycling. In addition, it has a very high thermal conductivity. These two properties make SiC a good packaging substrate and a good heat sink that can be bonded directly to silicon *dice* with little stress generation at elevated temperatures. Its high dielectric constant, however, makes it undesirable as a substrate to carry interconnections. Alumina and BeO have properties similar to SiC.[21]

TABLE 11.2A Thermal and Electrical Properties of Materials Used in Packaging

Metals	Coefficient of Thermal Expansion (CTE) (10^{-6} K^{-1})	Thermal Conductivity (W/cm-K)	Specific Electrical Resistance $10^{-6}\Omega$-cm
Aluminum	23	2.3	2.8
Silver	19	4.3	1.6
Copper	17	4.0	1.7
Molybdenum	5	1.4	5.3
Tungsten	4.6	1.7	5.3

Insulating Substrates	Coefficient of Thermal Expansion (CTE) (10^{-6} K^{-1})	Thermal Conductivity (W/cm-K)	Dielectric Constant
Alumina (Al_2O_3)	6.0	0.3	9.5
Beryllia (BeO)	6.0	2.0	6.7
Silicon carbide (SiC)	3.7	2.2	42
Silicon dioxide (SiO_2)	0.5	0.01	3.9

Semiconductors	Coefficient of Thermal Expansion (CTE) (10^{-6} K^{-1})	Thermal Conductivity (W/cm-K)	Dielectric Constant
Silicon	2.5	1.5	11.8
Germanium	5.7	0.7	16.0
Gallium arsenide	5.8	0.5	10.9

TABLE 11.2B Some Properties of Ceramic Packaging Materials

Property	BeO	AlN	Al_2O_3 (96%)	Al_2O_3 (99.5%)
Density (g/cm^3)	2.85	3.28	3.75	3.8
CTE (ppm/K)	6.3	4.3	7.1	7.1
TC (W/cm-K)	285	180	21	25.1
Dielectric const.	6.7	10	9.4	10.2
Loss tangent	0.0001	0.0005	0.0001	0.0001

11.5 Package Types

IC packages have been developed over time to meet the requirements of high speed and density. The history of IC package development has been the continuous battle to miniaturize.[22,23] Figure 11.3 illustrates the size and weight reduction of IC package over time.

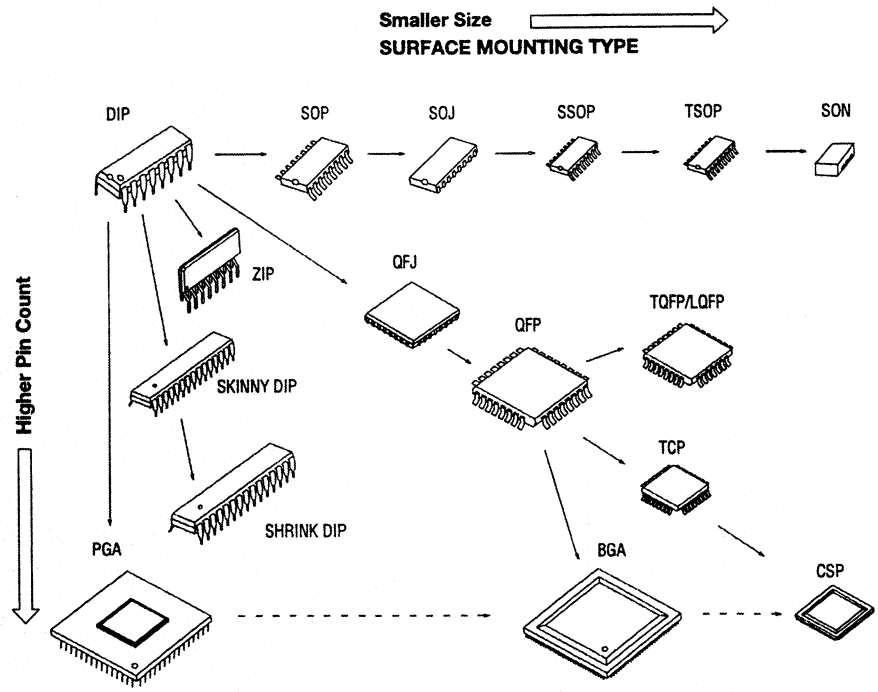


FIGURE 11.3 Packaging trends.

Several packages can be classified as follows.

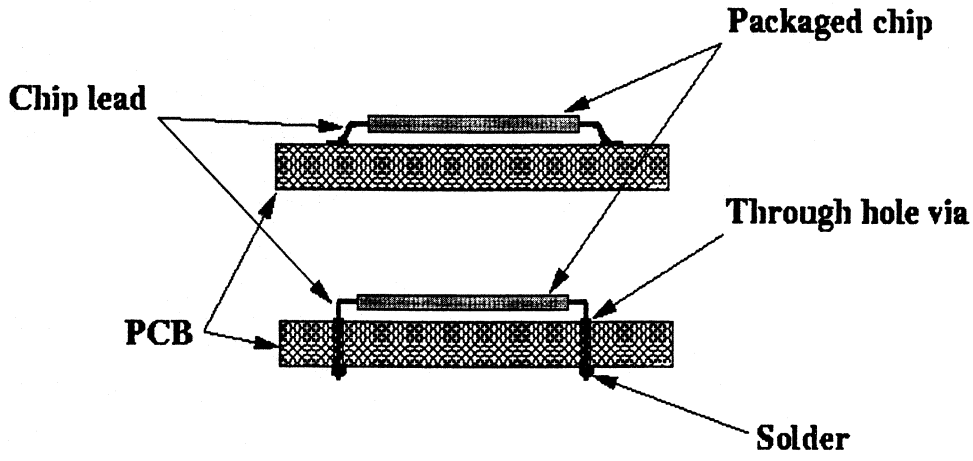
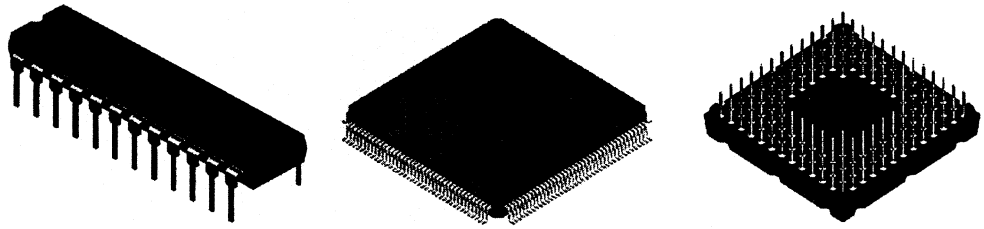


FIGURE 11.4 A generic schematic diagram showing the difference between the surface-mount technology (upper) and through hole mounting (lower).

Through Hole Packages

Through-the-board hole mounting technology uses precision holes drilled through the board and plated with copper. This copper plating forms the connections between separate layers. These layers consist of thin copper sheets stacked together and insulated by epoxy fiberglass. There are no dedicated via structures to make connections between wiring levels; through holes serve that purpose. Through holes form a sturdy support for the chip carrier and resist thermal and mechanical stresses caused by the variations in the expansions of components at raised temperatures. Different types (see Fig. 11.5) of through hole packages can be further classified as:



(a) Dual in-line package (DIP). **(b) Quad flat package (QFD).** **(c) Pin grid array package (PGA).**

FIGURE 11.5 Different through mount packages.

Dual-in-Line Packages (DIPs)

A dual-in-line package is a rectangular package with two rows of pins in its two sides. Here, first the die is bonded on the lead frame and in the next step, chip I/O and power/ground pads are wire-bonded to the lead frame, and the package is molded in plastic. DIPs are the workhorse of the high-volume and general-purpose logic products.

Quad Flat Packages (QFPs)

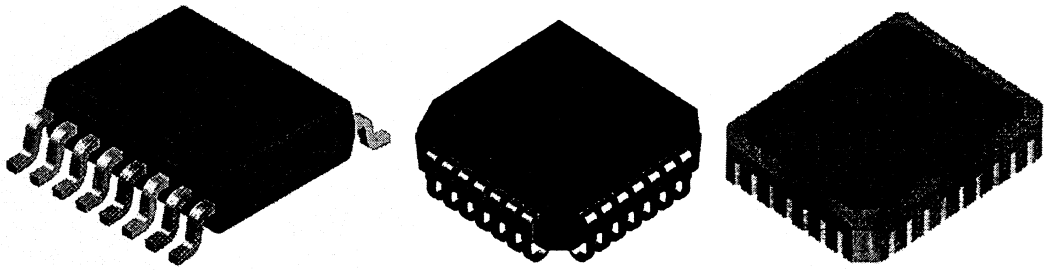
With the advances in VLSI technology, the lower available pin counts of the rectangular DIP became a limiting factor. With pins spaced 2.4 mm apart on only two sides of the package, the physical size of the DIP has become too great. On the other hand, the physical size of an unpackaged microelectronic circuit (bare die) has been reduced to a few millimeters. As a result, the DIP package has become up to 50 times larger than the bare die size itself, thus defeating the objective of shrinking the size of the integrated circuits. So, one solution is to provide pins all around. In QFPs, pins are provided on all four sides. Thin QFPs are developed to reduce the weight of the package.

Pin Grid Arrays (PGA)

A pin grid array has leads on its entire bottom surface rather than only at its periphery. This way it can offer a much larger pin count. It has cavity-up and cavity-down versions. In a cavity-down version, a die is mounted on the same side as the pins facing toward the PC board, and a heat sink can be mounted on its backside to improve the heat flow. When the cavity and the pins are on the same side, the total number of pins is reduced because the area occupied by the cavity is not available for brazed pins. The mounting and wire bonding of the dice are also more difficult because of the existence of the pins next to the cavity. High pin count and larger power dissipation capability of PGAs make them attractive for different types of packaging.

Surface-Mounted Packages

Surface mounting solves many of the shortcomings of through-the-board mounting. In this technology, a chip carrier is soldered to the pads on the surface of a board without requiring any through holes. The smaller component sizes, lack of through holes, and the possibility of mounting chips on both sides of the PC board improve the board density. This reduces package parasitic capacitances and inductances associated with the package pins and board wiring. Various types of surface-mount packages are available on the market and can be divided into the following categories (see Fig. 11.6):



(a) Small outline package (SOP). (b) Plastic-leaded chip carriers (PLCC). (c) Leadless ceramic chip carriers (LCCC).

FIGURE 11.6 Different surface-mount packages.

Small-Outline Packages (SOPs)

The small-outline package has gull-wing shaped leads. It requires less pin spacing than through-hole-mounted DIPs and PGAs. SOP packages usually have small lead counts and are used for discrete, analog, and SSI/MSI logic parts.

Plastic-leaded Chip Carriers (PLCCs)

Plastic-leaded chip carriers, such as gull-wing and J-leaded chip carriers, offer higher pin counts than SOP. J-leaded chip carriers pack denser and are more suitable for automation than gull-wing leaded carriers because their leads do not extend beyond the package.

Leadless Ceramic Chip Carriers (LCCCs)

Leadless ceramic chip carriers take advantage of multilayer ceramic technology. The conductors are left exposed around the package periphery to provide contacts for surface mounting. *Dice* in leadless chip carriers are mounted in cavity-down position, and the back side of the chip faces away from the board, providing a good heat removal path. The ceramic substrate also has a high thermal conductivity. LCCCs are hermetically sealed.

Flip-Chip Packages

The length of the electrical connections between the chip and the substrate can be minimized by placing solder bumps on the *dice*, flipping the chips over, aligning them with the contacts pads on the substrate, and reflowing the solder balls in a furnace to establish the bonding between the chips and the package. This method provides electrical connections with minute parasitic inductance and capacitance. In addition, contact pads are distributed over the entire chip surface. This saves silicon area, increases the maximum I/O and power/ground terminals available with a given die size, and provides more efficiently routed signal and power/ground interconnections on the chips.[24] (see Fig. 11.7.)

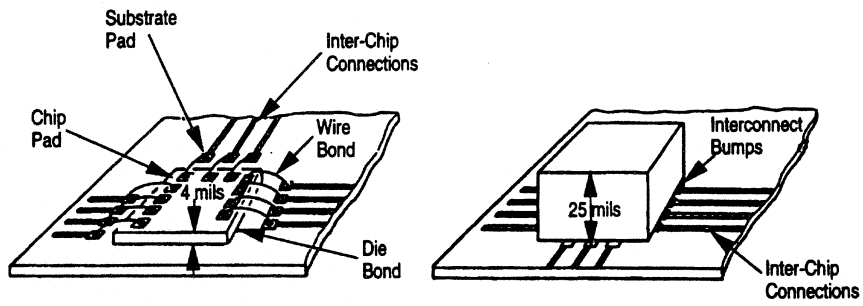


FIGURE 11.7 Flip-chip package and its interconnections.

Chip Size Packages (CSPs)

To combine the advantages of both packaged chip and bare chip in one solution, a variety of CSPs have been developed.[25,26] CSPs can be divided into two categories: the fan-in type and the fan-out type.

Fan-in type CSPs are suitable for memory applications that have relatively low pin counts. This type is further divided into two types, depending on the location of bonding pads on the chip surface; these are the center pad type and the peripheral pad type. This type of CSP keeps all the solder bumps within the chip area by arranging bumps in area array format on the chip surface.

The fan-out CSPs are used mainly for logic applications: because of the die size to pin count ratio, the solder bumps cannot be designed within the chip area.

Multi-Chip Modules (MCMs)

In a multi-chip module, several chips are supported on a single package. Most multi-chip packages are made of ceramic. By eliminating one level of packaging, the inductance and capacitance of the electrical connections among the *dice* are reduced. Usually, the *dice* are mounted on a multilayer ceramic substrate via solder bumps, and the ceramic substrate offers a dense interconnection network.[27,28] (See Fig. 11.8.) There are several advantages of multi-chip modules over single-chip carriers. The multi-chip module minimizes the chip-to-chip spacing and reduces the inductive and capacitive discontinuities between the chips mounted on the substrate by replacing the die-bump-interconnect-bump-die path. In addition, narrower and shorter wires on the ceramic substrate have much less capacitance and inductance than the PC board interconnections.

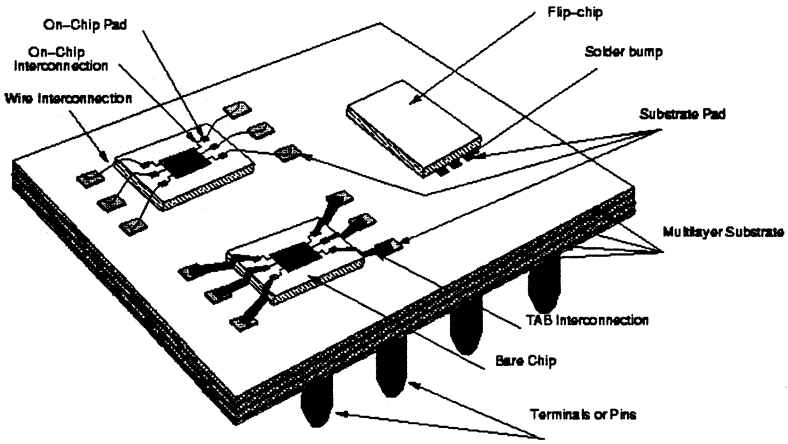


FIGURE 11.8 A generic schematic diagram of an MCM, showing how bare *dice* are interconnected to an MCM substrate using different interconnection technologies.

3-D VLSI Packaging

The driving forces behind the development of three-dimensional packaging technology are similar to the multi-chip module technology, although the requirements for the 3-D technology are more aggressive. These requirements include the need for significant size and weight reductions, higher performance, small delay, higher reliability, and potentially reduced power consumption.

Silicon-on-Silicon Hybrid

A silicon substrate can also be used as an interconnection medium to hold multi-chips as an alternative to ceramic substrates. This is called silicon-on-silicon packaging or, sometimes, hybrid wafer-scale

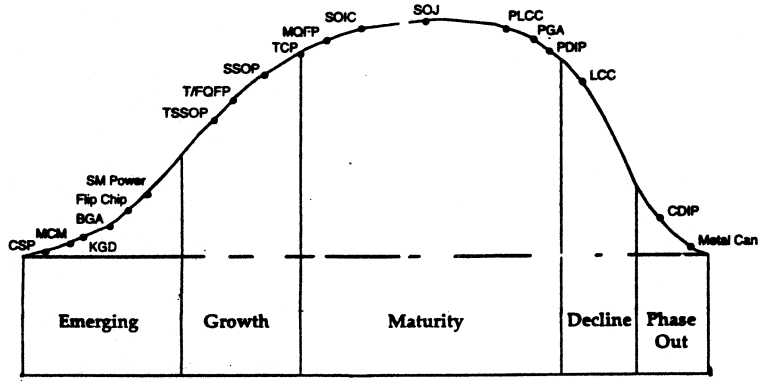


FIGURE 11.9 IC packaging life cycle.

integration. Thin-film interconnections are fabricated on a wafer and separately processed, and test dice are mounted on this silicon substrate via wire bonding, TAB, or solder bumps. Using this technique, chips fabricated in different technologies can be placed on the same hybrid package. The silicon substrate can also potentially contain active devices that serve as chip-to-chip drivers, bus and I/O multiplexers, and built-in test circuitry.[29]

11.6 Hermetic Packages

In hermetic packages, the packaged cavity is sealed in such a way that all external chemical species are permanently prevented from entering into it. In practice, however, a finite rate of leakage occurs through diffusion and permeation. Moisture is the principal cause of device failures. Moisture by itself does not cause electronic problems when trapped in an electronic package, because it is a poor electrical conductor. However, water can dissolve salts and other polar molecules to form an electrolyte, which together with the metal conductors and the potential difference between them, can create leakage paths as well as corrosion problems. Moisture is contributed mainly by the sealing ambient, the absorbed and dissolved water from the sealing materials, lid and the substrate and the leakage of external moisture through the seal. No material is truly hermetic to moisture. The permeability to moisture of glasses, ceramics, and metals, however, is very low and is orders of magnitude lower than for any plastic material. Hence, the only true hermetic packages are those made of metals, ceramics, and glasses. The common feature of hermetic packages is the use of a lid or a cap to seal in the semiconductor device mounted on a suitable substrate. The leads entering the package also need to be hermetically sealed.

11.7 Die Attachment Techniques

To provide electrical connections between the chip pads and package, different bonding techniques are used. These can be classified as follows.

Wire Bonding

Wire bonding (see Fig. 11.10) is a method used to connect a fine wire between an on-chip pad and a substrate pad. This substrate may simply be the ceramic base of a package or another chip. The common materials used are gold and aluminum. The main advantage of wire bonding technology is its low cost; but it cannot provide large I/O counts, and it needs large bond pads to make connections. The connections have relatively poor electrical performance.

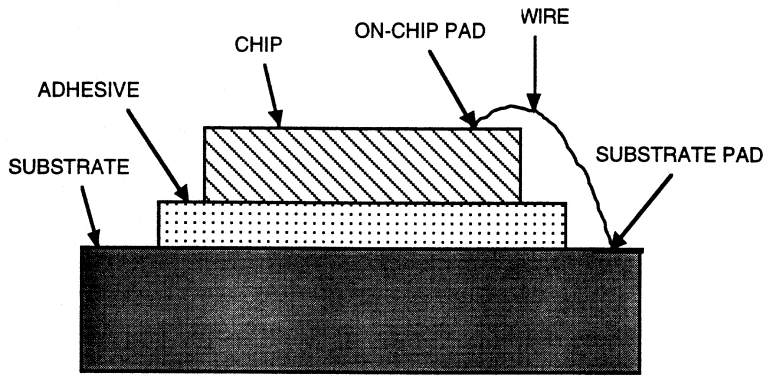


FIGURE 11.10 Wire bonding assembly.

Tape-Automated Bonding

In tape-automated bonding (TAB) technology, a chip with its attached metal films is placed on a multilayer polymer tape. The interconnections are patterned on a multilayer polymer tape. The tape is positioned above the "bare die" so that the metal tracks (on the polymer tape) correspond to the bonding sites on the die (Fig. 11.11). TAB technology provides several advantages over wire bonding technology. It requires a smaller bonding pad, smaller on-chip bonding pitch, and a decrease in the quantity of gold used for bonding.[30] It has better electrical performance, lower labor costs, higher I/O counts and lighter weight, greater densities, and the chip can be attached in a face-up or face-down configuration. TAB technology includes time and cost of designing and fabricating the tape and the capital expense of the TAB bonding equipment. In addition, each die must have its own tape patterned for its bonding configuration. Thus, TAB technology has typically been limited to high-volume applications.

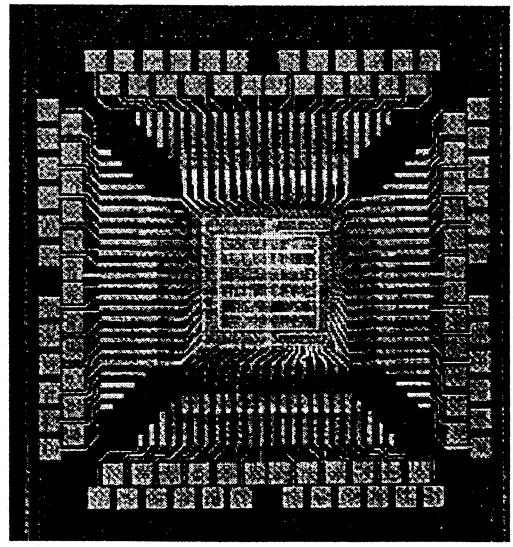


FIGURE 11.11 Tape-automated bonded die.

Solder Bump Bonding

Solder bumps are small spheres of solder (solder balls) that are bonded to contact areas or pads of semiconductor devices and subsequently used for face-down bonding. The length of the electrical

connections between the chip and the substrate can be minimized by placing solder bumps on the die, flipping the die over, aligning the solder bumps with the contact pads on the substrate, and re-flowing the solder balls in a furnace to establish the bonding between the die and the substrate[31] (Fig. 11.12). This technology provides electrical connections with minute parasitic inductances and capacitances. In addition, the contact pads are distributed over the entire chip surface rather than being confined to the periphery. As a result, the silicon area is used more efficiently, the maximum number of interconnects is increased, and signal interconnections are shortened. But this technique results in poor thermal conduction, difficult inspection of the solder bumps, and possible thermal expansion mismatch between the semiconductor chips and the substrate.

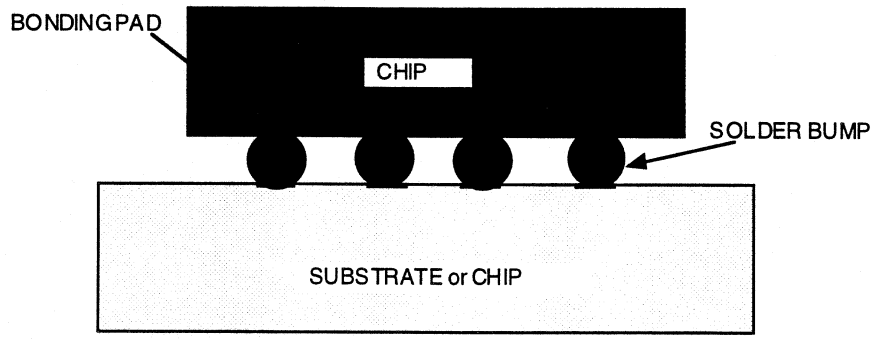


FIGURE 11.12 Flip-chip method using solder bumps.

11.8 Package Parasitics

Typically, the electrical interconnection of a chip in a package consists of chip-to-substrate interconnect, metal runs on the substrate, and finally, pins from the package. Associated with these are the electrical resistance, inductance and capacitance — referred to as package parasitics. The electrical parasitics are determined by the physical parameters such as interconnect width, thickness, length, spacing, and resistivity; by the thickness of the dielectric; and by the dielectric constant.

Resistance refers to both dc and ac. The dc resistance of an interconnect is a property of its cross-sectional area, length, and material resistivity. In addition, the ac resistance depends on the frequency of the signal and is higher than the dc resistance because of the skin effect. Resistance in the power distribution path results in attenuation of input signals to the device and output signals from the device. This has the effect of increasing the path delay.

Capacitance of an interconnect is a property of its area, the thickness of the dielectric separating it from the reference potential, and the dielectric constant of the dielectric. It is convenient to consider this as two parts: capacitance with respect to ground, and capacitance with respect to other interconnections. The capacitance with respect to ground is referred to as the *load capacitance*. This is seen as part of the load by the output driver and thus can slow down the rise time of the driver. Interlead capacitance couples the voltage change on the active interconnect to the quiet interconnect.[32] This is referred to as *crosstalk*.

Inductance can be defined only if the complete current path is known. In the context of component packages, the inductance of an interconnect should be understood as part of a complete current loop. Thus, if the placement of the package in the system alters the current path in the package, the package inductance will vary. Total inductance consists of self-inductance and mutual inductance. Mutual inductance between two interconnects generates a voltage in one when there is current change in the other. Inductive effects are the leading concern in the design of power distribution path in high-performance packages. They are manifested as “ground bounce” noise and “simultaneous switching” noise.

11.9 Package Modeling

As the complexity of devices increases, design and development efforts for packages become comparable to design and development efforts for chips. Many package design concepts must be simulated to assess their associated performance parameters.[33,34] Computer-aided design software and test chips are becoming indispensable design tools. Computer-aided design tools are extensively used to analyze the thermal, thermomechanical, mechanical, and electrical parameters of packages[35]; for example, electrical modeling extracts an equivalent electrical circuit that describes the physical structure of the package and, hence, the equivalent electrical circuit of the package can be used in circuit simulation programs to evaluate the overall performance of a packaged circuit. Until now, the equivalent electrical circuit incorporated only lumped electrical parameters; but as frequency of operation of the circuits is increasing, the distributed model of the package needs to be developed for high-frequency simulations.[36]

11.10 Packaging in Wireless Applications

Wireless applications typically involve RF, high-frequency digital, and mixed-mode circuits. Wireless packaging requires minimal electrical parasitic effects that need to be well-characterized.

In wireless applications, the trend is to integrate multiple modules on a single chip.[37] So, the thermal management of the whole chip becomes crucial. The IC package must have good thermal properties. Metal as a material shows optimal properties concerning thermal conductivity, electromagnetic shielding, mechanical and thermal stability. For thermal expansion, best match to semiconductor and ceramic material can be achieved with molybdenum, tungsten, or special composites like kovar. Ceramic materials are applied, both as parts of the package as well as for subsystem carrying RF transmission lines. To this end, and to provide electromagnetic shielding, these materials partly have to be metallized. Aluminum nitride, beryllia, aluminum silicon carbide, and CVD diamond show best thermal conductivity and are therefore applied in high-power applications,[38,39] while alumina is well known for standard microwave applications.[40]

Integration of passive components is a major challenge in wireless packages. More and more efforts are being made to integrate passive components, power devices on a chip with the other mixed signal circuits.[41] The size of the package becomes an issue. Micromachining technology provides a way to make miniature packages that conform to RF circuits, while providing physical and electrical shielding. Conformal packages made by applying micromachining technology provide the capability to isolate individual circuit elements and improve circuit performance by eliminating the radiation and cross-coupling between the adjacent circuits.[42,43]

At high frequencies, interconnections need to be carefully designed. Microstrip interconnects, coplanar waveguide are mostly used for microwave packaging.[44] Flip-chip packaging has tremendous potential for future RF packaging.[45]

11.11 Future Trends

Packaging is the bridge between silicon and electronics system. Packaging design and fabrication are increasingly important to system applications. Consideration of factors affecting waveform integrity for both power and signal (i.e., timing, cross-talk, and ground bounce) will affect device layout on the chip, chip layout on the package, and interconnect.

Conventional surface mount packages will dominate in the region of low pin count and low clock frequency. Ball-grid array packages and chip-scale packages will be used for medium pin counts. Technically bare chip solutions can cover the whole area, but have a reliability versus cost tradeoff. Bare chip solutions could be very competitive with packaged solutions, as they can accomplish very high density and very good electrical performance.

Packaging needs are driven as much by market application requirements as by silicon technology. Cost drives technology tradeoffs for all market segments. As the complexity of package technology continues to increase, new materials will be needed to meet design and performance challenges. Significant engineering development will be needed for power increases at each technology generation.

An integrated design environment of physical, electrical, thermal, thermo-mechanical, chip, package, and system design needs to be evolved. Most of these integrated solutions will provide modeling and simulation capabilities that will be embodied in packaging computer aided design systems. Design tools are required to manage the complexity of packaging that is being pushed to its performance limits.

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