Proposte di tesi in ambito architetture dei calcolatori

RISCV open source microprocessor enhancement // STMicroelectronics

Type: *thesis/stage* c.o. STMicroelectronics - Agrate Brianza

Description:

This research project is configured with the following design activities

- Evaluation of the RISCV microprocessor designed in the University of Berkeley, nowadays considered one of the most promising open source microprocessor.
- Extension of its basic instruction set (ISA) with a new group of digital signal processing and computer vision instructions to address new emerging IOT radios and deep learning applications.

The analysis of the new RISCV ISA will be performed at instruction abstraction level, the Chisel language could be one of the adopted solutions. The project can then be carried on in the hardware design phase if the candidate owns adequate skills and motivations.

Skills: microprocessor architectures — algorithms — knowledge for benchmarking — RTL coding — synthesis flow —

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Design of the next generation of STRED6 microprocessor-DSP // STMicroelectronics

Type: *thesis/stage* c.o. STMicroelectronics - Agrate Brianza

Description:

The consolidated trend in the digital design is described by the use of high performance and energy efficient microprocessors, used in single or multiple configurations, where the associated firmware defines the target system-on-chip functionality.

The STRED processor family is one of the key STMicroelectronics IP used in this set of advanced products. The new emerging applications require big changes in terms of performance in order to support advanced software defined radios and deep learning algorithms for computer vision.

The activity will be concentrated in the instruction set (ISA) upgrades and micro-architecture adjustment (pipeline).

The analysis of the new STRED6 ISA will be performed at instruction abstraction level. The project can then be completed with the hardware design.

Skills: microprocessor architectures — algorithms — deep learning architectures — RTL coding — synthesis flow —

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Definition of the next STREDL microprocessor for sensor processing // STMicroelectronics

Type: *thesis/stage* c.o. STMicroelectronics - Agrate Brianza

Description:

Every sensor is more and more associated to a close elaboration unit with the task to filter the data before the transmission to the next collection unit or the Cloud.

The next frontier is the adoption of neural network architectures, tightly coupled with the sensor, able to perform a first detection level of the retrieved information.

The STREDL microprocessor is one of the key STMicroelectronics IP planned to be used in the sensor domain.

Interacting with ST Deep Neural Network group the candidate should study and isolate the most promising net architectures for low power applications, suggest instruction set upgrades and micro-architecture adjustment.

The analysis of the new STREDL ISA will be performed at instruction abstraction level. The project can then be completed with the hardware design.

Skills: microprocessor architectures — algorithms — deep learning architectures — RTL coding — synthesis flow —

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