

POLITECNICO DI MILANO  
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THE TITLE

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This thesis has been developed  
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*Dedicato a tutti coloro che mi hanno voluto bene  
e che mi hanno sostenuto in questi anni.  
Grazie.*



# Sommario

*Abstract tradotto in italiano*



# **Abstract**

One page in english describing the summary of your work





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# Listings



# List of Abbreviations

<b>AES</b>	Advanced Encryption Standard
<b>ASIC</b>	Application-Specific Integrated Circuit
<b>AST</b>	Abstract Syntax Tree
<b>CAD</b>	Computer-Aided Design
<b>CASCA</b>	Countermeasure Against Side-Channel Attack
<b>CMOS</b>	Complementary Metal-Oxide Semiconductor
<b>CPA</b>	Correlation Power Analysis
<b>DAG</b>	Directed Acyclic Graph
<b>DES</b>	Data Encryption Standard
<b>DEMUX</b>	Demultiplexer
<b>DPA</b>	Differential Power Analysis
<b>DSL</b>	Domain-Specific Language
<b>DSEL</b>	Domain-Specific Embedded Language
<b>FHDL</b>	Functional Hardware Description Language
<b>FF</b>	Flip-flop
<b>FPGA</b>	Field Programmable Gate Array
<b>FSM</b>	Finite-State Machine
<b>GADT</b>	Generalized Algebraic Data Type



<b>GF</b>	Galois Field
<b>GE</b>	Gate Equivalent
<b>HD</b>	Hamming Distance
<b>HDL</b>	Hardware Description Language
<b>HOF</b>	Higher-Order Function
<b>HW</b>	Hamming Weight
<b>IC</b>	Integrated Circuit
<b>IP</b>	Intellectual Property
<b>LHS</b>	Left Hand Side
<b>LSB</b>	Least Significant Bit
<b>LUT</b>	Look-up Table
<b>MSB</b>	Most Significant Bit
<b>MPC</b>	Multi-Party Computation
<b>MUX</b>	Multiplexer
<b>REPL</b>	Read-Eval-Print Loop
<b>RHS</b>	Right Hand Side
<b>RTL</b>	Register-Transfer Level
<b>SAT</b>	Boolean Satisfiability Problem
<b>SCA</b>	Side-Channel Attack
<b>SMT</b>	Satisfiability Modulo Theories
<b>SNR</b>	Signal-to-Noise Ratio
<b>SPA</b>	Simple Power Analysis

# **Chapter 1**

## **Introduction**

Example of citation [1]



# Bibliography

- [1] N.I.S.T. Announcing the Advanced Encryption Standard (AES), November, 26 2001. Federal Information Processing Standards Publication, n. 197.





