Vittorio Zaccaria

CURRICULUM UPDATE - 2013 / 2019

Since 2013, I have expanded my interests to functional programming and domain specific languages with a focus on hardware synthesis. Recently (2017 and 2018) I have helped introduce some novel theoretical results in the field of cryptographic circuits which have been published on IEEE Transactions on Computers. In 2015 and 2017 I have been awarded with two grants from industrial partners for devising a reliable design methodology for cryptographic circuits protected against correlation power attacks.

GRANTS AS A PRINCIPAL INVESTIGATOR

- From 2017 to 2018 grant for **Metodologia e Strumenti per la Valutazione di Circuiti Crittografici** from STMicroelectronics, grant type: Grant from industrial partner,
- From 2015 to 2016 grant for **Strumenti di Progettazione e Verifica per Circuiti Crittografici** from STMicroelectronics, grant type: Grant from industrial partner

RESEARCH

Important publications from 2013

Spectral features of higher-order side-channel countermeasures. *V. Zaccaria, F. Melzani, G. Bertoni.* IEEE Transactions on Computers - 2018 -[Link]

CASCA: A Design Automation Approach for Designing Hardware Countermeasures Against Side-Channel Attacks. *L. Delledonne, V. Zaccaria, R. Susella, G. Bertoni, F. Melzani.* ACM Transactions on Design Automation of Electronic Systems (TODAES) - 2018 -[Link]

Symbolic analysis of higher-order side channel countermeasures. *E. Bisi, F. Melzani, V. Zaccaria.* IEEE Transactions on Computers - 2017 -[Link]

SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High-Level Synthesis. *S. Xydis, G. Palermo, V. Zaccaria, C. Silvano.* IEEE Transactions on Computer Aided Design of Integrated Circuits - 2015 -[Link]

DeSpErate++: An enhanced design space exploration framework using predictive simulation scheduling. *G. Mariani, G. Palermo, V. Zaccaria, C. Silvano.* IEEE Transactions on Computer Aided Design of Integrated Circuits - 2015 -[Link]

Design Space Exploration and Run-time Resource Management for Multi-cores. *G. Mariani, G. Palermo, V. Zaccaria, C. Silvano.* ACM Transactions on Embedded Computing Systems (TECS) - 2013 -[Link]

Other publications from 2013

Toward Truly Personal Chatbots: On the Development of Custom Conversational Assistants. *F. Daniel, M. Matera, V. Zaccaria, A. Dell'orto.* Proceedings of the 1st International Workshop on Software Engineering for Cognitive Services - 2018 -[Link]

Context-Aware Access to Heterogeneous Resources Through On-the-Fly Mashups. *F. Daniel, M. Matera, E. Quintarelli, L. Tanca, V. Zaccaria.* Advanced Information Systems Engineering - 30th International Conference, CAiSE 2018, Tallinn, Estonia, June 11-15, 2018, Proceedings - 2018 -[Link]

On the Role of Context in the Design of Mobile Mashups. *V. Cassani, S. Gianelli, M. Matera, R. Medana, E. Quintarelli, L. Tanca, V. Zaccaria.* Rapid Mashup Development Tools: Second International Rapid Mashup Challenge, RMC 2016, Lugano, Switzerland, June 6, 2016, Revised Selected Papers - 2016 -[Link]

Customization of OpenCL Applications for Efficient Task Mapping Under Heterogeneous Platform Constraints. *E. Paone, F. Robino, G. Palermo, V. Zaccaria, I. Sander, C. Silvano.* Proceedings of DATE 2015: International Conference on Design, Automation and Test in Europe - 2015 -[Link]

Combining application adaptivity and system-wide Resource Management on multi-core platforms. *G. Massari, E. Paone, P. Bellasi, G. Palermo, V. Zaccaria, W. Fornaciari, C. Silvano.* Proceedings of SAMOS 2014: XIVth International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation - 2014 -[Link]

OpenCL Application Auto-tuning and Run-Time Resource Management for Multi-core Platforms. *D. Gadioli, S. Libutti, G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano.* Proceedings of ISPA 2014: IEEE International Symposium on Parallel and Distributed Processing with Applications - 2014 -[Link]

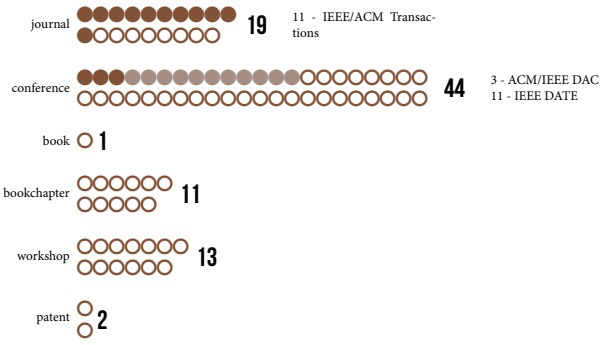
Evaluating orthogonality between application auto-tuning and run-time resource management for adaptive OpenCL applications. *E. Paone, D. Gadioli, G. Palermo, V. Zaccaria, C. Silvano.* Proceedings of ASAP 2014: IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors - 2014 -[Link]

Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures. *G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano.* Proceedings of ARC 2014: Reconfigurable Computing: Architectures, Tools, and Applications - 10th International Symposium - 2014 -[Link]

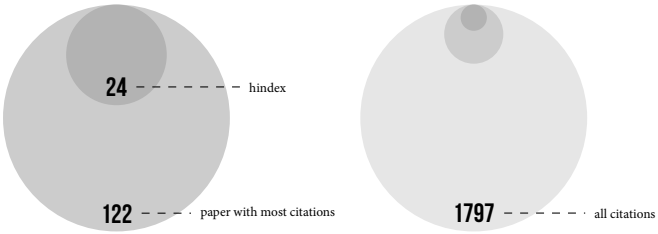
DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling. *G. Mariani, G. Palermo, V. Zaccaria, C. Silvano.* Proceedings of DATE 2014: International Conference on Design, Automation and Test in Europe - 2014 -[Link]

Run-time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction. *G. Mariani, V. Sima, G. Palermo, V. Zaccaria, G. Marchiri, C. Silvano, K. Bertels.* Proceedings of FPL 2013: International Conference on Field Programmable Logic and Applications - 2013 -[Link]

Publication statistics



Bibliometric indexes



From Google Scholar profile - June 25, 2019

TEACHING

Titolare

- **Technologies for Connected Products and Systems** at Politecnico di Milano - titolare: Vittorio Zaccaria ('18/19 - crediti totali: 3),
- **Informatica B** at Politecnico di Milano - titolare: Vittorio Zaccaria ('18/19, '17/18, '16/17, '15/16, '14/15, '13/14, '12/13 - crediti totali: 49)

Teaching assistant (Esercitatore)

- **Informatica B** at Politecnico di Milano - titolare: Vittorio Zaccaria ('18/19, '17/18, '16/17, '14/15) - ore totali: 102 ,
- **Hypermedia Applications (Web and multimedia)** at Politecnico di Milano - titolare: Franca Garzotto ('17/18, '16/17) - ore totali: 40 ,
- **Architettura dei Calcolatori e Sistemi Operativi** at Politecnico di Milano - titolare: Roberto Negrini ('14/15, '13/14) - ore totali: 21

VITTORIO ZACCARIA

POLITECNICO DI MILANO - PIAZZA LEONARDO DA VINCI, 32 — ITALY

+39 02 2399 3642 — WWW.VITTORIOZACCARIA.NET

CV updated on July 2, 2019

Education

- June 1998: Master in Computer engineering at Politecnico di Milano, Italy. Thesis topic: Java agents for a distributed file system.
- November 2002: Ph.D in Computer engineering at Politecnico di Milano, Italy. Thesis topic: "Power consumption estimation and optimization of VLIW processors. Sponsored by STMicroelectronics."

Current position

Assistant Professor at Politecnico di Milano - Milan, Italy.

Areas of specialization

Computer aided design of digital circuits. Multi-processor design space exploration. Low-power and high-performance design. Parallel processor architectures. Advanced parallel programming paradigms. Compilation and simulation methodologies for multi-processor-based systems.

Appointments held

2009 — : Assistant Professor, Politecnico di Milano - Milan, Italy

- Appointed as Principal Investigator for an industrial collaboration grant from STMicroelectronics related to the design cryptographic hardware using functional programming languages.
- Specified and developed the ReSPIR optimization algorithm for processor/SoC optimization. It enables efficient IP reuse in the context of virtual platforms (10x reduction in time, less than 1 percent error w.r.t. ideal).
- Succesfully brought a team of 5 people to prototype a new type of video-surveillance system in the context of the 2PARMA FP7 European Project.
- Led a team of 3 engineers to prototype a research software tool for processor customization. Prototypes were delivered on-time and within budget of several european FP7 projects.

2004 — 2007 : R&D Engineer, STMicroelectronics - Lugano, Switzerland

- Specified, prototyped and validated several ST200 processor architectural extensions. Vertical validation of the extensions from the ISA up to the application-layer/OS.
- Enabled secure co-hosting of more operating systems by means of secure storage extensions of the ST200 architecture.
- Collaborated to the specification, validation (by means of functional and timing simulation) and architectural exploration for symmetric multi-processing based on ST200.
- Architectural specification and design of multi-threaded architectures based on stream-programming paradigms.

2003 — 2004 : Research Consultant, STMicroelectronics - Milan, Italy

- Pioneered the field of Power Modeling of VLIW Cores (10 percent error RTL vs Gate-level).
- Introduced an effective methodology to minimize the effort of design of experiments for NoC power models (10x reduction in characterization time, 33 percent error).

2007 — 2009 : Research Associate, Politecnico di Milano - Milan, Italy

- Introduced advanced techniques for managing design of experiments and response surface methods in automatic design space exploration for multi-processors.
- Extended classical design space exploration to tackle the problem of process-variability-aware design of multi-processors.

Grants and funding

Period	*Grant type*	*Role*	*Project*	*Funding*
2017 - 2018	Grant from industrial partner STMicroelectronics	Principal investigator	Metodologia e Strumenti per la Valutazione di Circuiti Crittografici	30000 EUR
2015 - 2016	Grant from industrial partner STMicroelectronics	Principal investigator	Strumenti di Progettazione e Verifica per Circuiti Crittografici	30000 EUR
2001 - 2003	Post-Doc Grant Politecnico di Milano	Post Doc	Power estimation and exploration of the architectural space at the system level for systems-on-chip	
2007 - 2009	Research Grant Politecnico di Milano		Multi-Objective Design Space Exploration of Multi-Processor SOC Architectures for Embedded Multimedia Applications	
1999 - 2001	Ph.D. Fellowship STMicroelectronics		Methodologies for Power Estimation for VLIW Machines	

Teaching activity

He has been in full charge (*Titolare*) of the following courses:

Academic year	*Course name*	*Credits*	*Level, Institution*
2018/2019	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2018/2019	Technologies for Connected Products and Systems	3	Laurea Magistrale in Digital and Interaction Design, Politecnico di Milano
2017/2018	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2016/2017	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2015/2016	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2014/2015	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2013/2014	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2012/2013	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2011/2012	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2010/2011	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano

He has been teaching assistant (“esercitatore”) for the following courses:

Academic year	*Course name*	*Hours*	*Level, Institution*
2018/2019	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2017/2018	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2017/2018	Hypermedia Applications (Web and multimedia)	20	Laurea magistrale in Ingegneria Informatica, Politecnico di Milano
2016/2017	Hypermedia Applications (Web and multimedia)	20	Laurea magistrale in Ingegneria Informatica, Politecnico di Milano
2016/2017	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2014/2015	Architettura dei Calcolatori e Sistemi Operativi	10	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2014/2015	Informatica B	18	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2013/2014	Architettura dei Calcolatori e Sistemi Operativi	11	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2010/2011	Informatica ed Elementi di Informatica Medica	24	Laurea di primo livello in Ingegneria Biomedica, Politecnico di Milano
2009/2010	Architettura dei Calcolatori e Sistemi Operativi	38	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2009/2010	Informatica B	11	Laurea di primo livello in Ingegneria Elettrica, Politecnico di Milano
2009/2010	Architectures for Multimedia Systems	20	Laurea specialistica in Ingegneria Informatica, Politecnico di Milano

2009/2010	Informatica ed Elementi di Informatica Medica	17	Laurea di primo livello in Ingegneria Biomedica, Politecnico di Milano
2008/2009	Informatica B	15	Laurea di primo livello in Ingegneria Elettrica, Politecnico di Milano
2003/2003	Calcolatori Elettronici	20	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2001/2002	Calcolatori Elettronici	20	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2001/2002	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2000/2001	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2000/2001	Sistemi Operativi 1	15	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
1999/2000	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano

Award, prizes academic honors

- 2002 - Dimitris N. Chorafas Award, for the exceptional contribution to the state of the art of research in processor architecture.
- 2010 - HiPEAC Award, as a co-author of 'A Correlation-Based Design Space Exploration Methodology for Multiprocessor Systems-on-Chip' published at DAC 2010.
- 2012 - Idea2Product, 2nd r. up, for creating a valuable opportunity for product commercialization of research results.

Graduate students co-advised

Since 2001, he co-advised the following students in their Master-equivalent theses:

1. 2019 — Nicola Castaldo, Thesis title: *A conceptual modeling approach for the rapid development of chatbots for conversational data exploration.*
2. 2016 — Stefano Gianelli and Valerio Cassani, Thesis title: *Progettazione di mashup per dispositivi mobili un metodo basato sulla modellazione di contesto.*
3. 2017 — Stefano Lucchi and Davide Fava, Thesis title: *Mash-up based service and data integration in the CAMUS framework.*
4. 2017 — Lorenzo Delledonne, Thesis title: *A methodology based on functional languages for the design of hardware cryptographic primitives resistant to side-channel attacks.*
5. Simone Borgio and Davide Bosisio, Thesis title: *OpenStreamC - a development framework for streaming applications.*
6. Zhong Yi Hu, Thesis title: *Power modeling of Networks-on-chip.*
7. Fabrizio Lucini, Thesis title: *Specification and design of a prefetch unit for translating code at run-time.*
8. Simone Valsecchi, Thesis title: *An algorithm for the efficient exploration of the architectural design space for microprocessor-based systems.*

9. Gianluca Palermo, Thesis title: *A methodology for architectural exploration and information encoding for low-power digital systems.*
10. Alessandro Molgora and Claudio Lozza, Thesis title: *Low-power state encoding techniques for finite state machines.*
11. Marco Gavazzi, Thesis title: *Low-power VLIW re-scheduling algorithms.*
12. Lorenzo Salvemini, Thesis title: *An architectural exploration methodology for low-power digital systems.*
13. Andrea Bona, Thesis title: *A design of experiments methodology in a power estimation flow for VLIW processors.*

He has overseen part of the work of the following Ph. D. students:

- Maria Chiara Molteni, Università di Milano
- Edoardo Paone, Politecnico di Milano
- Giovanni Mariani, ALaRI - University of Lugano
- Fabrizio Castro, Politecnico di Milano.

Research interests and historical achievements

Countermeasures against side-channel attacks.

This project started from an actual industrial need, i.e., providing the designer of cryptographic algorithms with guidelines and tools that make it possible to implement and validate the primitive while assessing the desired level of protection.

The problems with existing methods and tools that brought us to seek new approaches are just a few; first, high level specification/prototyping of the algorithm is decoupled from low level implementation. This brings a host of issues, among which the fact that manual translation can introduce subtle bugs and unanticipated behavior. Besides this, the specification is usually done in weakly typed languages, bringing additional source of unexpected behavior, test and refactoring complexity.

My main goal is to investigate how a strongly typed functional programming language could be used to build a DSLs to synthesize these kind of algorithms in hardware, by bridging the gap between spec and implementation with automatic tools.

Techniques to support teaching to a massive amount of students.

In 2014 I realized that my computer science class was undergoing a major challenge. The number of students was becoming huge and resource assignment from my university (in terms of teaching assistants funded by the university) was on a decreasing trend. In fact, the ratio between qualified teaching assistants (those who have a degree in computer engineering) and students had fallen below 1/100, making it hard to bring students to complete even the simplest hands-on lab. I always had the ambition to not leave anyone behind so I gradually started to study the current MOOC technologies to see whether they could be used to keep the students on track.

Currently, I am creating the first online course that is meant to complement the face to face lectures that I give. The course can be edited collaboratively by teachers (on Github) through a YAML based format that I designed; it can then be imported into an EDX server to be used by the students who can submit their homework to an automatic grader that I wrote using containerization technology.

Achievements:

- Developed a YAML-based format to author course contents.
- Used containerization technology to build an automatic graders.

Front-end development and mobile apps.

I have been always interested in ways to model complex program behavior such as parallel and asynchronous programming. It turns out that web and mobile application present a lot of challenges from this point of view being inherently asynchronous.

In this area I have collaborated with some researchers on the implementation of context-based applications for the customization of the user experience on mobile devices. This kind of application is characterized a query engine that fetches and mashes up data from different kind of services into a unified view on a native application. We decided to simplify the construction of the mobile application by shifting all the burden of service querying into the server. The mobile app uses then a flexible querying interface towards the server that minimizes data transfered across the network.

Power estimation and optimization of processor-based systems.

Since 1999, I have been interested into estimating and optimizing the power consumption of microprocessors and microprocessor-based systems.

Achievements:

- Developed an analytical model that takes into account software-level parameters (instruction ordering, pipeline stall probability and instruction cache miss probability) and micro-architectural-level ones (pipeline stage power per instruction).
- Validated the model on an industrial VLIW processor jointly designed by HPLabs and STMicroelectronics.
- Defined a register file write inhibition scheme that exploits the forwarding paths in VLIW processors.
- Designed a dynamic power management policy for general purpose operating systems.
- Designed a method for the exploration of the architectural parameters of the memory sub-systems, from the energy-delay joint perspective.
- Developed Multicube Explorer, a tool for experimenting with multi-objective exploration.
- Developed accurate performance and power modeling characterization of applications with emphasis on parallel processors architectures and network-on-chips.
- Developed optimal tuning of the memory hierarchy, processor parallelism (intra and inter-task) and processor interconnection network.
- Developed optimal software task mapping and scheduling onto the target processor units and optimal communication scheduling.
- Designed run-time design space exploration for trading-off quality-of-service with actual power constraints.
- Robust optimization with respect to several levels of uncertainties such as workload variability, model estimation accuracy and manufacturing process variability.

- Specified and implemented power characterization and high-level power estimation work-flows for the STBus Network on Chip. The STBus is a high-performance, low-latency on chip parameterizable network supported by production grade specification and synthesis tools.

Task Level Parallelism.

During my 4 years stint in the industry, I have worked on a variety of projects related to exploiting task level parallelism. I have had the opportunity to work within an international team on the entire stack of hardware and software design tools for an embedded processor.

Achievements:

- Specified and validated embedded shared-memory multi-processor systems.
- Designed run-time and operating system components including embedded co-hosting technology for the ST230 microprocessor.
- Studied and created a parallel programming framework for industrial multi-processor architectures.
- Specified secure storage extensions for embedded processors.
- Developed secure co-hosting solutions for industrial applications.
- Involved in the study and implementation of novel cryptographic power attack techniques based on cache-miss induction.

Current teaching goals

Troughout the years, I discovered that I love teaching by making students passionate about computer engineering. I like matching conventional methods for teaching with novel technology such as MOOcs. In particular, I am running a teaching experiment, called [Polimi at Home](http://www.pah.polimi.it), where regular students can follow on-line tutorials (based on EDX technology) and be automatically graded.

Professional activities

National and international research projects

He has been actively involved in the following european projects:

- 2013 - 2016, Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties (CONTREX), project type: FP7, consortium:
  - Politecnico di Milano, Italy
  - STMicroelectronics, Italy
  - Offis e.V, Germany
  - GMV Aerospace and Defence SA, Spain)
  - Cobra, Switzerland
  - EUROTECH Group S.p.A., Italy

  - Intecs SpA, Italy
  - iXtronics GmbH, Germany
  - EDALab s.r.l., Italy
  - DOCEA Power, France
  - Politecnico di Torino, Italy
  - University of Cantabria, Spain
  - KTH (Royal Institute of Technology), Sweden
  - The European Electronic Chips and Systems design Initiative, France
  - ST-PoliTo s.c.a.r.l., Italy

- 2009 - 2013, CO-design and Power Management in PLatform-based Design Space EXploration (COMPLEX), project type: FP7, consortium:

  - Politecnico di Milano, Italy
  - STMicroelectronics, Italy
  - STMicroelectronics, China
  - Offis e.V, Germany
  - Thales Communications SA, France
  - GMV Aerospace and Defence SA, Spain
  - Synopsys Belgium NV, Belgium
  - ChipVision Design Systems AG, Germany
  - EDALab srl, Italy
  - Magillem Design Services SAS, France
  - Politecnico di Milano, Italy
  - Universidad de Cantabria, Spain
  - Politecnico di Torino, Italy
  - Interuniversitair Micro-Electronica Centrum vzw, Blegium
  - The European Electronic Chips and Systems design Initiative, France

- 2010 - 2012, PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures, project type: FP7, consortium:

  - Politecnico di Milano, Italy
  - STMicroelectronics, Italy
  - STMicroelectronics, France
  - Fraunhofer Institute for Telecommunications Heinrich Hertz Institute (HHI), Berlin
  - Institute of Communication and Computer Systems, Greece
  - Rheinisch-Westfaelische Technische Hochschule Aachen, Germany
  - Synopsys, Belgium

- 2008 - 2010, Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications, project type: FP7, consortium:
  - Politecnico di Milano, Italy
  - DS2, Spain
  - STMicroelectronics, Italy
  - STMicroelectronics, China
  - Imec, Belgium
  - Esteco, Italy
  - ALaRI, Switzerland
  - ICT, China

Program committee membership

- As ”membro del TPC” of PARMA-DITAM Workshop 2018, held in Manchester, United Kingdom on January 23, 2018.
- As ”membro del TPC” of ADAPT Workshop 2016, held in Prague, Czech Republic on January 18, 2016.
- As ”membro del TPC” of ADAPT Workshop 2015, held in Amsterdam, The Netherlands on January 21, 2015.
- As ”membro del TPC” of Trust Workshop 2014, held in Edinburgh, UK on June 12, 2014.
- As ”membro del TPC” of ADAPT Workshop 2014, held in Vienna, Austria on January 22, 2014.
- As ”membro del TPC e web chair” of DITAM Workshop 2013, held in Berlin, Germany on January 22, 2013.
- As ”membro del TPC” of NoCArc Workshop 2012, held in Vancouver, Canada on December 1, 2012.
- As ”program co-chair” of PARMA Workshop (co-located with ARCS) 2012, held in Munich, Germany on February 29, 2012.
- As ”membro del TPC e poster session chair” of DITAM Workshop 2012, held in Paris, France on December 24, 2012.
- As ”membro del TPC” of PARMA Workshop (co-located with ARCS) 2011, held in Como, Italy on February 23, 2011.
- As ”membro del TPC” of NoCArc Workshop 2010, held in Atlanta, USA on December 4, 2010.
- As ”membro del TPC” of PARMA Workshop (co-located with ARCS) 2010, held in Hannover, Germany on February 22, 2010.
- As ”membro del TPC e session chair” of DATE Conference - Track A8 (Multi-Core Platforms) 2009, held in Nice, France on April 20, 2009.
- As ”membro del TPC” of NoCArc Workshop 2009, held in New York City, USA on December 12, 2009.
- As ”membro del TPC” of DATE Conference - Track A8 (Multi-Core Platforms) 2008, held in Munich, Germany on March 10, 2008.
- As ”membro del local committee” of Micro Conference 2008, held in Como, Italy on November 10, 2008.
- As ”membro del TPC” of NoCArc Workshop 2008, held in Como, Italy on November 8, 2008.

Talks

- As 'relatore' of "On the Role of Context in the Design of Mobile Mashups", on June 6, 2016 at RMC Challenge - Lugano, Switzerland
- As 'relatore' of "An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to P2012", on March 22, 2013 at Platform 2012 / STHORM Workshop - Grenoble, France
- As 'Keynote speaker' of "Principles of Design Space Exploration in the Embedded Multi-core Era", on March 29, 2013 at HPSC Conference - Taipei, Taiwan
- As 'Keynote speaker' of "Design space exploration and run-time resource management in the embedded multi-core era", on October 11, 2012 at ESTIMEDA Workshop - Tampere, Finland
- As 'relatore' of "An efficient design space exploration methodology for on-chip multiprocessors subject to application-specific constraints", on September 8, 2008 at SASP Symposium - Anaheim, USA
- As 'relatore' of "Energy estimation and optimization of embedded VLIW processors based on instruction clustering", on June 13, 2002 at DAC Conference - New Orleans, USA
- As 'relatore' of "Fast system-level exploration of memory architectures driven by energy-delay metrics", on May 9, 2001 at ISCAS Conference - Sydney, Australia
- As 'relatore' of "A Design Framework to Efficiently Explore Energy-Delay Tradeoffs", on April 27, 2001 at CODES 2001 Symposium - Copenhagen, Denmark

Reviewing activities

Type	*Name*
journal	IEEE Transactions on Computers
journal	IEEE Transactions on Very Large Scale of Integration Circuits
journal	IEEE Transactions on Computer Aided Design of Integrated Circuits
conference	ADAPT (co-located with HIPEAC 2016)
journal	Journal of Low Power Electronics - JOLPE
conference	SASP
conference	IC-SAMOS
conference	DATE

Innovation, technology transfer patents

He has been awarded with the following patents:

- 7243213 US - July 2007, Patent title: "Process for translating instructions for an arm-type processor into instructions for a LX-type processor; relative translator device and computer program product", Authors: Andrea Pagni, Fabrizio Lucini, Danilo Pietro Pau, Antonio Maria Borneo, Vittorio Zaccaria
- 6889317 US - May 2005, Patent title: "Processor architecture", Authors: Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria, Danilo Pau, Roberto Zafalon

He produced significant public-domain and industrial technology transfer by developing the following projects:

- Multicube Explorer — an architectural exploration framework retargetable to different processor-based architectures and exploration algorithms. The tool contains also advanced algorithms for DoE generation and response surface modeling. It is scheduled to go open-source in January 2009 — open-source.
- xSTreamC compiler and nSTream simulator — a development toolchain for applications based on the stream oriented programming model. The toolchain has been released open-source in October 2008 — open-source.
- ST200-ISS — a production-grade instruction set simulator for the ST200 VLIW processor family (functional and timing behavior models). Kernel, device components, cache-coherency, secure-storage, co-hosting — proprietary.
- Tools for run-time power estimation of STBus proprietary bus technology (C/SystemC). These tools are currently part of the internal STBus product work-flow — proprietary.

Known languages

- Italian: Native
- English: Fluent

Como — July 2, 2019

Vittorio Zaccaria

VITTORIO ZACCARIA

POLITECNICO DI MILANO - PIAZZA LEONARDO DA VINCI, 32 — ITALY

+39 02 2399 3642 — WWW.VITTORIOZACCARIA.NET

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Vittorio Zaccaria