VITTORIO ZACCARIA

CV SUMMARY

EDUCATION

1998	**Master** in Computer engineering, Politecnico di Milano, Italy
2002	**Ph.D** in Computer engineering, Politecnico di Milano, Italy

CAREER

2020 —	**Associate Professor**, Politecnico di Milano Milan, Italy
2009 — 2020	**Assistant Professor**, Politecnico di Milano Milan, Italy
2004 — 2007	**R&D Engineer**, STMicroelectronics Lugano, Switzerland
2003 — 2004	**Research Consultant**, STMicroelectronics Milan, Italy
2007 — 2009	**Research Associate (assegnista di ricerca)**, Politecnico di Milano Milan, Italy

RESEARCH INTERESTS

Cryptography: side channel attacks and countermeasures, masking, threshold implementations, probing security.

Hardware: hardware description languages, design space exploration, power consumption, performance modeling and simulation.

Software: domain specific languages, functional programming.

LEADERSHIP IN INDUSTRIAL RESEARCH PROJECTS

March 2017 — March 2018	grant from **STMicroelectronics** — Principal investigator — 30000 EUR
July 2015 — July 2016	grant from **STMicroelectronics** — Principal investigator — 30000 EUR

SCIENTIFIC PRODUCTION

Total publications: 91, (76 entries on Scopus, 112 co-authors).
Co-author of 20 journal papers including 12 IEEE/ACM Transactions.
Co-author of 45 publications on peer reviewed conferences including DAC[1] and DATE[2].
Co-author of 1 scientific books.
Co-inventor of 2 patents with STMicroelectronics, all of them granted.

PUBLICATION IMPACT

Google Scholar (January 2021)	h-index: 26 with 2203 citations since January 2000
Scopus (November 2019)	h-index: 18 with 979 citations since January 2000

[1] Design Automation Conference
[2] Design Automation and Test Europe

AWARDS

2002 **Dimitris N. Chorafas Award** — Dimitris N. Chorafas Foundation — for the exceptional contribution to the state of the art of research in processor architecture.

2010 **HiPEAC Award** — HiPEAC (High Performance and Embedded Architecture and Compilation) — as a co-author of 'A Correlation-Based Design Space Exploration Methodology for Multiprocessor Systems-on-Chip' published at DAC 2010.

2012 **Idea2Product, 2nd runner up** — — for creating a valuable opportunity for product commercialization of research results.

INVITED TALKS AND SEMINARS

2012 — keynote at **ESTIMEDA Workshop** titled "Design space exploration and run-time resource management in the embedded multi-core era"

2013 — keynote at **HPSC Conference** titled "Principles of Design Space Exploration in the Embedded Multi-core Era"

TEACHING EXPERIENCE — past 5 years

Principi di Architetture dei Calcolatori (ECTS: 5, students: 200+) 2021/2022 – PoliMi - Ing. Elett. - 1 Liv
Advanced Operating Systems (ECTS: 5, students: 100+) 2021/2022 – PoliMi - Ing. Inf. LM
Principi di Architetture dei Calcolatori (ECTS: 5, students: 200+) 2020/2021 – PoliMi - Ing. Elett. - 1 Liv
Informatica B (ECTS: 7, students: 200+) 2020/2021 – PoliMi - Ing. Mec. e Ener. - 1 Liv
Principi di Architetture dei Calcolatori (ECTS: 5, students: 200+) 2019/2020 – PoliMi - Ing. Elett. - 1 Liv
Informatica B (ECTS: 7, students: 200+) 2019/2020 – PoliMi - Ing. Mec. e Ener. - 1 Liv
Technologies for Connected Products and Systems (ECTS: 3, students: 20+) 2018/2019 – PoliMi - Design - LM
Informatica B (ECTS: 7, students: 200+) 2018/2019 – PoliMi - Ing. Mec. e Ener. - 1 Liv
Informatica B (ECTS: 7, students: 200+) 2017/2018 – PoliMi - Ing. Mec. e Ener. - 1 Liv
Informatica B (ECTS: 7, students: 200+) 2016/2017 – PoliMi - Ing. Mec. e Ener. - 1 Liv
Informatica B (ECTS: 7, students: 200+) 2015/2016 – PoliMi - Ing. Mec. e Ener. - 1 Liv
Informatica B (ECTS: 7, students: 200+) 2014/2015 – PoliMi - Ing. Mec. e Ener. - 1 Liv

INSTITUTIONAL RESPONSIBILITIES

1999 —	advisor of 15 master students in Computer Engineering.
2017 —	advisor of 8 stages (tirocini) for undergraduate students in Computer Engineering.

SUPERVISION OF DOCTORAL AND POSTDOCTORAL STUDENTS

2018 - 2021	1 student at Università di Milano, role: co-advisor

PARTICIPATION IN EU-FUNDED RESEARCH PROJECTS

October 2013 — September 2016	**CONTREX** — FP7
December 2009 — March 2013	**COMPLEX** — FP7
January 2010 — December 2012	**2PARMA** — FP7
January 2008 — June 2010	**Multicube** — FP7

COMMISSION OF TRUST — selection

2021	membro del TPC — PARMA-DITAM Workshop
2021	membro del TPC — COMPSAC (SEPT)
2021	membro del TPC — COSADE
2021	membro del TPC — PARMA-DITAM Workshop
2020	membro del TPC — PARMA-DITAM Workshop
2018	membro del TPC — PARMA-DITAM Workshop

2016	membro del TPC — ADAPT Workshop
2012	program co-chair — PARMA Workshop (co-located with ARCS)
2008	membro del local committee — Micro Conference
2009	membro del TPC e session chair — DATE Conference - Track A8 (Multi-Core Platforms)
2008	membro del TPC — DATE Conference - Track A8 (Multi-Core Platforms)
2001 —	IEEE Embedded Systems Letters — expert reviewer
2001 —	Design Automation for Embedded Systems — expert reviewer
2001 —	IEEE Transactions on Computers — expert reviewer
2001 —	IEEE Transactions on Dependable and Secure Computing — expert reviewer
2001 —	IEEE Transactions on Computers — expert reviewer
2001 —	Concurrency and Computation: Practice and Experience — expert reviewer
2001 —	IEEE Transactions on Emerging Topics in Computing — expert reviewer
2001 —	Transactions on Embedded Computing Systems — expert reviewer
2001 —	Transactions on Embedded Computing Systems — expert reviewer
2001 —	Transactions on Embedded Computing Systems — expert reviewer
2001 —	IEEE Transactions on Very Large Scale Integration Systems — expert reviewer
2001 —	Journal of Low Power Electronics JOLPE — expert reviewer
2001 —	Transactions on Parallel and Distributed Systems — expert reviewer

10 MOST IMPACTFUL PUBLICATIONS – according to Google scholar

M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, An Instruction-Level Energy Model for Embedded VLIW Architectures — IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 22, pages 998 to 1010, September 2002. IEEE - Piscataway, NJ - USA.

C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao, T. Shibin, MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures — Lecture Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.), pages 47 to 63, 2011. Springer Science+Businness Media.

C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao, The MULTICUBE Design Flow — Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pages 3 to 17, 2011. Springer Science+Businness Media.

G. Mariani, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, G. Palermo, C. Silvano, V. Zaccaria, An industrial design space exploration framework for supporting run-time resource management on multi-core systems — Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe, pages 196 to 201, March 2010. ACM New York, NY - USA.

G. Palermo, C. Silvano, V. Zaccaria, ReSPIR: A Response Surface-based Pareto Iterative Refinement for Application-Specific Design Space Exploration — IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 28, pages 1816 to 1829, December 2009. IEEE - Piscataway, NJ - USA.

L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria, R. Zafalon, A Power Modeling and Estimation Framework for VLIW-based Embedded Systems — Proceedings of PATMOS 2001: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation, September 2001.

A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon, Energy estimation and optimization of embedded VLIW processors based on instruction clustering — Proceedings of DAC 2002: Design Automation Conference, pages 886 to 891, June 2002. ACM New York, NY - USA.

G. Bertoni, V. Zaccaria, L. Breveglieri, M. Monchiero, G. Palermo, AES Power Attack Based on Induced Cache Miss and Countermeasure — Proceedings of ITCC 2005: International conference on Information Technology, pages 586 to 591, April 2005. IEEE - Piscataway, NJ - USA.

G. Palermo, C. Silvano, V. Zaccaria, Multi-Objective Design Space Exploration of Embedded Systems — Journal of Embedded Computing, vol. 1, pages 305 to 316, 2005. IOS Press - The Netherlands.

A. Bona, V. Zaccaria, R. Zafalon, System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip — Ultra Low-Power Electronics and Design, E. Macii (ed.), pages 233 to 254, 2004. Springer US.

EVIDENCE OF TECHNICAL ACCOMPLISHMENT

CASCA — A language for designing hardware countermeasures against side channel attacks. It is based on a final tagless approach for embedding domain specific languages. – open source - role: **project supervision and development** — timeframe: 2016-2018

Polimi at Home (PAH) — An experiment in MOOC for my students of Informatica B. It allows to learn a Matlab-like language through a set of small lectures and automatically graded exercises. It uses the EDX stack. – online - role: **project supervision and development** — timeframe: 2015-2016

2PARMA Use case n. 6 — Integration of various technologies from different project partners to create a video-analytics application. – closed source - role: **project supervision** — timeframe: 2010-2013

Multicube Explorer — Architectural exploration framework retargetable to different processor-based architectures and exploration algorithms. The tool contains also advanced algorithms for DoE generation and response surface modeling. – open source - role: **project management and development** — timeframe: 2007-2010

xSTreamC compiler and nSTream simulator — Development toolchain for applications based on the stream oriented programming model. – open source - role: **development** — timeframe: 2004-2007

ST200-ISS — Production-grade instruction set simulator for the ST200 VLIW processor family (functional and timing behavior models). Kernel, device components, cache-coherency, secure-storage, co-hosting – proprietary - role: **development** — timeframe: 2004-2007

STBus Power estimation — Tools for run-time power estimation of STBus proprietary bus technology (C/SystemC). These tools are currently part of the internal STBus product work-flow – proprietary - role: **development** — timeframe: 2003-2004

LIST OF PEERS

Giuseppe Desoli	Director at STMicroelectronics — Castelletto, Milan (Italy) — giuseppe.desoli@st.com
Cristina Silvano	Professor at Politecnico di Milano — Milan (Italy) — cristina.silvano@polimi.it
Luca Benini	Professor at ETH Zurich — Zurich (Switzerland) — lbenini@iis.ee.ethz.ch
Guido Bertoni	CEO at Security Pattern — Brescia (Italy) — g.bertoni@securitypattern.com
Roberto Zafalon	Director at STMicroelectronics — Agrate Brianza (Italy) — roberto.zafalon@st.com

Como — July 26, 2022

Vittorio Zaccaria

VITTORIO ZACCARIA

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CV updated on July 26, 2022

Education

- June 1998: Master in Computer engineering at Politecnico di Milano, Italy. Thesis topic: Java agents for a distributed file system.
- November 2002: Ph.D in Computer engineering at Politecnico di Milano, Italy. Thesis topic: "Power consumption estimation and optimization of VLIW processors. Sponsored by STMicroelectronics."

Current position

Associate Professor at Politecnico di Milano - Milan, Italy.

Areas of specialization

side channel attacks (cryptography) computer aided design of digital circuits multi-processor design space exploration low-power and high-performance design parallel processor architectures advanced parallel programming paradigms compilation and simulation methodologies for multi-processor-based systems

Appointments held

2020 — : Associate Professor, Politecnico di Milano - Milan, Italy

2009 — 2020 : Assistant Professor, Politecnico di Milano - Milan, Italy

- Appointed as Principal Investigator for an industrial collaboration grant from STMicroelectronics related to the design cryptographic hardware using functional programming languages.
- Specified and developed the ReSPIR optimization algorithm for processor/SoC optimization. It enables efficient IP reuse in the context of virtual platforms (10x reduction in time, less than 1 percent error w.r.t. ideal).
- Succesfully brought a team of 5 people to prototype a new type of video-surveillance system in the context of the 2PARMA FP7 European Project.
- Led a team of 3 engineers to prototype a research software tool for processor customization. Prototypes were delivered on-time and within budget of several european FP7 projects.

2004 — 2007 : R&D Engineer, STMicroelectronics - Lugano, Switzerland

- Specified, prototyped and validated several ST200 processor architectural extensions. Vertical validation of the extensions from the ISA up to the application-layer/OS.
- Enabled secure co-hosting of more operating systems by means of secure storage extensions of the ST200 architecture.
- Collaborated to the specification, validation (by means of functional and timing simulation) and architectural exploration for symmetric multi-processing based on ST200.
- Architectural specification and design of multi-threaded architectures based on stream-programming paradigms.

2003 — 2004 : Research Consultant, STMicroelectronics - Milan, Italy

- Pioneered the field of Power Modeling of VLIW Cores (10 percent error RTL vs Gate-level).
- Introduced an effective methodology to minimize the effort of design of experiments for NoC power models (10x reduction in characterization time, 33 percent error).

2007 — 2009 : Research Associate (assegnista di ricerca), Politecnico di Milano - Milan, Italy

- Introduced advanced techniques for managing design of experiments and response surface methods in automatic design space exploration for multi-processors.
- Extended classical design space exploration to tackle the problem of process-variability-aware design of multi-processors.

Grants and funding

Period	*Grant type*	*Role*	*Project*	*Funding*
2017 - 2018	Grant from industrial partner STMicroelectronics	Principal investigator	Metodologia e Strumenti per la Valutazione di Circuiti Crittografici	30000 EUR
2015 - 2016	Grant from industrial partner STMicroelectronics	Principal investigator	Strumenti di Progettazione e Verifica per Circuiti Crittografici	30000 EUR
2001 - 2003	Post-Doc Grant Politecnico di Milano	Post Doc	Power estimation and exploration of the architectural space at the system level for systems-on-chip	
2007 - 2009	Research Grant Politecnico di Milano		Multi-Objective Design Space Exploration of Multi-Processor SOC Architectures for Embedded Multimedia Applications	
1999 - 2001	Ph.D. Fellowship STMicroelectronics		Methodologies for Power Estimation for VLIW Machines	

Teaching activity

He is / has been in full charge (*Titolare*) of the following courses:

Academic year	*Course name*	*Credits*	*Level, Institution*
2021/2022	Advanced Operating Systems	5	Laurea Magistrale in Ingegneria Informatica, Politecnico di Milano
2021/2022	Principi di Architetture dei Calcolatori	5	Laurea di primo livello in Ingegneria Elettronica, Politecnico di Milano
2020/2021	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2020/2021	Principi di Architetture dei Calcolatori	5	Laurea di primo livello in Ingegneria Elettronica, Politecnico di Milano
2019/2020	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2019/2020	Principi di Architetture dei Calcolatori	5	Laurea di primo livello in Ingegneria Elettronica, Politecnico di Milano
2018/2019	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2018/2019	Technologies for Connected Products and Systems	3	Laurea Magistrale in Digital and Interaction Design, Politecnico di Milano
2017/2018	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2016/2017	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2015/2016	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2014/2015	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2013/2014	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2012/2013	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2011/2012	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2010/2011	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano

He has been teaching assistant (“esercitatore”) for the following courses:

Academic year	*Course name*	*Hours*	*Level, Institution*
2020/2021	Principi di Architetture dei Calcolatori	20	Laurea di primo livello in Ingegneria Elettronica, Politecnico di Milano
2019/2020	Informatica B	26	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2019/2020	Principi di Architetture dei Calcolatori	20	Laurea di primo livello in Ingegneria Elettronica, Politecnico di Milano
2018/2019	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2018/2019	Hypermedia Applications (Web and multimedia)	20	Laurea magistrale in Ingegneria Informatica, Politecnico di Milano
2017/2018	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano

2017/2018	Hypermedia Applications (Web and multimedia)	20	Laurea magistrale in Ingegneria Informatica, Politecnico di Milano
2016/2017	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2016/2017	Hypermedia Applications (Web and multimedia)	20	Laurea magistrale in Ingegneria Informatica, Politecnico di Milano
2014/2015	Architettura dei Calcolatori e Sistemi Operativi	10	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2014/2015	Informatica B	18	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2013/2014	Architettura dei Calcolatori e Sistemi Operativi	11	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2010/2011	Informatica ed Elementi di Informatica Medica	24	Laurea di primo livello in Ingegneria Biomedica, Politecnico di Milano
2009/2010	Architettura dei Calcolatori e Sistemi Operativi	38	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2009/2010	Informatica B	11	Laurea di primo livello in Ingegneria Elettrica, Politecnico di Milano
2009/2010	Architectures for Multimedia Systems	20	Laurea specialistica in Ingegneria Informatica, Politecnico di Milano
2009/2010	Informatica ed Elementi di Informatica Medica	17	Laurea di primo livello in Ingegneria Biomedica, Politecnico di Milano
2008/2009	Informatica B	15	Laurea di primo livello in Ingegneria Elettrica, Politecnico di Milano
2003/2003	Calcolatori Elettronici	20	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2001/2002	Calcolatori Elettronici	20	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2001/2002	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2000/2001	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2000/2001	Sistemi Operativi 1	15	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
1999/2000	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano

Award, prizes academic honors

- 2002 - Dimitris N. Chorafas Award, for the exceptional contribution to the state of the art of research in processor architecture.
- 2010 - HiPEAC Award, as a co-author of 'A Correlation-Based Design Space Exploration Methodology for Multiprocessor Systems-on-Chip' published at DAC 2010.
- 2012 - Idea2Product, 2nd runner up, for creating a valuable opportunity for product commercialization of research results.

Graduate students co-advised

Since 2001, he co-advised the following students in their Master-equivalent theses:

1. 2019 — Alessandro Elio Cantini, Thesis title: *Progetto e valutazione di una rete neurale eseguita su un sistema embedded a bassa potenza.*
2. 2019 — Marco Redaelli, Thesis title: *(provisional): A side channel attack methodology.*
3. 2019 — Nicola Castaldo, Thesis title: *A conceptual modeling approach for the rapid development of chatbots for conversational data exploration.*
4. 2016 — Stefano Gianelli and Valerio Cassani, Thesis title: *Progettazione di mashup per dispositivi mobili un metodo basato sulla modellazione di contesto.*
5. 2017 — Stefano Lucchi and Davide Fava, Thesis title: *Mash-up based service and data integration in the CAMUS framework.*
6. 2017 — Lorenzo Delledonne, Thesis title: *A methodology based on functional languages for the design of hardware cryptographic primitives resistant to side-channel attacks.*
7. Simone Borgio and Davide Bosisio, Thesis title: *OpenStreamC - a development framework for streaming applications.*
8. Zhong Yi Hu, Thesis title: *Power modeling of Networks-on-chip.*
9. Fabrizio Lucini, Thesis title: *Specification and design of a prefetch unit for translating code at run-time.*
10. Simone Valsecchi, Thesis title: *An algorithm for the efficient exploration of the architectural design space for microprocessor-based systems.*
11. Gianluca Palermo, Thesis title: *A methodology for architectural exploration and information encoding for low-power digital systems.*
12. Alessandro Molgora and Claudio Lozza, Thesis title: *Low-power state encoding techniques for finite state machines.*
13. Marco Gavazzi, Thesis title: *Low-power VLIW re-scheduling algorithms.*
14. Lorenzo Salvemini, Thesis title: *An architectural exploration methodology for low-power digital systems.*
15. Andrea Bona, Thesis title: *A design of experiments methodology in a power estimation flow for VLIW processors.*

He has overseen part of the work of the following Ph. D. students:

- Maria Chiara Molteni, Università di Milano

Research interests and historical achievements

Countermeasures against side-channel attacks.

This project started from an actual industrial need, i.e., providing the designer of cryptographic algorithms with guidelines and tools that make it possible to implement and validate the primitive while assessing the desired level of protection.

The problems with existing methods and tools that brought us to seek new approaches are just a few; first, high level specification/prototyping of the algorithm is decoupled from low level implementation. This brings a host of issues, among which the fact that manual translation can introduce subtle bugs and unanticipated behavior. Besides this, the specification is usually done in weakly typed languages, bringing additional source of unexpected behavior, test and refactoring complexity.

My main goal is to investigate how a strongly typed functional programming language could be used to build a DSLs to synthesize these kind of algorithms in hardware, by bridging the gap between spec and implementation with automatic tools.

Techniques to support teaching to a massive amount of students.

In 2014 I realized that my computer science class was undergoing a major challenge. The number of students was becoming huge and resource assignment from my university (in terms of teaching assistants funded by the university) was on a decreasing trend. In fact, the ratio between qualified teaching assistants (those who have a degree in computer engineering) and students had fallen below 1/100, making it hard to bring students to complete even the simplest hands-on lab. I always had the ambition to not leave anyone behind so I gradually started to study the current MOOC technologies to see whether they could be used to keep the students on track.

Currently, I am creating the first online course that is meant to complement the face to face lectures that I give. The course can be edited collaboratively by teachers (on Github) through a YAML based format that I designed; it can then be imported into an EDX server to be used by the students who can submit their homework to an automatic grader that I wrote using containerization technology.

Achievements:

- Developed a YAML-based format to author course contents.
- Used containerization technology to build an automatic graders.

Front-end development and mobile apps.

I have been always interested in ways to model complex program behavior such as parallel and asynchronous programming. It turns out that web and mobile application present a lot of challenges from this point of view being inherently asynchronous.

In this area I have collaborated with some researchers on the implementation of context-based applications for the customization of the user experience on mobile devices. This kind of application is characterized a query engine that fetches and mashes up data from different kind of services into a unified view on a native application. We decided to simplify the construction of the mobile application by shifting all the burden of service querying into the server. The mobile app uses then a flexible querying interface towards the server that minimizes data transfered across the network.

Power estimation and optimization of processor-based systems.

Since 1999, I have been interested into estimating and optimizing the power consumption of microprocessors and microprocessor-based systems.

Achievements:

- Developed an analytical model that takes into account software-level parameters (instruction ordering, pipeline stall probability and instruction cache miss probability) and micro-architectural-level ones (pipeline stage power per instruction).
- Validated the model on an industrial VLIW processor jointly designed by HPLabs and STMicroelectronics.
- Defined a register file write inhibition scheme that exploits the forwarding paths in VLIW processors.

- Designed a dynamic power management policy for general purpose operating systems.
- Designed a method for the exploration of the architectural parameters of the memory sub-systems, from the energy-delay joint perspective.
- Developed Multicube Explorer, a tool for experimenting with multi-objective exploration.
- Developed accurate performance and power modeling characterization of applications with emphasis on parallel processors architectures and network-on-chips.
- Developed optimal tuning of the memory hierarchy, processor parallelism (intra and inter-task) and processor interconnection network.
- Developed optimal software task mapping and scheduling onto the target processor units and optimal communication scheduling.
- Designed run-time design space exploration for trading-off quality-of-service with actual power constraints.
- Robust optimization with respect to several levels of uncertainties such as workload variability, model estimation accuracy and manufacturing process variability.
- Specified and implemented power characterization and high-level power estimation work-flows for the STBus Network on Chip. The STBus is a high-performance, low-latency on chip parameterizable network supported by production grade specification and synthesis tools.

Task Level Parallelism.

During my 4 years stint in the industry, I have worked on a variety of projects related to exploiting task level parallelism. I have had the opportunity to work within an international team on the entire stack of hardware and software design tools for an embedded processor.

Achievements:

- Specified and validated embedded shared-memory multi-processor systems.
- Designed run-time and operating system components including embedded co-hosting technology for the ST230 microprocessor.
- Studied and created a parallel programming framework for industrial multi-processor architectures.
- Specified secure storage extensions for embedded processors.
- Developed secure co-hosting solutions for industrial applications.
- Involved in the study and implementation of novel cryptographic power attack techniques based on cache-miss induction.

Current teaching goals

Troughout the years, I discovered that I love teaching by making students passionate about computer engineering. I like matching conventional methods for teaching with novel technology such as MOOcs. In particular, I am running a teaching experiment, called [Polimi at Home](http://www.pah.polimi.it), where regular students can follow on-line tutorials (based on EDX technology) and be automatically graded.

Professional activities

National and international research projects

He has been actively involved in the following european projects:

- 2013 - 2016, Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties (CONTREX), project type: FP7, consortium:
  - Politecnico di Milano, Italy
  - STMicroelectronics, Italy
  - Offis e.V, Germany
  - GMV Aerospace and Defence SA, Spain)
  - Cobra, Switzerland
  - EUROTECH Group S.p.A., Italy
  - Intecs SpA, Italy
  - iXtronics GmbH, Germany
  - EDALab s.r.l., Italy
  - DOCEA Power, France
  - Politecnico di Torino, Italy
  - University of Cantabria, Spain
  - KTH (Royal Institute of Technology), Sweden
  - The European Electronic Chips and Systems design Initiative, France
  - ST-PoliTo s.c.a.r.l., Italy
- 2009 - 2013, CO-design and Power Management in PLatform-based Design Space EXploration (COMPLEX), project type: FP7, consortium:
  - Politecnico di Milano, Italy
  - STMicroelectronics, Italy
  - STMicroelectronics, China
  - Offis e.V, Germany
  - Thales Communications SA, France
  - GMV Aerospace and Defence SA, Spain
  - Synopsys Belgium NV, Belgium
  - ChipVision Design Systems AG, Germany
  - EDALab srl, Italy
  - Magillem Design Services SAS, France
  - Politecnico di Milano, Italy
  - Universidad de Cantabria, Spain

  - Politecnico di Torino, Italy
  - Interuniversitair Micro-Electronica Centrum vzw, Blegium
  - The European Electronic Chips and Systems design Initiative, France
- 2010 - 2012, PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures, project type: FP7, consortium:
  - Politecnico di Milano, Italy
  - STMicroelectronics, Italy
  - STMicroelectronics, France
  - Fraunhofer Institute for Telecommunications Heinrich Hertz Institute (HHI), Germany
  - Institute of Communication and Computer Systems, Greece
  - Rheinisch-Westfaelische Technische Hochschule Aachen, Germany
  - Synopsys, Belgium
- 2008 - 2010, Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications, project type: FP7, consortium:
  - Politecnico di Milano, Italy
  - DS2, Spain
  - STMicroelectronics, Italy
  - STMicroelectronics, China
  - Imec, Belgium
  - Esteco, Italy
  - ALaRI, Switzerland
  - ICT, China

Program committee membership

- As member of TPC of PARMA-DITAM Workshop 2021, held in Budapest, Hungary on January 19, 2021.
- As member of TPC of COSADE 2021, held in Lugano, Switzerland on October 20, 2021.
- As member of TPC of COMPSAC (SEPT) 2021, held in Virtual on July 12, 2021.
- As member of TPC of PARMA-DITAM Workshop 2021, held in Budapest, Hungary and Virtual on June 22, 2022.
- As member of TPC of PARMA-DITAM Workshop 2020, held in Bologna, Italy on January 21, 2020.
- As member of TPC of PARMA-DITAM Workshop 2018, held in Manchester, United Kingdom on January 23, 2018.
- As member of TPC of ADAPT Workshop 2016, held in Prague, Czech Republic on January 18, 2016.
- As member of TPC of ADAPT Workshop 2015, held in Amsterdam, The Netherlands on January 21, 2015.

- As member of TPC of Trust Workshop 2014, held in Edinburgh, UK on June 12, 2014.
- As member of TPC of ADAPT Workshop 2014, held in Vienna, Austria on January 22, 2014.
- As member of TPC of DITAM Workshop 2013, held in Berlin, Germany on January 22, 2013.
- As member of TPC of NoCArc Workshop 2012, held in Vancouver, Canada on December 1, 2012.
- As program co-chair of PARMA Workshop (co-located with ARCS) 2012, held in Munich, Germany on February 29, 2012.
- As member of TPC of DITAM Workshop 2012, held in Paris, France on December 24, 2012.
- As member of TPC of PARMA Workshop (co-located with ARCS) 2011, held in Como, Italy on February 23, 2011.
- As member of TPC of NoCArc Workshop 2010, held in Atlanta, USA on December 4, 2010.
- As member of TPC of PARMA Workshop (co-located with ARCS) 2010, held in Hannover, Germany on February 22, 2010.
- As member of TPC and session chair of DATE Conference - Track A8 (Multi-Core Platforms) 2009, held in Nice, France on April 20, 2009.
- As member of TPC of NoCArc Workshop 2009, held in New York City, USA on December 12, 2009.
- As member of TPC of DATE Conference - Track A8 (Multi-Core Platforms) 2008, held in Munich, Germany on March 10, 2008.
- As member of local committee of Micro Conference 2008, held in Como, Italy on November 10, 2008.
- As member of TPC of NoCArc Workshop 2008, held in Como, Italy on November 8, 2008.

Talks

- As speaker of "An F-algebra for analysing information leaks in the presence of glitches", on January 27, 2021 at TII Cryptoseminar - Abu Dhabi, United Arab Emirates
- As speaker of "On the Role of Context in the Design of Mobile Mashups", on June 6, 2016 at RMC Challenge - Lugano, Switzerland
- As speaker of "An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to P2012", on March 22, 2013 at Platform 2012 / STHORM Workshop - Grenoble, France
- As Keynote speaker of "Principles of Design Space Exploration in the Embedded Multi-core Era", on March 29, 2013 at HPSC Conference - Taipei, Taiwan
- As Keynote speaker of "Design space exploration and run-time resource management in the embedded multi-core era", on October 11, 2012 at ESTIMEDA Workshop - Tampere, Finland
- As speaker of "An efficient design space exploration methodology for on-chip multiprocessors subject to application-specific constraints", on September 8, 2008 at SASP Symposium - Anaheim, USA

- As speaker of "Energy estimation and optimization of embedded VLIW processors based on instruction clustering", on June 13, 2002 at DAC Conference - New Orleans, USA
- As speaker of "Fast system-level exploration of memory architectures driven by energy-delay metrics", on May 9, 2001 at ISCAS Conference - Sydney, Australia
- As speaker of "A Design Framework to Efficiently Explore Energy-Delay Tradeoffs", on April 27, 2001 at CODES 2001 Symposium - Copenhagen, Denmark

Reviewing activities

Date	*Name*
March 2022	ISC HPC
August 2021	IEEE Embedded Systems Letters
February 2021	Design Automation for Embedded Systems
November 2020	IEEE Transactions on Computers
July 2019	IEEE Transactions on Dependable and Secure Computing
August 2016	IEEE Transactions on Computers
May 2016	Concurrency and Computation: Practice and Experience
November 2014	IEEE Transactions on Emerging Topics in Computing
May 2013	Transactions on Parallel and Distributed Systems
April 2013	Transactions on Embedded Computing Systems
January 2012	Design automation conference
December 2011	Journal of Low Power Electronics JOLPE
May 2011	Transactions on Embedded Computing Systems
May 2011	IEEE Transactions on Very Large Scale Integration Systems
May 2011	Transactions on Embedded Computing Systems

Innovation, technology transfer patents

He has been awarded with the following patents:

- 7243213 US - July 2007, Patent title: "Process for translating instructions for an arm-type processor into instructions for a LX-type processor; relative translator device and computer program product", Authors: Andrea Pagni, Fabrizio Lucini, Danilo Pietro Pau, Antonio Maria Borneo, Vittorio Zaccaria
- 6889317 US - May 2005, Patent title: "Processor architecture", Authors: Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria, Danilo Pau, Roberto Zafalon

He produced significant public-domain and industrial technology transfer by developing the following projects:

- CASCA: A language for designing hardware countermeasures against side channel attacks. It is based on a final tagless approach for embedding domain specific languages.
- Polimi at Home (PAH): An experiment in MOOC for my students of Informatica B. It allows to learn a Matlab-like language through a set of small lectures and automatically graded exercises. It uses the EDX stack.
- 2PARMA Use case n. 6: Integration of various technologies from different project partners to create a video-analytics application.

- Multicube Explorer: Architectural exploration framework retargetable to different processor-based architectures and exploration algorithms. The tool contains also advanced algorithms for DoE generation and response surface modeling.
- xSTreamC compiler and nSTream simulator: Development toolchain for applications based on the stream oriented programming model.
- ST200-ISS: Production-grade instruction set simulator for the ST200 VLIW processor family (functional and timing behavior models). Kernel, device components, cache-coherency, secure-storage, co-hosting
- STBus Power estimation: Tools for run-time power estimation of STBus proprietary bus technology (C/SystemC). These tools are currently part of the internal STBus product work-flow

Known languages

- Italian: Native
- English: Fluent

Como — July 26, 2022

Vittorio Zaccaria

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Pubblicazioni

1. M. Molteni, P. Juergen, V. Zaccaria. *On robust strong-non-interferent low-latency multiplications*, IET Information Security, vol. 16(2), pp. 127 to 132. John Wiley and Sons Ltd on behalf of The Institution of Engineering and Technology. 2021.

2. M. Molteni, V. Zaccaria. *A relation calculus for reasoning about t-probing security*, Journal of Cryptographic Engineering, vol. 12, pp. 1 to 14. Springer, Berlin, Heidelberg. 2022.

3. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *DeSpErate++: An enhanced design space exploration framework using predictive simulation scheduling*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 34, pp. 293 to 306. IEEE - Piscataway, NJ - USA. 2015.

4. V. Zaccaria, F. Melzani, G. Bertoni. *Spectral features of higher-order side-channel countermeasures*, IEEE Transactions on Computers, vol. 67, pp. 596 to 603. IEEE - Piscataway, NJ - USA. April 2018.

5. L. Delledonne, V. Zaccaria, R. Susella, G. Bertoni, F. Melzani. *CASCA: A Design Automation Approach for Designing Hardware Countermeasures Against Side-Channel Attacks*, ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 23, pp. 69:1 to 69:17. ACM New York, NY - USA. November 2018.

6. E. Bisi, F. Melzani, V. Zaccaria. *Symbolic analysis of higher-order side channel countermeasures*, IEEE Transactions on Computers, vol. 66, pp. 1099 to 1105. IEEE - Piscataway, NJ - USA. June 2017.

7. S. Xydis, G. Palermo, V. Zaccaria, C. Silvano. *SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High-Level Synthesis*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 34, pp. 155 to 159. IEEE - Piscataway, NJ - USA. January 2015.

8. M. Molteni, V. Zaccaria. *On the spectral features of robust probing security*, IACR Transactions on Cryptographic Hardware and Embedded Systems, vol. 2020(4), pp. 24 to 48. IACR. August 2020.

9. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *ARTE: An Application-specific Run-Time managEment framework for multi-cores based on queuing models*, Parallel Computing, vol. 39, pp. 504 to 519. Elsevier - The Netherlands. September 2013.

10. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *Design Space Exploration and Run-time Resource Management for Multi-cores*, ACM Transactions on Embedded Computing Systems (TECS), vol. 13, pp. 20:1 to 20:27. ACM New York, NY - USA. September 2013.

11. S. Marceglia, S. Bonacina, V. Zaccaria, C. Pagliari, F. Pinciroli. *How might the iPad change healthcare?*, Journal of the Royal Society of Medicine, vol. 105, pp. 233 to 241. SAGE Publications. June 2012.

12. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria. *An Instruction-Level Energy Model for Embedded VLIW Architectures*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 22, pp. 998 to 1010. IEEE - Piscataway, NJ - USA. September 2002.

13. C. Ykman-couvreur, P. Avasare, G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *Linking run-time resource management of embedded multi-core platforms with automated design-time exploration*, Computers Digital Techniques, IET, vol. 5, pp. 123 to 135. IET. March 2011.

14. G. Palermo, C. Silvano, V. Zaccaria. *A Variability-Aware Robust Design Space Exploration Methodology for on-Chip Multiprocessors Subject to Application Specific Constraints*, ACM Transactions in Embedded Computing Systems, vol. 11, pp. 29:1 to 29:28. ACM New York, NY - USA. July 2012.

15. G. Palermo, C. Silvano, V. Zaccaria. *ReSPIR: A Response Surface-based Pareto Iterative Refinement for Application-Specific Design Space Exploration*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 28, pp. 1816 to 1829. IEEE - Piscataway, NJ - USA. December 2009.

16. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Reducing the Complexity of Instruction-Level Power Models for VLIW Processors*, Design Automation for Embedded Systems, vol. 10, pp. 49 to 67. Kluwer Academic Publishers - Boston. July 2006.

17. G. Palermo, C. Silvano, V. Zaccaria. *Multi-Objective Design Space Exploration of Embedded Systems*, Journal of Embedded Computing, vol. 1, pp. 305 to 316. IOS Press - The Netherlands. 2005.

18. C. Silvano, M. Monchiero, G. Palermo, M. Sami, V. Zaccaria, R. Zafalon. *Low-Power Branch Prediction Techniques for VLIW Architectures: A Compiler-Hints Based Approach*, Integration, The VLSI Journal, vol. 38, pp. 515 to 524. Elsevier - The Netherlands. January 2005.

19. L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria, R. Zafalon. *A Framework for Modeling and Estimating the Energy Dissipation of VLIW-based Embedded Systems*, Design Automation for Embedded Systems, vol. 7, pp. 183 to 203. Kluwer Academic Publishers - Boston. October 2002.

20. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Spaces*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 31, pp. 740 to 753. IEEE - Piscataway, NJ - USA. May 2012.

21. W. Fornaciari, D. Sciuto, C. Silvano, V. Zaccaria. *A Sensitivity-Based Design Space Exploration Methodology for Embedded Systems*, Design Automation for Embedded Systems, vol. 7, pp. 7 to 33. Kluwer Academic Publishers - Boston. September 2002.

22. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Low-Power Data Forwarding for VLIW Embedded Architectures*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, pp. 614 to 622. IEEE - Piscataway, NJ - USA. October 2002.

23. V. Zaccaria, M. Sami, D. Sciuto, C. Silvano. *Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems* , pp. 203. Kluwer Academic Publishers - Boston/Dordrecht/London - . April 2003.

24. A. Pagni, F. Lucini, D. Pau, A. Borneo, V. Zaccaria. *Process for translating instructions for an arm-type processor into instructions for a LX-type processor; relative translator device and computer program product*. Year: 2007, number: 7243213, country: US, status: granted.

25. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, D. Pau, R. Zafalon. *Processor architecture*. Year: 2005, number: 6889317, country: US, status: granted.

26. M. Molteni, V. Zaccaria, V. Ciriani. *ADD-based Spectral Analysis of Probing Security*, Proceedings of DATE 2022: International Conference on Design, Automation and Test in Europe held in Antwerp, Belgium, pp. 987 to 992. IEEE. March 2022.

27. V. Zaccaria, M. Molteni, F. Melzani, G. Bertoni. *Darth's Saber: A Key Exfiltration Attack for Symmetric Ciphers Using Laser Light*, Proceedings of FDTC 2018: Workshop on Fault Diagnosis and Tolerance in Cryptography held in Amsterdam, Netherlands, pp. 23 to 26. IEEE - Piscataway, NJ - USA. September 2018.

28. F. Daniel, M. Matera, V. Zaccaria, A. Dell'orto. *Toward Truly Personal Chatbots: On the Development of Custom Conversational Assistants*, Proceedings of the 1st International Workshop on Software Engineering for Cognitive Services held in Gothenburg, Sweden, pp. 31 to 36. ACM New York, NY - USA. 2018.

29. E. Paone, F. Robino, G. Palermo, V. Zaccaria, I. Sander, C. Silvano. *Customization of OpenCL Applications for Efficient Task Mapping Under Heterogeneous Platform Constraints*, Proceedings of DATE 2015: International Conference on Design, Automation and Test in Europe held in Grenoble, France, pp. 736 to 741. EDA Consortium. March 2015.

30. F. Daniel, M. Matera, E. Quintarelli, L. Tanca, V. Zaccaria. *Context-Aware Access to Heterogeneous Resources Through On-the-Fly Mashups*, Proceedings of CAISE 2018: Conference on Advanced Information Systems Engineering held in Tallinn, Estonia, pp. 119 to 134. Springer Cham. June 2018.

31. G. Massari, E. Paone, P. Bellasi, G. Palermo, V. Zaccaria, W. Fornaciari, C. Silvano. *Combining application adaptivity and system-wide Resource Management on multi-core platforms*, Proceedings of SAMOS 2014: XIVth International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation held in Samos, Greece, pp. 26 to 33. IEEE - Piscataway, NJ - USA. July 2014.

32. D. Gadioli, S. Libutti, G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano. *OpenCL Application Auto-tuning and Run-Time Resource Management for Multi-core Platforms*, Proceedings of ISPA 2014: IEEE International Symposium on Parallel and Distributed Processing with Applications held in Milan, Italy, pp. 127 to 133. IEEE - Piscataway, NJ - USA. August 2014.

33. E. Paone, D. Gadioli, G. Palermo, V. Zaccaria, C. Silvano. *Evaluating orthogonality between application auto-tuning and run-time resource management for adaptive OpenCL applications*, Proceedings of ASAP 2014: IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors held in Zurich, Switzerland, pp. 161 to 168. IEEE - Piscataway, NJ - USA. June 2014.

34. G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano. *Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures*, Proceedings of ARC 2014: Reconfigurable Computing: Architectures, Tools, and Applications - 10th International Symposium held in Vilamoura, Portugal, pp. 345 to 352. Springer Cham. April 2014.

35. G. Mariani, V. Sima, G. Palermo, V. Zaccaria, G. Marchiri, C. Silvano, K. Bertels. *Run-time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction*, Proceedings of FPL 2013: International Conference on Field Programmable Logic and Applications held in Porto, Portugal, pp. 1 to 8. IEEE - Piscataway, NJ - USA. September 2013.

36. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling*, Proceedings of DATE 2014: International Conference on Design, Automation and Test in Europe held in Dresden, Germany, pp. 1 to 4. IEEE - Piscataway, NJ - USA. March 2014.

37. A. Ashouri, V. Zaccaria, S. Xydis, G. Palermo, C. Silvano. *A Framework for Compiler Level Statistical Analysis over Customized VLIW Architecture*, Proceedings of VLSI-SoC 2013: International Conference on Very Large Scale Integration and System-on-Chip held in Instanbul, Turkey, pp. 124 to 129. ACM New York, NY - USA. October 2013.

38. E. Paone, G. Palermo, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou, T. Lepley. *An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to an Industrial Multi-Cluster Architecture*, Proceedings of CODES+ISSS 2012: International Conference on Hardware/Software codesign and System Synthesis held in Tampere, Finland, pp. 503 to 512. ACM New York, NY - USA. October 2012.

39. E. Paone, N. Vahabi, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou, T. Lepley. *Improving Simulation Speed and Accuracy for Many-Core Embedded Platforms with Ensemble Models*, Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe held in Grenoble, France, pp. 671 to 676. EDA Consortium. March 2013.

40. S. Xydis, G. Palermo, V. Zaccaria, C. Silvano. *A Meta-Model Assisted Coprocessor Synthesis Framework for Compiler/Architecture Parameters Customization*, Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe held in Grenoble, France, pp. 659 to 664. EDA Consortium. March 2013.

41. G. Palermo, C. Silvano, V. Zaccaria. *Power-Performance System-Level Exploration of a MicroSPARC2-Based Embedded Architecture*, Proceedings of DATE 2003 Designers Forum: IEEE Design, Automation and Test Conference in Europe held in Munich, Germany, pp. 20182. IEEE - Piscataway, NJ - USA. March 2003.

42. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J. Zins, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, H. Meyr, J. Ansari, P. Mahonen, B. Vanthournout. *Parallel Paradigms and Run-time Management Techniques for Many-core Architectures: 2PARMA Approach*, Proceedings of INDIN 2011: IEEE Conference on Industrial Informatics held in Caparicia, Lisbon Portugal, pp. 835 to 840. IEEE - Piscataway, NJ - USA. July 2011.

43. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *ARTE: an Application-specific Run-Time Management Framework for Multi-core Systems*, Proceedings of SASP 2011: IEEE Symposium on Application Specific Processors held in San Diego, CA - USA, pp. 86 to 93. IEEE - Piscataway, NJ - USA. June 2011.

44. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao, T. Shibin. *MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures*, Proceedings of ISVLSI 2010: IEEE Annual Symposium on VLSI held in Lixouri, Kefalonia - Greece, pp. 488 to 493. IEEE - Piscataway, NJ - USA. July 2010.

45. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Siorpaes, H. Huebert, B. Stabernack,

J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Meyr, J. Ansari, P. Mahonen, B. Vanthournout. *2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures*, Proceedings of ISVLSI 2010: IEEE Annual Symposium on VLSI held in Lixouri, Kefalonia - Greece, pp. 494 to 499. IEEE - Piscataway, NJ - USA. July 2010.

46. G. Mariani, A. Brankovic, J. Jovic, G. Palermo, V. Zaccaria, C. Silvano. *A Correlation-based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip*, Proceedings of DAC 2010: Design Automation Conference held in Anaheim, CA - USA, pp. 120 to 125. ACM New York, NY - USA. June 2010.

47. A. Gellert, A. Florea, L. Vintan, G. Palermo, V. Zaccaria, C. Silvano. *Energy-Performance Design Space Exploration of SMT Architectures Exploiting Selective Load Value Predictions*, Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe held in Dresden, Germany, pp. 271 to 274. ACM New York, NY - USA. March 2010.

48. G. Mariani, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, G. Palermo, C. Silvano, V. Zaccaria. *An industrial design space exploration framework for supporting run-time resource management on multi-core systems*, Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe held in Dresden, Germany, pp. 196 to 201. ACM New York, NY - USA. March 2010.

49. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *A Design Space Exploration Methodology Supporting Run-Time Resource Management for Multi-Processors System on-Chip*, Proceedings of IEEE Symposium on Application Specific Processors 2009 held in San Francisco, CA - USA, pp. 21 to 28. IEEE - Piscataway, NJ - USA. July 2009.

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51. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *Multiprocessor System-on-Chip Design Space Exploration based on Multi-level Modeling Techniques*, Proceedings of IEEE IC-SAMOS'09 - International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation held in Samos, Greece, pp. 118 to 124. IEEE - Piscataway, NJ - USA. July 2009.

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53. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *An Efficient Design Space Exploration Methodology for Multi-Cluster VLIW Architectures based on Artificial Neural Networks*, Proceedings of IFIP VLSI-SOC 2008: International Conference on Very Large Scale Integration held in Rhodes Island, Greece, pp. 213 to 218. . October 2008.

54. G. Palermo, C. Silvano, V. Zaccaria. *Discrete Particle Swarm Optimization for Multi-objective Design Space Exploration*, Proceedings of DSD 2008: IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools held in Parma, Italy, pp. 641 to 644. IEEE - Piscataway, NJ - USA. September 2008.

55. G. Palermo, C. Silvano, V. Zaccaria. *An Efficient Design Space Exploration Methodology for Multiprocessor SoC Architectures based on Response Surface Methods*, Proceedings of IC-SAMOS 2008: International Conference on Embedded Computer Systems Architectures, Modeling and Simulation held in Samos, Greece, pp. 150 to 157. IEEE - Piscataway, NJ - USA. July 2008.

56. G. Palermo, C. Silvano, V. Zaccaria. *An Efficient Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints*, Proceedings of SASP 2008: IEEE Symposium on Application Specific Processors held in Anaheim, CA - USA, pp. 75 to 82. IEEE - Piscataway, NJ - USA. June 2008.

57. A. Bona, V. Zaccaria, R. Zafalon. *System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip*, Proceedings of DATE 2004: IEEE Design, Automation and Test Conference in Europe held in Paris - France, pp. 318 to 323. IEEE - Piscataway, NJ - USA. February 2004.

58. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Energy estimation and optimization of embedded VLIW processors based on instruction clustering*, Proceedings of DAC 2002: Design Automation Conference held in New Orleans, LA - USA, pp. 886 to 891. ACM New York, NY - USA. June 2002.

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