Vittorio Zaccaria

CURRICULUM UPDATE - 2013 / 2018

Since 2013, I have expanded my interests to functional programming and domain specific languages with a focus on hardware synthesis. Recently (2017 and 2018) I have helped introduce some novel theoretical results in the field of cryptographic circuits which have been published on IEEE Transactions on Computers. In 2015 and 2017 I have been awarded with two grants from industrial partners for devising a reliable design methodology for cryptographic circuits protected against correlation power attacks.

GRANTS AS A PRINCIPAL INVESTIGATOR

- From 2017 to 2018 grant for **Metodologia e Strumenti per la Valutazione di Circuiti Crittografici** from STMicroelectronics, grant type: Grant from industrial partner,
- From 2015 to 2016 grant for **Strumenti di Progettazione e Verifica per Circuiti Crittografici** from STMicroelectronics, grant type: Grant from industrial partner

RESEARCH

Important publications from 2013

Spectral features of higher-order side-channel countermeasures. *V. Zaccaria, F. Melzani, G. Bertoni.* IEEE Transactions on Computers - 2018 -[Link]

Symbolic analysis of higher-order side channel countermeasures. *E. Bisi, F. Melzani, V. Zaccaria.* IEEE Transactions on Computers - 2017 -[Link]

SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High-Level Synthesis. *S. Xydis, G. Palermo, V. Zaccaria, C. Silvano.* IEEE Transactions on Computer Aided Design of Integrated Circuits - 2015 -[Link]

Design Space Exploration and Run-time Resource Management for Multi-cores. *G. Mariani, G. Palermo, V. Zaccaria, C. Silvano.* ACM Transactions on Embedded Computing Systems (TECS) - 2013 -[Link]

Other publications from 2013

On the Role of Context in the Design of Mobile Mashups. *V. Cassani, S. Gianelli, M. Matera, R. Medana, E. Quintarelli, L. Tanca, V. Zaccaria.* Rapid Mashup Development Tools: Second International Rapid Mashup Challenge, RMC 2016, Lugano, Switzerland, June 6, 2016, Revised Selected Papers - 2017 -[Link]

Combining application adaptivity and system-wide Resource Management on multi-core platforms. *G. Massari, E. Paone, P. Bellasi, G. Palermo, V. Zaccaria, W. Fornaciari, C. Silvano.* Proceedings of SAMOS 2014: XIVth International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation - 2014 -[Link]

OpenCL Application Auto-tuning and Run-Time Resource Management for Multi-core Platforms. *D. Gadioli, S. Libutti, G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano.* Proceedings of ISPA 2014: IEEE International Symposium on Parallel and Distributed Processing with Applications - 2014 -[Link]

Evaluating orthogonality between application auto-tuning and run-time resource management for adaptive OpenCL applications. *E. Paone, D. Gadioli, G. Palermo, V. Zaccaria, C. Silvano.* Proceedings of ASAP 2014: IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors - 2014 -[Link]

Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures. *G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano.* Proceedings of ARC 2014: Reconfigurable Computing: Architectures, Tools, and Applications - 10th International Symposium - 2014 -[Link]

Run-time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction. *G. Mariani, V. Sima, G. Palermo, V. Zaccaria, G. Marchiri, C. Silvano, K. Bertels.* Proceedings of FPL 2013: International Conference on Field Programmable Logic and Applications - 2013 -[Link]

DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling. *G. Mariani, G. Palermo, V. Zaccaria, C. Silvano.* Proceedings of DATE 2014: International Conference on Design, Automation and Test in Europe - 2014 -[Link]

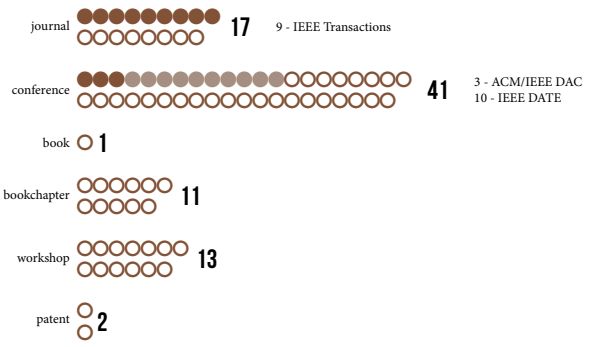
A Framework for Compiler Level Statistical Analysis over Customized VLIW Architecture. *A. Ashouri, V. Zaccaria, S. Xydis, G. Palermo, C. Silvano.* Proceedings of VLSI-SoC 2013: International Conference on Very Large Scale Integration and System-on-Chip - 2013 -[Link]

ARTE: An Application-specific Run-Time managEment framework for multi-cores based on queuing models. *G. Mariani, G. Palermo, V. Zaccaria, C. Silvano.* Parallel Computing - 2013 -[Link]

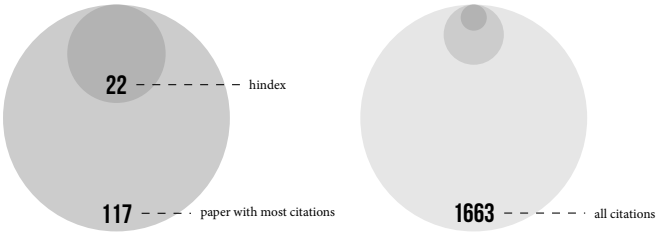
Improving Simulation Speed and Accuracy for Many-Core Embedded Platforms with Ensemble Models. *E. Paone, N. Vahabi, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou, T. Lepley.* Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe - 2013 -[Link]

A Meta-Model Assisted Coprocessor Synthesis Framework for Compiler/Architecture Parameters Customization. *S. Xydis, G. Palermo, V. Zaccaria, C. Silvano.* Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe - 2013 -[Link]

Publication statistics



Bibliometric indexes



From Google Scholar profile - February 22, 2018

TEACHING

Titolare

- **Informatica B** at Politecnico di Milano - titolare: Vittorio Zaccaria ('17/18, '16/17, '15/16, '14/15, '13/14, '12/13 - crediti totali: 42)

Teaching assistant (Esercitatore)

- **Informatica B** at Politecnico di Milano - titolare: Vittorio Zaccaria ('17/18, '16/17, '14/15) - ore totali: 74 ,
- **Hypermedia Applications (Web and multimedia)** at Politecnico di Milano - titolare: Franca Garzotto ('16/17) - ore totali: 20 ,
- **Architettura dei Calcolatori e Sistemi Operativi** at Politecnico di Milano - titolare: Roberto Negrini ('14/15, '13/14) - ore totali: 21

VITTORIO ZACCARIA

POLITECNICO DI MILANO - PIAZZA LEONARDO DA VINCI, 32 — ITALY

+39 02 2399 3642 — WWW.VITTORIOZACCARIA.NET

CV updated as of April 3, 2018

Education

- June 1998: Master in Computer engineering at Politecnico di Milano, Italy. Thesis topic: Java agents for a distributed file system.
- November 2002: Ph.D in Computer engineering at Politecnico di Milano, Italy. Thesis topic: "Power consumption estimation and optimization of VLIW processors. Sponsored by STMicroelectronics."

Current position

Assistant Professor at Politecnico di Milano - Milan, Italy.

Areas of specialization

Computer aided design of digital circuits. Multi-processor design space exploration. Low-power and high-performance design. Parallel processor architectures. Advanced parallel programming paradigms. Compilation and simulation methodologies for multi-processor-based systems.

Appointments held

2009 — : Assistant Professor, Politecnico di Milano - Milan, Italy

- Appointed as Principal Investigator for an industrial collaboration grant from STMicroelectronics related to the design cryptographic hardware using functional programming languages.
- Specified and developed the ReSPIR optimization algorithm for processor/SoC optimization. It enables efficient IP reuse in the context of virtual platforms (10x reduction in time, less than 1 percent error w.r.t. ideal).
- Succesfully brought a team of 5 people to prototype a new type of video-surveillance system in the context of the 2PARMA FP7 European Project.
- Led a team of 3 engineers to prototype a research software tool for processor customization. Prototypes were delivered on-time and within budget of several european FP7 projects.

2004 — 2007 : R&D Engineer, STMicroelectronics - Lugano, Switzerland

- Specified, prototyped and validated several ST200 processor architectural extensions. Vertical validation of the extensions from the ISA up to the application-layer/OS.
- Enabled secure co-hosting of more operating systems by means of secure storage extensions of the ST200 architecture.
- Collaborated to the specification, validation (by means of functional and timing simulation) and architectural exploration for symmetric multi-processing based on ST200.
- Architectural specification and design of multi-threaded architectures based on stream-programming paradigms.

2003 — 2004 : Research Consultant, STMicroelectronics - Milan, Italy

- Pioneered the field of Power Modeling of VLIW Cores (10 percent error RTL vs Gate-level).
- Introduced an effective methodology to minimize the effort of design of experiments for NoC power models (10x reduction in characterization time, 33 percent error).

2007 — 2009 : Research Associate, Politecnico di Milano - Milan, Italy

- Introduced advanced techniques for managing design of experiments and response surface methods in automatic design space exploration for multi-processors.
- Extended classical design space exploration to tackle the problem of process-variability-aware design of multi-processors.

Grants and funding

Period	*Grant type*	*Role*	*Project*	*Funding*
2017 - 2018	Grant from industrial partner STMicroelectronics	Principal investigator	Metodologia e Strumenti per la Valutazione di Circuiti Crittografici	30000 EUR
2015 - 2016	Grant from industrial partner STMicroelectronics	Principal investigator	Strumenti di Progettazione e Verifica per Circuiti Crittografici	30000 EUR
2001 - 2003	Post-Doc Grant Politecnico di Milano	Post Doc	Power estimation and exploration of the architectural space at the system level for systems-on-chip	
2007 - 2009	Research Grant Politecnico di Milano		Multi-Objective Design Space Exploration of Multi-Processor SOC Architectures for Embedded Multimedia Applications	
1999 - 2001	Ph.D. Fellowship STMicroelectronics		Methodologies for Power Estimation for VLIW Machines	

Teaching activity

He has been in full charge (*Titolare*) of the following courses

Academic year	*Course name*	*Credits*	*Level, Institution*
2010/2011	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2011/2012	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2012/2013	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2013/2014	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2014/2015	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2015/2016	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2016/2017	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2017/2018	Informatica B	7	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano

He has been teaching assistant ("esercitatore") for the following courses:

Academic year	*Course name*	*Hours*	*Level, Institution*
1999/2000	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2000/2001	Sistemi Operativi 1	15	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2000/2001	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2001/2002	Advanced Computer Architectures	20	Master of Science in Electrical Engineering, University of Illinois at Chicago and Politecnico di Milano
2001/2002	Calcolatori Elettronici	20	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2003/2003	Calcolatori Elettronici	20	Laurea quinquennale in Ingegneria Informatica, Politecnico di Milano
2008/2009	Informatica B	15	Laurea di primo livello in Ingegneria Elettrica, Politecnico di Milano
2009/2010	Informatica ed Elementi di Informatica Medica	17	Laurea di primo livello in Ingegneria Biomedica, Politecnico di Milano
2009/2010	Architectures for Multimedia Systems	20	Laurea specialistica in Ingegneria Informatica, Politecnico di Milano
2009/2010	Informatica B	11	Laurea di primo livello in Ingegneria Elettrica, Politecnico di Milano
2009/2010	Architettura dei Calcolatori e Sistemi Operativi	38	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2010/2011	Informatica ed Elementi di Informatica Medica	24	Laurea di primo livello in Ingegneria Biomedica, Politecnico di Milano
2013/2014	Architettura dei Calcolatori e Sistemi Operativi	11	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2014/2015	Informatica B	18	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2014/2015	Architettura dei Calcolatori e Sistemi Operativi	10	Laurea di primo livello in Ingegneria Informatica, Politecnico di Milano
2016/2017	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano
2016/2017	Hypermedia Applications (Web and multimedia)	20	Laurea magistrale in Ingegneria Informatica, Politecnico di Milano
2017/2018	Informatica B	28	Laurea di primo livello in Ingegneria Meccanica ed Energetica, Politecnico di Milano

Award, prizes academic honors

- 2002 - Dimitris N. Chorafas Award, for the exceptional contribution to the state of the art of research in processor architecture.
- 2010 - HiPEAC Award, as a co-author of 'A Correlation-Based Design Space Exploration Methodology for Multiprocessor Systems-on-Chip' published at DAC 2010.
- 2012 - Idea2Product, 2nd r. up, for creating a valuable opportunity for product commercialization of research results.

Graduate students co-advised

Since 2001, he co-advised the following students in their Master-equivalent theses:

1. 2016 — Stefano Gianelli and Valerio Cassani, Thesis title: *Progettazione di mashup per dispositivi mobili un metodo basato sulla modellazione di contesto.*
2. 2017 — Stefano Lucchi and Davide Fava, Thesis title: *Mash-up based service and data integration in the CAMUS framework.*
3. 2017 — Lorenzo Delledonne, Thesis title: *A methodology based on functional languages for the design of hardware cryptographic primitives resistant to side-channel attacks.*
4. Simone Borgio and Davide Bosisio, Thesis title: *OpenStreamC - a development framework for streaming applications.*
5. Zhong Yi Hu, Thesis title: *Power modeling of Networks-on-chip.*
6. Fabrizio Lucini, Thesis title: *Specification and design of a prefetch unit for translating code at run-time.*
7. Simone Valsecchi, Thesis title: *An algorithm for the efficient exploration of the architectural design space for microprocessor-based systems.*
8. Gianluca Palermo, Thesis title: *A methodology for architectural exploration and information encoding for low-power digital systems.*
9. Alessandro Molgora and Claudio Lozza, Thesis title: *Low-power state encoding techniques for finite state machines.*
10. Marco Gavazzi, Thesis title: *Low-power VLIW re-scheduling algorithms.*
11. Lorenzo Salvemini, Thesis title: *An architectural exploration methodology for low-power digital systems.*
12. Andrea Bona, Thesis title: *A design of experiments methodology in a power estimation flow for VLIW processors.*

He has overseen part of the work of the following Ph. D. students:

- Edoardo Paone, Politecnico di Milano
- Giovanni Mariani, ALaRI - University of Lugano
- Fabrizio Castro, Politecnico di Milano.

Research interests and historical achievements

Countermeasures against side-channel attacks.

This project started from an actual industrial need, i.e., providing the designer of cryptographic algorithms with guidelines and tools that make it possible to implement and validate the primitive while assessing the desired level of protection.

The problems with existing methods and tools that brought us to seek new approaches are just a few; first, high level specification/prototyping of the algorithm is decoupled from low level implementation. This brings a host of issues, among which the fact that manual translation can introduce subtle bugs and unanticipated behavior. Besides this, the specification is usually done in weakly typed languages, bringing additional source of unexpected behavior, test and refactoring complexity.

My main goal is to investigate how a strongly typed functional programming language could be used to build a DSLs to synthesize these kind of algorithms in hardware, by bridging the gap between spec and implementation with automatic tools.

Techniques to support teaching to a massive amount of students.

In 2014 I realized that my computer science class was undergoing a major challenge. The number of students was becoming huge and resource assignment from my university (in terms of teaching assistants funded by the university) was on a decreasing trend. In fact, the ratio between qualified teaching assistants (those who have a degree in computer engineering) and students had fallen below 1/100, making it hard to bring students to complete even the simplest hands-on lab. I always had the ambition to not leave anyone behind so I gradually started to study the current MOOC technologies to see whether they could be used to keep the students on track.

Currently, I am creating the first online course that is meant to complement the face to face lectures that I give. The course can be edited collaboratively by teachers (on Github) through a YAML based format that I designed; it can then be imported into an EDX server to be used by the students who can submit their homework to an automatic grader that I wrote using containerization technology.

Achievements:

- Developed a YAML-based format to author course contents.
- Used containerization technology to build an automatic graders.

Front-end development and mobile apps.

I have been always interested in ways to model complex program behavior such as parallel and asynchronous programming. It turns out that web and mobile application present a lot of challenges from this point of view being inherently asynchronous.

In this area I have collaborated with some researchers on the implementation of context-based applications for the customization of the user experience on mobile devices. This kind of application is characterized a query engine that fetches and mashes up data from different kind of services into a unified view on a native application. We decided to simplify the construction of the mobile application by shifting all the burden of service querying into the server. The mobile app uses then a flexible querying interface towards the server that minimizes data transfered across the network.

Power estimation and optimization of processor-based systems.

Since 1999, I have been interested into estimating and optimizing the power consumption of microprocessors and microprocessor-based systems.

Achievements:

- Developed an analytical model that takes into account software-level parameters (instruction ordering, pipeline stall probability and instruction cache miss probability) and micro-architectural-level ones (pipeline stage power per instruction).
- Validated the model on an industrial VLIW processor jointly designed by HPLabs and STMicroelectronics.
- Defined a register file write inhibition scheme that exploits the forwarding paths in VLIW processors.
- Designed a dynamic power management policy for general purpose operating systems.
- Designed a method for the exploration of the architectural parameters of the memory sub-systems, from the energy-delay joint perspective.
- Developed Multicube Explorer, a tool for experimenting with multi-objective exploration.
- Developed accurate performance and power modeling characterization of applications with emphasis on parallel processors architectures and network-on-chips.
- Developed optimal tuning of the memory hierarchy, processor parallelism (intra and inter-task) and processor interconnection network.
- Developed optimal software task mapping and scheduling onto the target processor units and optimal communication scheduling.
- Designed run-time design space exploration for trading-off quality-of-service with actual power constraints.
- Robust optimization with respect to several levels of uncertainties such as workload variability, model estimation accuracy and manufacturing process variability.
- Specified and implemented power characterization and high-level power estimation work-flows for the STBus Network on Chip. The STBus is a high-performance, low-latency on chip parameterizable network supported by production grade specification and synthesis tools.

Task Level Parallelism.

During my 4 years stint in the industry, I have worked on a variety of projects related to exploiting task level parallelism. I have had the opportunity to work within an international team on the entire stack of hardware and software design tools for an embedded processor.

Achievements:

- Specified and validated embedded shared-memory multi-processor systems.
- Designed run-time and operating system components including embedded co-hosting technology for the ST230 microprocessor.
- Studied and created a parallel programming framework for industrial multi-processor architectures.

- Specified secure storage extensions for embedded processors.
- Developed secure co-hosting solutions for industrial applications.
- Involved in the study and implementation of novel cryptographic power attack techniques based on cache-miss induction.

Current teaching goals

Troughout the years, I discovered that I love teaching by making students passionate about computer engineering. I like matching conventional methods for teaching with novel technology such as MOOcs. In particular, I am running a teaching experiment, called [Polimi at Home](http://www.pah.polimi.it), where regular students can follow on-line tutorials (based on EDX technology) and be automatically graded.

Professional activities

National and international research projects

He has been actively involved in the following european projects:

- 2010 - 2012, PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures
- 2008 - 2010, Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications

Program committee membership and referee services

Year	*Role*	*Institution*
2001	reviewer	DATE,
2007	reviewer	IC-SAMOS,
2007	reviewer	SASP,
2008	Local Committee	Micro, Como - Italy
2008	TPC member	NoCArch,
2008	TPC member	DATE - Track A8 (Multi-Core Platforms),
2009	TPC member	2PARMA Workshop (co-located with ARCS 2010),
2009	TPC member	NoCArch,
2009	reviewer	Journal of Low Power Electronics - JOLPE,
2009	Session Chair	DATE, Nice - France
2009	TPC member	DATE - Track A8 (Multi-Core Platforms),
2010	TPC member	NoCArch,
2010	Session Chair	DATE, Dresden - Germany
2011	TPC member	2PARMA Workshop (co-located with ARCS 2011), Como - Italy
2012	Keynote Speaker	ESTIMEDA, Tampere - Finland
2012	Program Co-Chair	2PARMA Workshop (co-located with ARCS 2012), Munich - Germany
2012	TPC member	NoCArch,
2014	TPC member	ADAPT (co-located with HIPEAC 2014),
2016	reviewer	ADAPT (co-located with HIPEAC 2016),
	reviewer	IEEE Transactions on Computer Aided Design of Integrated Circuits,
	reviewer	IEEE Transactions on Very Large Scale of Integration Circuits,
	reviewer	IEEE Transactions on Computers,

Innovation, technology transfer patents

He produced significant public-domain and industrial technology transfer by developing the following projects:

- Multicube Explorer — an architectural exploration framework retargetable to different processor-based architectures and exploration algorithms. The tool contains also advanced algorithms for DoE generation and response surface modeling. It is scheduled to go open-source in January 2009 — open-source.
- xSTreamC compiler and nSTream simulator — a development toolchain for applications based on the stream oriented programming model. The toolchain has been released open-source in October 2008 — open-source.
- ST200-ISS — a production-grade instruction set simulator for the ST200 VLIW processor family (functional and timing behavior models). Kernel, device components, cache-coherency, secure-storage, co-hosting — proprietary.
- Tools for run-time power estimation of STBus proprietary bus technology (C/SystemC). These tools are currently part of the internal STBus product work-flow — proprietary.

Known languages

- Italian: Native
- English: Fluent

Como — April 3, 2018

Vittorio Zaccaria

VITTORIO ZACCARIA

POLITECNICO DI MILANO - PIAZZA LEONARDO DA VINCI, 32 — ITALY

+39 02 2399 3642 — WWW.VITTORIOZACCARIA.NET

Pubblicazioni

1. V. Zaccaria, F. Melzani, G. Bertoni. *Spectral features of higher-order side-channel countermeasures*, IEEE Transactions on Computers, vol. 67, pp. 596 to 603. IEEE - Piscataway, NJ - USA. April 2018.

2. E. Bisi, F. Melzani, V. Zaccaria. *Symbolic analysis of higher-order side channel countermeasures*, IEEE Transactions on Computers, vol. 66, pp. 1099 to 1105. IEEE - Piscataway, NJ - USA. June 2017.

3. S. Xydis, G. Palermo, V. Zaccaria, C. Silvano. *SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High-Level Synthesis*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 34, pp. 155 to 159. IEEE - Piscataway, NJ - USA. January 2015.

4. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *ARTE: An Application-specific Run-Time managEment framework for multi-cores based on queuing models*, Parallel Computing, vol. 39, pp. 504 to 519. Elsevier - The Netherlands. September 2013.

5. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *Design Space Exploration and Run-time Resource Management for Multi-cores*, ACM Transactions on Embedded Computing Systems (TECS), vol. 13, pp. 20:1 to 20:27. ACM New York, NY - USA. September 2013.

6. S. Marceglia, S. Bonacina, V. Zaccaria, C. Pagliari, F. Pinciroli. *How might the iPad change healthcare?*, Journal of the Royal Society of Medicine, vol. 105, pp. 233 to 241. SAGE Publications. June 2012.

7. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria. *An Instruction-Level Energy Model for Embedded VLIW Architectures*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 22, pp. 998 to 1010. IEEE - Piscataway, NJ - USA. September 2002.

8. C. Ykman-couvreur, P. Avasare, G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *Linking run-time resource management of embedded multi-core platforms with automated design-time exploration*, Computers Digital Techniques, IET, vol. 5, pp. 123 to 135. IET. March 2011.

9. G. Palermo, C. Silvano, V. Zaccaria. *A Variability-Aware Robust Design Space Exploration Methodology for on-Chip Multiprocessors Subject to Application Specific Constraints*, ACM Transactions in Embedded Computing Systems, vol. 11, pp. 29:1 to 29:28. ACM New York, NY - USA. July 2012.

10. G. Palermo, C. Silvano, V. Zaccaria. *ReSPIR: A Response Surface-based Pareto Iterative Refinement for Application-Specific Design Space Exploration*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 28, pp. 1816 to 1829. IEEE - Piscataway, NJ - USA. December 2009.

11. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Reducing the Complexity of Instruction-Level Power Models for VLIW Processors*, Design Automation for Embedded Systems, vol. 10, pp. 49 to 67. Springer - The Netherlands. July 2006.

12. G. Palermo, C. Silvano, V. Zaccaria. *Multi-Objective Design Space Exploration of Embedded Systems*, Journal of Embedded Computing, vol. 1, pp. 305 to 316. IOS Press - The Netherlands. 2005.

13. C. Silvano, M. Monchiero, G. Palermo, M. Sami, V. Zaccaria, R. Zafalon. *Low-Power Branch Prediction Techniques for VLIW Architectures: A Compiler-Hints Based Approach*, Integration, The VLSI Journal, vol. 38, pp. 515 to 524. Elsevier - The Netherlands. January 2005.

14. L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria, R. Zafalon. *A Framework for Modeling and Estimating the Energy Dissipation of VLIW-based Embedded Systems*, Design Automation for Embedded Systems, vol. 7, pp. 183 to 203. Kluwer Academic Publishers - Boston. October 2002.

15. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Spaces*, IEEE Transactions on Computer Aided Design of Integrated Circuits, vol. 31, pp. 740 to 753. IEEE - Piscataway, NJ - USA. May 2012.

16. W. Fornaciari, D. Sciuto, C. Silvano, V. Zaccaria. *A Sensitivity-Based Design Space Exploration Methodology for Embedded Systems*, Design Automation for Embedded Systems, vol. 7, pp. 7 to 33. Kluwer Academic Publishers - Boston. September 2002.

17. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Low-Power Data Forwarding for VLIW Embedded Architectures*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, pp. 614 to 622. IEEE - Piscataway, NJ - USA. October 2002.

18. V. Zaccaria, M. Sami, D. Sciuto, C. Silvano. *Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems* , pp. 203. Kluwer Academic Publishers - Boston/Dordrecht/London - . April 2003.

19. A. Pagni, F. Lucini, D. Pau, A. Borneo, V. Zaccaria. *Process for translating instructions for an arm-type processor into instructions for a LX-type processor; relative translator device and computer program product*. Year: 2007, number: 7243213, country: US, status: granted.

20. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, D. Pau, R. Zafalon. *Processor architecture*. Year: 2005, number: 6889317, country: US, status: granted.

21. G. Massari, E. Paone, P. Bellasi, G. Palermo, V. Zaccaria, W. Fornaciari, C. Silvano. *Combining application adaptivity and system-wide Resource Management on multi-core platforms*, Proceedings of SAMOS 2014: XIVth International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, pp. 26 to 33. - Samos, Greece. July 2014.

22. D. Gadioli, S. Libutti, G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano. *OpenCL Application Auto-tuning and Run-Time Resource Management for Multi-core Platforms*, Proceedings of ISPA 2014: IEEE International Symposium on Parallel and Distributed Processing with Applications, pp. 127 to 133. IEEE - Piscataway, NJ - USA - Milan, Italy. August 2014.

23. E. Paone, D. Gadioli, G. Palermo, V. Zaccaria, C. Silvano. *Evaluating orthogonality between application auto-tuning and run-time resource management for adaptive OpenCL applications*, Proceedings of ASAP 2014: IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors, pp. 161 to 168. IEEE - Piscataway, NJ - USA - Zurich, Switzerland. June 2014.

24. G. Massari, E. Paone, M. Scandale, P. Bellasi, G. Palermo, V. Zaccaria, G. Agosta, W. Fornaciari, C. Silvano. *Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures*, Proceedings of ARC 2014: Reconfigurable Computing: Architectures, Tools, and Applications - 10th International Symposium, pp. 345 to 352. - Vilamoura, Portugal. April 2014.

25. G. Mariani, V. Sima, G. Palermo, V. Zaccaria, G. Marchiri, C. Silvano, K. Bertels. *Run-time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction*, Proceedings of FPL 2013: International Conference on Field Programmable Logic and Applications, pp. 1 to 8. - Porto, Portugal. September 2013.

26. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling*, Proceedings of DATE 2014: International Conference on Design, Automation and Test in Europe, pp. 1 to 4. - Dresden, Germany. March 2014.

27. A. Ashouri, V. Zaccaria, S. Xydis, G. Palermo, C. Silvano. *A Framework for Compiler Level Statistical Analysis over Customized VLIW Architecture*, Proceedings of VLSI-SoC 2013: International Conference on Very Large Scale Integration and System-on-Chip, pp. 124 to 129. - Instanbul, Turkey. October 2013.

28. E. Paone, G. Palermo, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou, T. Lepley. *An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to an Industrial Multi-Cluster Architecture*, Proceedings of CODES+ISSS 2012: International Conference on Hardware/Software codesign and System Synthesis, pp. 503 to 512. ACM New York, NY - USA - . 2012.

29. E. Paone, N. Vahabi, V. Zaccaria, C. Silvano, D. Melpignano, G. Haugou, T. Lepley. *Improving Simulation Speed and Accuracy for Many-Core Embedded Platforms with Ensemble Models*, Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe, pp. 671 to 676. - . March 2013.

30. S. Xydis, G. Palermo, V. Zaccaria, C. Silvano. *A Meta-Model Assisted Coprocessor Synthesis Framework for Compiler/Architecture Parameters Customization*, Proceedings of DATE 2013: International Conference on Design, Automation and Test in Europe, pp. 659 to 664. - . March 2013.

31. G. Palermo, C. Silvano, V. Zaccaria. *Power-Performance System-Level Exploration of a MicroSPARC2-Based Embedded Architecture*, Proceedings of DATE 2003 Designers Forum: IEEE Design, Automation and Test Conference in Europe, pp. 20182. - Munich, Germany. March 2003.

32. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J. Zins, D. Siorpaes, H. Huebert, B. Stabernack,

J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, H. Meyr, J. Ansari, P. Mahonen, B. Vanthournout. *Parallel Paradigms and Run-time Management Techniques for Many-core Architectures: 2PARMA Approach*, Proceedings of INDIN 2011: IEEE Conference on Industrial Informatics, pp. 835 to 840. - Caparicia, Lisbon Portugal. July 2011.

33. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *ARTE: an Application-specific Run-Time Management Framework for Multi-core Systems*, Proceedings of SASP 2011: IEEE Symposium on Application Specific Processors, pp. 86 to 93. - San Diego, CA - USA. June 2011.

34. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao, T. Shibin. *MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures*, Proceedings of ISVLSI 2010: IEEE Annual Symposium on VLSI, pp. 488 to 493. - Lixouri, Kefalonia - Greece. July 2010.

35. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Meyr, J. Ansari, P. Mahonen, B. Vanthournout. *2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures*, Proceedings of ISVLSI 2010: IEEE Annual Symposium on VLSI, pp. 494 to 499. - Lixouri, Kefalonia - Greece. July 2010.

36. G. Mariani, A. Brankovic, J. Jovic, G. Palermo, V. Zaccaria, C. Silvano. *A Correlation-based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip*, Proceedings of DAC 2010: Design Automation Conference, pp. 120 to 125. - Anaheim, CA - USA. June 2010.

37. A. Gellert, A. Florea, L. Vintan, G. Palermo, V. Zaccaria, C. Silvano. *Energy-Performance Design Space Exploration of SMT Architectures Exploiting Selective Load Value Predictions*, Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe, pp. 271 to 274. - Dresden, Germany. March 2010.

38. G. Mariani, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, G. Palermo, C. Silvano, V. Zaccaria. *An industrial design space exploration framework for supporting run-time resource management on multi-core systems*, Proceedings of DATE 2010: IEEE Design, Automation and Test Conference in Europe, pp. 196 to 201. - Dresden, Germany. March 2010.

39. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *A Design Space Exploration Methodology Supporting Run-Time Resource Management for Multi-Processors System on-Chip*, Proceedings of IEEE Symposium on Application Specific Processors 2009, pp. 21 to 28. - San Francisco, CA - USA. July 2009.

40. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *Meta-model Assisted Optimization for Design Space Exploration of Multi-Processor Systems-on-Chip*, Proceedings of Euromicro Conference on Digital System Design (DSD), pp. 383 to 389. - Patras, Greece. August 2009.

41. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *Multiprocessor System-on-Chip Design Space Exploration based on Multi-level Modeling Techniques*, Proceedings of IEEE IC-SAMOS'09 - International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation, pp. 118 to 124. - Samos, Greece. July 2009.

42. G. Palermo, C. Silvano, V. Zaccaria. *Variability-Aware Robust Design Space Exploration of Chip Multiprocessor Architectures*, Proceedings of IEEE/ACM ASPDAC 2009: Asia and South Pacific Design Automation Conference, pp. 323 to 328. - Yokohama, Japan. January 2009.

43. G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *An Efficient Design Space Exploration Methodology for Multi-Cluster VLIW Architectures based on Artificial Neural Networks*, Proceedings of IFIP VLSI-SOC 2008: International Conference on Very Large Scale Integration, pp. 213 to 218. - Rhodes Island, Greece. October 2008.

44. G. Palermo, C. Silvano, V. Zaccaria. *Discrete Particle Swarm Optimization for Multi-objective Design Space Exploration*, Proceedings of DSD 2008: IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools, pp. 641 to 644. - Parma, Italy. September 2008.

45. G. Palermo, C. Silvano, V. Zaccaria. *An Efficient Design Space Exploration Methodology for Multiprocessor SoC Architectures based on Response Surface Methods*, Proceedings of IC-SAMOS 2008: International Conference on Embedded Computer Systems Architectures, Modeling and Simulation, pp. 150 to 157. - Samos, Greece. July 2008.

46. G. Palermo, C. Silvano, V. Zaccaria. *An Efficient Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints*, Proceedings of SASP 2008: IEEE Symposium on Application Specific Processors, pp. 75 to 82. - Anaheim, CA - USA. June 2008.

47. A. Bona, V. Zaccaria, R. Zafalon. *System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip*, Proceedings of DATE 2004: IEEE Design, Automation and Test Conference in Europe, pp. 318 to 323. - Paris - France. February 2004.

48. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Energy estimation and optimization of embedded VLIW processors based on instruction clustering*, Proceedings of DAC 2002: Design Automation Conference, pp. 886 to 891. - New Orleans, LA - USA. June 2002.

49. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria. *Instruction-Level Power Estimation for Embedded VLIW Cores*, Proceedings of CODES-2000: 8th ACM/IEEE International Workshop on Hardware/Software Co-Design, pp. 34 to 38. - San Diego, CA - USA. May 2000.

50. G. Bertoni, V. Zaccaria, L. Breveglieri, M. Monchiero, G. Palermo. *AES Power Attack Based on Induced Cache Miss and Countermeasure*, Proceedings of ITCC 2005: International conference on Information Technology, pp. 586 to 591. - Las Vegas, NV - USA. April 2005.

51. W. Fornaciari, D. Sciuto, C. Silvano, V. Zaccaria. *A Design Framework to Efficiently Explore Energy-Delay Tradeoffs*, Proceedings of CODES 2001: 9th ACM/IEEE International Symposium on Hardware/Software Co-Design, pp. 260 to 265. - Copenhagen, Denmark. April 2001.

52. M. Monchiero, G. Palermo, M. Sami, C. Silvano, V. Zaccaria, R. Zafalon. *Power-Aware Branch Prediction Techniques: A Compiler-Hints Based Approach for VLIW Processors*, Proceedings of GLSVLSI 2004: Great Lakes Symposium on VLSI, pp. 440 to 443. - Boston, MA - USA. April 2004.

53. G. Bertoni, A. Bircan, L. Breveglieri, P. Fragneto, M. Macchetti, V. Zaccaria. *About the performance of the advanced encryption standard in embedded systems with cache memory*, Proceedings of ISCAS 2003: IEEE Int. Symposium on Circuits and Systems, pp. 145 to 148. - Bangkok, Thailand. May 2003.

54. G. Palermo, C. Silvano, S. Valsecchi, V. Zaccaria. *A System-Level Methodology for Fast Multi-Objective Design Space Exploration*, Proceedings of GLSVLSI 2003: Great Lakes Symposium on VLSI, pp. 92 to 95. - Washington, DC - USA. April 2003.

55. G. Palermo, C. Silvano, V. Zaccaria, R. Zafalon. *Branch Prediction Techniques for Low-Power VLIW Processors*, Proceedings of GLSVLSI 2003: Great Lakes Symposium on VLSI, pp. 225 to 228. - Washington, DC - USA. April 2003.

56. G. Mariani, V. Sima, G. Palermo, V. Zaccaria, C. Silvano, K. Bertels. *Using multi-objective design space exploration to enable run-time resource management for reconfigurable architectures*, Proceedings of DATE 2012: IEEE Design, Automation and Test Conference in Europe, pp. 1379 to 1384. IEEE - Piscataway, NJ - USA - Dresden, Germany. March 2012.

57. L. Salvemini, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *A Methodology for the Efficient Architectural Exploration of Energy-Delay Trade-offs for Embedded Systems*, Proceedings of SAC 2003: Symposium on Applied Computing, pp. 672 to 678. - Melbourne, FL - USA. March 2003.

58. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria. *Power Exploration for Embedded VLIW Architectures*, Proceedings of ICCAD-2000: IEEE/ACM Int. Conference on Computer Aided Design, pp. 498 to 503. - San Jose, CA - USA. November 2000.

59. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *An instruction-level methodology for power estimation and optimization of embedded VLIW cores*, Proceedings of DATE 2002: IEEE Design, Automation and Test Conference in Europe, pp. 1128 to 1128. - Paris, France. March 2002.

60. W. Fornaciari, D. Sciuto, C. Silvano, V. Zaccaria. *Fast System-Level Exploration of Memory Architectures Driven by Energy-Delay Metrics*, Proceedings of ISCAS 2001: IEEE Int. Symposium on Circuits and Systems, pp. 502 to 505. - Sydney, Australia. May 2001.

61. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon. *Exploiting Data Forwarding to Reduce the Power Budget of VLIW Embedded Processors*, Proceedings of DATE 2001: IEEE Design, Automation and Test Conference in Europe, pp. 252 to 257. - Munich, Germany. March 2001.

62. V. Cassani, S. Gianelli, M. Matera, R. Medana, E. Quintarelli, L. Tanca, V. Zaccaria. *On the Role of Context in the Design of Mobile Mashups* , pp. 108 to 128 in *Rapid Mashup Development Tools: Second International Rapid Mashup Challenge, RMC 2016, Lugano, Switzerland, June 6, 2016, Revised Selected Papers*. Springer International Publishing - Cham. January 2017.

63. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao, T. Shibin. *MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures* , pp. 47 to 63 in *Lecture

Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.)*. Springer Science+Businness Media - . 2011.

64. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Melpignano, J. Zins, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Meyr, J. Ansari, P. Mahonen, B. Vanthournout. *2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures* , pp. 65 to 79 in *Lecture Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.)*. Springer Science+Businness Media - . 2011.

65. G. Mariani, C. Ykman-couvreur, P. Avasare, G. Vanmeerbeeck, G. Palermo, C. Silvano, V. Zaccaria. *Design Space Exploration for Run-time Management of a Reconfigurable System for Video Streaming* , pp. 189 to 204 in *Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)*. Springer Science+Businness Media - . 2011.

66. C. Kavka, L. Onesti, E. Rigoni, A. Turco, S. Bocchio, F. Castro, G. Palermo, C. Silvano, V. Zaccaria, G. Mariani, F. Dongrui, Z. Hao, T. Shibin. *Design Space Exploration of Parallel Architectures* , pp. 171 to 187 in *Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)*. Springer Science+Businness Media - . 2011.

67. P. Avasare, C. Ykman-couvreur, G. Vanmeerbeeck, G. Mariani, G. Palermo, C. Silvano, V. Zaccaria. *Design Space Exploration Supporting Run-Time Resource Management* , pp. 93 to 107 in *Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)*. Springer Science+Businness Media - . 2011.

68. G. Palermo, C. Silvano, V. Zaccaria, E. Rigoni, C. Kavka, A. Turco, G. Mariani. *Response Surface Modeling for Design Space Exploration of Embedded Systems* , pp. 75 to 91 in *Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)*. Springer Science+Businness Media - . 2011.

69. E. Rigoni, C. Kavka, A. Turco, G. Palermo, C. Silvano, V. Zaccaria, G. Mariani. *Optimization Algorithms for Design Space Exploration of Embedded Systems* , pp. 51 to 73 in *Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)*. Springer Science+Businness Media - . 2011.

70. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao. *The MULTICUBE Design Flow* , pp. 3 to 17 in *Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.)*. Springer Science+Businness Media - . 2011.

71. G. Bertoni, L. Breveglieri, M. Monchiero, G. Palermo, V. Zaccaria. *A Power Attack Methodology to AES Based on Induced Cache Misses: Procedure, Evaluation and Possible Countermeasures* , pp. 37 to 52 in *New Trends in Cryptographic Systems, N. Nedjah and L.M. Mourelle (Eds.)*. Nova Science Publishers - . 2006.

72. A. Bona, V. Zaccaria, R. Zafalon. *System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip* , pp. 233 to 254 in *Ultra Low-Power Electronics and Design, E. Macii (ed.)*. Springer US - . 2004.

73. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J. Zins, H. Hubert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, I. Anagnostopoulos, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, J. Ansari, P. Mahonen, B. Vanthournout. *Parallel paradigms and run-time management techniques for many-core architectures: the 2PARMA approach* , Proceedings of INA-OCMC 2012: Interconnection Network Architecture: On-Chip, Multi-Chip, pp. 39 to 42. - Paris, France. January 2012.

74. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J. Zins, H. Hubert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-couvreur, I. Anagnostopoulos, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, J. Ansari, P. Mahonen, B. Vanthournout. *Invited paper: Parallel programming and run-time resource management framework for many-core platforms: The 2PARMA approach* , Proceedings of ReCoSoC 2011: Reconfigurable Communication-centric Systems-on-Chip, pp. 1 to 7. - . June 2011.

75. G. Mariani, G. Palermo, V. Zaccaria, C. Silvano. *Evaluating Run-time Resource Management Policies for Multi-core Embedded Platforms with the EMME Evaluation Framework* , Proceedings of the ARCS Workshops 2012, pp. 363 to 374. - . February 2012.

76. D. Matos, G. Palermo, V. Zaccaria, C. Reinbrecht, A. Susin, C. Silvano, L. Carro. *Floorplanning-aware design space exploration for application-specific hierarchical networks on-chip* , Proceedings of NoCArc 2011: 4th International Workshop on Network on Chip Architectures, pp. 31 to 36. - Porto Alegre, Brazil. December 2011.

77. V. Zaccaria, G. Palermo, F. Castro, C. Silvano, G. Mariani. *Multicube Explorer: An Open Source Framework for Design Space Exploration of Chip Multi-Processors* , Proceedings of 2PARMA: Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures, pp. 325 to 331. - Hannover, Germany. February 2010.

78. A. Choudury, G. Palermo, C. Silvano, V. Zaccaria. *Yield Enhancement by Robust Application-specific Mapping on Network-on-Chips* , Proceedings of NoCArc '09: International Workshop on Network on Chip Architectures, pp. 37 to 42. - New York, NY - USA. December 2009.

79. G. Palermo, C. Silvano, V. Zaccaria. *A DoE/RSM-based Strategy for an Efficient Design Space Exploration targeted to CMPs* , Proceedings of RAPIDO 2009: Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools. - Paphos, Cyprus. January 2009.

80. V. Zaccaria. *Data Flow Deadlock Avoidance for Streaming Applications Mapped on Network-on-Chips* , Workshop on Streaming Systems: From Web and Enterprise to Multicore (in conjunction with IEEE/ACM Micro-41), Como, Italy. - . November 2008.

81. G. Palermo, C. Silvano, V. Zaccaria. *Robust Optimization of SoC Architectures: A Multi-Scenario Approach* , Proceedings of ESTIMEDIA 2008: IEEE/ACM/IFIP Workshop on Embedded Systems for Real-Time Multimedia, pp. 7 to 12. - Atlanta, GA - USA. October 2008.

82. L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria, R. Zafalon. *A Power Modeling and Estimation Framework for VLIW-based Embedded Systems* , Proceedings of PATMOS 2001: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation. - Yverdon-les-Bains, Switzerland. September 2001.

83. A. Bona, V. Zaccaria, R. Zafalon. *Low Effort, High Accuracy Network-on-Chip Power Macro Modeling* , Proceedings of PATMOS 2004: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 541 to 552. - Isle of Santorini, Greece. September 2004.

84. G. Palermo, C. Silvano, V. Zaccaria. *A Flexible Framework for Fast Multi-Objective Design Space Exploration of Embedded Systems* , Proceedings of PATMOS 2003: IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 249 to 258. - Torino, Italy. September 2003.

85. W. Fornaciari, V. Piuri, A. Prestileo, V. Zaccaria. *An Agent-based Approach to Full Interoperability and Allocation Transparency in Distributed File Systems* , Proceedings of MATA 2001: Third International Workshop On Mobile Agents For Telecommunication Applications, pp. 153 to 162. - Monreal, Canada. August 2001.

Como — 3 aprile 2018

Vittorio Zaccaria