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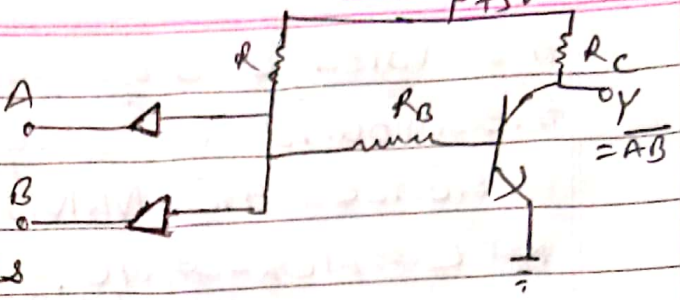
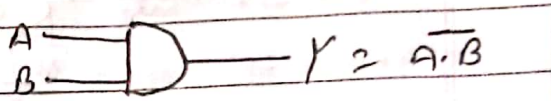
DTL NAND gate :



The ckt diagram for the DTL NAND gate has been shown in the fig.



Let us take the truth table the ckt operation has been described below :

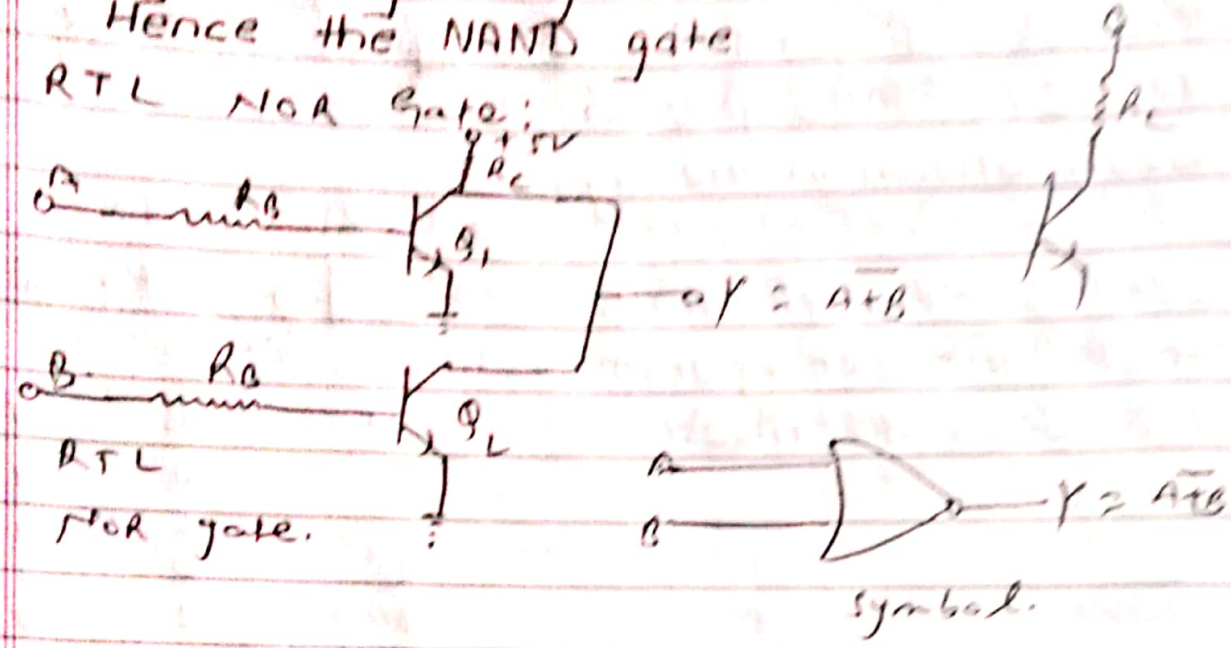
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

When both A and B inputs are low, both the diodes are grounded and the supply +5V passes through them to the ground. Hence there is no voltage drop across R_B, the transistor remains unbiased and hence the voltage drop across R_C appears in the output as $Y = 1$. For the entries $A = 0$, $B = 1$; The voltage drops across R. Hence no voltage drop across R_B, the transistor remains off and the voltage drop across R_C appears in the output yielding $Y = 1$. For $A = 1$, $B = 0$, the similar case as explained above in the 2nd entry happens and $Y = 1$. For the last entry $A = 1$, $B = 1$, both the diodes are reverse biased. There is voltage drop across R_B, the transistor is biased, it conducts and hence

the voltage drop across R_c by passes to the ground yielding $Y = 0$.

Hence the NAND gate

RTL NOR Gate:



The RTL ckt for the NOR gate has been outlined in the fig. The truth table for the NOR gate is given below:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

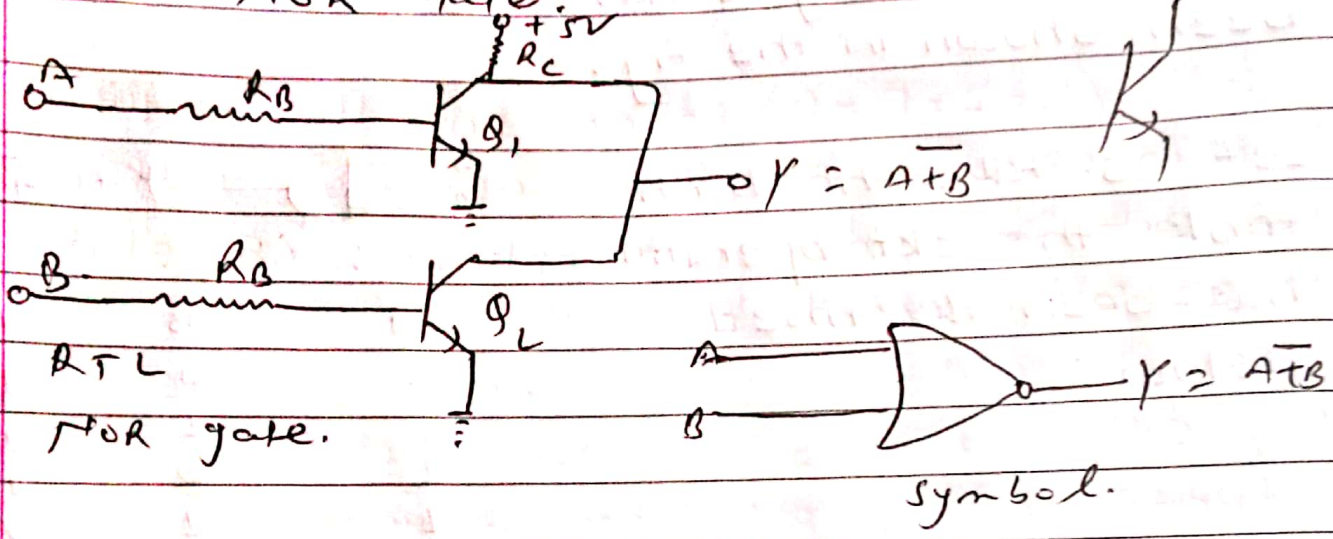
For the first entry, $A = 0$, $B = 0$, no voltage drops across base resistors R_B and hence both the transistors remain off. Hence the supply voltage across R_c appears in the output and $Y = 1$.

For the 2nd entry, $A = 0$, $B = 1$, the upper transistor remains off while there is voltage drop across R_B R_B of the lower base resistor that biases

the voltage drop across R_C by passes to the ground yielding Y = 0.

Hence the NAND gate

RTL NOR Gate:



The RTL ckt for the NOR gate has been outlined in the fig. The truth table for the NOR gate is given below:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

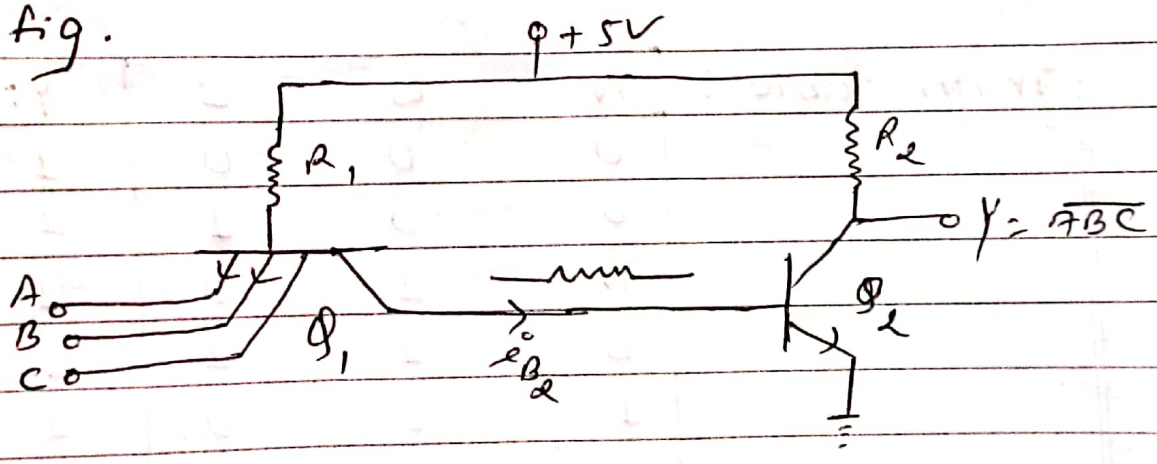
For the first entry, A = 0, B = 0, no voltage drops across base resistors R_B and hence both the transistors remain off. Hence the supply voltage across R_C appears in the output and Y = 1.

For the 2nd entry, A = 0, B = 1, the upper transistor remains off while there is voltage drop across R_B R_B of the lower base resistor that biases

the lower transistor, it conducts and the supply voltage by passes thereby giving Y=0. For the 3rd entry A=1, B=0; the same thing happens as in the 2nd entry. For the last entry A=1, B=1 both the transistors bias by the voltage drops across R_B and the supply voltage across R_C passes to the ground thereby giving Y=0. Hence the NOR gate.

TTL NAND gate:

The TTL NAND ckt has been outlined in the fig.



Q_1 is the transistor with multiple emitter inputs (A, B, C). When one of the inputs (A or B or C) is low, the supply voltage drop across R_1 biases the PN junction of Base-emitter of Q_1 and passes to the ground. Hence Q_2 is unbiased, it remains OFF and the voltage seeing across R_2

appears in the output i.e. Y = 1.
When any two of the inputs or all the inputs are low, the same situation appears as described above and hence Y = 1 again.

When all the inputs (A = B = C = 1), the base-emitter junction of Q_1 is reverse biased while Base-collector junction of the same transistor is forward biased. Hence transister Q_2 remains forward biased and the supply voltage across R_c goes to the ground thereby ~~providi~~ producing a low output i.e. Y = 0

Truth table :

A	B	C	Y = ~~ABC~~
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0