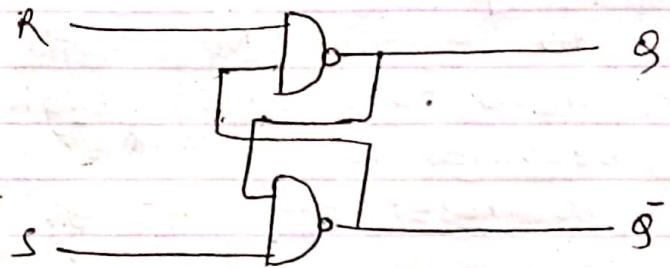


Memory Circuits

The basic memory circuit is called the Flip-Flop that has two stable states. Hence a Flip-Flop is a bistable electronic circuit whose output is either 0 or 1. Hence a Flip-Flop has memory as its output remains as set until something is done to change it.

There are different Flip-Flops. Here we are going to discuss two basic Flip-Flops; 'RS Flip-Flop' and 'Data Flip-Flop' (or D Flip-Flop)

- ① RS Flip-Flop (or Latch): The RS Flip-Flop (Reset set Flip-Flop) using NAND gates has been shown in the fig



R	S	Q	Action
0	0	?	Forbidden
0	1	1	SET
1	0	0	RESET
1	1	Last value	No change

To aid your understanding of the operation of the circuit, recall that a logic 0 at any input of a NAND gate forces its output to a logic 1.

The input condition $R=0, S=0$, is forbidden as it forces the output of both NAND gates to the high state i.e., $Q=1, \bar{Q}=1$ that violates the basic definition of the Flip-Flop. Hence it is generally never agreed to impose such a condition.

For $R=0, S=1$ forces the output of NAND gate A high. Now both inputs of NAND gate B are high resulting low output at \bar{Q} i.e., $Q=1, \bar{Q}=0$, and 1 is set at Q.

For the input $R=1, S=0$ forces lower NAND gate to be high. Now both inputs for the upper NAND gate being high, the output Q becomes low i.e., $Q=0, \bar{Q}=1$ and there is reset of 0 at Q.

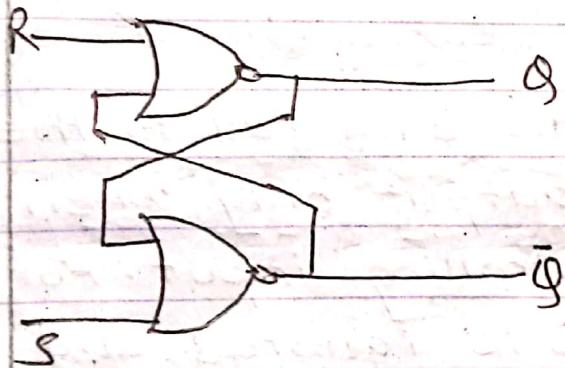
For the final entry

$R=1, S=1$, there is no effect on the output of the NAND gate, the Flip-Flop simply remains in its own present state i.e., Q remains unchanged (the last state). Hence the peculiarity of latch occurs here.

RS Flip-Flop (Using NOR gate)

The RS Flip-Flop or latch using a NOR gate is explained in a similar way as in the NAND gate above.

To aid the understanding of the operation, it is to recall that a logic 1 at any input of a NOR gate forces its output to a logic 0.



R	S	Q	Action
0	0	last value	No change
0	1	1	SET
1	0	0	RESET
1	1	?	Forbidden

The D Flip-Flop

It is the slight modification on latch where there is no need to activate the inputs. Fig below shown an outline of the D Flip-Flop.

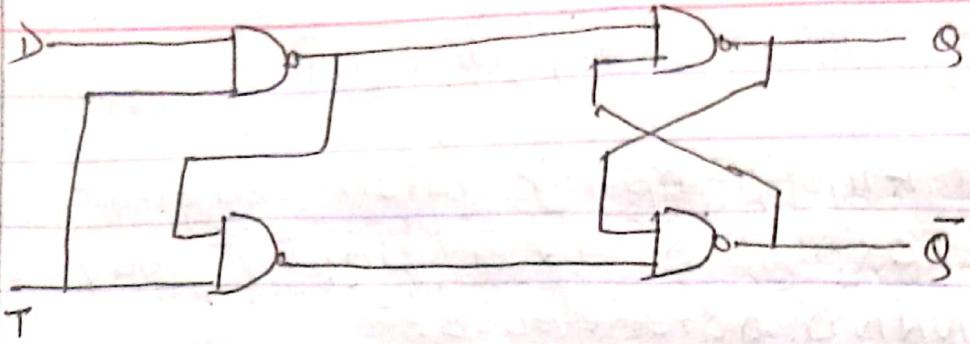


Fig memory circuit showing the data Flip-Flop constructed with four NAND gates.

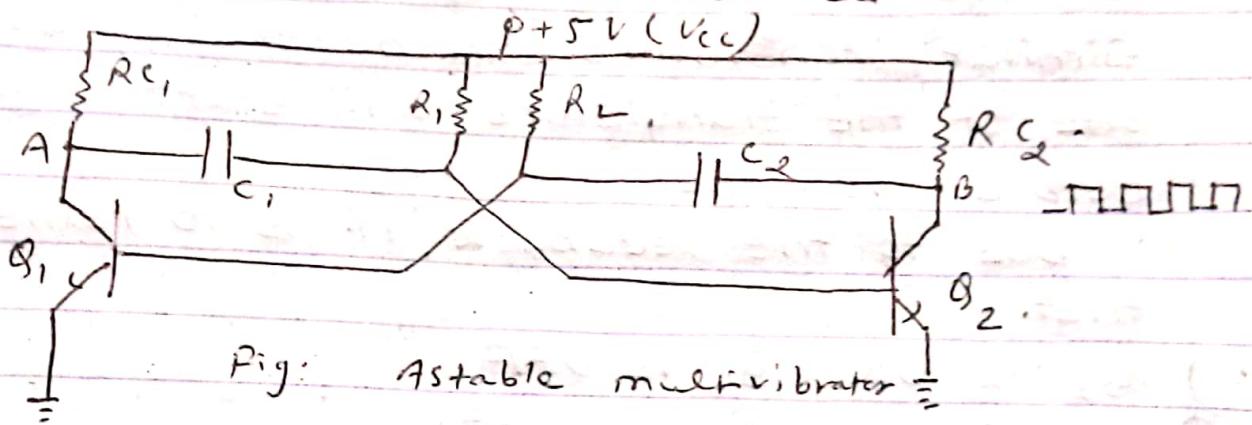
In the D Flip-Flop, the data fed to the D input is stored as output only when $T = 1$. Here T is the controlling input. For $T = 0$, the data fed to D is ignored and remains in the previous state.

Let $D = 1$, $T = 1$. The first NAND gate yields 0 output and the gate 2 yield 1 output. Hence 0 input to gate 3 yield $Q = 1$ and high inputs (1, 1) to gate 4 yields $\bar{Q} = 0$.

Let $T = 0$ and D is removed ($D = 0$), then the output remains unchanged. Again when $T = 1$ with D same ($D = 0$), then $Q = 0$ and $\bar{Q} = 1$ i.e. the output is changed.

Hence $T = 1$ causes something new to happen in the output.

In this way, the D Flip-Flop stores the data fed into the D at Q only when $T=1$ and keeps it until the new data is fed.



Clock Circuit:

Clock circuits are used to generate periodic pulses to drive gates in digital instruments. Multivibrators are used to generate pulses.

1. Astable Multivibrator:

The astable multivibrators using two transistors has been outlined in the fig above. It consists of two CE amplifier stages with positive feedback to each other of unit feedback ratio. Because of the strong feedback signal, the transistors are driven either to Saturation or to cut-off.

Circuit Operation :

As the characteristics of no two seemingly similar transistors can be exactly alike, one of the transistors will start conducting before the other.

Due to the feedback, it is to remember that

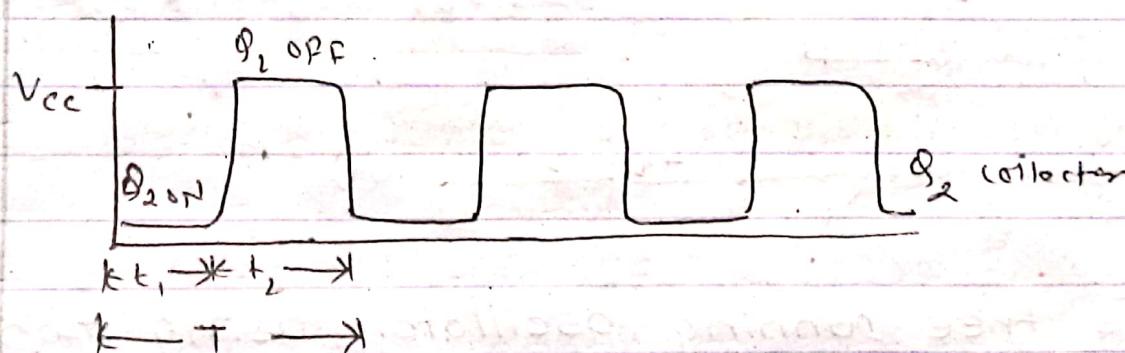
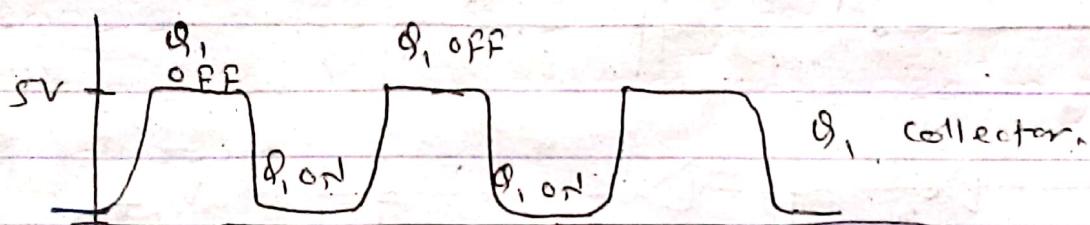
- ① Q_1 is ON, Q_2 is OFF.
- ② Q_2 is ON, Q_1 is OFF.

Let the supply voltage ($V_{cc} = +5V$) is given and the followings be the consequences:

- ① Suppose Q_1 conducts first, it saturates and A is at ground potential. The supply voltage drops across RC_1 .
- ② Q_2 is OFF, no current is conducted through it and hence no potential across RC_2 and hence point B is found at 5V still.
- ③ Now C_1 changes through R_1 to 5V (V_{cc}).
- ④ When voltage across C_1 rises sufficiently, Q_2 is forward biased, it conducts current and point B is at zero potential.
- ⑤ V_{C_1} goes on decreasing and becomes zero when Q_2 is saturated. There is OV at B, and hence Q_1 is turned OFF.

- ⑥ Beginning of the charging of C_2 through R_2 occurs.
- ⑦ The charge greater than (0.7V) at C_2 biases Q_1 , it saturates and soon there is zero charge at C_2 and A is at 0V thereby causing Q_2 OFF.

Since the transistors are driven either to saturation or to cut-off alternately, the voltage wave forms at either collector is essentially a square wave form with a peak amplitude of 5V (The 0V and 5V at either collector alternately)



Switching Times:

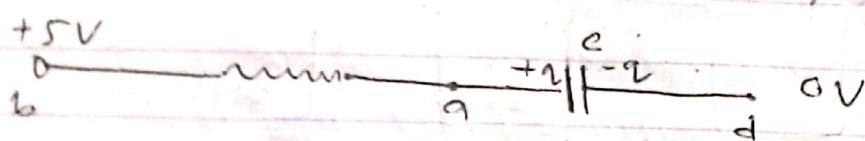
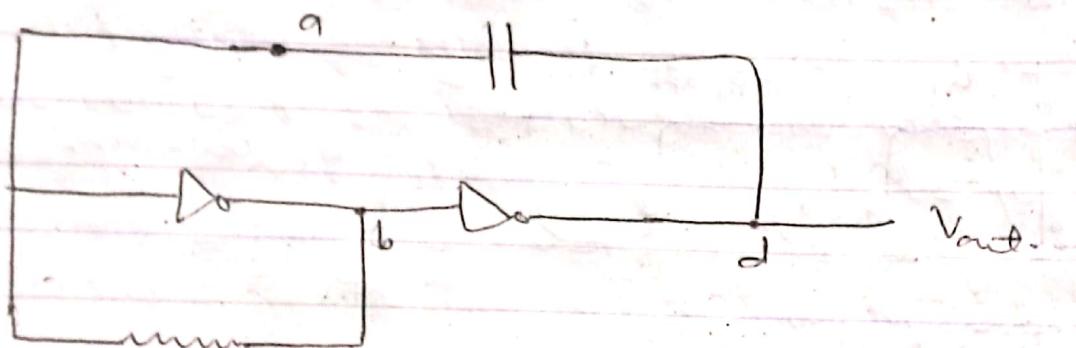
The OFF time for Q_1 , $t_1 = 0.69 R_1 C_1$
 $(\because RC \rightarrow \text{Charging time})$
 and ON time for Q_2 , $t_2 = 0.69 R_2 C_2$

$$\begin{aligned}\text{Time period, } T &= t_1 + t_2 \\ &= 0.69(R_1C_1 + R_2C_2)\end{aligned}$$

$$\begin{aligned}\text{For } R_1 = R_2 = R, C_1 = C_2 = C, \\ T &= 1.38RC\end{aligned}$$

$$\begin{aligned}\therefore \text{The frequency of oscillation, } f &= \frac{1}{T} \\ &= \frac{0.7}{RC}\end{aligned}$$

IC Free Running Oscillation Clock

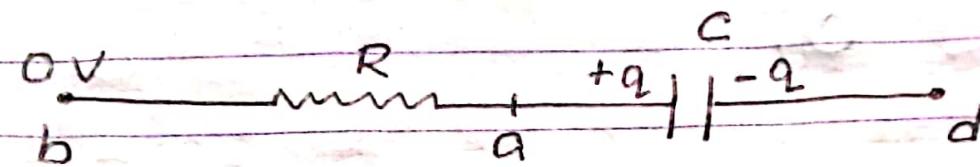


The free running oscillator using two inverters is shown in the fig.

Let us assume that initially $V_a = 0$ then $V_B = 5V$ and $V_d = 0V$.

Now capacitor begins to change through R . The charging will last until the voltage

at a risen sufficiently to cause the output of the inverter to change.



The capacitor will now discharge in such a way that the voltage at point a has dropped enough to cause the output of the first inverter to change back to high i.e., $V_b = 5V$ and $V_d = 0V$

In this way the charging and discharging again takes the new cycle

Semi-conductor Purification :

Here are some processes to obtain basic silicon used in the fabrication of semi-conductor devices :

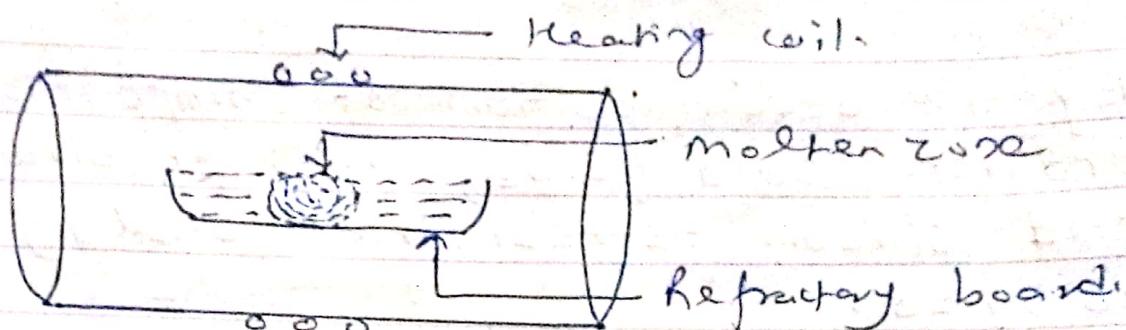
- By the decomposition of compound such as ordinary sand (SiO_2), trichlorosilane (SiHCl_3), and silicon tetrachloride (SiCl_4); silicon is obtained.
- Treating this silicon with different chemicals, it is purified with impurity concentration of about one part per million.
- The form is then melted and cast into an ingot that is polycrystalline in nature.
- To obtain device grade, such ingot is transformed into a large single crystal.
- Finally, the stringent purity requirement is obtained by the method known as 'Zone Refining.'

Zone Refining :

It consists of moving a molten zone along the length of an ingot. The process is repeated for several times so that the impurities go to collect at one end of the ingot.

Zone Refining is similar to the process on how water crystallizes leaving behind the

impurities of salt on lowering the temperature of the water salt solution. The impurities goes on increasing in the succeeding crystallized parts.



As indicated in the figure above, the Si ingot is kept in a chemically stable, non-melting boat that is pulled slowly through a furnace in one side. The narrow region of the furnace above the melting point of Si creates a narrow molten zone on the ingot. The motion of the boat along the furnace makes the molten zone move out of the furnace that goes on freezing. The first frozen part has comparatively lower concentration of the impurity. The process is repeated for the several times. The ingot first melting towards the furnace and then on freezing away from the furnace goes on purifying the crystal. Hence the first frozen part is extremely pure as compared to the part on the later end. Finally the later end that is frozen at the last hour of

the ingot is cut off. and the pure form of Si is obtained.

Single Crystal Growth :

An IC is small in size and the production of such a single IC is complex, time consuming and likely to have defects as well as costly.

Hence to produce sophisticated ICs at reasonable price method of mass production of growing large single crystal of Si has been developed. This process involves the single crystal growth of IC.

Finally, small pieces of wafers are cut out and hundreds of identical integrated circuits are formed using IC fabrication technique.

Here are some of the methods for single crystal growth:

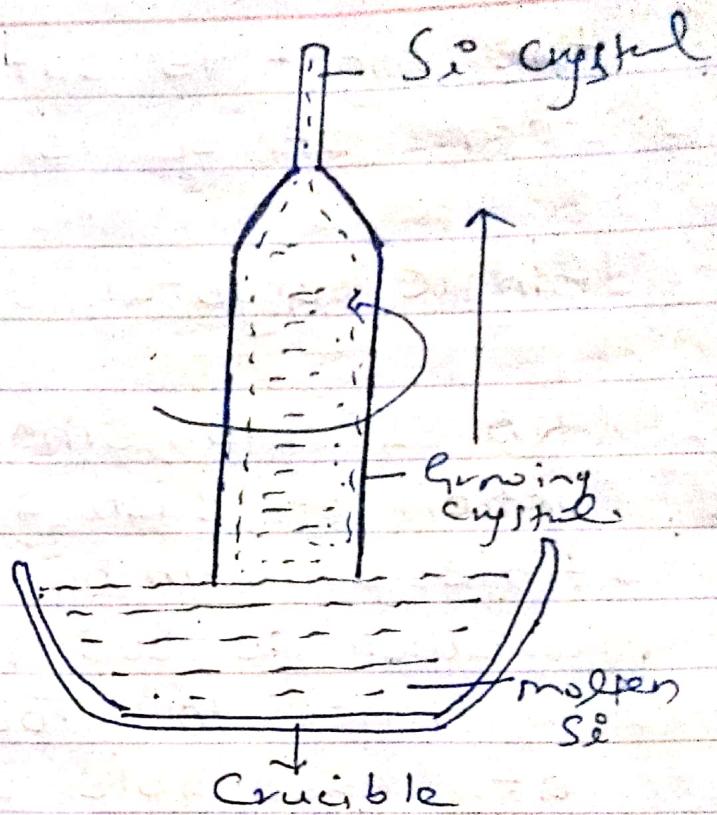
① The Czochralski method :

The Czochralski method for the single crystal growth has been shown in the figure.

Here a seed crystal in the form of a rod is dipped inside a crucible containing molten silicon.

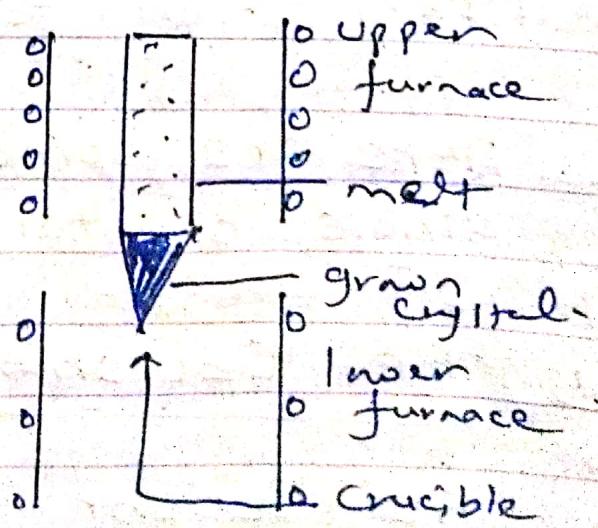
The seed crystal is slowly pulled upwards with rotatory motion too so that the seed crystal goes on growing.

The rotatory motion gives the uniformity on the crystal growth and the rate of motion depends on the size of the crystal to be grown.



② The Bridgman - Stockbarger method :

The method is outlined in the fig. The upper furnace is maintained a few degrees above the melting point while the lower furnace is slightly below the few degrees of the melting point.



The Si material is placed in a crucible with a conical tip. The polycrystalline Si is first melted in an upper furnace that is slowly lowered to the lower furnace that goes on forming a small crystal at the tip. Finally the crystal as a small seed goes on increasing as a crystal growth.

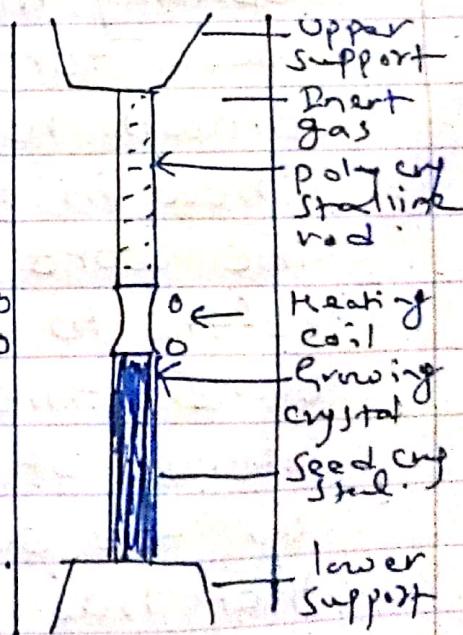
③ Floating Zone Method :

The method has been shown in the fig. below :

It is the method that overcomes the defect of dissolving of the melt with the oxygen on the walls of the crystal i.e. SiO_2 .

It is a method that is overcomes employed in zone refining.

A polycrystalline rod to be grown is placed between the supports inside a furnace filled with inert gas environment. A seed crystal is then placed between the lower post and the lower end of the rod. A small molten zone



is created there near the furnace region at the end of the rod that is in contact with the seed. The coil is slowly moved upwards leaving behind the crystal solidifying and growing onto the seed. The molten zone bet' n the two parts is possible due to the surface tension force.

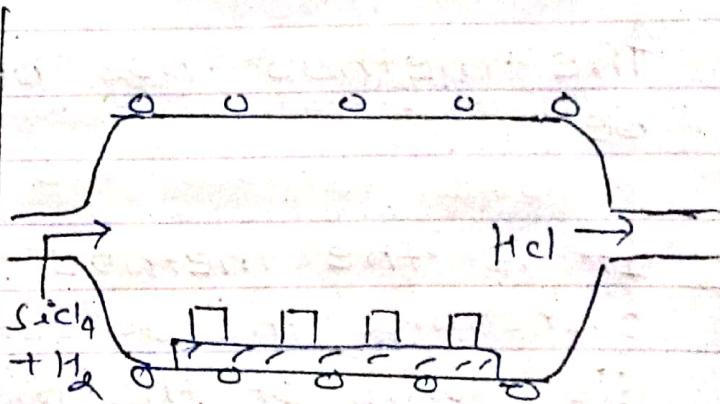
④ Vapor-phase Epitaxy :

The vapor-phase epitaxy method has been for the crystal growth has been shown in the fig.

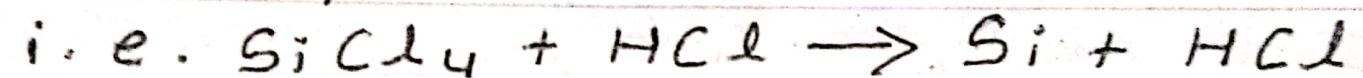
The word epitaxy refers to arrangement. In this method,

atoms of Si from a vapour are deposited on the substrate (wafer) as a layer that has the same crystal structure and orientation as the substrate. The substrate acts as the seed crystal and each comming layer acts as a substrate for the upcoming second layer.

There are single wafer of Si placed in a heated chamber called the 'reactor'. The gaseous compounds of Si (SiCl_4)



along with the reactant gas, H₂ are introduced into the reactor. The reaction finally liberates the Si by decomposition of the compound at 1250°C.



The Si released as a reaction is deposited on the crystal wafer as an epitaxial layer. The purity of such a layer deposited depends on the purity of the chemicals used.

The P-type or N-type doping is done by the same method using either boron or phosphorus atoms.

IC Fabrication

The process of IC Production(Fabrication)
(The Photolithographic process).

The components of an Integrated Circuit are all constructed on a single, tiny piece of a semiconductor crystal, called a chip, that may contain hundreds of diodes, transistors, resistors and capacitors (but no inductors). The conducting paths that interconnect the components of an integrating circuit are contained entirely within the device and the only leads that are brought out are those necessary for power supply connections, grounds and circuit inputs - outputs.

Followings are the processes involved in the IC fabrication processes:

i) Epitaxial Growth :

The epitaxial growth is the deposition of the Si atoms from a vapour on the substrate as a layer that has the same crystal structure and orientation as the substrate. It has been discussed just above.

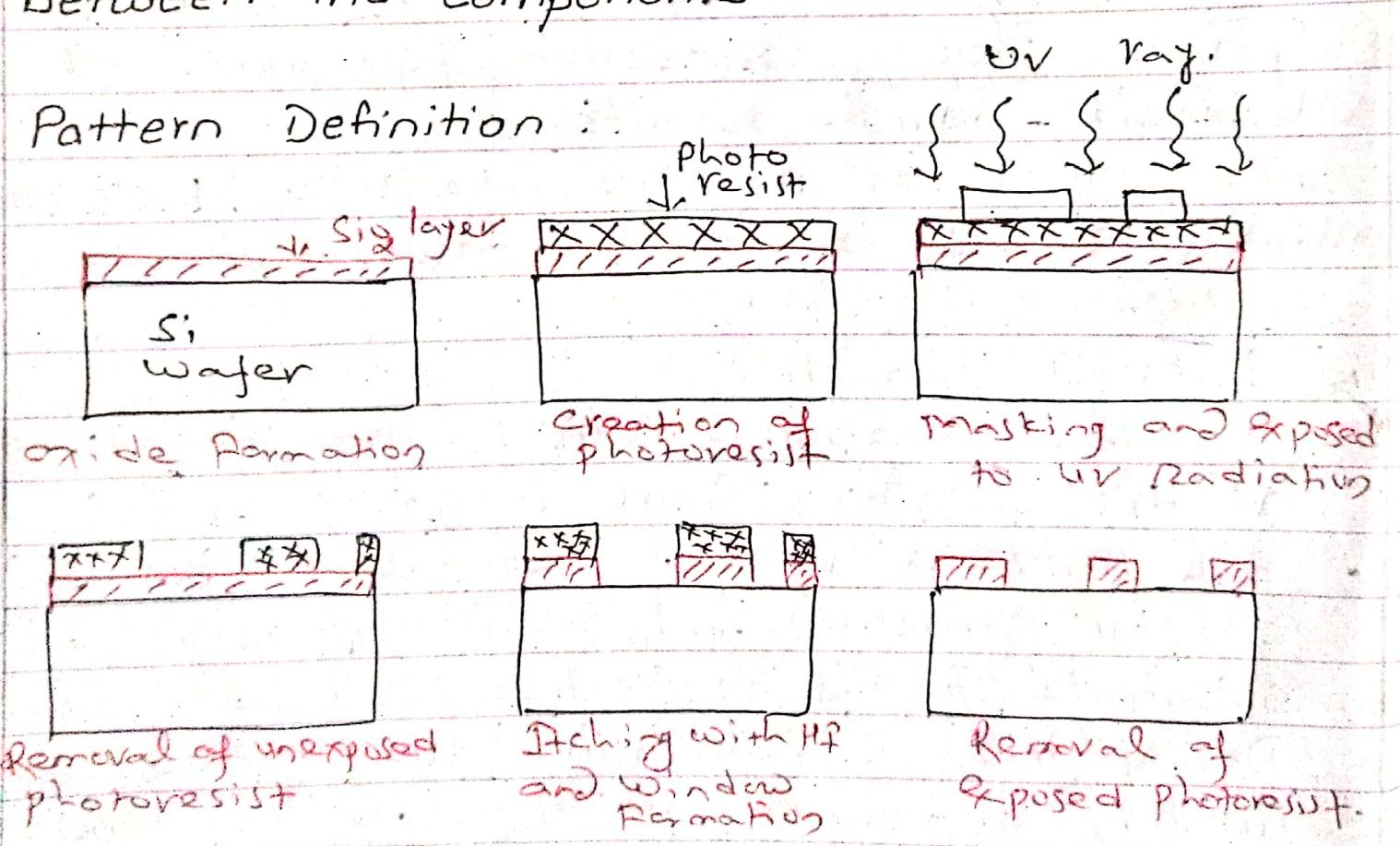
During the IC fabrication, this method is already employed and Si wafer is made pure and ready.

ii) Oxidation :

It is another process that is accomplished by heating

a Si crystal wafer at 1000°C to 1200°C in presence of oxygen or steam. Then a layer of SiO_2 is constructed on the wafer. The thickness of SiO_2 layer depends on temperature, oxidation time and the nature of the atmosphere.

The purpose of oxidation (Formation of a SiO_2 layer) to permit the opening of the windows on wafer surface, block impurities to pass to it to contaminate PN junction and enhances interelectrode connection between the components.



Pattern definition involves the methods to locate the desired places for the IC components to be formed.

The first step here is to coat the SiO_2

layer by a photoresist (PR) material. It is the material that alters the chemical composition (becomes polymerized) when exposed to uv light. Then masking is made i.e., ^{for} the desired locations, for the opening of window are selected ~~use~~ using masking. Then the film of PR is exposed to uv radiation. The exposed PR is polymerised ($\text{Cl} - \text{C} = \text{C} - \text{Cl}$) and hence the exposed $\text{Cl} - \text{H} \uparrow$ (trichloroethyne) and the unexposed PR have different solubilities on certain chemicals. Now the unexposed PR is removed by treating on such chemicals. Finally the SiO_2 is ~~not protected by PR~~ itched way by treating it with HF. and the openings of the windows are created there. After it, the remaining PR, exposed to uv, is washed away in some solvent. The wafer hence become ready for the dopants and metallic conduction.

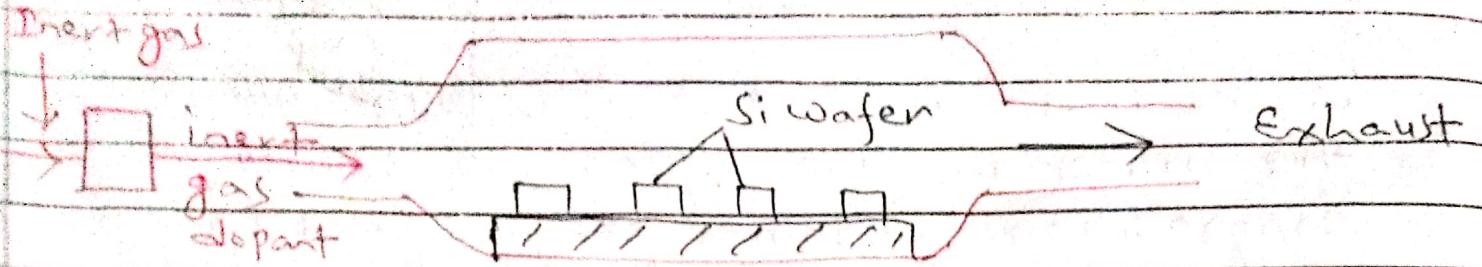
Doping :

It is the process of injecting impurity atoms (P-type or N-type) into the selective region of the chip.

It is done in two ways; diffusion and ion implementation.

Diffusion:

Inert gas



The schematic fig. to illustrate diffusion has been shown in the figure.

On heating Si wafer at around 1000°C , some of the atoms move out of their lattice sites, leaving behind the empty lattice sites that migrate entire of the sample. If the heating is made in the environment of boron or phosphorus, their atoms occupy such lattice sites and spread over the bulk of the Silicon. The diffusion layer is controlled on diffusion time and temperature that can be stopped by cooling the wafer. The SiO_2 layer acts as a mask to provide selective diffusion.

The dopants are passed into the heating furnace with the help of inert carrier gas in the form of bubble. Moreover, gaseous compounds such as diborane (B_2H_6) or phosphorus trifluoride (PF_3) can be diffused directly.

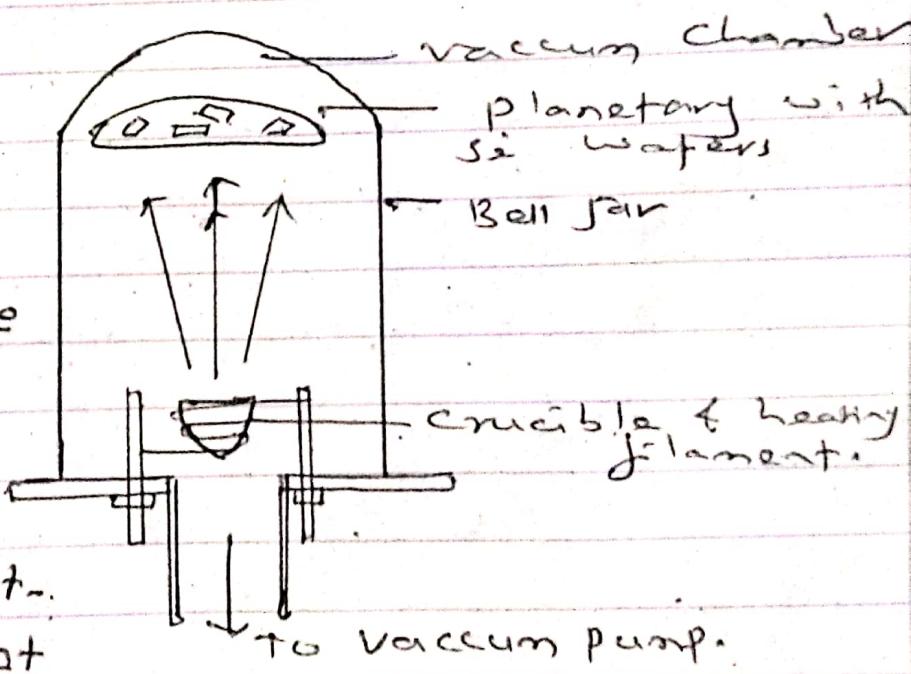
It is found that an approx. of $1 \mu\text{m}$ diffusion layer of phosphorus sets up in 1 hr at 1000°C .

Connection of Components in a Chip:

For a complete ckt within a chip, the electronic components within a layer as well as the layers themselves must be electrically connected. Mostly it is accomplished by metallic thin film evaporation.

The schematic diagram has been outlined in the fig.:

The metal is to be evaporated (aluminium or gold) is placed in a crucible wrapped with a heating coil. The vapour of the metal is produced by heating the crucible that



is allowed to hit the cooled masked wafer placed just above it in a planetary.

The vapour finally condenses in a desired pattern.

The entire procedure is conducted in a vacuum to avoid contamination with oxygen and .

Electronic Component (Fabrication on a Chip)

Here we discuss how the techniques can be used to fabricate basic components of a ckt i.e., transistors, diodes, resistors and capacitors.

Transistors and Diodes :

Following are the steps:

- * First an epilayer of N-type is grown onto a P-type wafer. (Fig i)
- * The N-layer is then oxidised (SiO_2), masked, exposed to uv light and so on, that results to the formation of window on the oxide layer (discussed in pattern definition)
- * Acceptors impurities are diffused to convert part of the exposed N-layer to P-typed layer. A part of this p-layer acts as a base.

- * The wafer is again oxidised and a window is opened in the new oxide layer, and donor impurities layer is diffused on it to convert a part of P-layer to N-layer that acts as emitter of the transistor.
- * At last, the wafer is again reoxidised to open three windows on collector, base and emitter separately. Aluminium is evaporated and connected to these three elements; collector base and emitter to other components of the ckt.
- * For the diode to fabricate, it is similar to the fabrication of the transistor mentioned above where the last step of diffusion to emitter is omitted.

SiO₂

↓↓↓↓ Acceptors

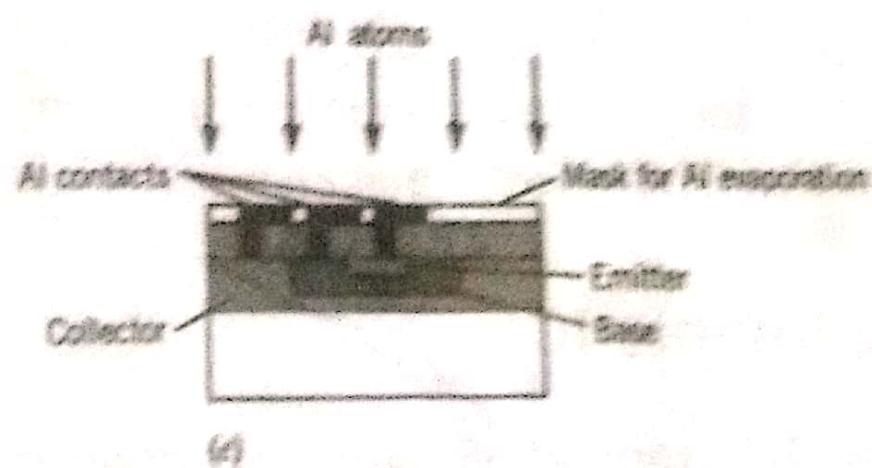
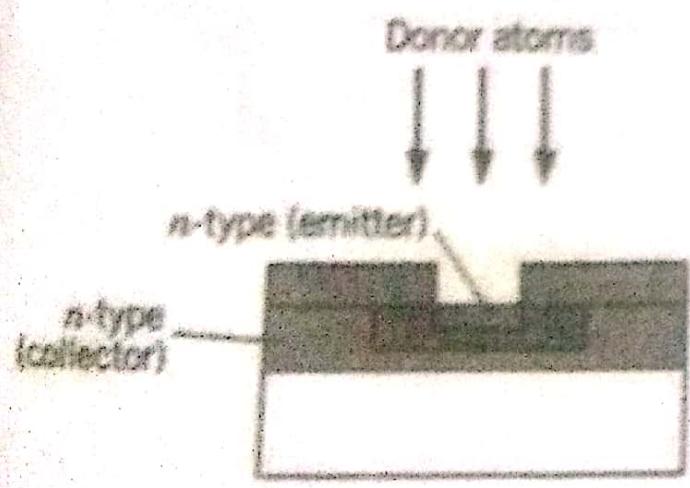
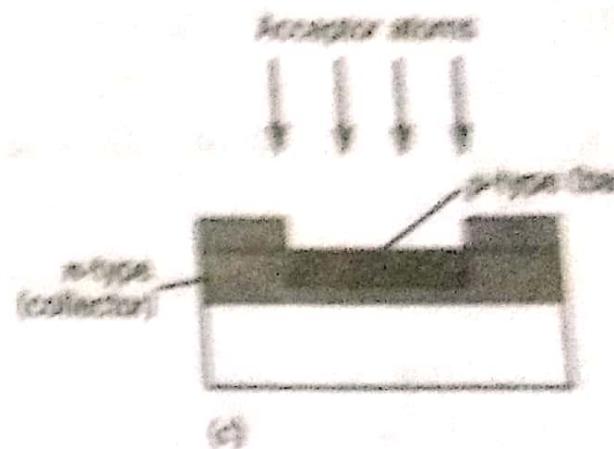
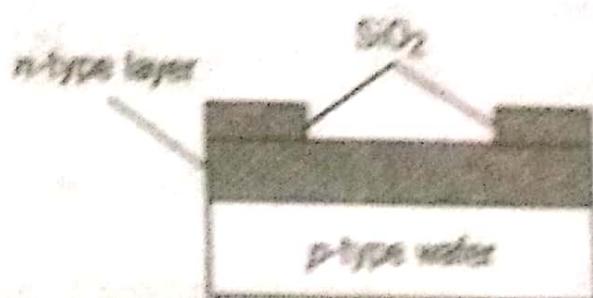
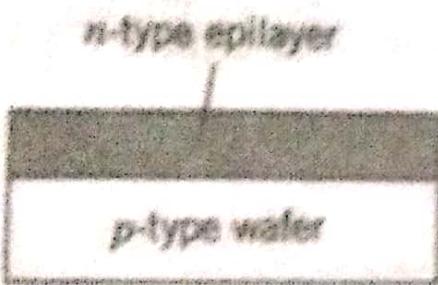


Fig. 10.11. One method to fabricate a transistor on a silicon chip.

Resistors:

The resistor as an IC component is fabricated by a shallow diffusion of a P-type channel into an N region or vice versa. The current is constituted by the reverse bias of the PN arrangement. The resistance made depends on the length of the channel, cross-sectional area of the channel and doping concentration.

Due to some conductivity of Si, a large value of resistance can't be obtained by this method.

Hence, a CE mode transistor is considered as a base current-controlled resistors and is introduced in a ckt where resistor is needed.

Capacitor:

It consists of two metal electrodes separated by some insulating medium.

An epitaxial layer of highly dopped (highly conductive) region acts as an electrode. The region is covered by SiO_2 layer and the second electrode is set up by evaporating a conducting aluminium film on the oxide layer. The detailed illustration is outlined in the fig:

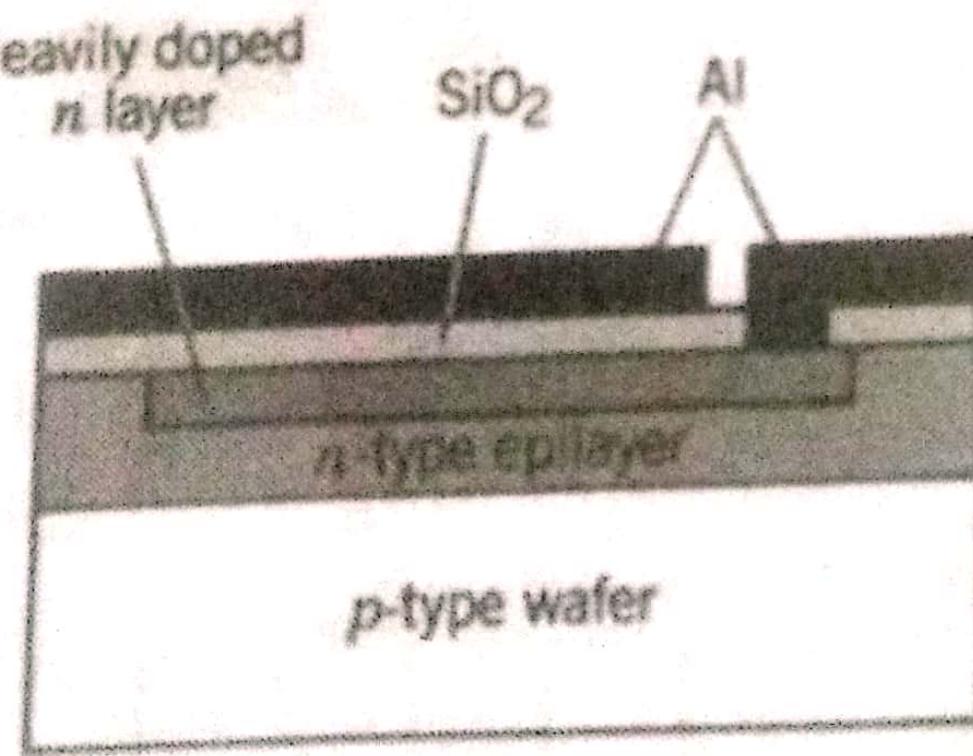


Figure 17.15: Microelectronic capacitor on a silicon chip.