Laboratory Manual

Digital Logic Design
(CSC-111)

By: Abhimanu Yadav

Department of Computer Science and Information Technology

Kathmandu BernHardt College

Tribhuvan University

Bafal, Kathmandu,Nepal

Tel: 5237330, 5237361

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1. Guide to Assembling your Circuits:

In this section we describe the use of the breadboard and give basic hints about the wiring process needed to power up and interconnect your circuits.

Assembling circuits on your breadboard is a fast and easy process once you get used to it. To assemble your circuit first select the chips that you need, insert them in the breadboard, wire up the power and ground connections as described in the next section and next wire the logic elements according to the circuit connections that you obtained from the design process.

Before you insert a chip into the breadboard, make sure it is properly oriented and that when you press it down the pins of the chip actually enter the holes and do not bend underneath the chip package.

When wiring, be careful to hit the right hole needed in the connection, because this is one of the most common mistakes found to cause an error in your projects.

2. Breadboard Description:

In order to build the circuit, a digital design kit that contains a power supply, switches for input, light emitting diodes (LEDs), and a breadboard will be used. Make sure to follow your instructor's safety instructions when assembling, debugging, and observing your circuit. You may also need other items for your lab such as: logic chips, wire, wire cutters, a transistor, etc. Figure 1 shows a common breadboard, while Figure 2 shows how each set of pins are tied together electronically.

For these labs, the highest voltage used in your designs will be five volts or +5V and the lowest will be 0V or ground.

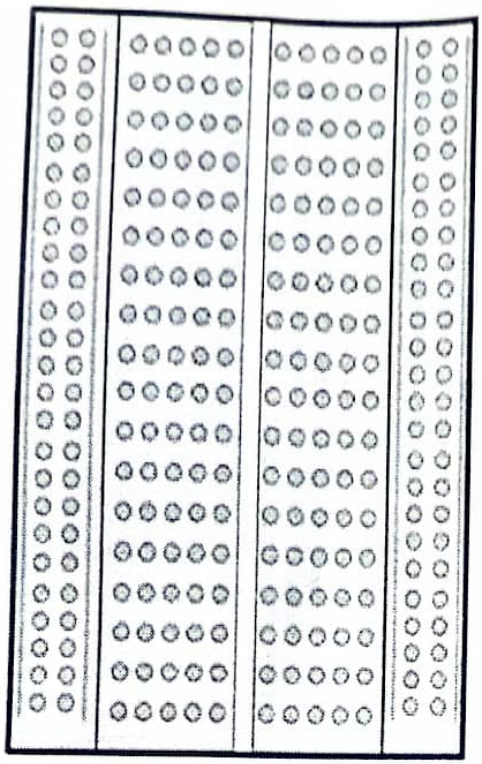


Figure 1: Breadboard

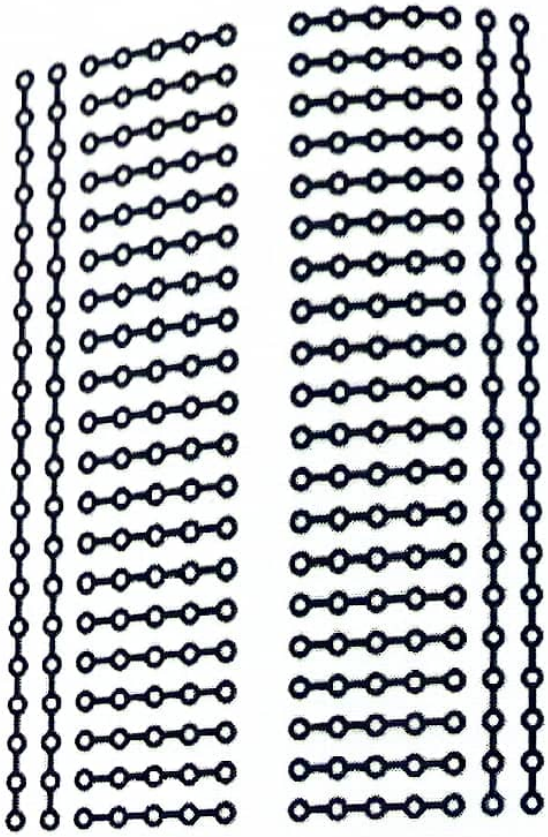


Figure 2 Common connections

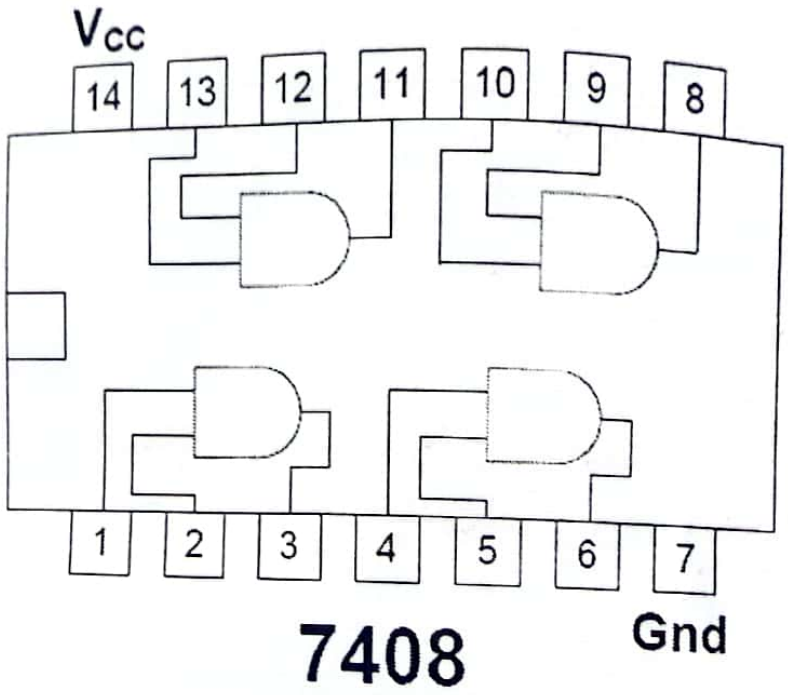
3. Common Causes of Problems:

- Not connecting the ground and/or power pins for all chips.
- Not turning on the power supply before checking the operation of the circuit.
- Leaving out wires.
- Plugging wires into the wrong holes.
- Driving a single gate input with the outputs of two or more gates.
- Modifying the circuit with the power on.

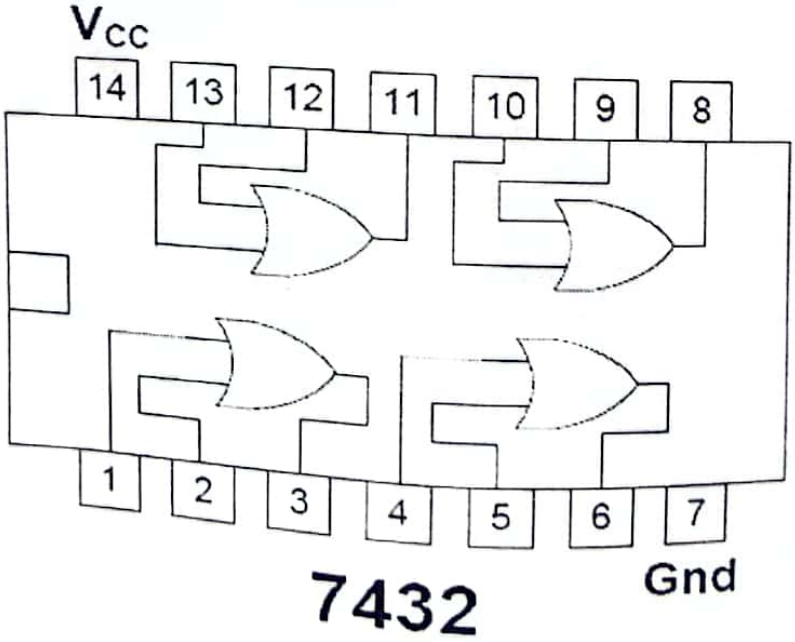
Note: In all experiments, you will be expected to obtain all instruments, leads, components at the start of the experiment and return them to their proper place after you have finished the experiment.

4. Pin diagram of all gates:

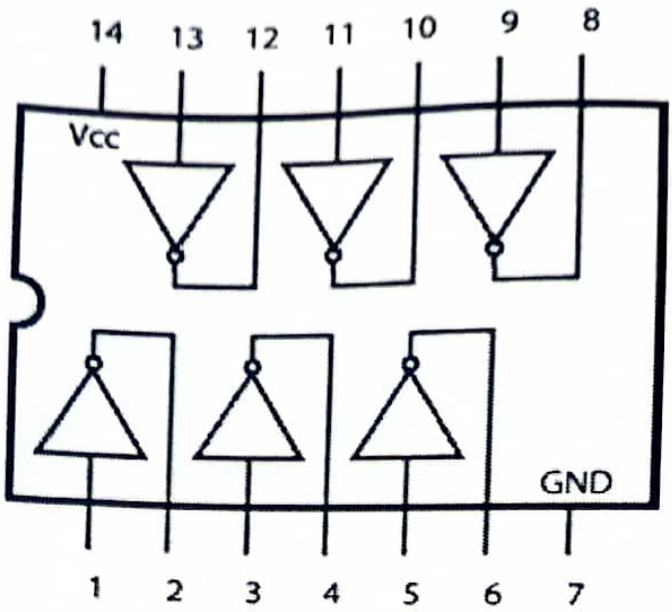
a. AND GATE 7408 (Quad 2 input)



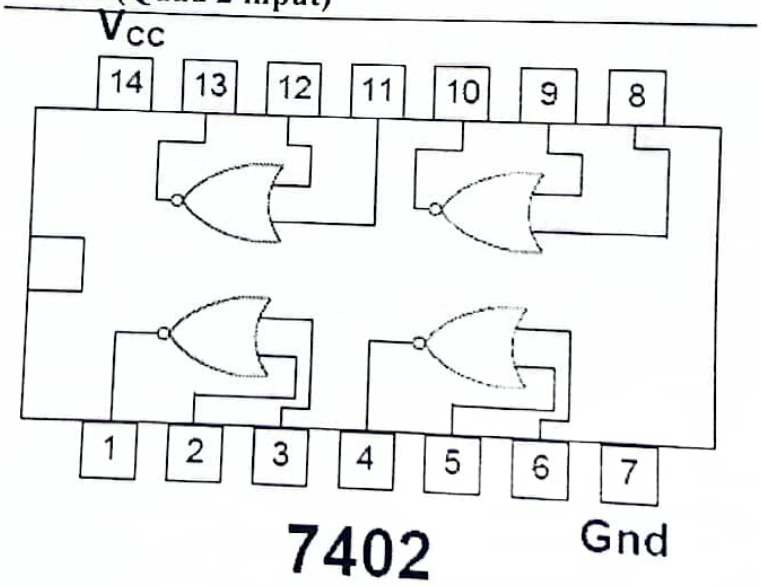
b. OR GATE 7432 (Quad 2 input)



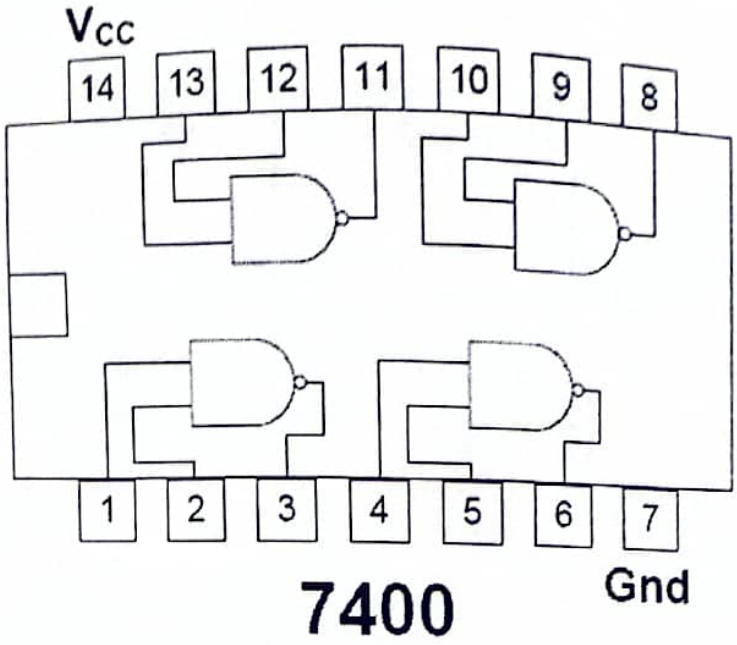
c. NOT GATE 7404



d. NOR GATE 7402 (Quad 2 input)

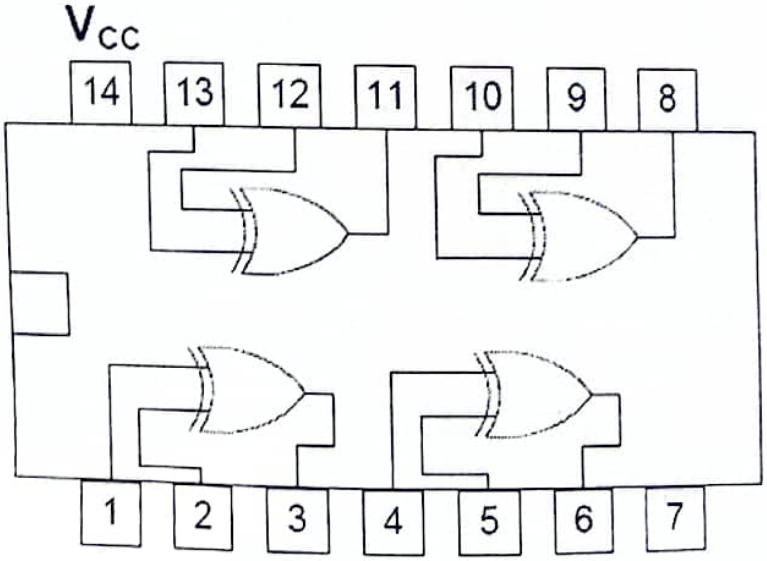


e. NAND GATE 7400 (Quad 2 input)



7400

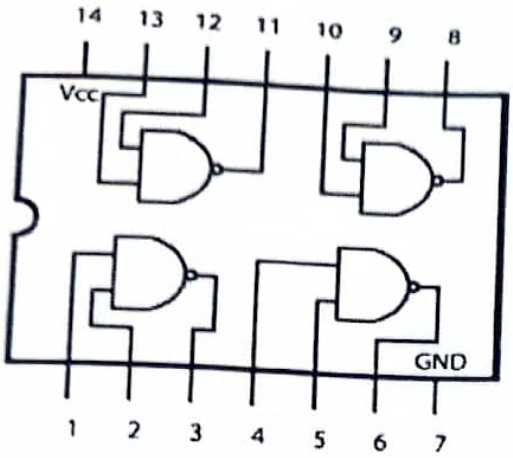
f. EXCLUSIVE XOR GATE 7486 (Quad 2 input)



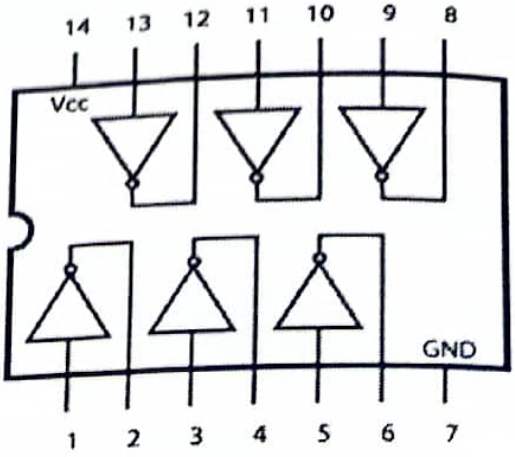
7486

5. Example Implementation of a Logic Circuit

Build a circuit to implement the Boolean function $F = A \cdot B$ using TTL IC 74LS00 (NAND gate) and TTL IC 7404 (INVERTER) as per discussed in figure.



Quad 2 Input 7400



Hex 7404 Inverter

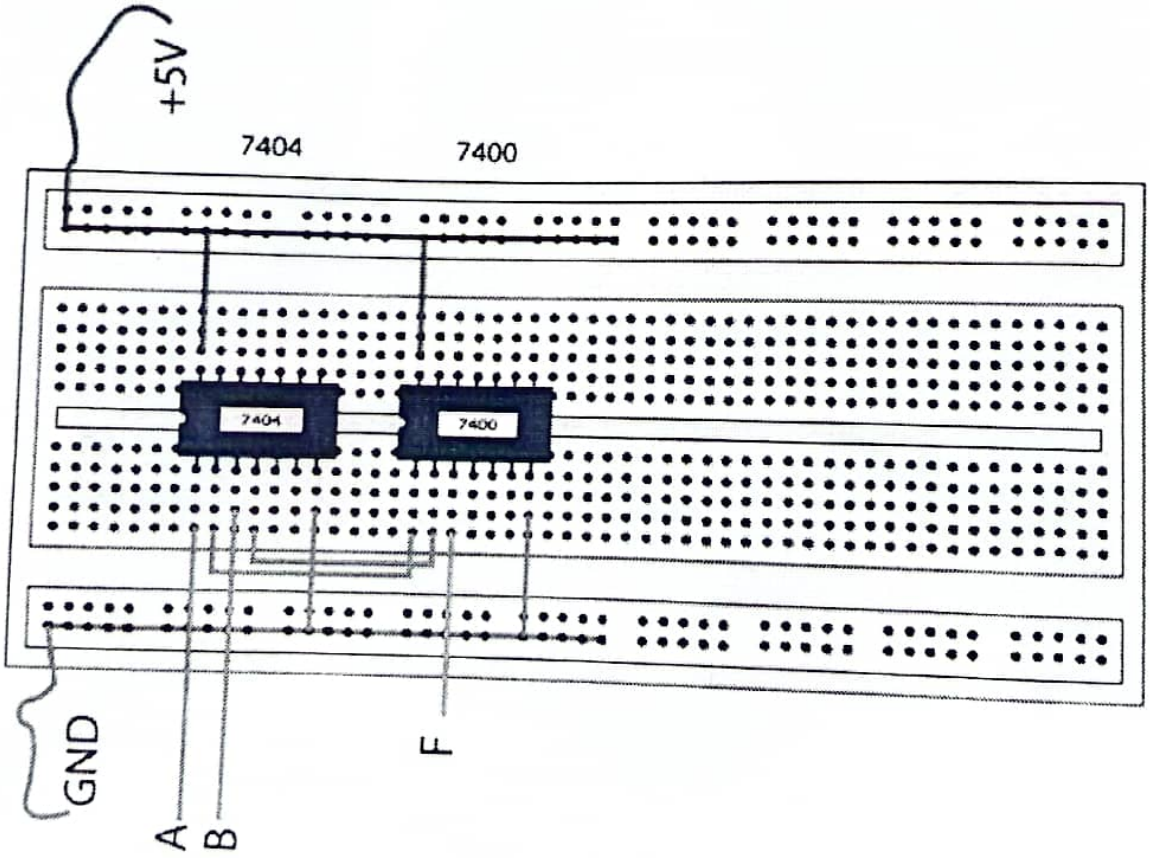


Figure: The complete designed and connected circuit

EXPERIMENT NO: 1

Aim: - Introduction to digital electronics Lab-nomenclature of digital ICs, specifications, study of the data sheet, concept of VCC and Ground, verification of truth tables of logic gates using TTL ICs.

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, and IC's.

Gates	IC NO.
AND	7408
OR	7432
NAND	7400
NOR	7402
NOT	7404
XOR	74136

THEORY: Explain Theory.

PROCEDURE:

a) Fix the IC's on breadboard & give the supply.
b) Connect the +ve terminal of supply to pin 14 & -ve to pin 7.
c) Give input at pin 1, 2 & take output from pin 3. It is same for all except NOT & NOR IC.
d) For NOR, pin 1 is output & pin 2&3 are inputs.
e) For NOT, pin 1 is input & pin 2 is output.
f) Note the values of output for different combination of inputs & draw the TRUTH TABLE.

RESULT: All gates are verified. Observed output matches theoretical concepts.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

4. While making connections main voltage should be kept switched off.
5. Never touch live and naked wires.

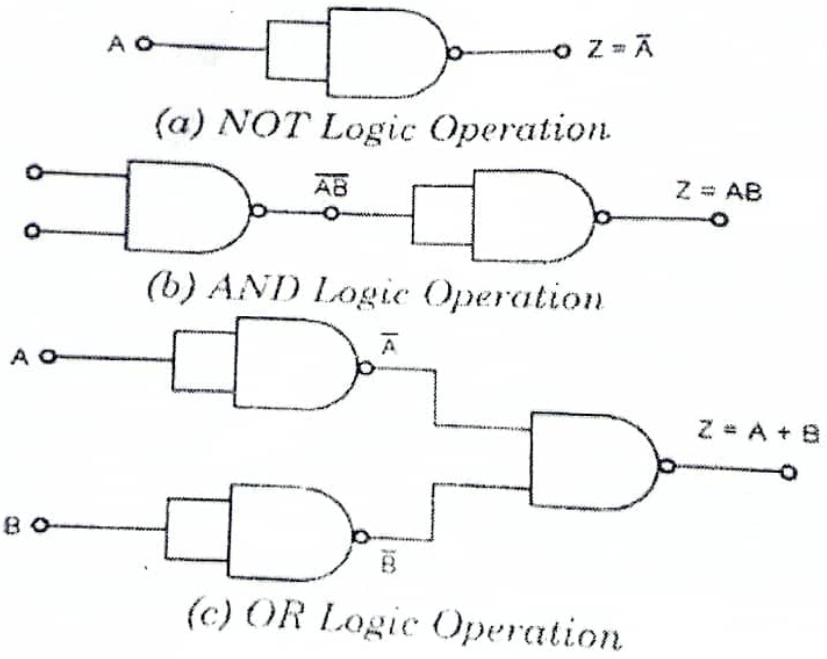
EXPERIMENT NO: 2

Aim: - To study and verify NAND and NOR gate as universal gate.

APPARATUS REQUIRED – Digital trainer kit, IC 7400 (NAND gate).

THEORY – NAND or NOR sufficient for the realization of any logic expression, because of this reason, NAND and NOR gates are known as UNIVERSAL gates.

LOGIC DIAGRAM –



PROCEDURE –

a) Make the connections as per the logic diagram
b) Connect +5v to pin 14 & ground to pin 7
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for NAND as universal gate.

e) Verify the truth table.

RESULT: All Universal gates are verified. Observed output matches theoretical concepts.

EXPERIMENT NO: 3

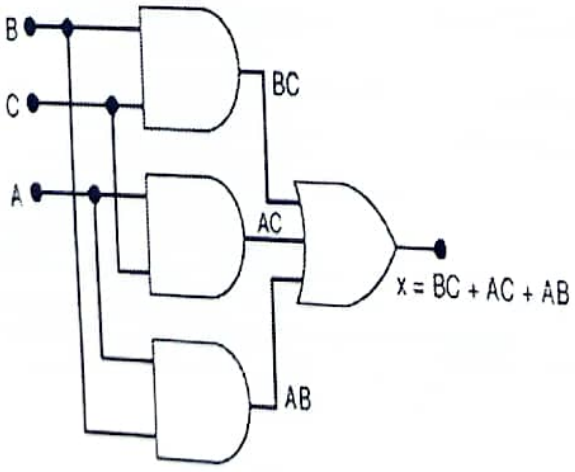
Aim: - Implementation of the given Boolean function using logic gates in both POS and SOP forms.

APPARATUS REQUIRED: Power Supply, Digital Trainer, IC's (7404, 7408, 7432) Connecting leads.

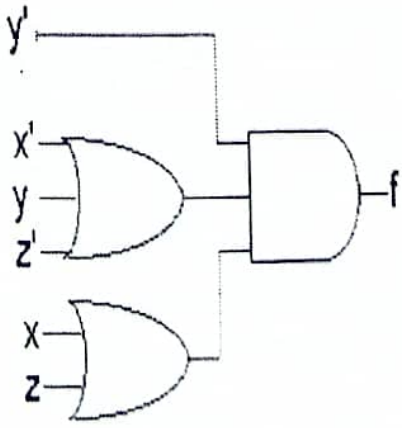
THEORY: Karnaugh maps are perhaps the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n-variables.

Example- f(A,B,C,D)=A'BC+AB'C+ABC'+ABC (SOP) Reduced form is BC+AC+AB, and POS form is f(X,Y,Z)= Y'(X'+Y+Z')(X+Z).

CIRCUIT DIAGRAM:



SOP Form



POS Form

PROCEDURE:

a) With given equation in SOP/POS form first of all draw a K-map.
b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.
c) Make group of adjacent ones.
d) From group write the minimized equation.
e) Design the ckt. of minimized equation & verify the truth table.

RESULT:

Implementation of SOP and POS form is obtained with AND and OR gates.

EXPERIMENT NO: 4

Aim: - To design and verify operation of half adder and full adder.

APPARATUS REQUIRED: Power supply, IC's (7486, 7432 and 7408). Digital Trainer, Connecting leads.

THEORY: We are familiar with ALU, which performs all arithmetic and logic operation but ALU doesn't perform/ process decimal no's. They process binary no's.

Half Adder: It is a logic circuit that adds two bits. It produces the O/P, sum & carry. The Boolean equation for sum & carry are

$$SUM = A \oplus B$$

$$CARRY = A.B$$

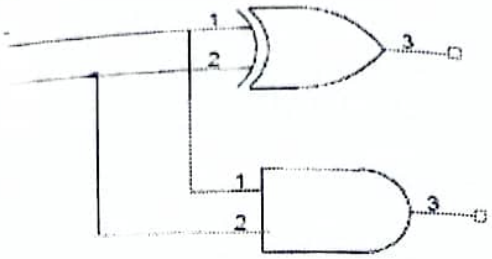
Therefore, sum produces 1 when A&B are different and carry is 1when A&B are 1. Application of Half adder is limited.

Truth Table:

Truth Table

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

CIRCUIT DAIGRAM:



Full Adder: It is a logic circuit that can add three bits. It produces two O/P sum & carry. The Boolean Equation for sum & carry are

$$SUM = (A \text{ XOR } B) \text{ XOR } C_{in} = (A \oplus B) \oplus C_{in}$$

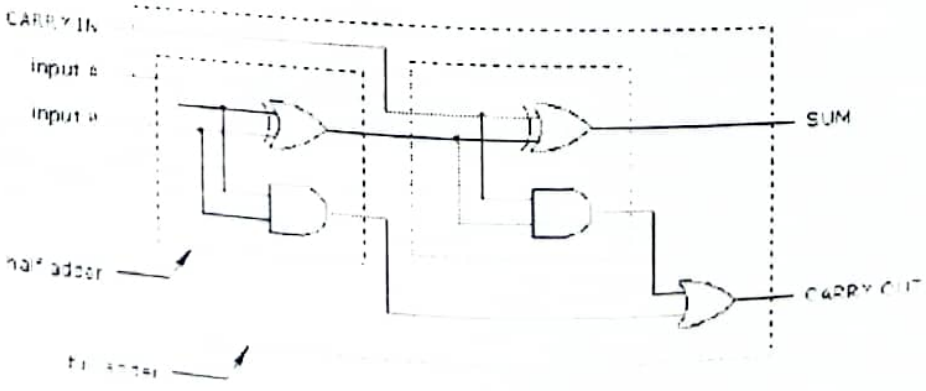
$$CARRY = A \text{ AND } B \text{ OR } C_{in}(A \text{ XOR } B) = A.B + C_{in}(A \oplus B)$$

Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

Truth Table:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CIRCUIT DAIGRAM:



RESULT: The Half Adder & Full Adder ckts. are verified.

EXPERIMENT NO: 5

Aim: - To design and verify operation of half subtractor and full subtractor.

APPARATUS REQUIRED: – Digital trainer kit,

IC 7486 (EX-OR),

IC 7408 (AND gate),

IC 7404 (NOT gate).

THEORY:

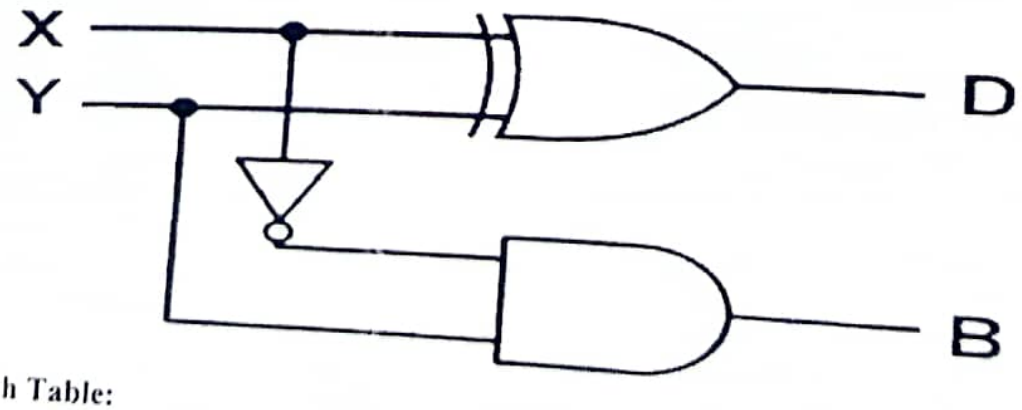
The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs Difference and Borrow.

The Boolean expression:

$$\text{Difference} = A \oplus B$$

$$\text{Borrow} = A' B$$

CIRCUIT DAIGRAM:



Truth Table:

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

A full subtractor is a combinational circuit that performs subtraction involving three bits, namely A (minuend), B (subtrahend), and B_{in} (borrow-in). It accepts three inputs: A (minuend), B (subtrahend) and a B_{in} (borrow bit) and it produces two outputs: D (difference) and Bout (borrow out).

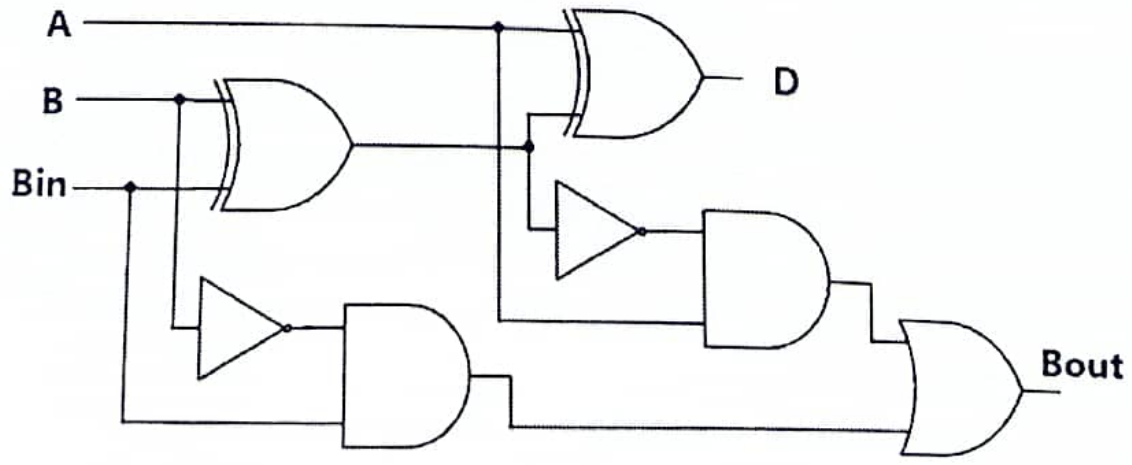
The Boolean expression:

$$D = A \oplus B \oplus B_{in}$$

$$B_{out} = A' B_{in} + A' B + B B_{in}$$

CIRCUIT DAIGRAM:

Truth Table:



Truth Table:

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

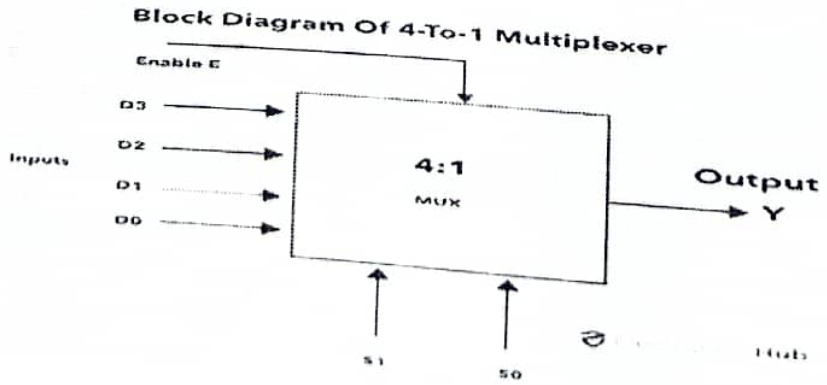
RESULT – Half subtractor and Full subtractor circuit is studied and verified.

EXPERIMENT NO: 6

Aim: - Implementation of 4*1 multiplexer using logic gates.

APPARATUS REQUIRED: Power Supply. Digital Trainer, Connecting Leads, IC`s 74153(4x1 multiplexer).

THEORY: A **4-to-1 multiplexer** consists four data input lines as D0 to D3, two select lines as S0 and S1 and a single output line Y. The select lines S0 and S1 select one of the four input lines to connect the output line. The figure below shows the block diagram of a 4-to-1 multiplexer in which, the multiplexer decodes the input through select line.



The **truth table** of a 4-to-1 multiplexer is shown below in which four input combinations 00, 10, 01 and 11 on the select lines respectively switches the inputs D0, D2, D1 and D3 to the output. That means when S0=0 and S1 =0, the output at Y is D0, similarly Y is D1 if the select inputs S0=0 and S1= 1 and so on.

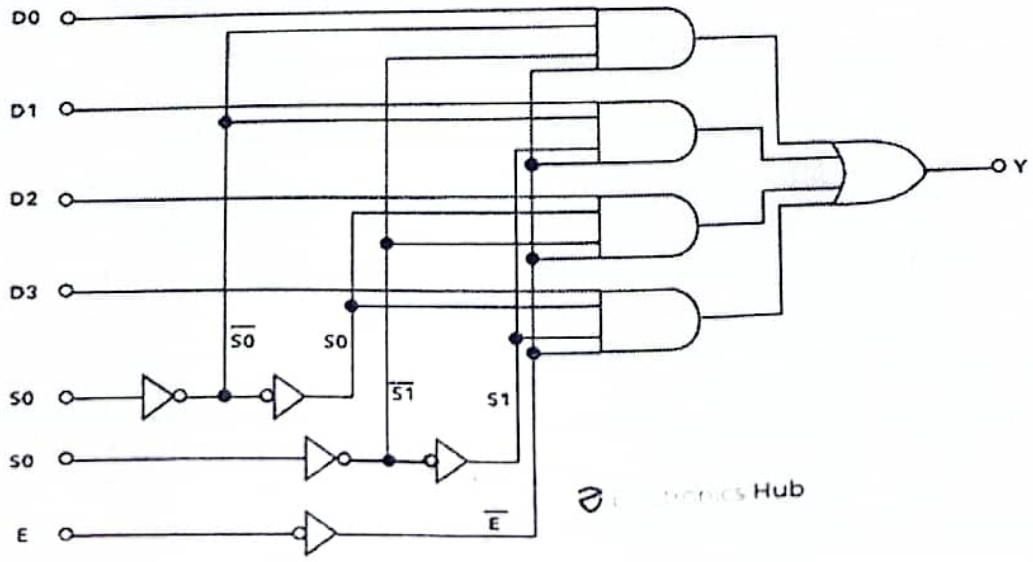
S0	S1	D0	D1	D2	D3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Expressions as follows:

$$Y = \overline{S0}\,\overline{S1}\,D0 + \overline{S0}\,S1\,D1 + S0\,\overline{S1}\,D2 + S0\,S1\,D3$$

A 4-to-1 multiplexer can be implemented by using basic logic gates. The below figure shows the logic circuit of 4:1 MUX which is implemented by four 3-inputs AND gates, two 1-input NOT gates, and one 4-inputs OR gate.

Logical Circuit Of 4-To-1 Multiplexer

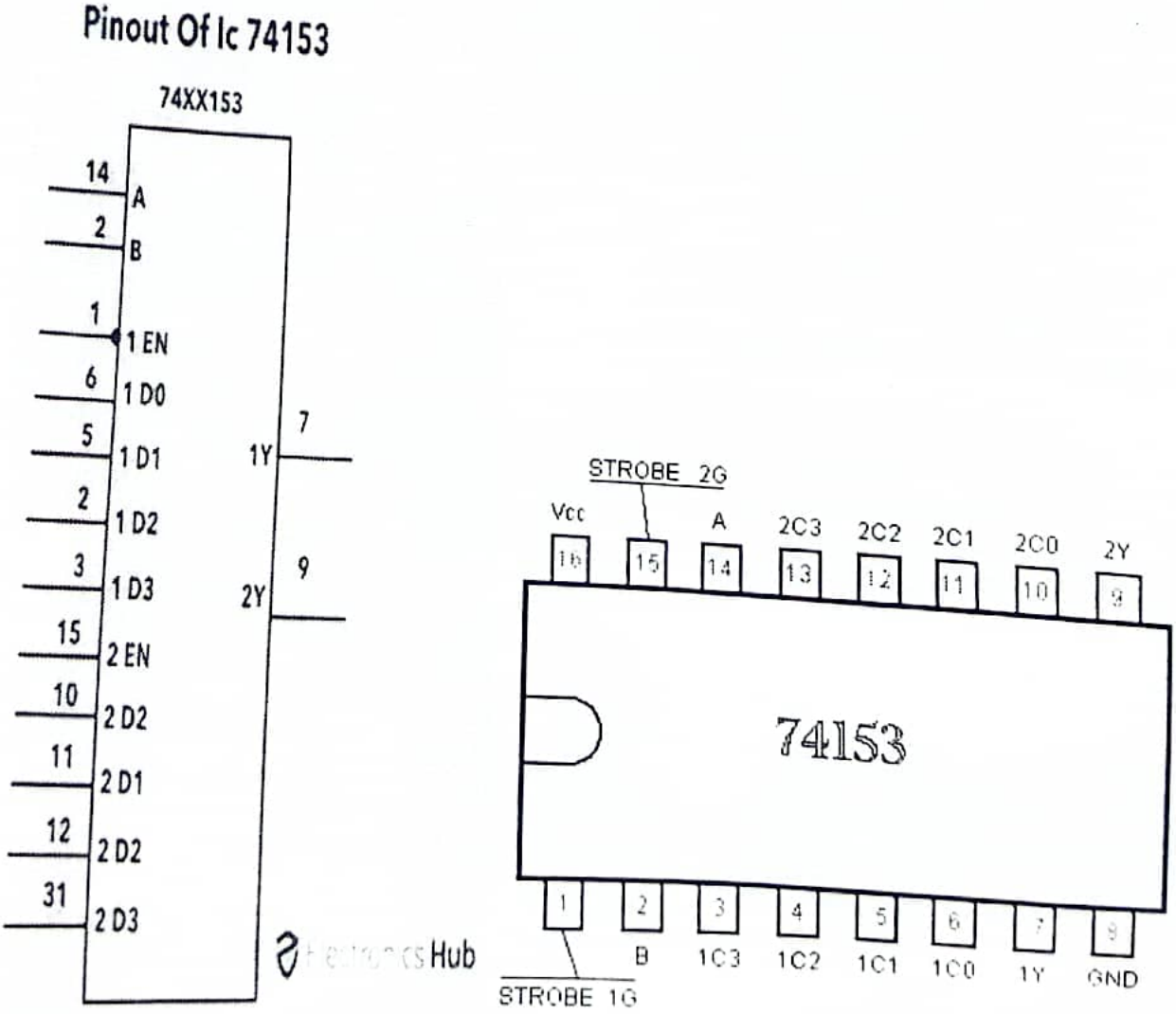


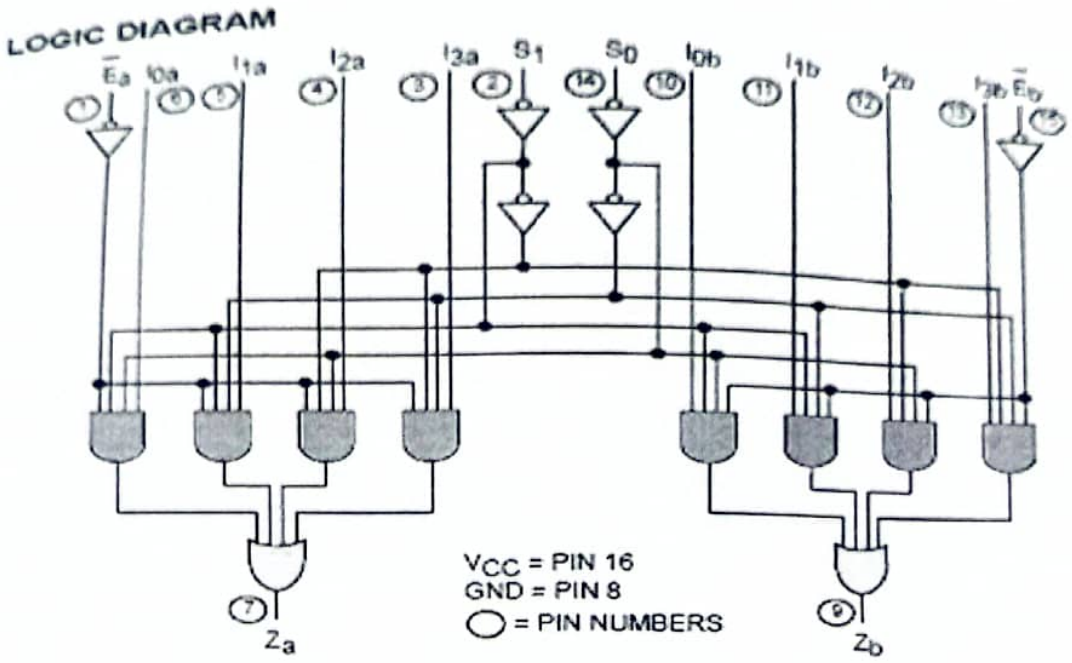
In this circuit, each data input line is connected as input to an AND gate and two select lines are connected as other two inputs to it. Additionally, there is also an Enable Signal. The output of all the AND gates are connected to inputs of OR gate in order to produce the output Y.

CIRCUIT DIAGRAM:

Generally, this type of multiplexers is available in IC with dual mode i.e., there will be two 4-to-1 Multiplexers in a single IC. The most common and popular 4-to-1 line multiplexer is IC 74153 which, is a dual 4-to-1 line multiplexer. It consists of two identical 4-to-1 multiplexers. It has two separate enable or strobe inputs to switch ON or OFF the individual multiplexers. But the Select lines are common to both the Multiplexers.

The figure below shows the pin diagram of IC74153.





Detail:
https://www.electronicshub.org/multiplexerandmultiplexing/#:~:text=The%20most%20common%20and%20popular,%2Dto%2D1%20line%20multiplexer.

RESULT: Verify the truth table of multiplexer for various inputs.

EXPERIMENT NO: 7

Aim: - Implementation and verification of Decoder/ DE multiplexer and Encoder using logic gates.