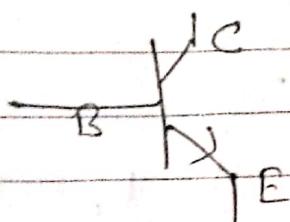
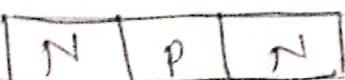


The Bipolar Junction Transistor

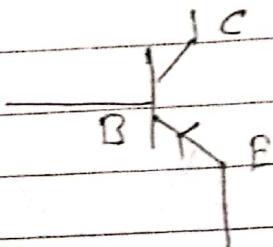
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When a third, doped material is connected to a pn diode, the resulting device is called as a transistor.



Npn symbol.



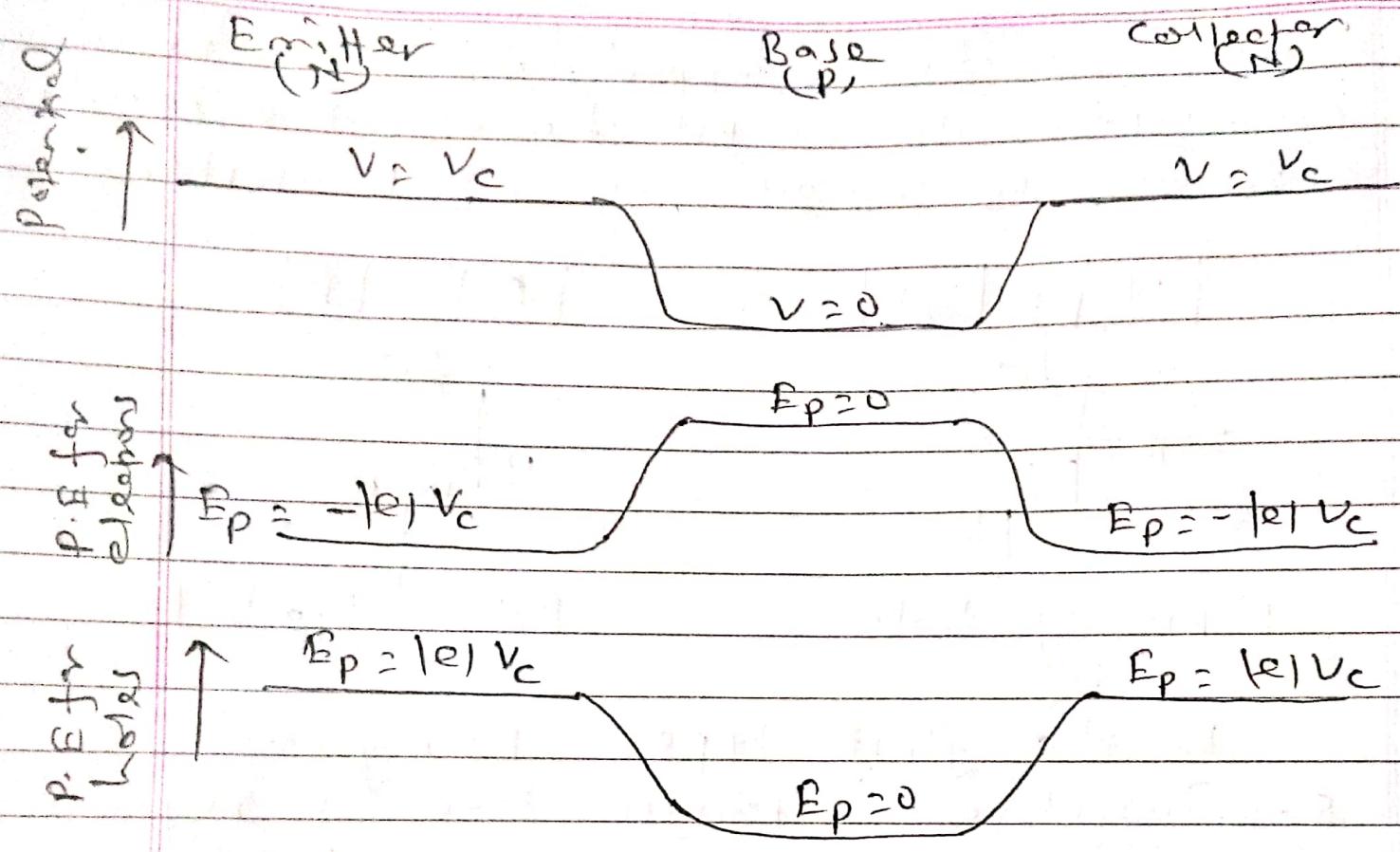
Pnp symbol

In the first type, p-region is sandwiched between two n regions while in the second case n-type is sandwiched between two p types.

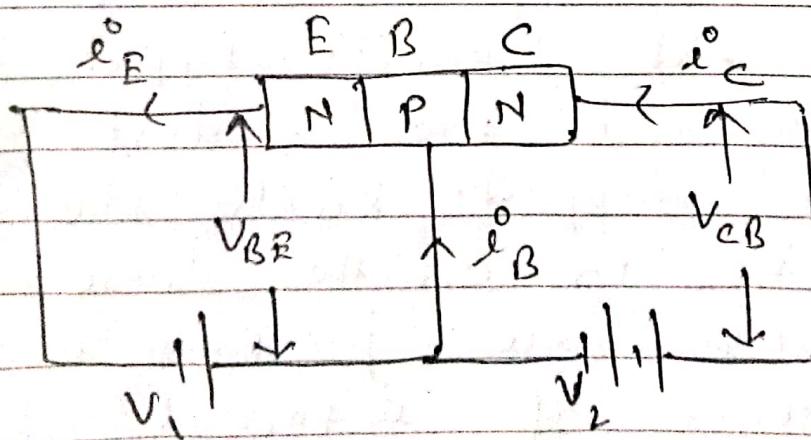
The base region is lightly doped and very thin while emitter region is wide and heavily doped and the collector region is the widest and moderately doped. Both the contact potential, V_c in emitter base junction and collector base junction is same.

In absence of external bias, the potential of n side is greater than the potential of p side by an amount V_b .

The potential and the associated potential energy barrier for electrons and holes are illustrated below:



Common Base Configuration



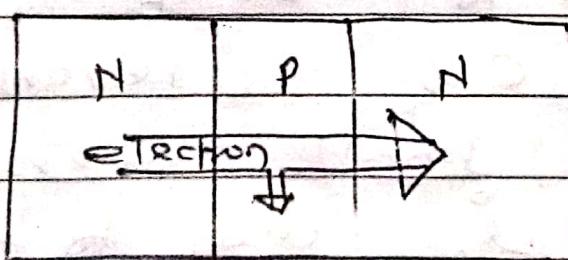
The common base configuration ckt has been shown in the fig above.

As indicated in the fig, the base emitter junction is forward biased using V_1 and the collector base junction is reverse biased using V_2 . The base is common in the either case and hence the common base configuration.

In the input section, the battery V_1 will raise the potential of the p type base relative to the n type emitter by an amount V_{BE} . Hence the potential difference bet' the emitter and base is reduced to $V_e - V_{BE}$.

For the CB junction, the potential of p type base is lowered as compared to the collector and hence the collector base voltage is increased to $V_c + V_{CB}$.

The potential difference, the associated P.E for the electrons and holes are sketched in the fig.



Emitter Base collector.

The lower potential of emitter injects the electrons to the base side and those

electrons that do not recombine with the holes in the base and do not lead to the contact potential flow towards the collector.

The emitter current is due to the flow of electrons (majority charge carriers) from emitter to base and the holes (majority charge carriers) from base to the emitter.
i.e $i_E = i_{eE} + i_{pE}$

As the base is small in size and lightly doped, $i_{eE} \gg i_{pE}$

$$\therefore i_E = i_{eE}$$

For the collector current, the electrons injected to the base that do not recombine with the holes will pass to the collector which is equal to αi_E .

Since CB is reverse biased, there is small reverse saturation current i_0 due to the minority carriers.

$$\therefore i_C = \alpha i_E + i_0$$

THE BIPOLAR JUNCTION TRANSISTOR

n-type
emitter

p-type
base

n-type
collector

Potential, V
(voltage)

$$V = V_c$$

$$V = V_c - V_{BE}$$

$$V = 0$$

$$V = V_c + V_{CB}$$

(a)

$$E_p = 0$$

Potential energy, E_p
(for electrons)

$$E_p = -|e| (V_c - V_{BE})$$

$$E_p = -|e| V_c$$

$$E_p = -|e| V_c$$

$$E_p = -|e| (V_c + V_{CB})$$

(b)

Potential energy, E_p
(for holes)

$$E_p = |e| V_c$$

$$E_p = |e| (V_c - V_{BE})$$

$$E_p = 0$$

$$E_p = |e| (V_c + V_{CB})$$

$$E_p = |e| V_c$$

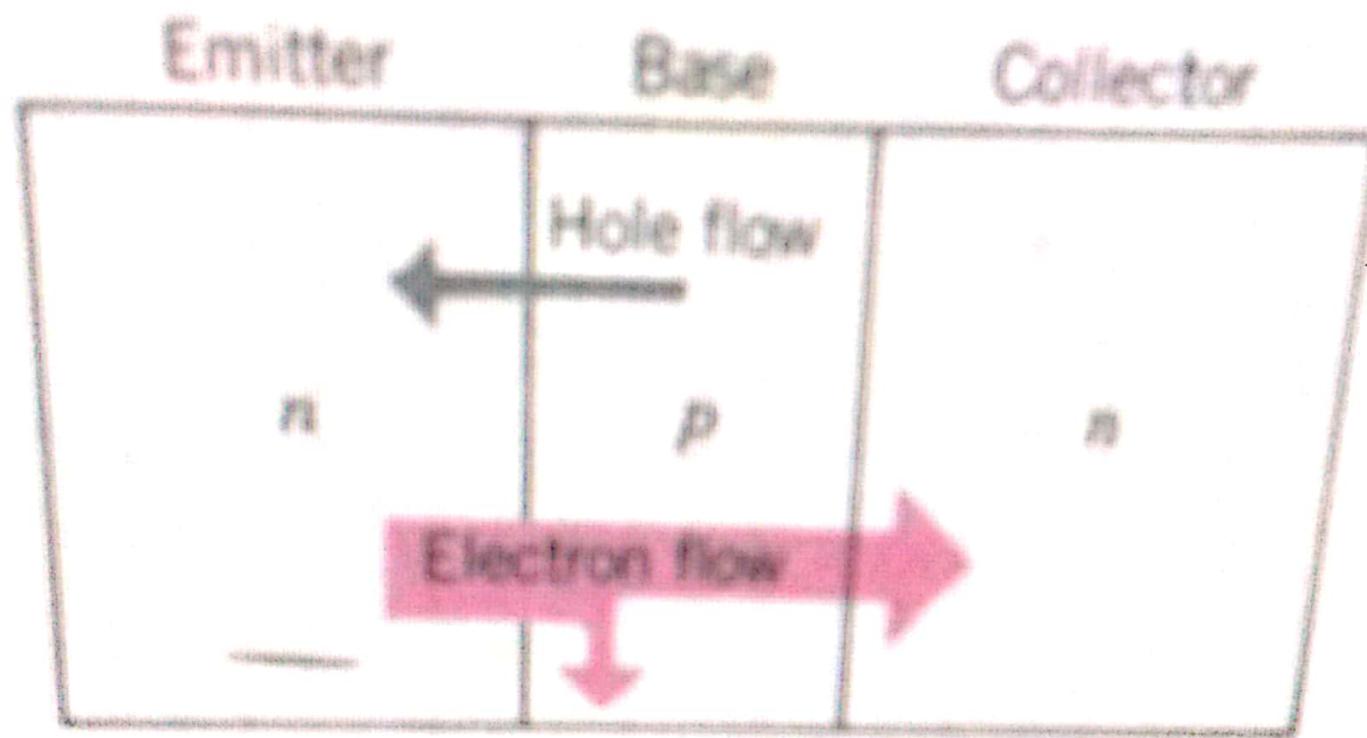
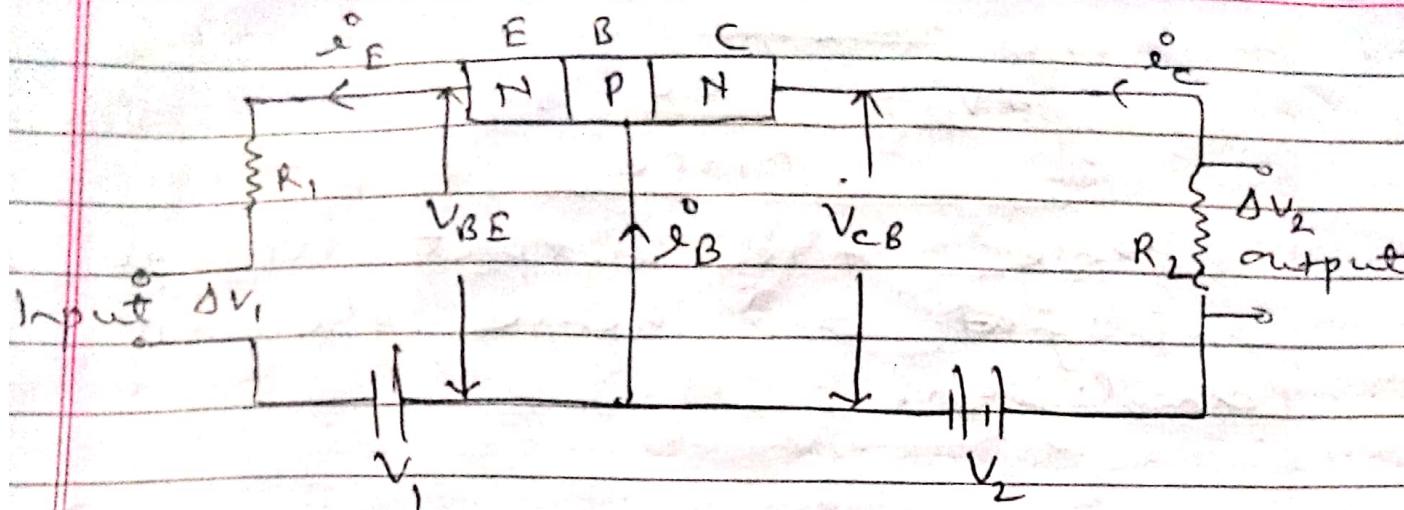


FIGURE 26-17
Schematic representation of the flow of electrons and holes across the energy barriers at the two junctions of the transistor for the common base configuration circuit of Fig. 26-15.

The Transistor as a Voltage Amplifier.

Page No.



The common base transistor amplifier has been shown in the fig. Let R_1 and R_2 be the two resistors inserted in the input and output. R_2 is very large as compared to R_1 .

Let ΔV_1 be the input signal fed and ΔV_2 be the output taken across R_2 .

Clearly, the change in emitter current,

$$\Delta i_E = \frac{\Delta V_1}{R_1 + R_E}$$

and the corresponding change in collector current, $\Delta i_C \approx \alpha \Delta i_E = \alpha \frac{\Delta V_1}{R_1 + R_E}$

$$\begin{aligned} \Delta V_2 &= \Delta i_C \cdot R_2 \\ &= \alpha \frac{\Delta V_1}{R_1 + R_E} \cdot R_2 = \alpha \frac{R_2}{R_1 + R_E} \Delta V_1 \end{aligned}$$

But $\alpha \approx 1$.

$$\therefore \Delta V_2 = \frac{R_2}{R_1 + R_2} \Delta V_1$$

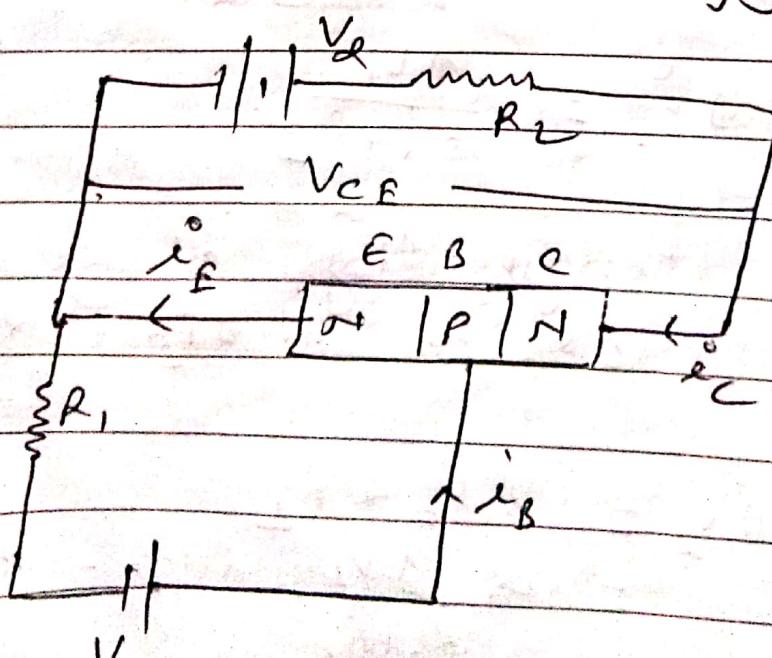
Hence the output voltage is amplified and hence the CB amplifier.

Let $R_E = 10\Omega$; $R_1 = 100\Omega$ and $R_2 = 50k\Omega$.

$$\therefore \Delta V_2 = \frac{5 \times 10^4}{100 + 10} \Delta V_1 \\ = 455 \Delta V_1$$

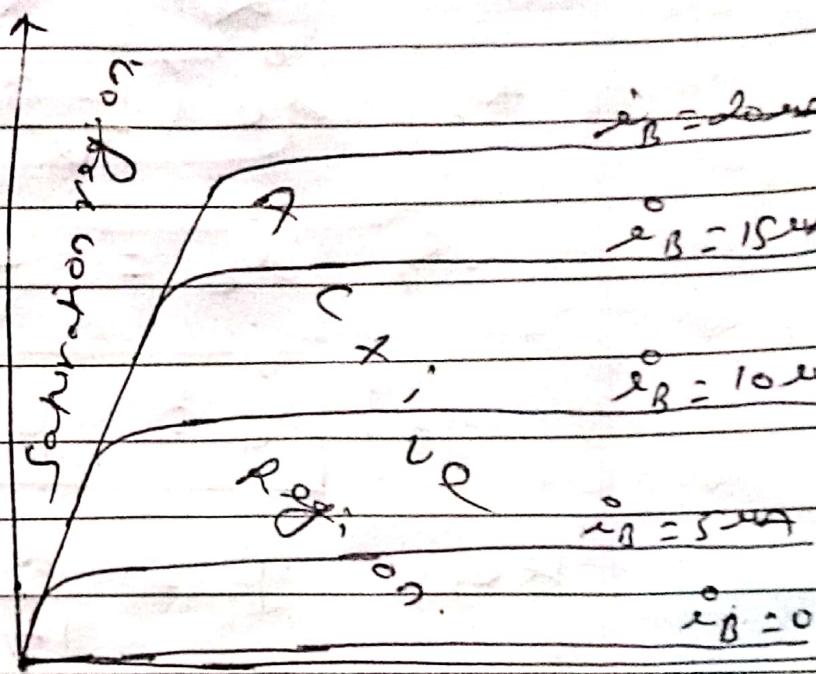
i.e., the output is 455 times the input.

Common Emitter Configuration:



The CE configuration mode has been shown in the ckt. The input terminal is forward biased while the output terminal is reverse biased.

The i_c vs V_{CE} , i_c (mA) called the output characteristics of CE configuration has been shown in the fig.



The voltage at which current $\rightarrow V_{CE}(V)$ fairly remains constant is the knee voltage. Towards the right of the knee voltage there is ~~cutoff~~^{active} region. The current here almost remains constant even on increasing V_{CE} .

Towards the left of the knee voltage, there is a saturation region. In it current has a sharp increase even on increasing a slight voltage.

Here,

$$\dot{i}_E = \dot{i}_B + \dot{i}_C$$

$$\therefore \frac{\dot{i}_C - \dot{i}_C}{\alpha} = \dot{i}_B$$

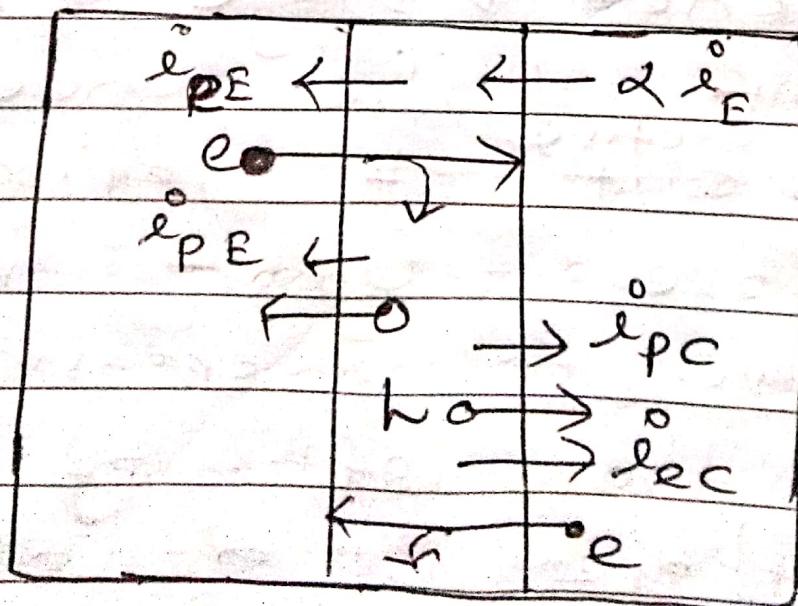
$$\therefore \dot{i}_C \left(\frac{1-\alpha}{\alpha} \right) = \dot{i}_B$$

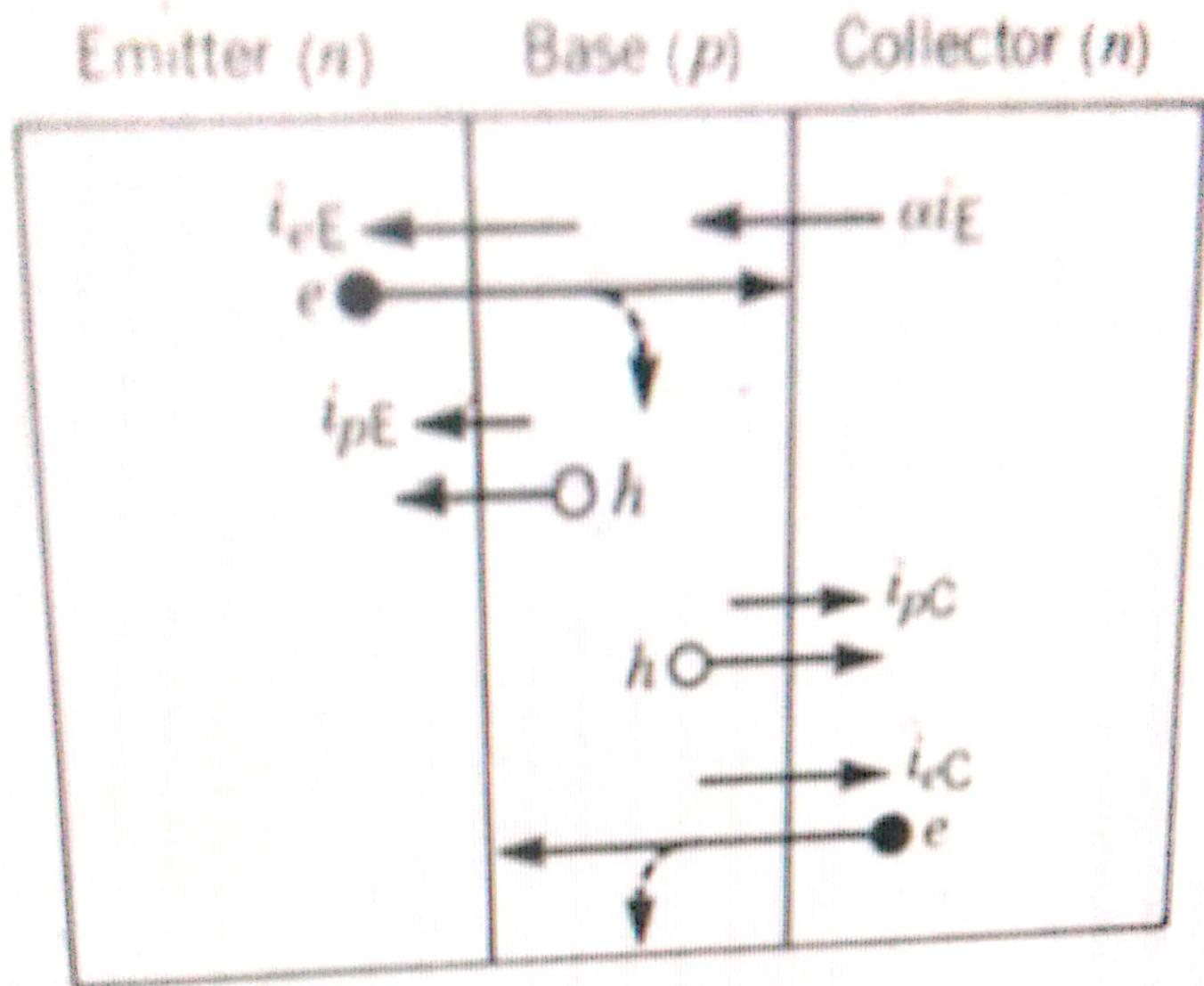
$$\therefore \dot{i}_C = \frac{\alpha}{1-\alpha} \dot{i}_B$$

$$\therefore \boxed{\dot{i}_C = \beta \dot{i}_B}$$

Here $\beta = \frac{\alpha}{1-\alpha}$ is the

current gain parameter.



**FIGURE 26-21**

Schematic representation of the flow of electrons and holes across the two junctions of a transistor, connected in the common emitter configuration, when V_{BE} is less than a few tenths of a volt.

Field Effect Transistor

Date / /

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(FET)

Junction Field Effect
Transistor (JFET)

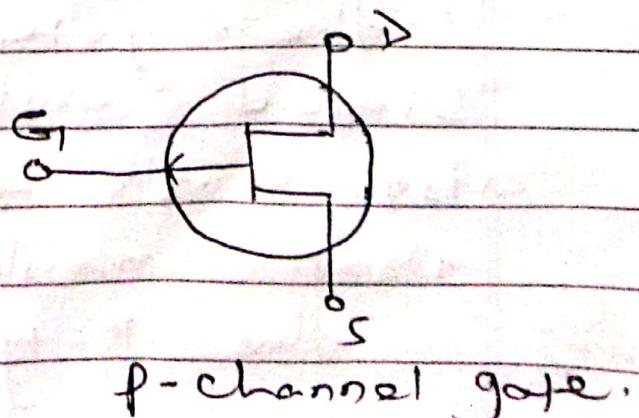
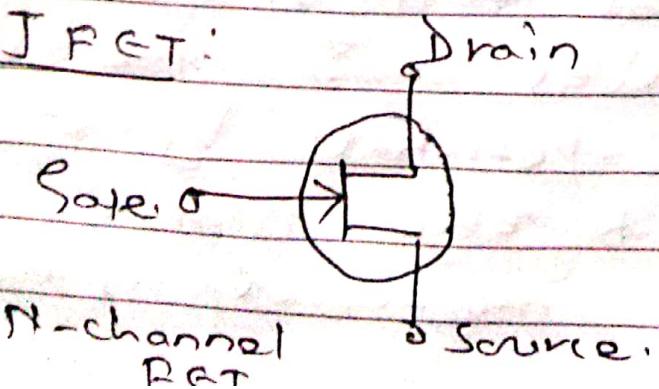
metal oxide field
Effect Transistor.

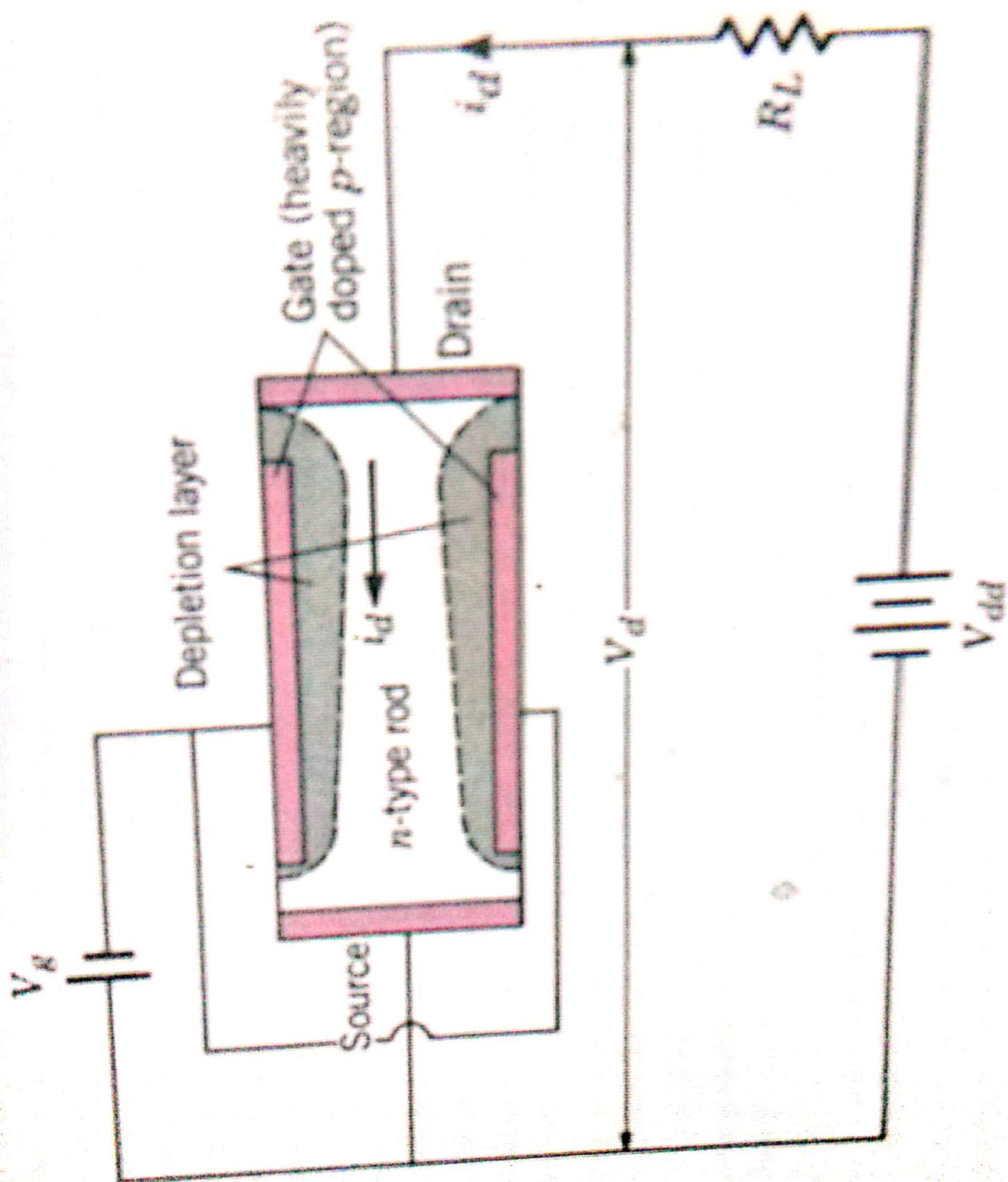
The disadvantage of the low resistive path in the input in BJT version transistor is overcome by the introduction of the FETs. The low resistive path changes current and so the magnitude of the voltage across the resistor.

Salient features:

- * FETs are the voltage controlled devices i.e., current is controlled by the electric field applied at the gate of the FET and hence the name Field Effect Transistor.
- * The current is constituted by only one type of carriers while it is done by both electrons and holes in BJT.

JFET:





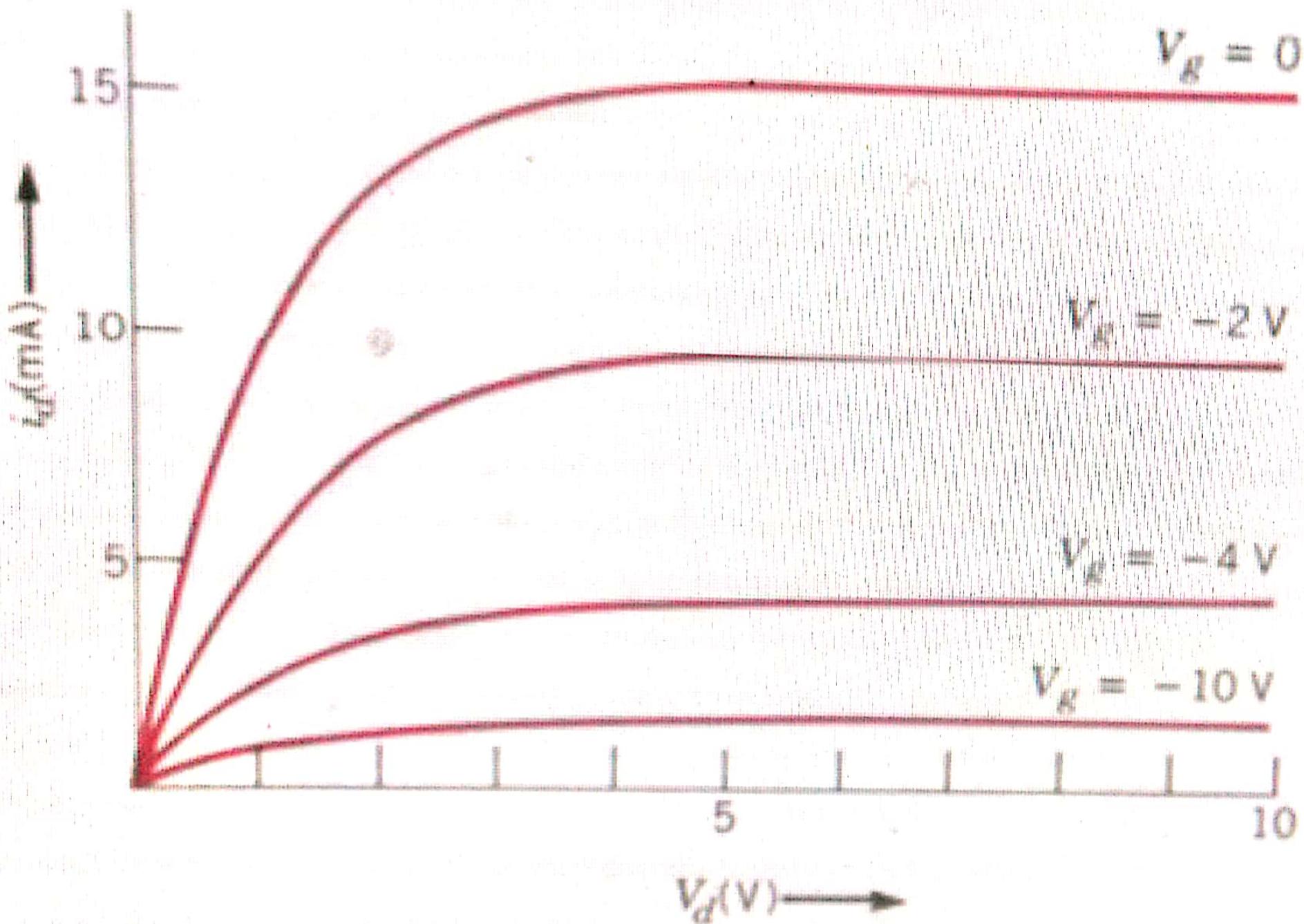
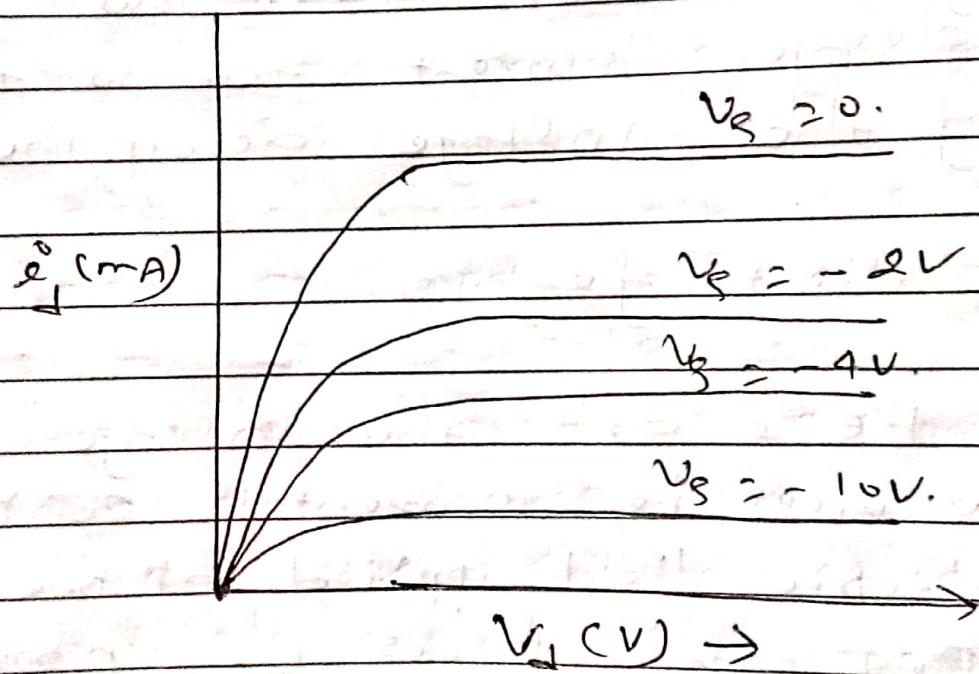
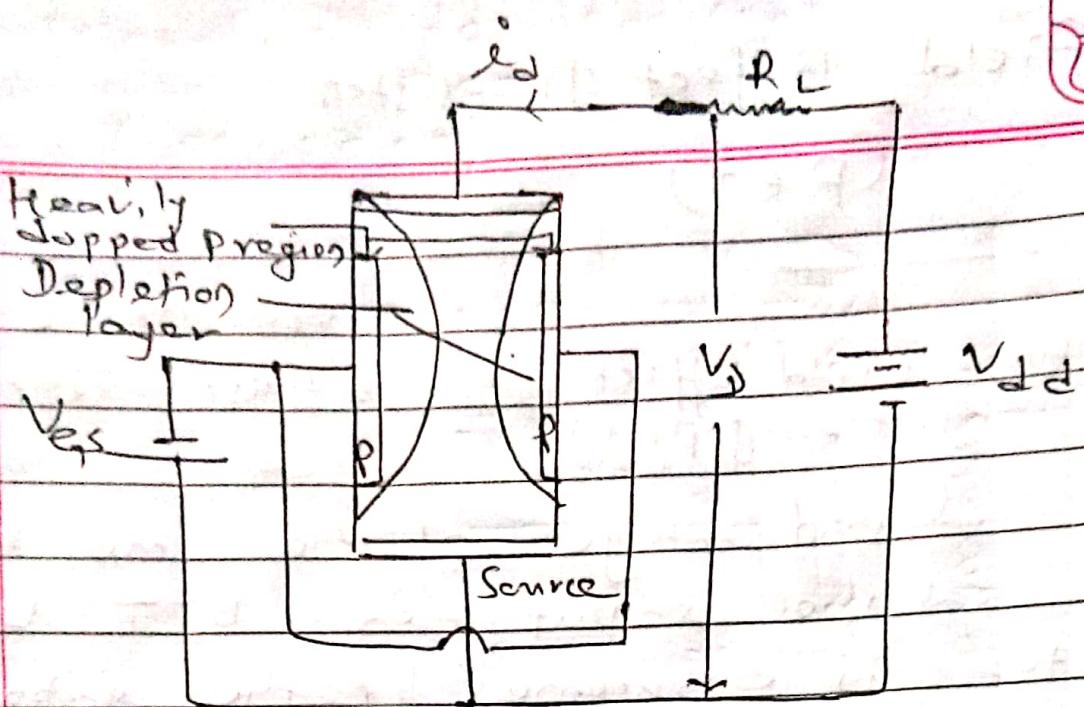


FIG
Out
ver
the
circ



Here are three regions, the gate (G) interconnected, the drain (D) and the source (S).

The gate is always reverse biased with V_{GS} and the drain also with +ve potential V_D at drain that vanishes to zero near the source.

The P-type material is embeded

On a N-type rod, the rod hence from J to S acts as an n^+ -channel.

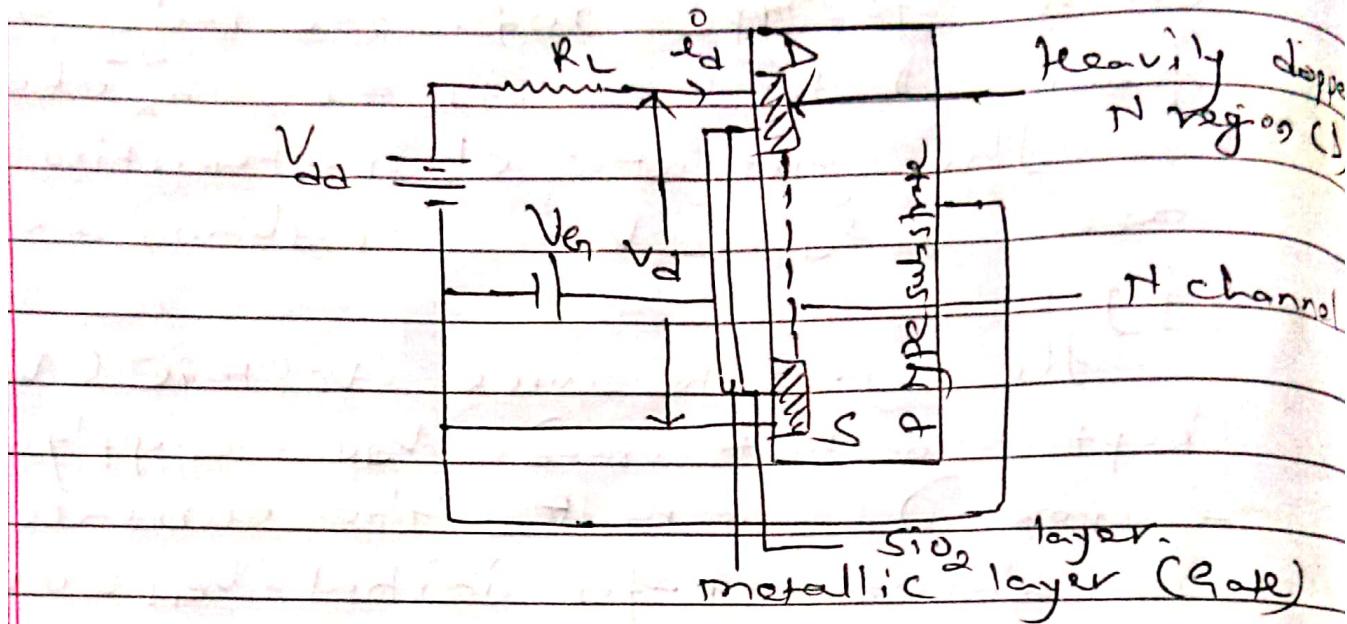
The output characteristics curves are (i_d vs V_d) is shown in the fig.

The gate to source voltage (V_{gs}) is kept constant and V_{dd} supply is increased so that the current goes on increasing for initial $V_{gs} = 0V$ and finally levels off.

The V_{gs} is varied for -2V, -4V, -10V and so on. The PN junction is reverse biased, the depletion region widens, the N-channel becomes narrow, the i_d current increases initially and immediately levels off with the increasing order of V_{gs} . The characteristic curves are shown in the fig.

Metal-oxide Semiconductor FET (mosfet)

Date / /
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The circuit diagram for the mosfet has been outlined in the fig. There is a p substrate on which two heavily doped N regions as drain and source are made. A metallic layer, called the gate is deposited upon SiO_2 layer on the p substrate.

For $V_g = 0$, there is no current as V_{dd} acts as a reverse bias to p substrate and the heavily doped N regions (J and S). For the +ve potential on the gate electrons from the p substrate are attracted to the SiO_2 layer. These electrons recombine with the holes

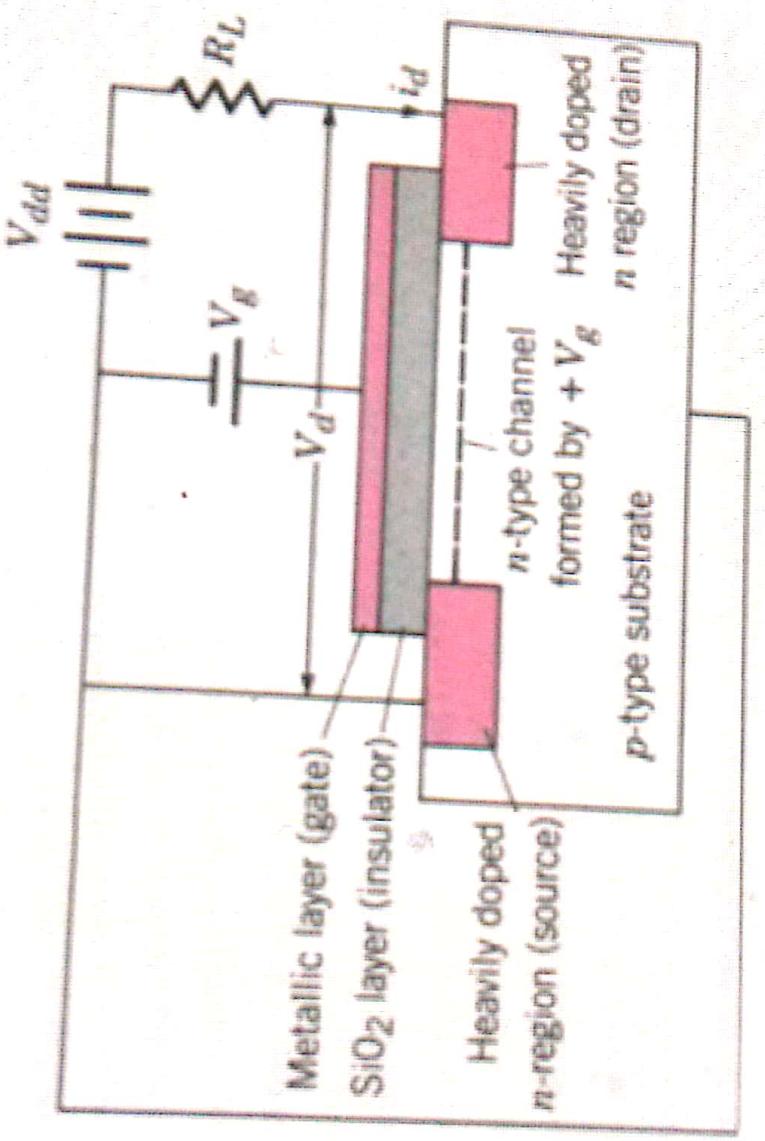


FIGURE 26-25

Structure of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

$$V_g = +5V$$

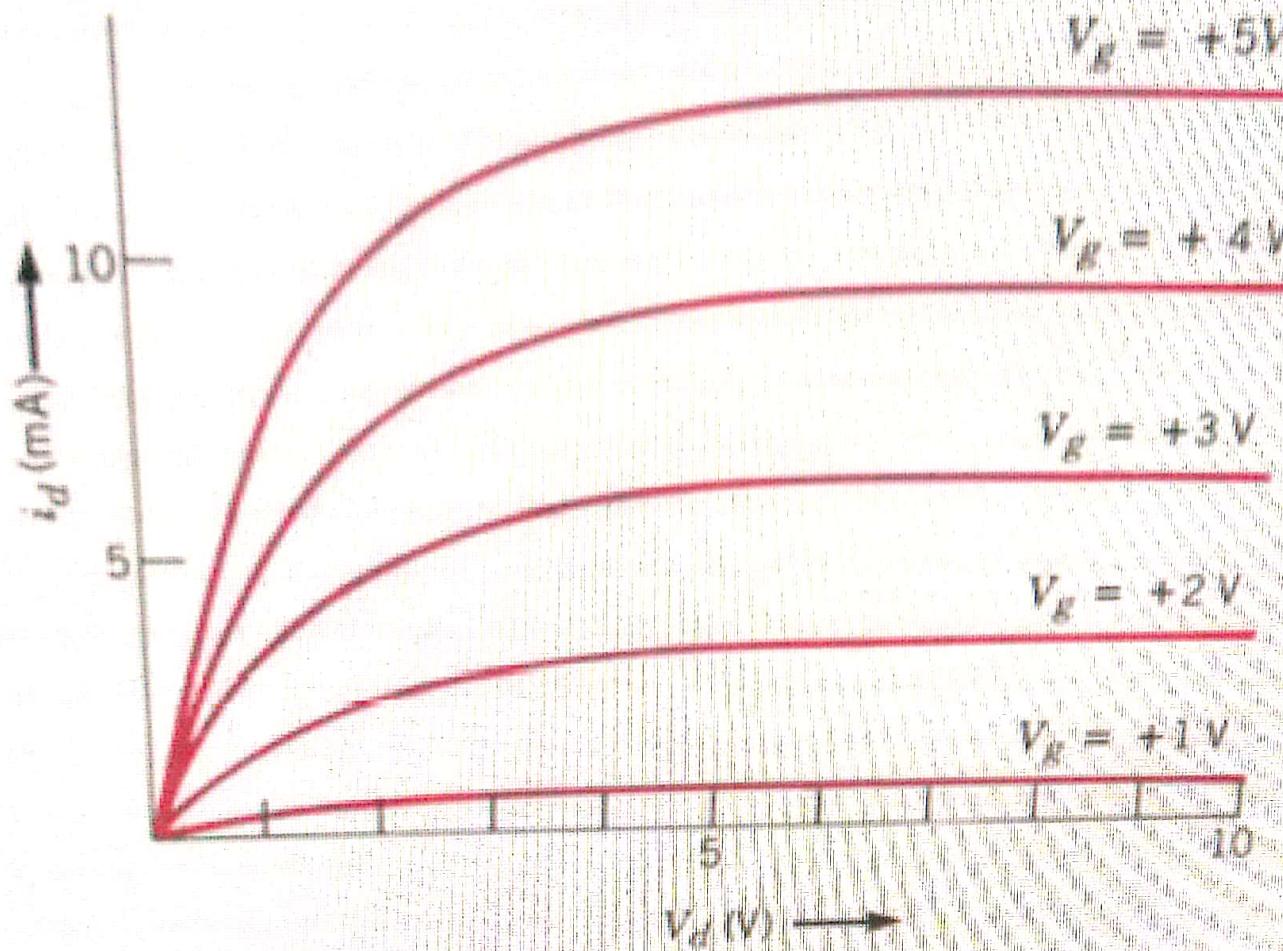
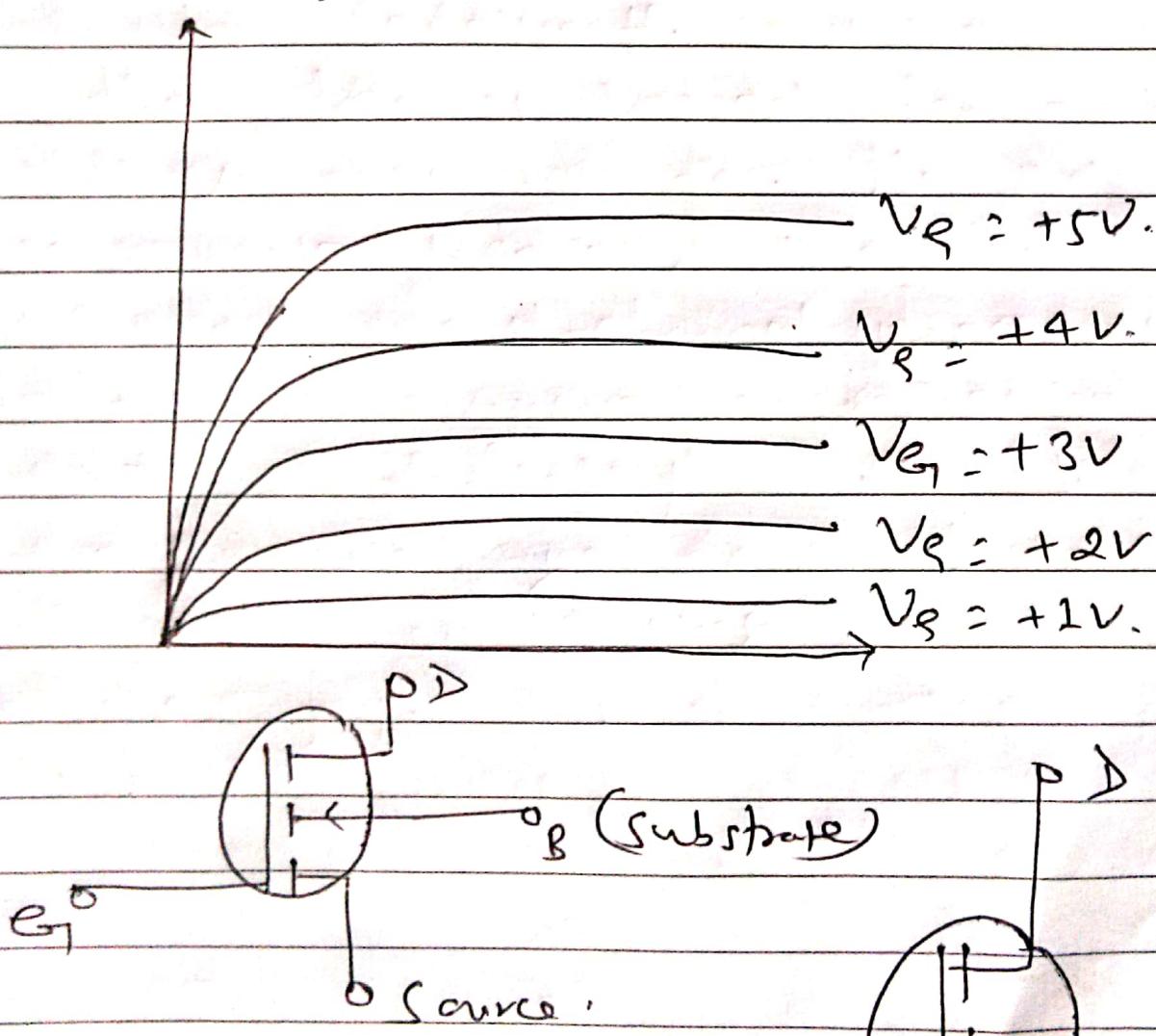


FIGURE 26-26
Output characteristic curves— i_d versus V_d —for several values of the gate voltage V_g for the MOSFET circuit of Fig. 26-25.

in the region of P substrate near the SiO_2 interface. As a result, a small N channel layer forms near the interface along which I_d begins to flow. The greater the value of V_g , the wider the channel and hence greater I_d will flow for the given V_t . The I_d vs V_g for various values of V_d are shown below.



N channel
(P type substrate)

p ch channel

N-type