

IC Fabrication

The process of IC Production(Fabrication)
(The Photolithographic process).

The components of an Integrated Circuit are all constructed on a single, tiny piece of a semiconductor crystal, called a chip; that may contain hundreds of diodes, transistors, resistors and capacitors (but no inductors). The conducting paths that interconnect the components of an integrating circuit are contained entirely within the device and the only leads that are brought out are those necessary for power supply connections, grounds and circuit inputs - outputs.

Followings are the processes involved in the IC fabrication processes:

i) Epitaxial Growth :

The epitaxial growth is the deposition of the Si atoms from a vapour on the substrate as a layer that has the same crystal structure and orientation as the substrate. It has been discussed just above. During the IC fabrication, this method is already employed and Si wafer is made pure and ready.

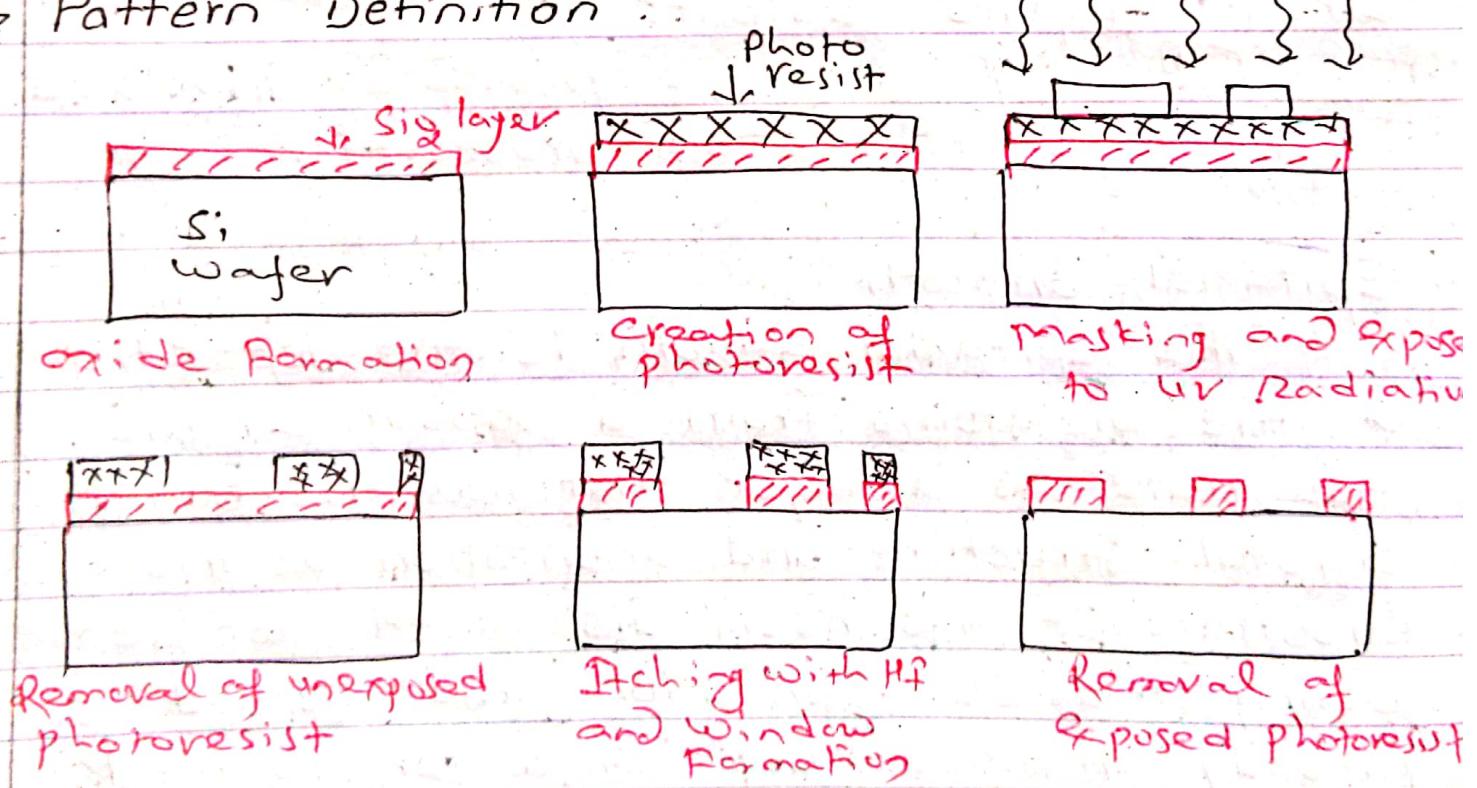
ii) Oxidation :

The method is accomplished by heating

a Si crystal wafer at 1000°C to 1200°C in presence of oxygen or steam. Then a layer of SiO_2 is constructed on the wafer. The thickness of SiO_2 layer depends on temperature, oxidation time and the nature of the atmosphere.

The purpose of oxidation (Formation of a SiO_2 layer) to permit the opening of the windows on wafer surface, block impurities to pass to it to contaminate PN junction and enhances interelectrode connection between the components.

Pattern Definition :



Pattern definition involves the methods to locate the desired places for the IC components to be formed.

The first step here is to coat the SiO_2

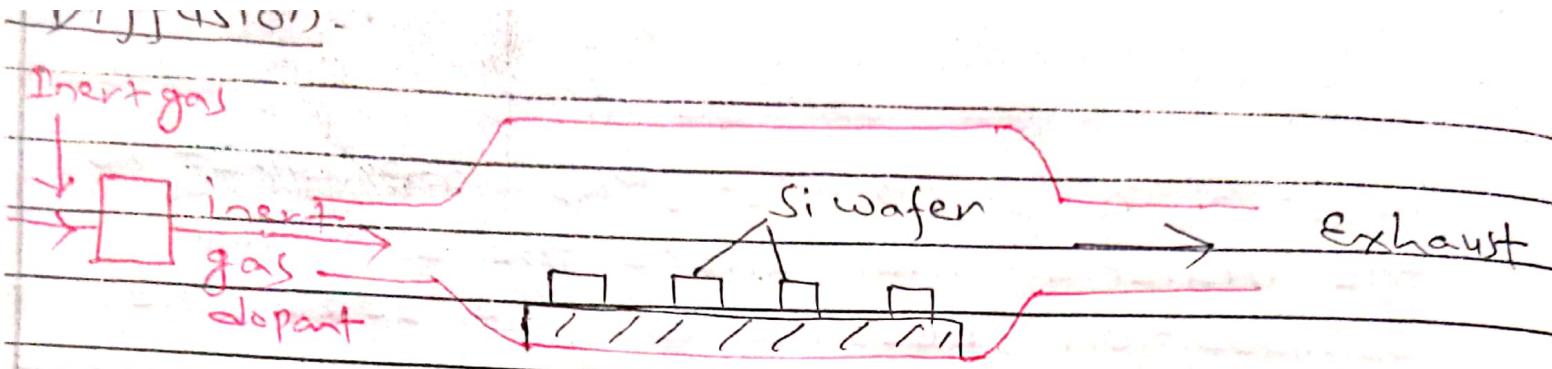
layer by a photoresist (PR) material. It is the material that alters the chemical composition (becomes polymerized) when exposed to uv light. Then masking is made i.e., the desired locations, for the opening of window are selected ~~use~~ using masking. Then the film of PR is exposed to uv radiation. The exposed PR is polymerised ($\text{Cl} - \overset{\text{C}}{\underset{\text{Cl}}{\text{C}}} = \overset{\text{C}}{\underset{\text{H}}{\text{C}}} - \text{Cl}$) and hence the exposed and the unexposed PR have different solubilities on certain chemicals. Now the unexposed PR is removed by treating on such chemicals. Finally the SiO_2 is etched away by treating it with HF. and the openings of the windows are created there. After it, the remaining PR, exposed to uv, is washed away in some solvent. The wafer hence become ready for the dopants and metallic conduction.

Doping :

It is the process of injecting impurity atoms (P-type or N-type) into the selective region of the chip.

It is done in two ways; diffusion and ion implementation.

Diffusion :



The schematic fig. to illustrate diffusion has been shown in the figure.

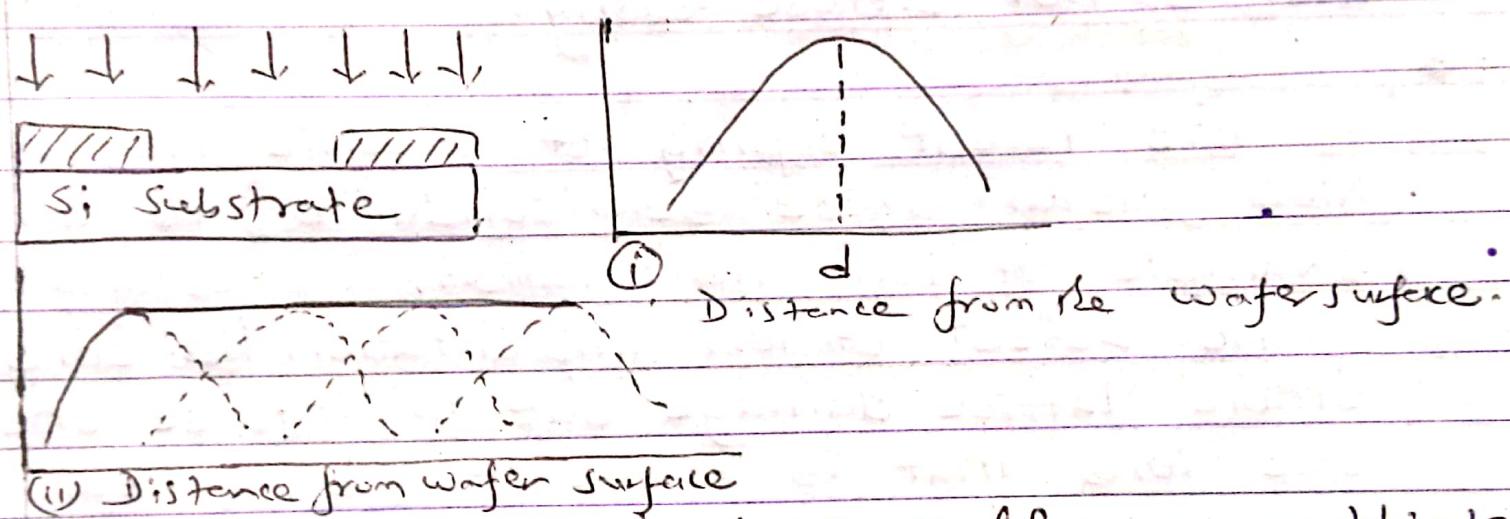
On heating Si wafer at around 1000°C some of the atoms move out of their lattice sites, leaving behind the empty lattice sites that migrate entire of the sample. If the heating is made in the environment of boron or phosphorus, their atoms occupy such lattice sites and spread over the bulk of the Silicon. The diffusion layer is controlled on diffusion time and temperature that can be stopped by cooling the wafer. The SiO_2 layer acts as a mask to provide selective diffusion.

The dopants are passed into the heating furnace with the help of inert carrier gas in the form of bubble. Moreover, gaseous compounds such as diborane (B_2H_6) or phosphorus trifluoride (PF_3) can be diffused directly.

It is found that an approx. of $1 \mu\text{m}$ diffusion layer of phosphorus sets up in 1 hr at 1000°C .

Ion Implantation

It is an alternative method of introducing ions into the semiconductor. In this method, ions of the concerned dopants are accelerated in a vacuum by a p.d of several volts.



The accelerated ions suffer a multiple collision within the wafer that finally come to the rest. Since the collision is not uniform, their distribution is as indicated in the fig (i) above which is a gaussian like.

The average distribution is uniform on accelerating the ions on varying p.d. as in fig (ii)

The individual gaussian distribution dotted is due to the specific voltage. The horizontal thick line by summing the individual gaussian distribution gives the average distribution.

The ion implantation has many more advantages over the diffusion process.

Connection of Components in a Chip:

For a complete ckt within a chip, the electronic components within a layer as well as the layers themselves must be electrically connected. Mostly it is accomplished by metallic thin film evaporation.

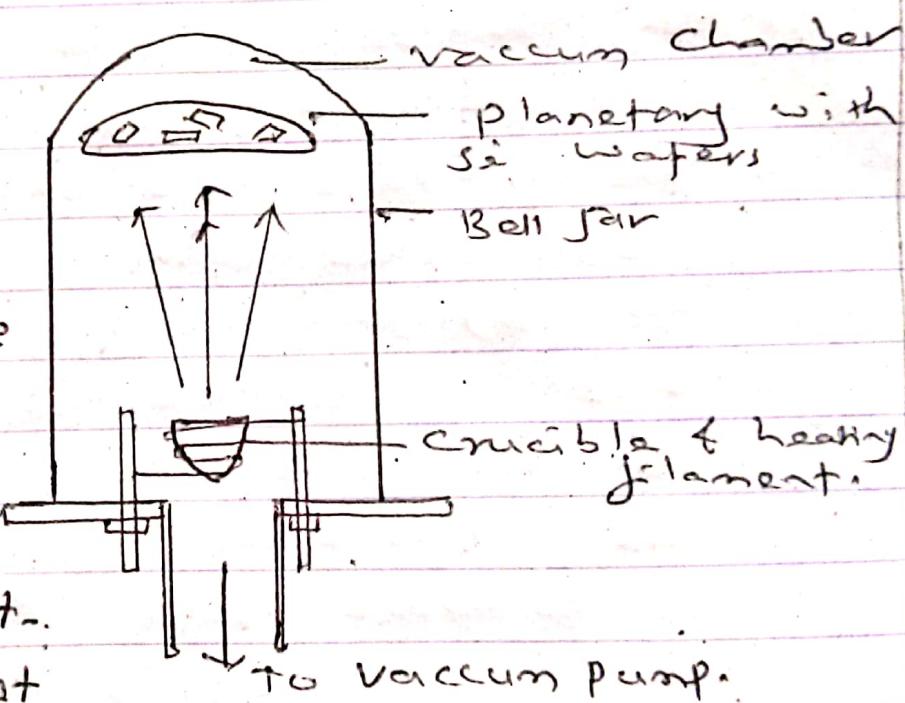
The schematic diagram has been outlined in the fig.:

The metal is to be evaporated (aluminium or gold) is placed in a crucible wrapped with a heating coil. The vapour of the metal is produced by heating the crucible that

is allowed to hit the cooled masked wafer placed just above it in a planetary.

The vapour finally condenses in a desired pattern.

The entire procedure is conducted in a vacuum to avoid contamination with oxygen gas.



Electronic Component (Fabrication on a Chip)

Here we discuss how the techniques can be used to fabricate basic components of a ckt i.e., transistors, diodes, resistors and capacitors.

Transistors and Diodes :

Following are the steps:

- * First an epilayer of N-type is grown onto a P-type wafer (fig i).
- * The N-layer is then oxidised (SiO_2), masked, exposed to uv light and so on, that results to the formation of window on the oxide layer (discussed in pattern definition).
- * Acceptors impurities are diffused to convert part of the exposed N-layer to P-typed layer. A part of this p-layer acts as a base.

The wafer is again oxidised and a window is opened in the new oxide layer, and donor impurities layer is diffused on it to convert a part of P-layer to N-layer that acts as emitter of the transistor.

At last, the wafer is again reoxidised to open three windows on collector, base and emitter separately. Aluminium is evaporated and connected to these three elements; collector base and emitter to other components of the ckt.

For the diode to fabricate ; it is similar to the fabrication of the transistor mentioned above where the last step of diffusion to emitter is omitted.

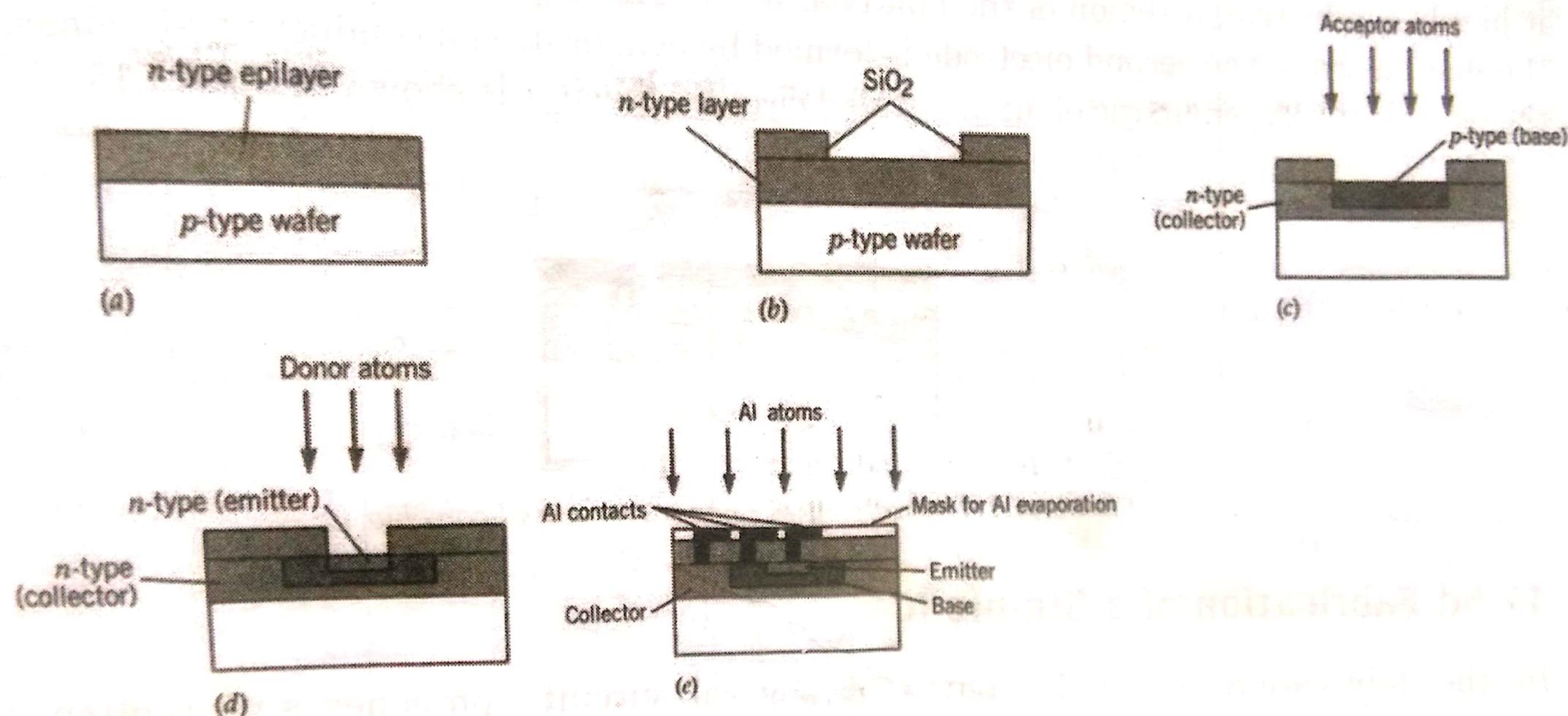


Figure 17.14: Steps involved in the fabrication of a transistor on a silicon chip

Resistors:

The resistor as an IC component is fabricated by a shallow diffusion of a P-type channel into an N region or vice versa. The current is constituted by the reverse bias of the PN arrangement. The resistance made depends on the length of the channel, cross-sectional area of the channel and doping concentration.

Due to some conductivity of Si, a large value of resistance can't be obtained by this method.

Hence a CE mode transistor is considered as a base current-controlled resistors and is introduced in a ckt where resistor is needed.

Capacitor:

It consists of two metal electrodes separated by some insulating medium.

An epitaxial layer of highly dopped (highly conductive) region acts as an electrodes. The region is covered by SiO_2 layer and the second electrode is set up by evaporating a conducting aluminium film on the oxide layer. The detailed illustration is outlined in the fig:

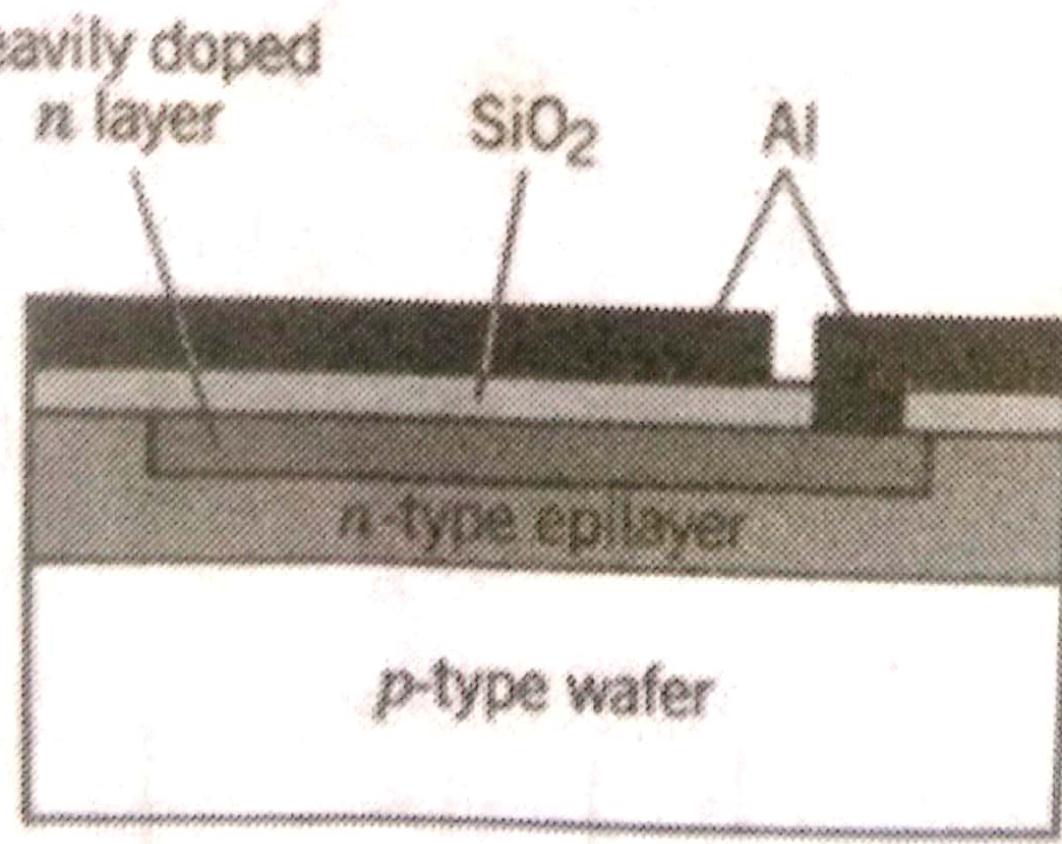
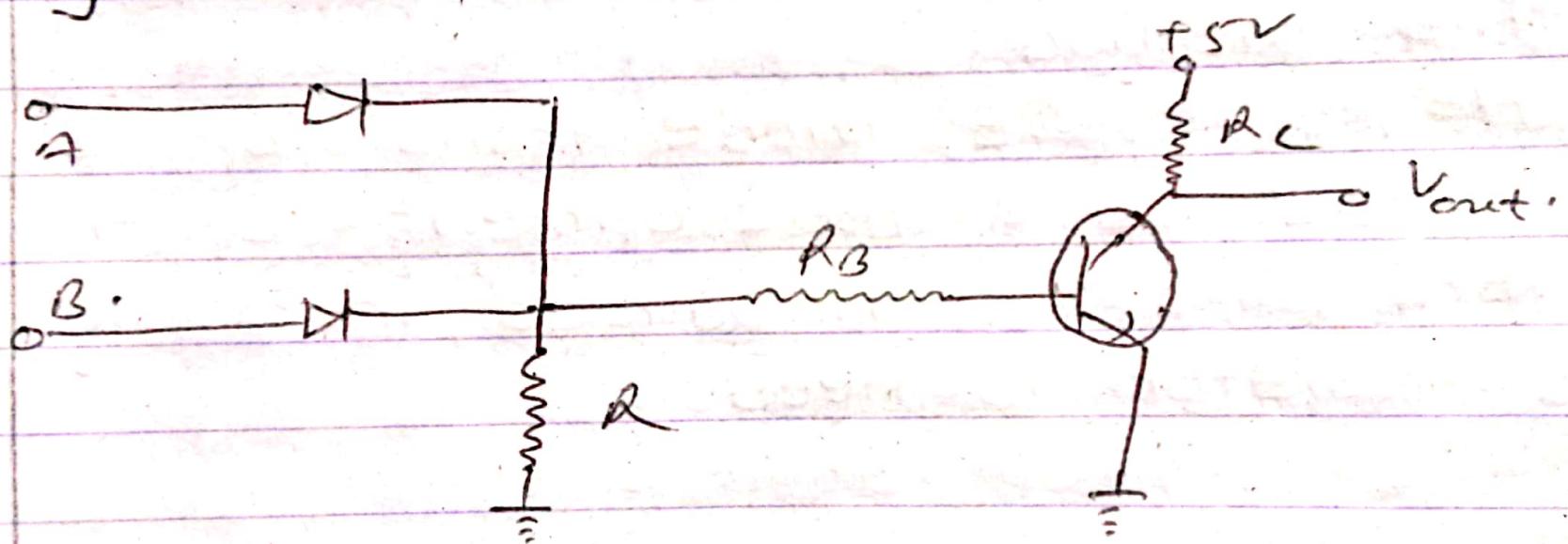


Figure 17.15: Microelectronic capacitor on a silicon chip.

Fabrication of a simple IC :

Let us take the simple ckt of a NOR gate.



Since the ckt has three distinct components: transistor, resistor and diode; we first have to create three openings for the three islands.

Followings are the key points to be noted for the purpose:

An n-epilayer is made on the P type substrate. Fig (a)

The n-layer is oxidised (SiO_2) and then coated with photoresist material.

Fig (b)

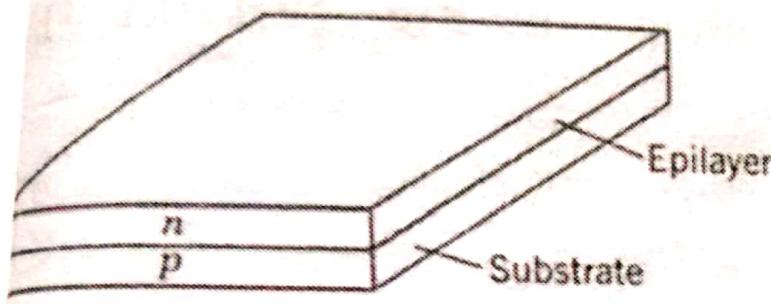
Masking for the islands is used and it is illuminated by the uv rays. Fig (c)

The photoresist not covered by the mask is removed using some chemicals and the SiO_2 layer is etched way using HF.

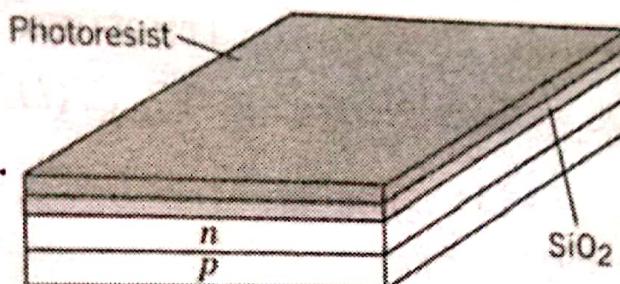
The opening of the window is created and distinctly three islands are seen there. Fig (d)

Acceptor atoms are diffused through these windows so that N layer (unmasked one) becomes P typed without penetrating it and photoresist as well as SiO_2 on the islands are removed using the process in photolithography. Finally here we see three N-type islands on a P type substance.

Such three N type islands serve for transistor, diode and resistors respectively. Fig (e)



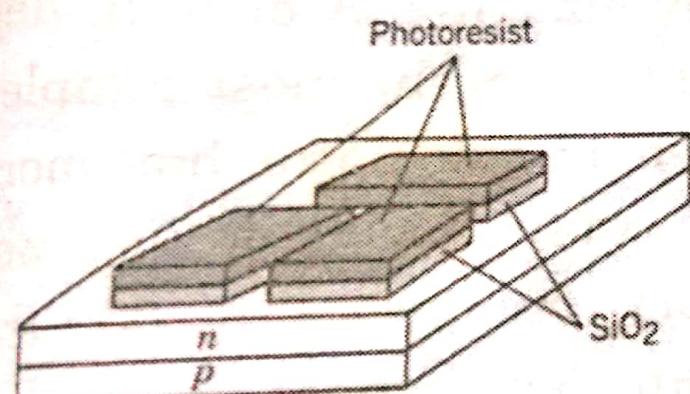
(a) *n*-type epitaxial layer
grown on *p*-type wafer



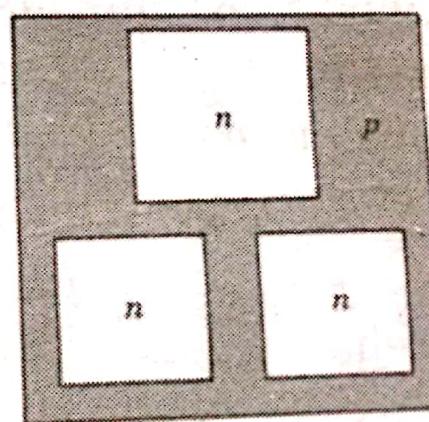
(b) Oxidation of *n*-type layer
followed by photoresist coating



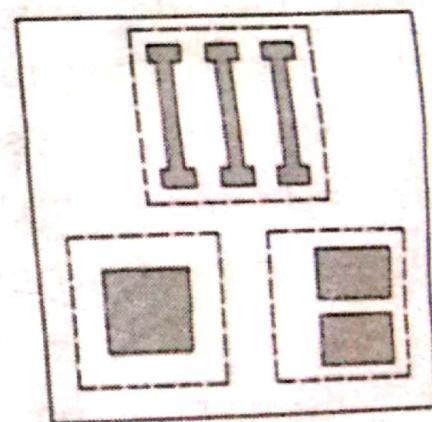
(c) Mask for *n*-type island
formation



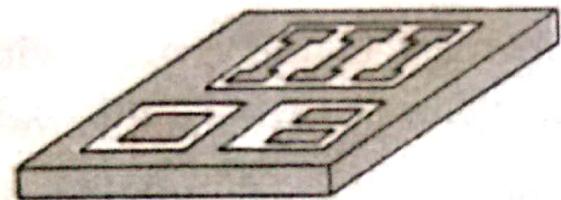
(d) Formation of oxide island
with exposed photoresist on top



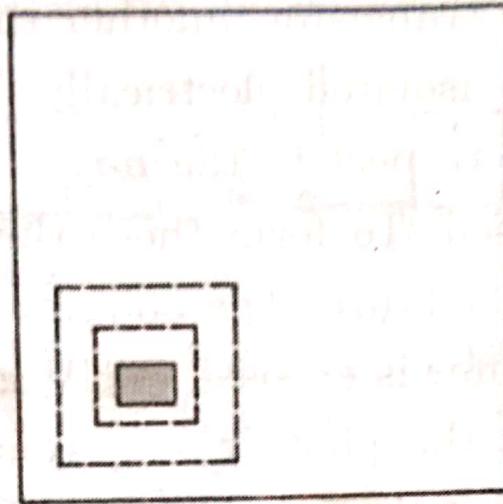
(e) Top view of wafer after
n-type island formation



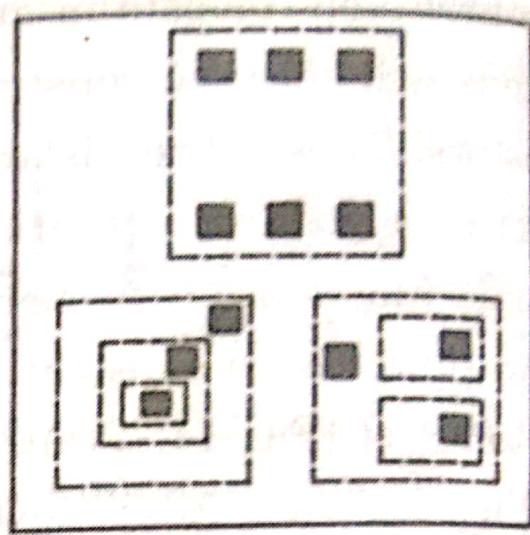
(f) Mask for *p* dopant diffusion



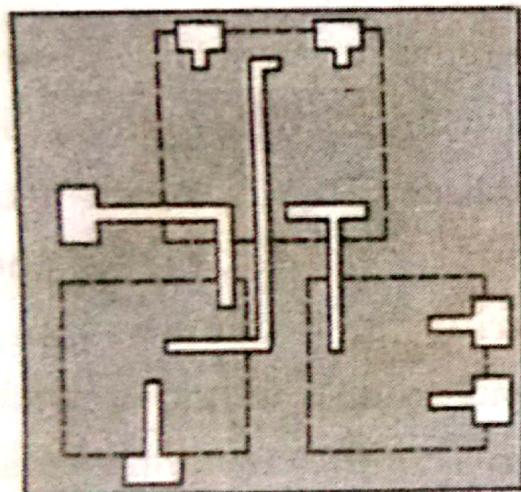
(g) State of the chip after p -type diffusion; shaded areas are p -type, white areas are n -type



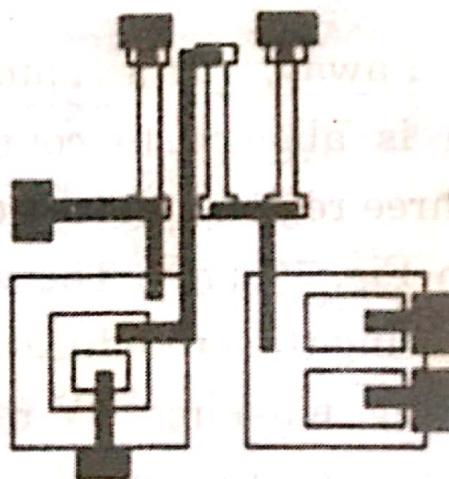
(h) Mask for emitter diffusion



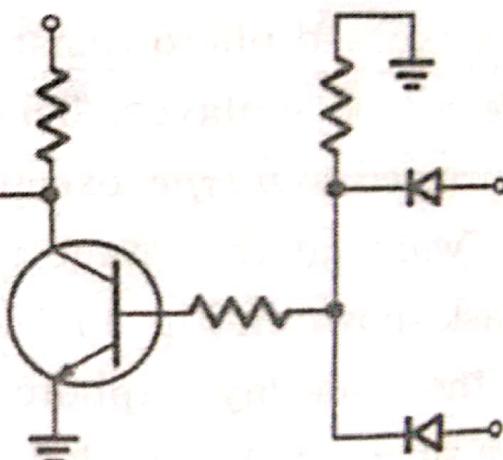
(i) Mask for electrical contact window-opening



(j) Mask for aluminum evaporation



(k) Complete and interconnected circuit



(l) Gate using conventional electronic symbols

Figure 17.17: Steps involved in the fabrication of the NOR gate of Fig. 17.16 in integrated form.

All the components are now in place and they must now be interconnected. To

- * The wafer is reoxidised (SiO_2), coated with photoresist, masking and illuminated with uv light windows with the shaded area Fig (f) are made. Acceptor impurities are diffused without penetrating N type through these windows on the n-type islands. Hence there are three resistors, in the upper island, the collector and the base of an NPN transistor the lower left island and two diodes with n side common in the lower right side. Fig (g)
- * The wafer is again oxidised, and following the processes of photolithography, window is created onto the base of the transistor and n-type dopants are diffused to form n type emitter. Fig (h)
- * Now three distinct components that are ready are to be interconnected. For this, oxidising all the steps of photolithography are followed, and small windows are opened in the both ends of the resistors three elements of the transistor and both sides of the diode. Fig (i)

Now again the wafer is masked with photolithography Fig (j). Aluminium vapour is deposited onto the window openings on the masking so that the components finally are interconnected as shown in the fig (k) and the outlined ckt is redrawn which is as outlined initially.