Matthew Wong

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Education

University of Southern California — Los Angeles, CA
M.S. in Electrical Engineering — GPA: 3.85 – *Expected May 2027*
Courses: Analog IC, Mixed-Signal IC, VLSI Circuit Design, Computer Architecture

University of California, Berkeley — Berkeley, CA
B.S. in Electrical Engineering and Computer Science — *December 2024*

Experience

Design Verification Intern — May 2025 – August 2025
Celestial AI (Acquired by Marvell Technology) — *Santa Clara, CA*

- Developed UVM RAL sequence to verify read/write permissions across register hierarchies, using front-door and back-door access methods
- Implemented custom VPI (Verilog Procedural Interface) functions to enable force write and read operations on real-valued signals
- Created behavioral models of analog circuits (bandgap reference, variable resistors, oscillators) for co-simulation

Research Assistant — August 2024 – May 2025
Chien Lab, Berkeley Sensor and Actuator Center — *Berkeley, CA*

- Co-led the design of an automated aptamer-based biosensor system for 3-electrode experiments
- Fabricated multilayer PCBs considering power integrity, layer stack up, and design for test
- Wrote firmware libraries for SPI and I2C protocols

Projects

Variable Gain Amplifier | *Cadence Virtuoso*

- Designed a two-stage, fully differential amplifier using 45 nm technology with gain settings of 2, 4, and 8 using resistive feedback
- Performed device characterization to utilize gm/ID methodology for sizing devices
- Implemented Miller compensation for stability
- Created CMFB blocks and current mirrors to obtain a CMRR of 115 dB
- Achieved gain of 72 dB, phase margin of 67°, power consumption of 3.5 mW, and UGBW of 1.1 GHz

Temperature Sensor IC | *Ngspice, Xschem*

- Achieved accuracy of ± 5°C, active current of 1 μA, sampling time of 100 ms, conversion time of 30 μs, and area of 160x110 μm
- Implemented bandgap circuit and relaxation oscillator circuits to convert temperature to frequency domain
- Utilized RTL counter and FSM to calculate temperature output

RISC-V Softcore Processor | *SystemVerilog, Vivado*

- Designed a 5-stage pipelined processor for PYNQ Z2 running at 125 MHz
- Resolved data hazards with HDU, forwarding unit, and stalling logic
- Achieved 90% branch prediction utilizing a 2-bit predictor and flushing logic

FIR Filter | *SystemVerilog, Python, Vivado*

- Created a 7th order moving average filter for reducing white noise in audio applications
- Designed HDMI interface to display pre-processed and post-processed waveforms

Skills

Languages: SystemVerilog, Verilog-A, Python, C, MATLAB
Tools: Virtuoso (Schematic & ADE), Spectre, SimVision, Ngspice, Xschem, Magic, Altium