Matthew Wong

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Education

University of Southern California — Los Angeles, CA
M.S. in Electrical and Computer Engineering — *Expected May 2027*
Concentration: Analog, Mixed-Signals, RF Integrated Circuits

University of California, Berkeley — Berkeley, CA
B.S. in Electrical Engineering and Computer Science — *GPA: 3.61 — May 2025*
Relevant Courses: Digital Integrated Circuits, Analog Integrated Circuits, Computer Architecture, Integrated Circuit Devices, Microfabrication Technology

Experience

Research Assistant | *Altium, Matlab, Python, Soildworks* — August 2024 – Present
Chien Lab, Berkeley Sensor and Actuator Center — *Berkeley, CA*

- Led the design of an automated aptamer-based biosensor system for 3-electrode experiments
- Fabricated multilayer PCBs considering signal integrity, power distribution, and thermal management
- Wrote firmware libraries for SPI and performed system verification
- Electrochemical sensing for the aptamers kanamycin (used in treating MDR tuberculosis) and doxorubicin (chemotherapeutic agent for breast, bladder, and other cancers)

Projects

LCD Display Driver | *Cadence Virtuoso, Python* — December 2024

- Designed a differential input, single-ended output amplifier in 45nm CMOS to display pixels at 60 Hz
- Two-stage op-amp: telescopic cascode stage (high gain) and class AB output stage (avoid slewing)
- Miller compensation for stability
- Switched-capacitor feedback in closed loop, RC load to model driving the pixel
- Achieved gain of 71 dB, phase margin of 55°, power consumption of 2 mW, and settling time of 160 ns

RISC-V Softcore Processor | *SystemVerilog, Synopsys VCS, Cadence Innovus* — December 2024

- Designed a 5-stage CPU for FPGA running at 130 MHz and average cycles per instruction of 1.3
- Implemented branch prediction and forwarding paths
- Utilized AXI to communicate with cache

DAC Design | *Cadence Virtuoso* — September 2024

- Implemented R-2R ladder topology for an 8-bit DAC
- Reached ± 0.5 LSB accuracy and settling time of 5 μS
- Performed verification and characterization tests for linearity analysis

FPGA Facial Recognition | *SystemVerilog, Python, Vivado* — August 2024

- Implemented the Haar cascade algorithm for face detection and the Local Binary Pattern Histogram (LBPH) for feature extraction
- Enabled real-time results through dual core processor to parallelize detection and recognition data

Skills

Languages: SystemVerilog, Python, MATLAB, C, Java, RISC-V
Tools: Vivado, TCL, Virtuoso, Altium, Innovus, Solidworks
Circuits: TIA, LDO, Comparators, Switch-Capacitor, SAR ADC, DAC, FIFO
Communication Protocols: UART, I2C, SPI, AXI