Matthew Wong

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Education

University of California, Berkeley Berkeley, CA
Bachelor of Science in Electrical Engineering and Computer Sciences *December 2024*
Relevant Courses: Digital Integrated Circuits, Analog Integrated Circuits, Computer Architecture, Integrated Circuit Devices, Microfabrication Technology

Experience

Undergraduate Research Assistant August 2024 – Present
Chien Lab, Berkeley Sensor and Actuator Center *Berkeley, CA*

- Designed and implemented an integrated system combining a pipetting robot and a potentiostat to automate 3-electrode system experiments
- Fabricated PCB to support 24 different experiment protocols and 3D-printed mounting components
- Utilized I2C buses to connect micro controller with multiple bi-channel multiplexers
- Achieved 4x increase in weekly experiment throughput compared to non-automated process

Data Engineering Intern May 2024 – August 2024
Citylitics *Toronto, ON*

- Improved demographic database accuracy by 15% through Levenshtein distance calculations for duplicates detection and parameter updates (county, zip-code, etc.)
- Developed a snippet labeling application to assist in training an AutoML classifier
- Created a data visualization dashboard using BigQuery to document Django admin permissions

Projects

LCD Display Design | *Cadence Virtuoso* Ongoing

- Developing a driver for a 38-mm Apple watch display
- Analyzing trade-offs between resolution, refresh rate, and power consumption
- Testing 2-stage amplifier with telescopic NMOS stage (optimized for gain) and common source stage (optimized for slew rate)

FPGA Facial Recognition | *SystemVerilog, Python, Vivado* June 2024 – July 2024

- Implemented Haar cascade algorithm for face detection and Local Binary Pattern Histogram (LBPH) for feature extraction
- Utilized ARM A9 dual core processor to parallelize detection and recognition data for real time results
- Achieved 88% accuracy with 720p laptop camera and HDMI connection

ASIC RISC-V CPU | *Verilog, DVE, Hammer* March 2024 – May 2024

- Designed a 3-stage CPU running at 81.42 MHz
- Implemented a 4KB direct-mapped cache with SRAMs
- Verified edge-cases through testbenches
- Optimized layout placement and routing through trace analysis to minimize wire delay

Audio Visualizer PCB Design | *Altium* February 2024

- Designed and assembled a PCB that converts audio input into LED patterns
- Implemented a filtering circuit to distinguish bass, mid, and treble frequencies
- Gained hands on experience in soldering and debugging practices with multimeter and oscilloscope

Technical Skills

Languages: Verilog, SystemVerilog, Python, MATLAB, C, Java, RISC-V Assembly
Tools: Vivado, Cadence Virtuoso, Altium, Cadence Innovus, Synopsys Sentaurus, Autodesk Inventor