Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course Integrated Systems Architecture

Master degree in Electrical Engineering

Authors: group 31

Stefano Giorgio S286291 Armando Ruggiero S286892 William Tessitore S292444

November 21, 2022

Contents

CHAPTER 1

Lab 1: design and implementation of a digital filter

1.1 Reference model development

The aim of this laboratory is to design a digital filter with a cut-off frequency of 2 kHz and sampling frequency of 10 kHz. According to the algorithm, the filter that will be designed is an Infinite Inpulse Response (IIR) with the following parameters:

$$N = 2$$

$$n_b = 9$$

where N is the order of the filter and n_b is the number of bit.

1.1.1 Matlab model

The filter has been designed by means of Matlab both for the floating point and fixed point precision of coefficients. The frequency response of the filter is shown in Figure 1.1.

As it can be seen, the cut-off frequency is compliant with the specifications for both precisions since the -3 dB point is at a normalized frequency of $0.4 \cdot f_{Nyq} = 2kHz$. The coefficients of the filter have one bit for the integer part and 8 bits for the fractional part. They correspond to the integer values shown in Table 1.1.

a_0	256
a_1	-95
a_2	50
b_0	52
b_1	105
b_2	52

Table 1.1: Quantized coefficients.

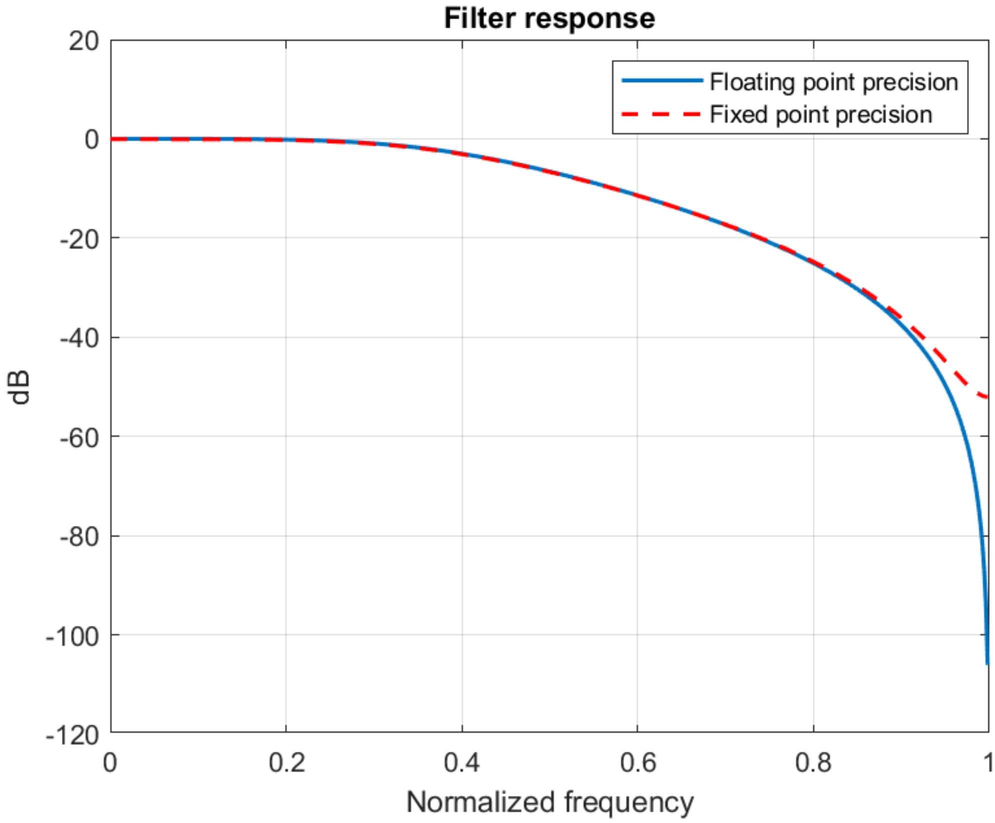


Figure 1.1: Filter response for both floating point and fixed point coefficients. The frequency has been normalized with respect to the Nyquist frequency (5 kHz).

1.1.2 C model and THD

A *C model* of the filter has been developed considering a reduction of precision for the multiplications. The parameter responsible for this reduction is the $SHAMT$ that represents the number of bits to be discarded after each multiplication. The output results obtained from the *C model* have been analyzed in order to achieve a maximum THD of -30 dB.

Comparing figures 1.2 and 1.3 is possible to deduce that the $SHAMT$ that allows to meet the specifications is 11. The number of bits after each multiplication is 7. With this configuration the THD achieved is -30.83 dB.

1.1.3 Explanations, comparisons and comments

Comparing the results obtained from the Matlab simulation and the C model with $SHAMT = 11$, it is possible to point out that the maximum difference between the output samples is 17 with an average difference of 3.84. The quantization error introduced by the C model leads to an increased THD that for the Matlab floating point precision is -52 dB.

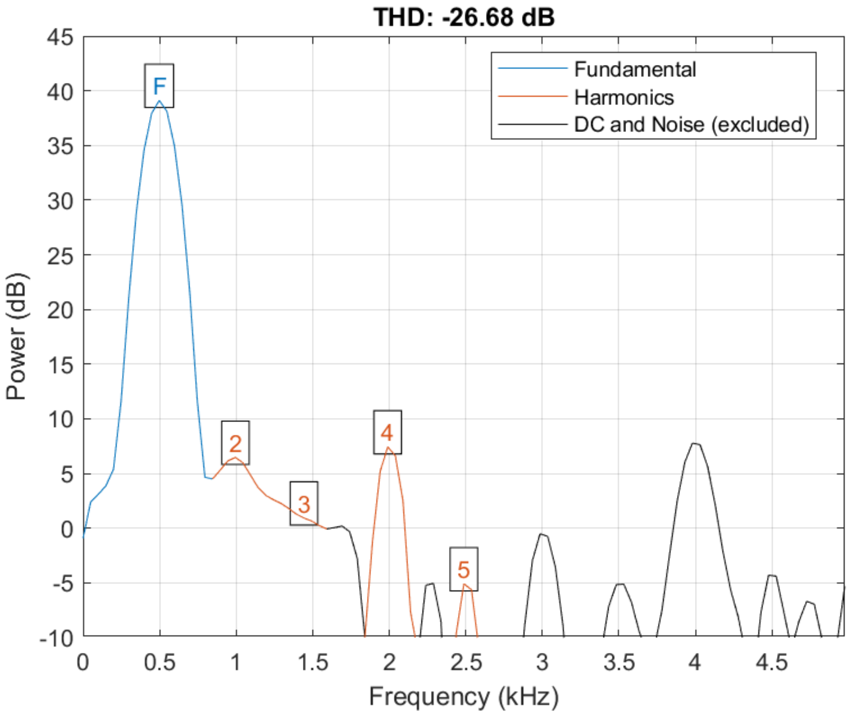


Figure 1.2: THD analysis for $SHAMT = 12$.

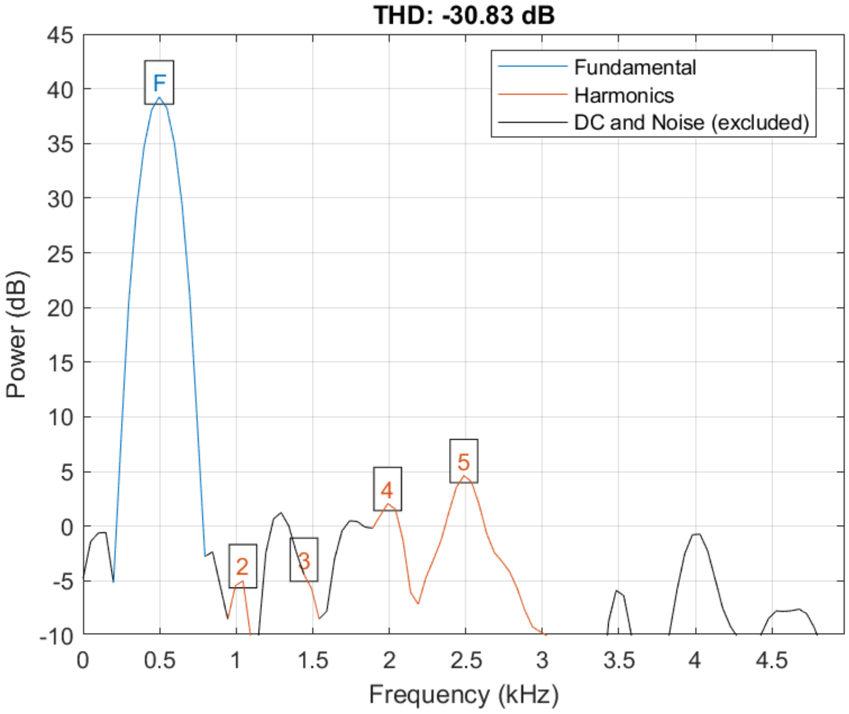


Figure 1.3: THD analysis for $SHAMT = 11$.

1.2 VLSI implementation

1.2.1 Architecture

The architecture of the filter is shown in Figure 1.4 and the timing diagram in Figure 1.5. The IIR filter is based on a Direct Form II model, according to given specifications.

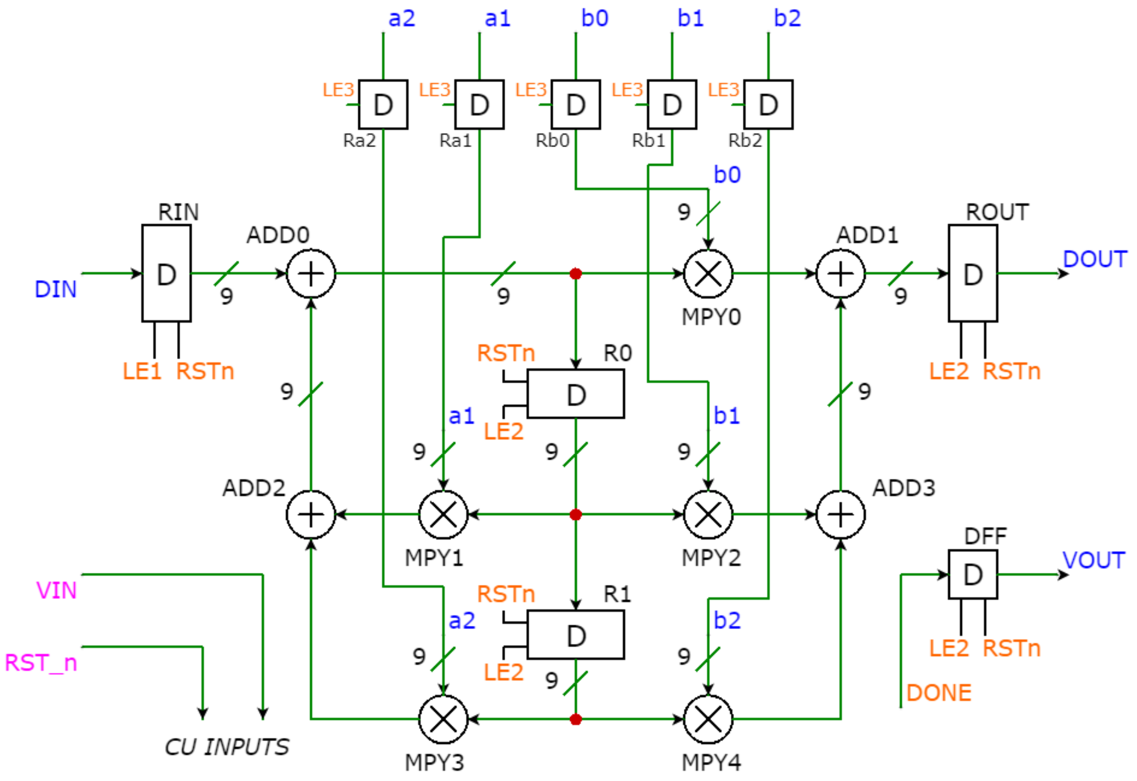


Figure 1.4: IIR filter standard architecture; pink signals are CU inputs, orange signals are CU outputs.

1.2.2 Simulation

To process all the samples the simulation lasts 39000 ns. A snapshot from 0 ns to 2139 ns is shown in Figure 1.6 to highlight the behaviour of the filter when `VIN` moves from 0 to 1 and viceversa.

1.2.3 Logic synthesis

Logic synthesis has been performed through Synopsys Design Compiler. The steps followed to obtain a deterministic maximum clock frequency which not depends from the previous synthesis are:

1. force the clock period to 0 when applying the constraints and run the simulation;

2. start a new synthesis (cleaning the work) adding to the clock period the slack obtained in the previous step;

3. repeat the step 2 until the Slack is `MET` and equal to 0.

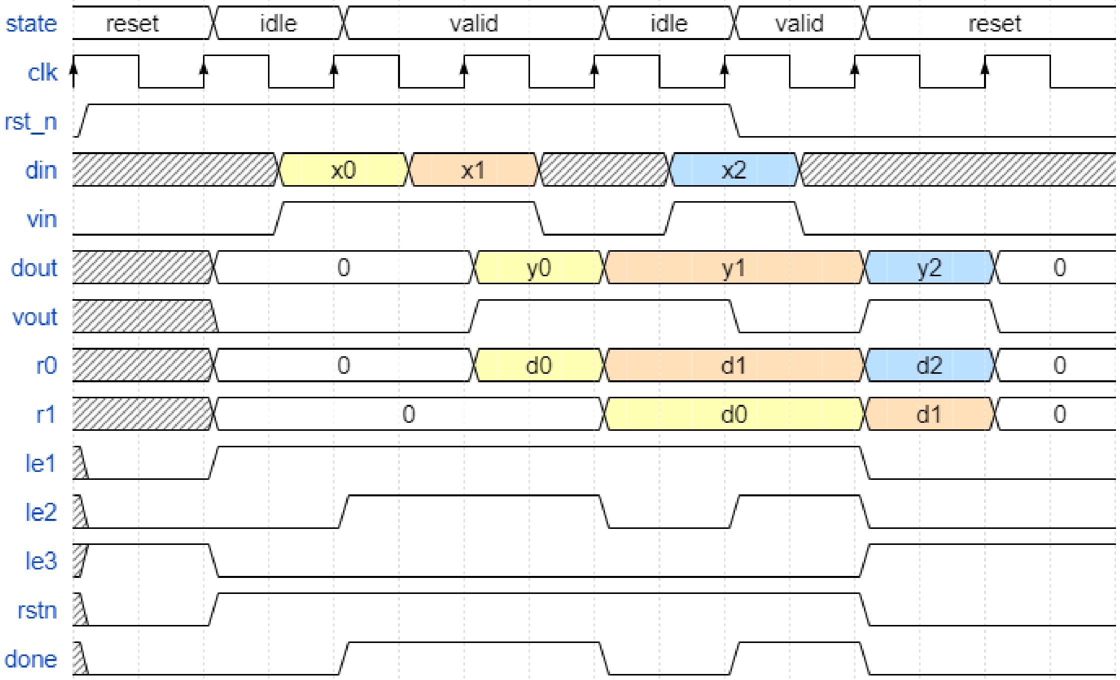


Figure 1.5: IIR filter timing; the last five signals are command signals. `r0` and `r1` represents respectively the output signals of register `R0` and `R1`.

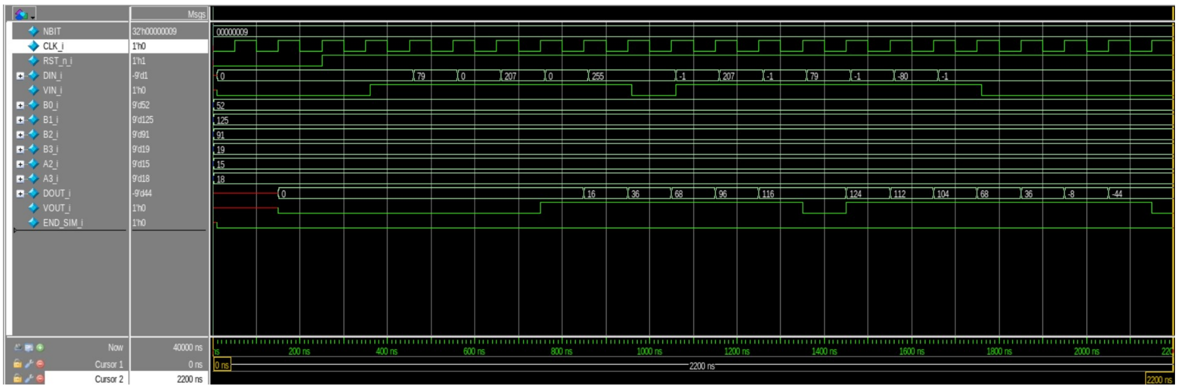
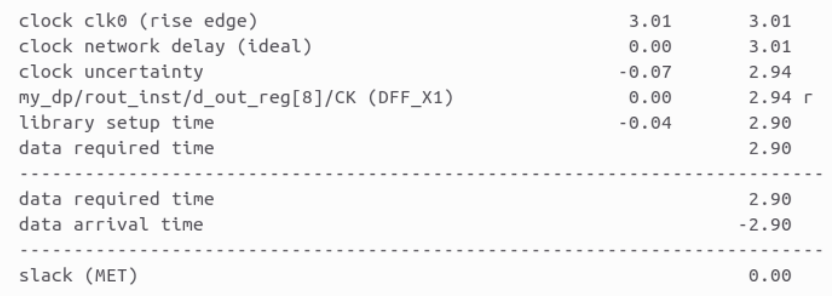
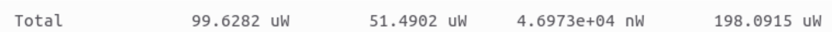


Figure 1.6: IIR filter simulation results.



```
clock clk0 (rise edge)                          3.01       3.01
clock network delay (ideal)                     0.00       3.01
clock uncertainty                              -0.07       2.94
my_dp/rout_inst/d_out_reg[8]/CK (DFF_X1)        0.00       2.94 r
library setup time                             -0.04       2.90
data required time                                         2.90
---------------------------------------------------------------------------
data required time                                         2.90
data arrival time                                         -2.90
---------------------------------------------------------------------------
slack (MET)                                                0.00
```

Figure 1.7: Timing report showing slack `MET` and equal to 0.



```
Total              99.6282 uW         51.4902 uW      4.6973e+04 nW       198.0915 uW
```

Figure 1.8: Power report of the filter after the logic synthesis.

The minimum clock period found is $T_{CLK_{MIN}} = 3.01ns$. Snapshots showing slack `MET` and equal to 0 ($T_{CLK_{MIN}}$) and power consumption for $f = f_M/4$ are shown in Figure 1.7 and 1.8.
Results of the synthesis are shown in Table 1.2.

$f_M = 332MHz$	$A = 2600\mu m^2$	-	$T = 1174ns$
$f_M/4 = 83MHz$	$A = 2335\mu m^2$	$P = 198\mu W$	$T = 4680ns$

Table 1.2: Summary for filter design after logic synthesis: A is the area, P is the power consumption and T is the simulation time.

1.2.4 Place and route

Place and route of the filter designed at $f_{CLK} = 83MHz$ has been performed through Cadence Innovus. The final result is shown in figure 1.9.

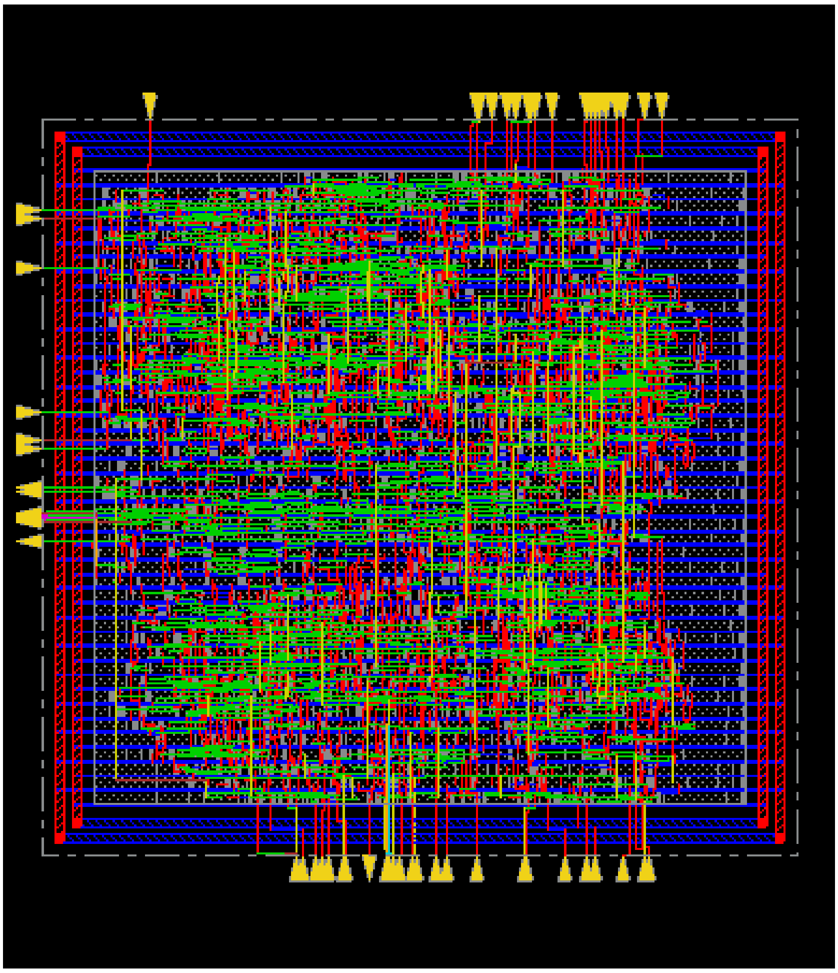


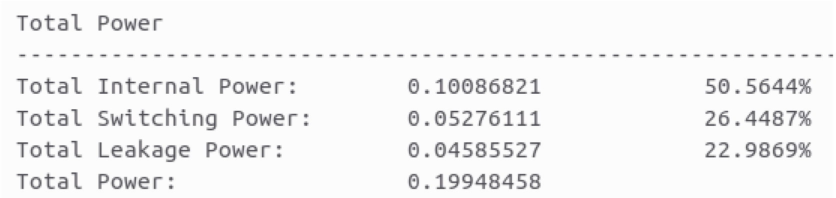
Figure 1.9: Place and route layout of the filter.

Results of the place and route are shown in Table 1.3.

$f_M/4 = 83MHz$	$A = 2291\mu m^2$	$P = 199\mu W$	$T = 4680ns$

Table 1.3: Summary for filter design after place and route: A is the area, P is the power consumption and T is the simulation time.

Reports showing no timing violation (timeDesign Summary table for both setup and hold modes) are listed in Appendix A.1 and A.2. Snapshot showing power consumption is shown in Figure 1.10.



```
Total Power
-----------------------------------------------------------
Total Internal Power:        0.10086821           50.5644%
Total Switching Power:       0.05276111           26.4487%
Total Leakage Power:         0.04585527           22.9869%
Total Power:                 0.19948458
```

Figure 1.10: Power report after place and route.

1.2.5 Explanations, comparisons and comments

Control Unit Reusability

By comparing the timing diagram of our filters it can be observed that, if we focus on a specific state, the configuration of the command signals is exactly the same in both the implementations: in fact, our Control Unit was designed so that it can be reused with both the standard and the look-ahead solutions: in other words, the standard filter and the look-ahead one, were designed with the same CU. This implies that in the timing diagram for the two filters, the command signals behave exactly in the same way.

1.3 Advanced architecture development

1.3.1 Derivation of the look-ahead transfer function

In order to derive the new coefficients for the look-ahead filter, it is necessary to derive its transfer function. In the case of our standard filter, the transfer function is:

$$H(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 + a_1 \cdot z^{-1} + a_2 \cdot z^{-2}}$$

Moreover, it can be shown that in order to derive the corrispondent look-ahead solution, a "correction factor" should be considered as well:

$$H'(z) = \frac{1 + a_1 \cdot z^{-1}}{1 + a_1 \cdot z^{-1}}$$

Hence, the look-ahead transfer function, can be derived as:

$$H_{LA}(z) = H(z) \cdot H'(z) = \frac{b_0 + (b_1 - a_1 b_0)z^{-1} + (b_2 - a_1 b_1)z^{-2} - a_1 b_2 z^{-3}}{1 + (a_2 - a_1^2)z^{-2} - a_1 a_2 z^{-3}}$$

where the coefficients are related to the standard tranfer function.

In conclusion, from the previous expression, it is straightforward to derive the new coefficients; their integer representation is reported in table 1.4.

a_0	256
a_1	0
a_2	15
a_3	18
b_0	52
b_1	125
b_2	91
b_3	19

Table 1.4: Quantized coefficients for the look-ahead filter.

1.3.2 C model and THD

As in the standard design, a C model has been developed considering a reduction of precision for the multiplications.

The parameter responsible is still *SHAMT* that represents the number of bits to be discarded after each multiplication. The output results obtained from the C model have been analyzed in order to achieve a maximum THD of -30 dB. In this case, comparing figures 1.11 and 1.12 is possible to deduce that the *SHAMT* that allows to meet the specifications is 10. The number of bits after each multiplication is 8. With this configuration the THD achieved is -37.57 dB.

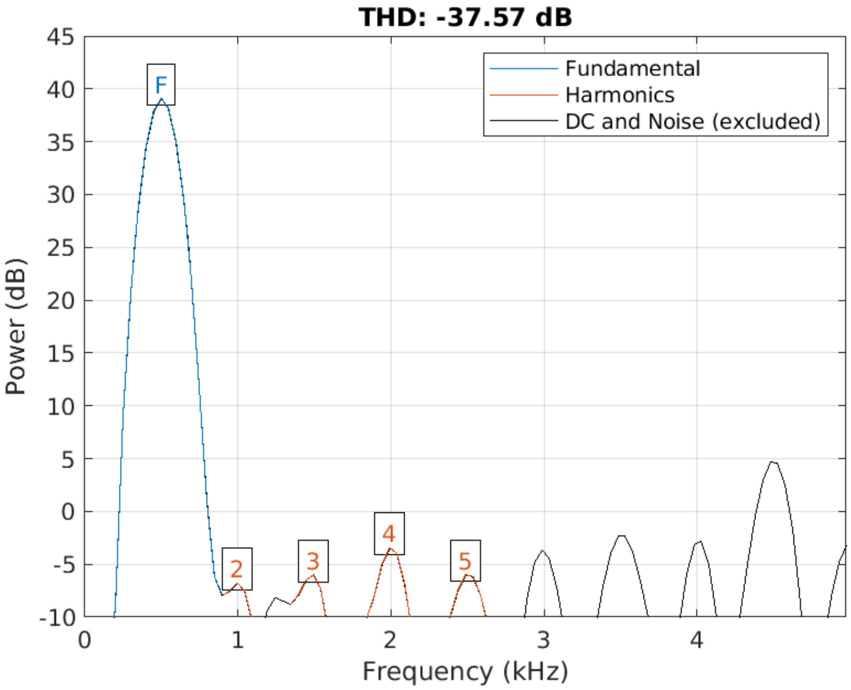


Figure 1.11: THD analysis for $SHAMT = 10$.

1.3.3 Architecture

The architecture of the look-ahead filter is shown in Figure 1.13 and the timing diagram in Figure 1.14.

As in the previous case, the filter is based on the Direct Form II model, in particular:

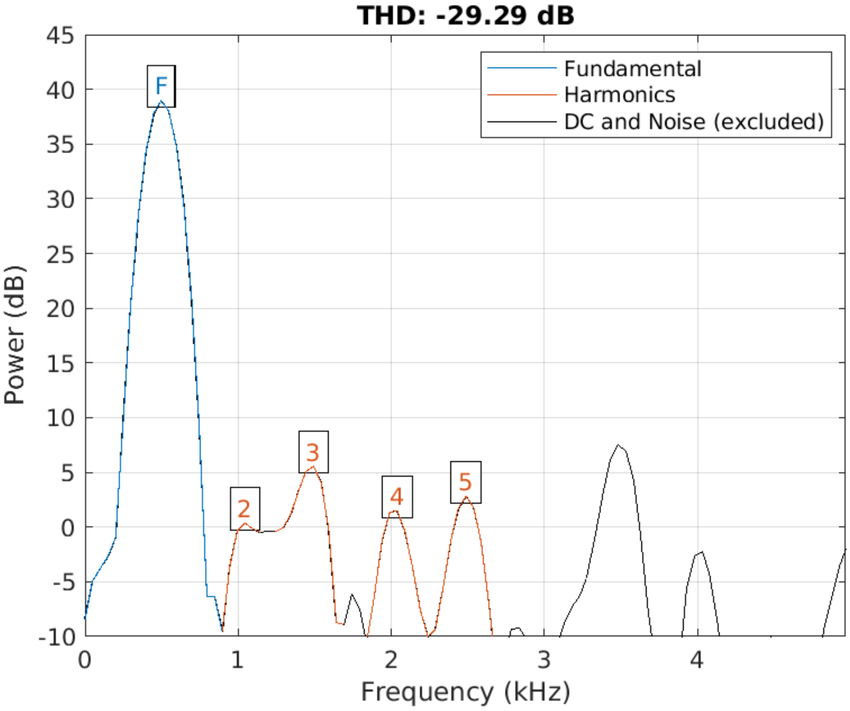


Figure 1.12: THD analysis for $SHAMT = 11$.

- registers `r6, r7, r8, r9, r10` were obtained by applying retiming on two initial registers.
- registers `r0, r4, r5` represents the first layer of pipe introduced inside the filter.
- registers `r1, r3` represents the second layer of pipe introduced inside the filter.
- register `r2` remains unchanged.

Important note: as pointed out later in the report, in order to allow a valid sample to correctly flow through the pipeline chain, it is necessary to delay the enable signal `LE2` of the pipe stages: this is accomplished by synchronization registers (not shown inside the netlist figure) and it is the reason why, in figure 1.14, the first time `LE2` is being sampled as “1”, only `r0` (first pipe layer) updates its output, while `r1` (second pipe layer) will change during the next cycle.

1.3.4 Simulation

To process all the samples the simulation lasts 39000 ns. A snapshot from 0 ns to 2200 ns is shown in Figure 1.15 to highlight the behaviour of the filter when `VIN` moves from 0 to 1 and viceversa.

1.3.5 Logic synthesis

Logic synthesis has been performed through Synopsys Design Compiler. The steps followed to obtain a deterministic maximum clock frequency which not depends from the previous synthesis are the those highlighted in the paragraph 1.2.3. The minimum clock period found is $T_{CLK_{MIN}} = 1.56ns$. In order to correctly simulate such clock period with proper precision, time resolution has been increased to $1ps$. Snapshots showing slack `MET` and equal to 0 ($T_{CLK_{MIN}}$) and power consumption for $f = f_M/4$ are shown in Figure 1.16 and 1.17.

Results of the synthesis are shown in Table 1.5.

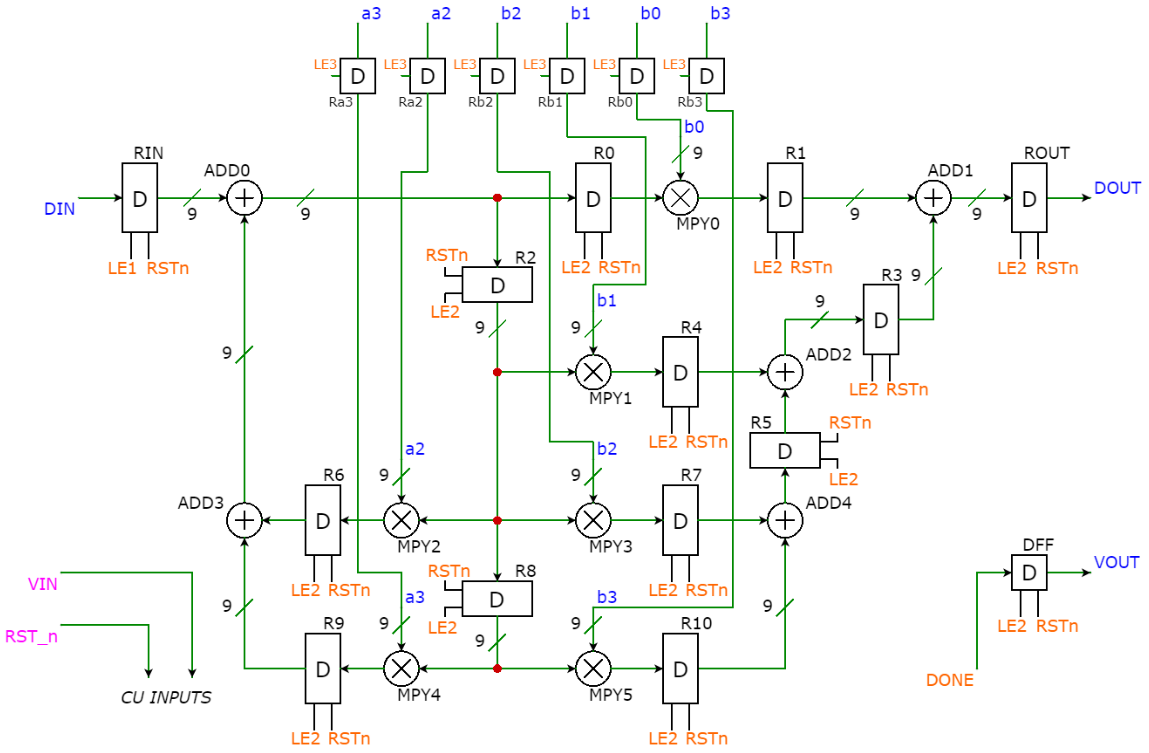


Figure 1.13: IIR look-ahead filter architecture; pink signals are CU inputs, orange signals are CU outputs.

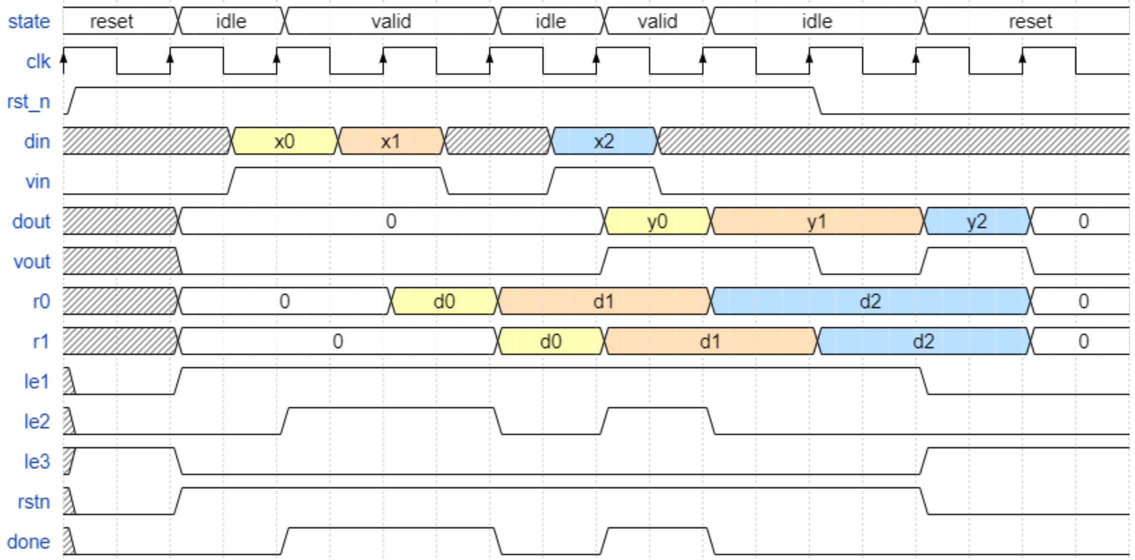


Figure 1.14: IIR look-ahead filter timing

1.3.6 Place and route

Place and route of the filter designed at $f_{CLK} = 160MHz$ has been performed through Cadence Innovus. The final result is shown in figure 1.18.

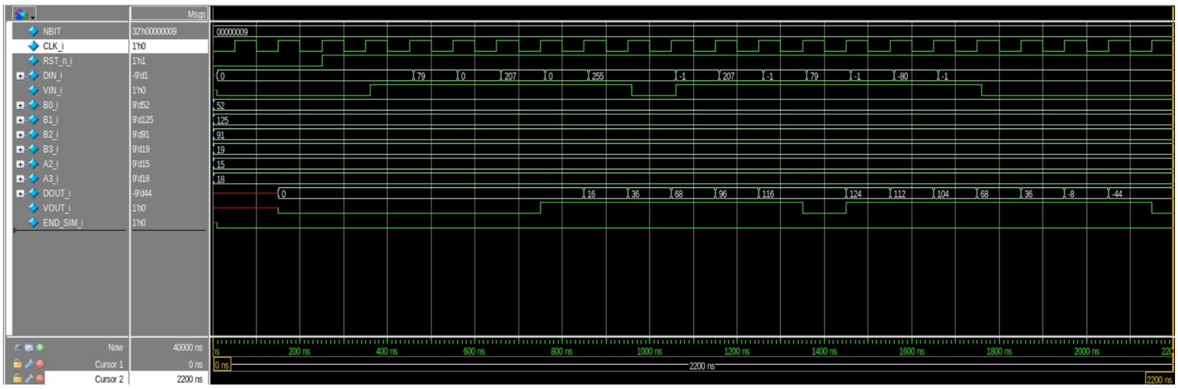
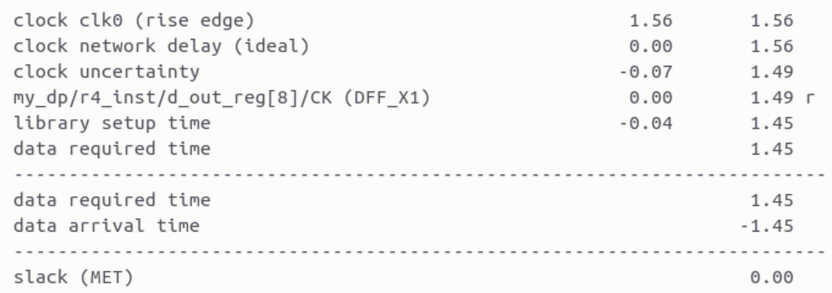
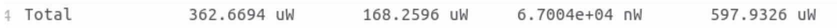


Figure 1.15: IIR look-ahead filter simulation results.



```
clock clk0 (rise edge)                                 1.56       1.56
clock network delay (ideal)                            0.00       1.56
clock uncertainty                                     -0.07       1.49
my_dp/r4_inst/d_out_reg[8]/CK (DFF_X1)                 0.00       1.49 r
library setup time                                    -0.04       1.45
data required time                                                1.45
--------------------------------------------------------------------------
data required time                                                1.45
data arrival time                                                -1.45
--------------------------------------------------------------------------
slack (MET)                                                       0.00
```

Figure 1.16: Timing report of the look-ahead design showing slack MET and equal to 0.



```
Total            362.6694 uW       168.2596 uW      6.7004e+04 nW       597.9326 uW
```

Figure 1.17: Power report of the look ahead implementation of the filter after the logic synthesis.

$f_M = 640MHz$	$A = 3752\mu m^2$	-	$T = 608ns$
$f_M/4 = 160MHz$	$A = 3337\mu m^2$	$P = 598\mu W$	$T = 2427ns$

Table 1.5: Summary for look-ahead design after logic synthesis: A is the area, P is the power consumption and T is the simulation time.

Results of the place and route are shown in Table 1.6.

$f_M/4 = 160MHz$	$A = 3288\mu m^2$	$P = 606.5\mu W$	$T = 2433ns$

Table 1.6: Summary for look-ahead design after place and route: A is the area, P is the power consumption and T is the simulation time.

Reports showing no timing violation (timeDesign Summary table for both setup and hold modes) are listed in Appendix A.3 and A.4. Snapshot showing power consumption are shown in Figure 1.19.

1.3.7 Explanations, comparisons and comments

Use of synchronization registers

In order to correctly design the pipelined filter, it is necessary to insert some "intermediate" registers between Control Unit and Data-Path, these registers are used to delay the LE2 signal toward pipeline

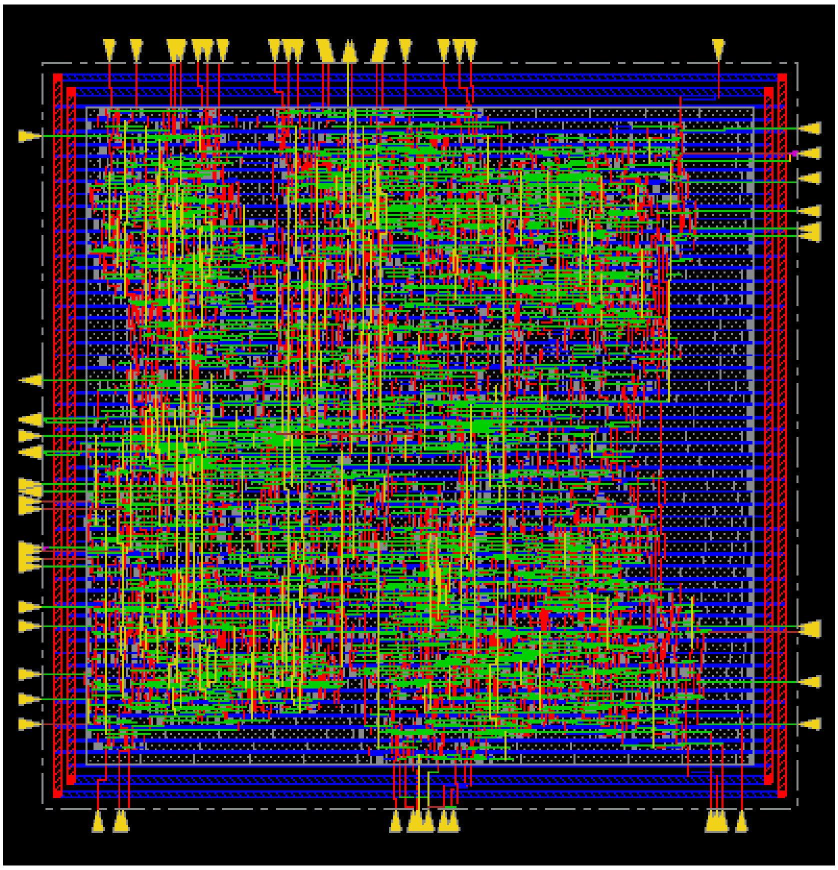
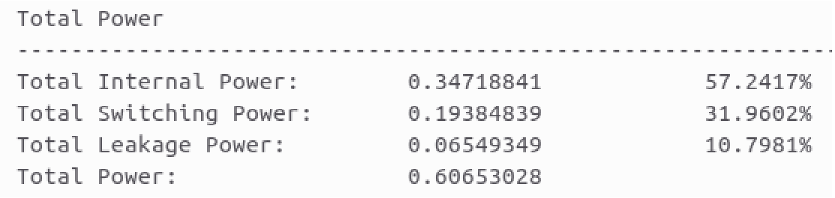


Figure 1.18: Place and route layout of look-ahead implementation of the filter.



```
Total Power
-----------------------------------------------------------
Total Internal Power:        0.34718841            57.2417%
Total Switching Power:       0.19384839            31.9602%
Total Leakage Power:         0.06549349            10.7981%
Total Power:                 0.60653028
```

Figure 1.19: Power report for look-ahead design after place and route.

and `ROUT` registers.
If we assume that during clock cycle `X` a valid data `d0` was sampled by `RIN`, then:

- the first pipe layer composed by `r0, r4, r5` must be enabled during the current clock cycle `X`, so there is no need to delay `LE2`.
- the second pipe layer composed by `r1, r3` must be enabled during the following clock cycle `X+1`, so we insert one intermediate register (say `RA`).
- the output register `ROUT` must be enabled during the clock cycle `X+2`, so we insert two intermediate registers (say `RB, RC`).

Note that, since `LE2` is already being delayed of one clock cycle by `RA`, there is actually no need to use other two registers `RB, RC`: it is enough to just use `RB`, in series to `RA`.

APPENDIX A

Timing Reports

A.1 Summary table for setup mode

```
# Format: clock  timeReq  slackR/slackF  setupR/setupF  instName/pinName  # cycle(s)
clk0(R)->clk0(R) 11.937   */8.844        */0.038         my_dp_rout_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.937   */8.917        */0.038         my_dp_rout_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.937   */8.990        */0.038         my_dp_rout_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.937   */9.063        */0.038         my_dp_rout_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.937   */9.135        */0.038         my_dp_rout_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.937   */9.207        */0.038         my_dp_rout_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.943   9.987/*        0.031/*         my_dp_r0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.942   10.056/*       0.031/*         my_dp_r0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.943   10.128/*       0.031/*         my_dp_r0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.942   10.201/*       0.031/*         my_dp_r0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.942   10.271/*       0.031/*         my_dp_r0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.935   */10.381       */0.038         my_dp_r0_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.470   11.371/*       0.500/*        DOUT[7]    1
clk0(R)->clk0(R) 11.470   11.371/*       0.500/*        DOUT[6]    1
clk0(R)->clk0(R) 11.470   11.371/*       0.500/*        DOUT[8]    1
clk0(R)->clk0(R) 11.470   11.371/*       0.500/*        DOUT[4]    1
clk0(R)->clk0(R) 11.470   11.373/*       0.500/*        DOUT[5]    1
clk0(R)->clk0(R) 11.470   11.373/*       0.500/*        DOUT[1]    1
clk0(R)->clk0(R) 11.470   11.373/*       0.500/*        DOUT[3]    1
clk0(R)->clk0(R) 11.470   11.374/*       0.500/*        DOUT[0]    1
clk0(R)->clk0(R) 11.470   11.374/*       0.500/*        DOUT[2]    1
clk0(R)->clk0(R) 11.470   11.377/*       0.500/*        VOUT    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rin_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rin_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rin_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rin_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rin_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.935   */11.396       */0.038         my_dp_rb0_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rb1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.038         my_dp_rb0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.038         my_dp_rb1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rb1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rb1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.038         my_dp_rin_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.038         my_dp_rb0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.038         my_dp_rb0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.934   */11.396       */0.039         my_dp_rb1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rin_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rb0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rin_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.039         my_dp_rb1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rb1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rb1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rb0_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.935   */11.397       */0.038         my_dp_rin_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rb1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.934   */11.397       */0.038         my_dp_rb0_inst_d_out_reg_0_/D    1
```

```
clk0(R)->clk0(R) 11.935   */11.397     */0.038      my_dp_rb0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.936   */11.398     */0.038      my_dp_rb0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.938   */11.400     */0.038      my_dp_rb2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.938   */11.400     */0.038      my_dp_rb2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.937   */11.400     */0.038      my_dp_rb2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.938   */11.400     */0.038      my_dp_rb2_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.938   */11.400     */0.038      my_dp_rb2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.938   */11.401     */0.038      my_dp_rb2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.938   */11.401     */0.038      my_dp_rb2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.938   */11.401     */0.038      my_dp_rb2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.938   */11.401     */0.038      my_dp_rb2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.940   */11.401     */0.037      my_dp_ra1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.940   */11.401     */0.038      my_dp_ra2_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.038      my_dp_ra2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.038      my_dp_ra1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.038      my_dp_ra2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.941   11.402/*     0.031/*      my_cu_state_reg_0_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.037      my_dp_ra1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.940   */11.402     */0.038      my_dp_ra2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.940   */11.402     */0.038      my_dp_ra2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.038      my_dp_ra2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.037      my_dp_ra1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.940   */11.402     */0.037      my_dp_ra1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.939   */11.402     */0.037      my_dp_ra1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.940   */11.402     */0.037      my_dp_ra1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.940   */11.403     */0.037      my_dp_ra2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.940   */11.403     */0.037      my_dp_ra2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.940   */11.403     */0.037      my_dp_ra1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.940   */11.403     */0.037      my_dp_ra1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.940   */11.403     */0.037      my_dp_ra2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.933   */11.418     */0.040      my_cu_state_reg_1_/D    1
clk0(R)->clk0(R) 11.942   11.538/*     0.031/*      my_dp_r0_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.944   11.538/*     0.031/*      my_dp_r1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 11.942   11.538/*     0.031/*      my_dp_r0_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.941   11.539/*     0.031/*      my_dp_r0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.944   11.539/*     0.031/*      my_dp_r1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 11.945   11.539/*     0.031/*      my_dp_r1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 11.944   11.539/*     0.031/*      my_dp_r1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 11.944   11.539/*     0.031/*      my_dp_r1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 11.945   11.539/*     0.031/*      my_dp_r1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.944   11.539/*     0.031/*      my_dp_r1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 11.945   11.540/*     0.031/*      my_dp_r1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.945   11.541/*     0.031/*      my_dp_r1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.937   */11.626     */0.038      my_dp_rout_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 11.937   */11.626     */0.038      my_dp_rout_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 11.938   */11.651     */0.037      my_dp_rout_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 11.929   */11.678     */0.043      my_dp_dff_inst_d_out_reg/D    1
```

A.2 Summary table for hold mode

```
# Format: clock   timeReq   slackR/slackF   holdR/holdF   instName/pinName   # cycle(s)
clk0(R)->clk0(R) 0.070    */0.015        */-0.002       my_cu_state_reg_1_/D    1
clk0(R)->clk0(R) 0.073    */0.041        */-0.003       my_dp_rout_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.070    */0.042        */-0.002       my_cu_state_reg_0_/D    1
clk0(R)->clk0(R) 0.077    0.047/*        -0.006/*       my_dp_rb2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.074    0.047/*        -0.006/*       my_dp_rb0_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.074    0.048/*        -0.006/*       my_dp_rb1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.079    0.048/*        -0.006/*       my_dp_ra1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.079    0.050/*        -0.007/*       my_dp_ra2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.077    0.054/*        -0.006/*       my_dp_rout_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 0.077    0.054/*        -0.006/*       my_dp_rout_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 0.077    0.055/*        -0.006/*       my_dp_rout_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 0.073    0.055/*        -0.006/*       my_dp_rin_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 0.077    0.055/*        -0.006/*       my_dp_rout_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 0.077    0.055/*        -0.006/*       my_dp_rout_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 0.073    0.055/*        -0.006/*       my_dp_rin_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 0.070    */0.055        */-0.002       my_dp_dff_inst_d_out_reg/D    1
clk0(R)->clk0(R) 0.073    0.055/*        -0.006/*       my_dp_rin_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.074    0.055/*        -0.006/*       my_dp_rin_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 0.073    0.056/*        -0.006/*       my_dp_rin_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 0.077    0.056/*        -0.006/*       my_dp_rout_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 0.074    0.056/*        -0.006/*       my_dp_rin_inst_d_out_reg_7_/D    1
```

```
clk0(R)->clk0(R)  0.075    0.056/*         -0.006/*        my_dp_rin_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.073    0.056/*         -0.006/*        my_dp_rin_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.077    0.056/*         -0.006/*        my_dp_rout_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.079    0.056/*         -0.006/*        my_dp_ra2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.077    0.056/*         -0.006/*        my_dp_rout_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.077    0.057/*         -0.006/*        my_dp_rb2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.074    0.057/*         -0.006/*        my_dp_rb0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.079    0.057/*         -0.007/*        my_dp_ra1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.074    0.057/*         -0.006/*        my_dp_rb1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.077    0.057/*         -0.006/*        my_dp_rb2_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.077    0.057/*         -0.006/*        my_dp_rb2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.073    0.057/*         -0.006/*        my_dp_rb0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.079    0.058/*         -0.006/*        my_dp_ra2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.074    0.059/*         -0.006/*        my_dp_rb1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.074    0.059/*         -0.006/*        my_dp_rb0_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.079    0.059/*         -0.006/*        my_dp_ra2_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.079    0.060/*         -0.007/*        my_dp_ra1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.079    0.060/*         -0.007/*        my_dp_ra1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.074    0.061/*         -0.006/*        my_dp_rb1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.071    */0.067         */-0.003        my_dp_r0_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.070    */0.078         */-0.002        my_dp_rin_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.074    */0.084         */-0.003        my_dp_r1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.075    */0.087         */-0.003        my_dp_r1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.074    */0.088         */-0.003        my_dp_r1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.073    */0.089         */-0.003        my_dp_r1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.074    */0.089         */-0.003        my_dp_r1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.074    */0.089         */-0.003        my_dp_r1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.074    */0.089         */-0.003        my_dp_r1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.074    */0.090         */-0.003        my_dp_r1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.070    */0.091         */-0.002        my_dp_rb1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.074    */0.091         */-0.003        my_dp_r1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.074    */0.091         */-0.003        my_dp_rb2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.070    */0.092         */-0.002        my_dp_rb0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.070    */0.092         */-0.002        my_dp_rb1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.072    */0.092         */-0.003        my_dp_rb0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.073    */0.092         */-0.003        my_dp_rb2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.070    */0.092         */-0.002        my_dp_rb1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.071    */0.092         */-0.002        my_dp_rb0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.075    */0.092         */-0.003        my_dp_ra1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.075    */0.092         */-0.003        my_dp_ra1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.070    */0.093         */-0.002        my_dp_rb0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.075    */0.093         */-0.003        my_dp_ra2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.076    */0.093         */-0.003        my_dp_ra2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.074    */0.093         */-0.003        my_dp_rb2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.076    */0.093         */-0.003        my_dp_ra2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.076    */0.093         */-0.003        my_dp_ra1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.074    */0.093         */-0.003        my_dp_rb2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.071    */0.093         */-0.002        my_dp_r0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.075    */0.094         */-0.003        my_dp_ra1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.070    */0.095         */-0.002        my_dp_rb1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.075    */0.095         */-0.003        my_dp_ra2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.076    */0.095         */-0.003        my_dp_ra1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.070    */0.095         */-0.002        my_dp_rb1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.074    */0.096         */-0.003        my_dp_rb2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.076    */0.096         */-0.003        my_dp_ra2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.072    */0.098         */-0.003        my_dp_r0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.072    */0.098         */-0.003        my_dp_r0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.071    */0.098         */-0.003        my_dp_rb0_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.072    */0.098         */-0.003        my_dp_r0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.071    */0.099         */-0.003        my_dp_r0_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.071    */0.099         */-0.003        my_dp_r0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.072    */0.100         */-0.003        my_dp_r0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.071    */0.101         */-0.003        my_dp_r0_inst_d_out_reg_2_/D    1
```

A.3 Summary table for setup mode - Look Ahead implementation

```
# Format: clock   timeReq  slackR/slackF  setupR/setupF  instName/pinName    # cycle(s)
clk0(R)->clk0(R)  6.232    4.530/*         0.028/*        my_dp_r7_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.232    4.539/*         0.028/*        my_dp_r6_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.230    4.541/*         0.028/*        my_dp_r4_inst_d_out_reg_8_/D    1
```

```
clk0(R)->clk0(R)  6.231    4.548/*         0.028/*         my_dp_r10_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.231    4.553/*         0.028/*         my_dp_r1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.230    4.558/*         0.028/*         my_dp_r9_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.232    4.600/*         0.028/*         my_dp_r7_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.232    4.612/*         0.028/*         my_dp_r6_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.230    4.612/*         0.028/*         my_dp_r4_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.231    4.619/*         0.028/*         my_dp_r10_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.231    4.626/*         0.028/*         my_dp_r1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.233    4.634/*         0.028/*         my_dp_r9_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.232    4.673/*         0.028/*         my_dp_r7_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.232    4.682/*         0.028/*         my_dp_r6_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.230    4.686/*         0.028/*         my_dp_r4_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.231    4.692/*         0.028/*         my_dp_r10_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.232    4.696/*         0.028/*         my_dp_r1_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.233    4.707/*         0.028/*         my_dp_r9_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.232    4.743/*         0.028/*         my_dp_r7_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.232    4.755/*         0.028/*         my_dp_r6_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.230    4.756/*         0.028/*         my_dp_r4_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.231    4.764/*         0.028/*         my_dp_r10_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.232    4.769/*         0.028/*         my_dp_r1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.233    4.779/*         0.028/*         my_dp_r9_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.231    4.815/*         0.028/*         my_dp_r7_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.231    4.826/*         0.028/*         my_dp_r6_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.230    4.828/*         0.028/*         my_dp_r4_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.231    4.837/*         0.028/*         my_dp_r10_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.232    4.841/*         0.028/*         my_dp_r1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.233    4.849/*         0.028/*         my_dp_r9_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.231    4.885/*         0.028/*         my_dp_r7_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.230    4.897/*         0.028/*         my_dp_r6_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.230    4.901/*         0.028/*         my_dp_r4_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.234    4.911/*         0.028/*         my_dp_r10_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.232    4.912/*         0.028/*         my_dp_r1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.233    4.921/*         0.028/*         my_dp_r9_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.231    4.957/*         0.028/*         my_dp_r7_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  6.230    4.969/*         0.028/*         my_dp_r4_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  6.230    4.969/*         0.028/*         my_dp_r6_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  6.231    4.979/*         0.028/*         my_dp_r10_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  6.232    4.984/*         0.028/*         my_dp_r1_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  6.233    4.992/*         0.028/*         my_dp_r9_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  6.232    5.265/*         0.028/*         my_dp_r0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.232    5.265/*         0.028/*         my_dp_r2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.231    5.336/*         0.028/*         my_dp_r0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.231    5.336/*         0.028/*         my_dp_r2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.232    5.406/*         0.028/*         my_dp_r2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.231    5.407/*         0.028/*         my_dp_r0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.231    5.454/*         0.028/*         my_dp_rout_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.230    5.454/*         0.028/*         my_dp_r3_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.231    5.459/*         0.028/*         my_dp_r5_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  6.231    5.477/*         0.028/*         my_dp_r2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.232    5.479/*         0.028/*         my_dp_r0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.231    5.526/*         0.028/*         my_dp_rout_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.230    5.527/*         0.028/*         my_dp_r3_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.231    5.530/*         0.028/*         my_dp_r5_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  6.232    5.551/*         0.028/*         my_dp_r0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  6.232    5.551/*         0.028/*         my_dp_r2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  5.670    5.556/*         0.500/*         DOUT[2]     1
clk0(R)->clk0(R)  5.670    5.559/*         0.500/*         DOUT[5]     1
clk0(R)->clk0(R)  5.670    5.559/*         0.500/*         DOUT[1]     1
clk0(R)->clk0(R)  5.670    5.559/*         0.500/*         DOUT[4]     1
clk0(R)->clk0(R)  5.670    5.560/*         0.500/*         DOUT[3]     1
clk0(R)->clk0(R)  5.670    5.560/*         0.500/*         VOUT    1
clk0(R)->clk0(R)  5.670    5.560/*         0.500/*         DOUT[7]     1
clk0(R)->clk0(R)  5.670    5.561/*         0.500/*         DOUT[0]     1
clk0(R)->clk0(R)  5.670    5.561/*         0.500/*         DOUT[6]     1
clk0(R)->clk0(R)  5.670    5.561/*         0.500/*         DOUT[8]     1
clk0(R)->clk0(R)  6.231    5.599/*         0.028/*         my_dp_rout_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.232    5.600/*         0.028/*         my_dp_r3_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.230    5.601/*         0.028/*         my_dp_r5_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  6.232    5.623/*         0.028/*         my_dp_r0_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.232    5.624/*         0.028/*         my_dp_r2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  6.232    5.672/*         0.028/*         my_dp_rout_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.230    5.672/*         0.028/*         my_dp_r3_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.231    5.674/*         0.028/*         my_dp_r5_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  6.226    5.687/*         0.028/*         my_dp_rin_inst_d_out_reg_3_/D    1
```

```
clk0(R)->clk0(R) 6.227   5.688/*    0.028/*    my_cu_state_reg_0_/D   1
clk0(R)->clk0(R) 6.227   5.689/*    0.028/*    my_dp_rin_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.227   5.690/*    0.028/*    my_dp_rin_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.227   5.690/*    0.028/*    my_dp_rin_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.228   5.690/*    0.028/*    my_dp_rin_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.228   5.692/*    0.028/*    my_dp_rin_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.232   5.694/*    0.028/*    my_dp_rin_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.232   5.694/*    0.028/*    my_dp_r2_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.231   */5.694    */0.024    my_dp_ra2_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.232   5.695/*    0.028/*    my_dp_rin_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.232   5.695/*    0.028/*    my_dp_r0_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.232   5.695/*    0.028/*    my_dp_rin_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.234   */5.697    */0.024    my_dp_rb1_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.234   */5.697    */0.024    my_dp_rb1_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.234   */5.697    */0.024    my_dp_rb1_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.234   */5.697    */0.024    my_dp_rb1_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.234   */5.697    */0.024    my_dp_rb1_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.234   */5.697    */0.024    my_dp_rb1_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.236   */5.698    */0.024    my_dp_rb2_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.236   */5.698    */0.024    my_dp_rb2_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.236   */5.698    */0.024    my_dp_rb2_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.236   */5.698    */0.024    my_dp_rb2_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.236   */5.699    */0.024    my_dp_rb2_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.236   */5.699    */0.024    my_dp_rb2_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.236   */5.699    */0.024    my_dp_rb2_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.234   */5.699    */0.024    my_dp_rout_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.236   */5.699    */0.024    my_dp_rb2_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.237   */5.699    */0.024    my_dp_rb1_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.237   */5.699    */0.024    my_dp_rb1_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.234   */5.699    */0.024    my_dp_rout_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.236   */5.699    */0.024    my_dp_rb2_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.238   */5.699    */0.024    my_dp_ra3_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.237   */5.699    */0.024    my_dp_rb0_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.237   */5.699    */0.024    my_dp_rb0_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.238   */5.700    */0.024    my_dp_ra3_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb1_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.238   */5.700    */0.024    my_dp_ra3_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.237   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.238   */5.700    */0.024    my_dp_rb0_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.238   */5.701    */0.024    my_dp_ra3_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.236   */5.701    */0.024    my_dp_rout_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.236   */5.701    */0.024    my_dp_rout_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.236   */5.701    */0.024    my_dp_rout_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.238   */5.701    */0.024    my_dp_ra3_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.239   */5.701    */0.024    my_dp_ra3_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.240   */5.701    */0.024    my_dp_rb3_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.239   */5.701    */0.024    my_dp_ra3_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.239   */5.701    */0.024    my_dp_ra3_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.239   */5.701    */0.024    my_dp_ra3_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.240   */5.702    */0.024    my_dp_rb3_inst_d_out_reg_7_/D   1
clk0(R)->clk0(R) 6.240   */5.702    */0.024    my_dp_rb3_inst_d_out_reg_0_/D   1
clk0(R)->clk0(R) 6.240   */5.702    */0.024    my_dp_rb3_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.240   */5.702    */0.024    my_dp_rb3_inst_d_out_reg_1_/D   1
clk0(R)->clk0(R) 6.240   */5.702    */0.024    my_dp_rb3_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.240   */5.703    */0.024    my_dp_rb3_inst_d_out_reg_8_/D   1
clk0(R)->clk0(R) 6.240   */5.703    */0.024    my_dp_rb3_inst_d_out_reg_6_/D   1
clk0(R)->clk0(R) 6.240   */5.703    */0.024    my_dp_rb3_inst_d_out_reg_5_/D   1
clk0(R)->clk0(R) 6.234   */5.708    */0.024    my_dp_r5_inst_d_out_reg_3_/D   1
clk0(R)->clk0(R) 6.234   */5.709    */0.024    my_dp_r5_inst_d_out_reg_2_/D   1
clk0(R)->clk0(R) 6.234   */5.709    */0.024    my_dp_r5_inst_d_out_reg_4_/D   1
clk0(R)->clk0(R) 6.234   */5.709    */0.024    my_dp_r5_inst_d_out_reg_0_/D   1
```

```
clk0(R)->clk0(R) 6.234    */5.709        */0.024        my_dp_r5_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.226    5.710/*        0.029/*        my_cu_state_reg_1_/D    1
clk0(R)->clk0(R) 6.233    */5.715        */0.024        my_dp_r3_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.233    */5.715        */0.024        my_dp_r3_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.234    */5.716        */0.024        my_dp_r3_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 6.234    */5.716        */0.024        my_dp_r3_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.237    */5.717        */0.024        my_dp_r8_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.236    */5.717        */0.024        my_dp_r3_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R) 6.238    */5.717        */0.024        my_dp_r8_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R) 6.238    */5.718        */0.024        my_dp_r8_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 6.236    */5.723        */0.024        my_dp_r2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.236    */5.725        */0.024        my_dp_r2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.236    */5.725        */0.024        my_dp_r0_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.236    */5.726        */0.024        my_dp_r0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.230    5.774/*        0.028/*        my_dp_r7_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.230    5.776/*        0.028/*        my_dp_r4_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.230    5.776/*        0.028/*        my_dp_r10_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.230    5.778/*        0.028/*        my_dp_r1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.230    5.781/*        0.028/*        my_dp_r9_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.231    5.782/*        0.028/*        my_dp_r6_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.231    5.785/*        0.027/*        my_dp_r7_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.231    5.786/*        0.027/*        my_dp_r10_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.230    5.787/*        0.027/*        my_dp_r4_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.232    5.790/*        0.028/*        my_dp_r1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.231    5.791/*        0.028/*        my_dp_r9_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 6.231    5.792/*        0.028/*        my_dp_r6_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 6.227    5.839/*        0.031/*        my_dp_dff0_inst_d_out_reg/D    1
clk0(R)->clk0(R) 6.227    5.839/*        0.031/*        my_dp_dff3_inst_d_out_reg/D    1
clk0(R)->clk0(R) 6.227    5.839/*        0.031/*        my_dp_dff2_inst_d_out_reg/D    1
clk0(R)->clk0(R) 6.228    5.841/*        0.031/*        my_dp_dff1_inst_d_out_reg/D    1
clk0(R)->clk0(R) 6.229    5.842/*        0.031/*        my_dp_dff4_inst_d_out_reg/D    1
```

A.4 Summary table for hold mode - Look Ahead implementation

```
# Format: clock    timeReq  slackR/slackF  holdR/holdF  instName/pinName   # cycle(s)
clk0(R)->clk0(R) 0.073    */0.104        */-0.011       my_cu_state_reg_1_/D    1
clk0(R)->clk0(R) 0.075    */0.135        */-0.011       my_dp_r4_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.076    */0.135        */-0.011       my_dp_r10_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.077    */0.135        */-0.011       my_dp_r1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.076    */0.135        */-0.011       my_dp_r9_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.076    */0.135        */-0.011       my_dp_r7_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.076    */0.136        */-0.011       my_dp_r6_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.073    */0.136        */-0.011       my_cu_state_reg_0_/D    1
clk0(R)->clk0(R) 0.085    0.138/*        -0.018/*       my_dp_rb1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.086    0.139/*        -0.018/*       my_dp_rb0_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.080    0.139/*        -0.018/*       my_dp_ra2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.085    0.139/*        -0.018/*       my_dp_rb2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.087    0.139/*        -0.018/*       my_dp_ra3_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.088    0.140/*        -0.018/*       my_dp_rb3_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.076    */0.140        */-0.011       my_dp_r6_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.076    */0.141        */-0.011       my_dp_r1_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.076    */0.141        */-0.011       my_dp_r10_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.076    */0.141        */-0.011       my_dp_r7_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.075    */0.141        */-0.011       my_dp_r4_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.087    0.142/*        -0.020/*       my_dp_dff4_inst_d_out_reg/D    1
clk0(R)->clk0(R) 0.076    */0.142        */-0.011       my_dp_r9_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R) 0.086    0.143/*        -0.020/*       my_dp_dff3_inst_d_out_reg/D    1
clk0(R)->clk0(R) 0.083    0.144/*        -0.018/*       my_dp_r1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 0.083    0.144/*        -0.018/*       my_dp_r5_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R) 0.083    0.144/*        -0.018/*       my_dp_r10_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 0.084    0.144/*        -0.018/*       my_dp_rin_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R) 0.083    0.144/*        -0.018/*       my_dp_r5_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R) 0.084    0.144/*        -0.018/*       my_dp_r1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R) 0.083    0.144/*        -0.018/*       my_dp_r4_inst_d_out_reg_8_/D    1
```

```
clk0(R)->clk0(R)  0.083   0.144/*    -0.018/*    my_dp_r5_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.082   0.144/*    -0.018/*    my_dp_r3_inst_d_out_reg_1_/D     1
clk0(R)->clk0(R)  0.082   0.144/*    -0.018/*    my_dp_r3_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r3_inst_d_out_reg_0_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r3_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.084   0.145/*    -0.018/*    my_dp_r6_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.085   0.145/*    -0.018/*    my_dp_r1_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r10_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r10_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.084   0.145/*    -0.018/*    my_dp_r7_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r4_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.086   0.145/*    -0.020/*    my_dp_dff1_inst_d_out_reg/D    1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r5_inst_d_out_reg_1_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r10_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r3_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r4_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.079   0.145/*    -0.018/*    my_dp_rin_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r10_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r5_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r4_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r3_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r10_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.084   0.145/*    -0.018/*    my_dp_r3_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r5_inst_d_out_reg_0_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r6_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.084   0.145/*    -0.018/*    my_dp_r6_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.082   0.145/*    -0.018/*    my_dp_r4_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.083   0.145/*    -0.018/*    my_dp_r5_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.081   0.145/*    -0.018/*    my_dp_rin_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.084   0.145/*    -0.018/*    my_dp_r1_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.085   0.145/*    -0.018/*    my_dp_r1_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.085   0.145/*    -0.018/*    my_dp_r1_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_r3_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_r7_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.082   0.146/*    -0.018/*    my_dp_r3_inst_d_out_reg_8_/D     1
clk0(R)->clk0(R)  0.085   0.146/*    -0.018/*    my_dp_r6_inst_d_out_reg_8_/D     1
clk0(R)->clk0(R)  0.085   0.146/*    -0.018/*    my_dp_r9_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.081   0.146/*    -0.018/*    my_dp_rin_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_r7_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.082   0.146/*    -0.018/*    my_dp_r4_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.083   0.146/*    -0.018/*    my_dp_r5_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.085   0.146/*    -0.018/*    my_dp_r9_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_rin_inst_d_out_reg_1_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_r7_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_r7_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.085   0.146/*    -0.018/*    my_dp_r1_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.086   0.146/*    -0.018/*    my_dp_r10_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_r6_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.082   0.146/*    -0.018/*    my_dp_r6_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.084   0.146/*    -0.018/*    my_dp_rin_inst_d_out_reg_8_/D     1
clk0(R)->clk0(R)  0.082   0.146/*    -0.018/*    my_dp_r4_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.085   0.146/*    -0.018/*    my_dp_r9_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.082   0.146/*    -0.018/*    my_dp_r9_inst_d_out_reg_8_/D     1
clk0(R)->clk0(R)  0.079   0.146/*    -0.018/*    my_dp_rin_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.085   0.147/*    -0.018/*    my_dp_r9_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.084   0.147/*    -0.018/*    my_dp_r7_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.082   0.147/*    -0.018/*    my_dp_r5_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.086   0.147/*    -0.021/*    my_dp_dff2_inst_d_out_reg/D    1
clk0(R)->clk0(R)  0.085   0.147/*    -0.018/*    my_dp_r6_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.085   0.147/*    -0.018/*    my_dp_r9_inst_d_out_reg_5_/D     1
clk0(R)->clk0(R)  0.085   0.147/*    -0.018/*    my_dp_r7_inst_d_out_reg_8_/D     1
clk0(R)->clk0(R)  0.079   0.147/*    -0.018/*    my_dp_rin_inst_d_out_reg_7_/D     1
clk0(R)->clk0(R)  0.085   0.148/*    -0.018/*    my_dp_r9_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.079   0.148/*    -0.018/*    my_dp_rin_inst_d_out_reg_3_/D     1
clk0(R)->clk0(R)  0.086   0.148/*    -0.018/*    my_dp_rb1_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.085   0.148/*    -0.018/*    my_dp_rb2_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.085   0.148/*    -0.018/*    my_dp_rb2_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.088   0.148/*    -0.018/*    my_dp_rb3_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.080   0.149/*    -0.018/*    my_dp_ra2_inst_d_out_reg_2_/D     1
clk0(R)->clk0(R)  0.088   0.149/*    -0.018/*    my_dp_rb3_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.083   0.149/*    -0.018/*    my_dp_rb1_inst_d_out_reg_6_/D     1
clk0(R)->clk0(R)  0.087   0.149/*    -0.018/*    my_dp_ra3_inst_d_out_reg_4_/D     1
clk0(R)->clk0(R)  0.083   0.149/*    -0.018/*    my_dp_rout_inst_d_out_reg_8_/D     1
clk0(R)->clk0(R)  0.084   0.149/*    -0.018/*    my_dp_rout_inst_d_out_reg_6_/D     1
```

```
clk0(R)->clk0(R)  0.087   0.149/*     -0.018/*    my_dp_ra3_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.080   0.149/*     -0.018/*    my_dp_ra2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.085   0.149/*     -0.018/*    my_dp_rout_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.085   0.149/*     -0.018/*    my_dp_rout_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.080   0.149/*     -0.018/*    my_dp_ra2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.086   0.150/*     -0.018/*    my_dp_rb0_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.085   0.150/*     -0.018/*    my_dp_rb2_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.088   0.150/*     -0.018/*    my_dp_rb3_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.084   0.150/*     -0.018/*    my_dp_rout_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.088   0.150/*     -0.018/*    my_dp_ra3_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.083   0.151/*     -0.018/*    my_dp_rb1_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.085   0.151/*     -0.018/*    my_dp_rout_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.083   0.151/*     -0.018/*    my_dp_rout_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.085   0.151/*     -0.018/*    my_dp_rout_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.086   0.151/*     -0.018/*    my_dp_rb0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.083   0.153/*     -0.018/*    my_dp_rout_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.086   0.153/*     -0.018/*    my_dp_rb0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.076   */0.157     */-0.011    my_dp_dff0_inst_d_out_reg/D    1
clk0(R)->clk0(R)  0.079   */0.167     */-0.011    my_dp_r8_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.079   */0.168     */-0.011    my_dp_r8_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.077   */0.168     */-0.011    my_dp_r0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.077   */0.168     */-0.011    my_dp_r0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.077   */0.169     */-0.011    my_dp_r0_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.079   */0.169     */-0.011    my_dp_r8_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.077   */0.169     */-0.011    my_dp_r0_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.077   */0.170     */-0.011    my_dp_r0_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.079   */0.170     */-0.011    my_dp_r8_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.077   */0.170     */-0.011    my_dp_r0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.077   */0.170     */-0.011    my_dp_r0_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.079   */0.170     */-0.011    my_dp_r8_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.077   */0.170     */-0.011    my_dp_r0_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.077   */0.171     */-0.011    my_dp_r0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.077   */0.171     */-0.011    my_dp_r2_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.079   */0.171     */-0.011    my_dp_r8_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.079   */0.172     */-0.011    my_dp_r8_inst_d_out_reg_0_/D    1
clk0(R)->clk0(R)  0.079   */0.173     */-0.011    my_dp_r8_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.077   */0.177     */-0.011    my_dp_r2_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.077   */0.182     */-0.011    my_dp_r2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.077   */0.182     */-0.011    my_dp_r2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.077   */0.182     */-0.011    my_dp_r2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.077   */0.183     */-0.011    my_dp_r2_inst_d_out_reg_4_/D    1
clk0(R)->clk0(R)  0.077   */0.183     */-0.011    my_dp_r2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.078   */0.186     */-0.011    my_dp_rb1_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.080   */0.186     */-0.011    my_dp_ra3_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.073   */0.186     */-0.011    my_dp_ra2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.078   */0.187     */-0.011    my_dp_rb2_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.081   */0.187     */-0.011    my_dp_rb3_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.079   */0.187     */-0.011    my_dp_rb0_inst_d_out_reg_1_/D    1
clk0(R)->clk0(R)  0.076   */0.187     */-0.011    my_dp_rb1_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.081   */0.187     */-0.011    my_dp_rb3_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.081   */0.187     */-0.011    my_dp_rb3_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.076   */0.188     */-0.011    my_dp_rb1_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.080   */0.188     */-0.011    my_dp_ra3_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.078   */0.188     */-0.011    my_dp_rb2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.073   */0.188     */-0.011    my_dp_ra2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.073   */0.188     */-0.011    my_dp_ra2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.079   */0.188     */-0.011    my_dp_rb0_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.081   */0.188     */-0.011    my_dp_rb3_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.079   */0.188     */-0.011    my_dp_rb0_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.076   */0.188     */-0.011    my_dp_rb1_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.079   */0.188     */-0.011    my_dp_ra3_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.078   */0.189     */-0.011    my_dp_rb2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.079   */0.189     */-0.011    my_dp_ra3_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.084   0.189/*     -0.018/*    my_dp_r2_inst_d_out_reg_2_/D    1
clk0(R)->clk0(R)  0.078   */0.189     */-0.011    my_dp_rb2_inst_d_out_reg_8_/D    1
clk0(R)->clk0(R)  0.073   */0.189     */-0.011    my_dp_ra2_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.084   0.190/*     -0.018/*    my_dp_r2_inst_d_out_reg_5_/D    1
clk0(R)->clk0(R)  0.079   */0.190     */-0.011    my_dp_rb0_inst_d_out_reg_7_/D    1
clk0(R)->clk0(R)  0.080   */0.190     */-0.011    my_dp_ra3_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.073   */0.191     */-0.011    my_dp_ra2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.078   */0.191     */-0.011    my_dp_rb2_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.079   */0.191     */-0.011    my_dp_r8_inst_d_out_reg_6_/D    1
clk0(R)->clk0(R)  0.076   */0.191     */-0.011    my_dp_rb1_inst_d_out_reg_3_/D    1
clk0(R)->clk0(R)  0.079   */0.191     */-0.011    my_dp_rb0_inst_d_out_reg_3_/D    1
```

```
clk0(R)->clk0(R)  0.081    */0.192          */-0.011          my_dp_rb3_inst_d_out_reg_3_/D    1
```