Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course
Integrated Systems Architecture

Master degree in Electrical Engineering

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Contents

CHAPTER 1

Lab 2: Digital arithmetic

1.1 FPU model

1.1.1 Simulation

The FPU has been stimulated with the following numbers, corresponding to the hexadecimal configuration shown in Table 1.1.

Table 1.1: Stimuli and related results

a		b		r	
15	0x41700000	204	0x434c0000	3060	0x453f4000
204	0x434c0000	1204	0x44800000	208896	0x484c0000
1024	0x44800000	-15	0xc1700000	-15360	0xc6700000
-15	0xc1700000	-204	0xc34c0000	3060	0x453f4000
-204	0xc34c0000	-1024	0xc4800000	208896	0x484c0000
-1024	0xc4800000	15	0x41700000	-15360	0xc6700000
-6.7e-12	0xacebbc3c	358	0x43b30000	2.3986e-9	0xb124d49e
5.6e-29	0x108dfa14	7e22	0x656d2b52	3.92e-6	0x3683888b
-4000	0xc57a0000	-358	0xc3b30000	1432000	0x49aece00
4000	0x457a0000	-9999	0xc61c3c00	-39996000	0xcc189298

Figure 1.1 shows a snapshot of the simulation. As it can be observed, stimulating the FPU with the numbers shown in Table 1.1 the results are the expected ones.

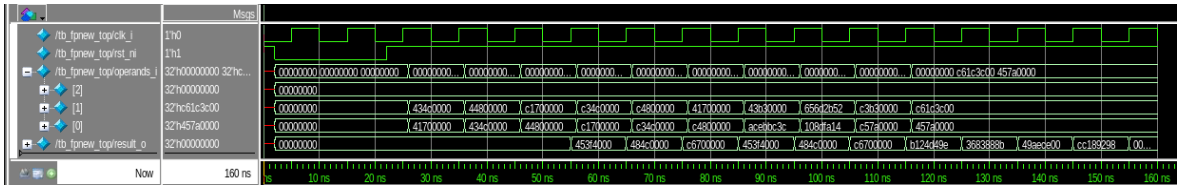

Figure 1.1: Result of the simulation

1.1.2 Synthesis

Table 1.2 shows the results of the experiments required in the assignment.

Table 1.2: Results of the syntheses

commands	**implementation set for multiplier**	**maximum frequency** $f_{max}(MHz)$	**area** (μm^2)
compile	-	340	9978
compile + optimize_registers	-	540	12162
compile_ultra	-	374	9196
set_implementation + compile + optimize_registers	CSA	401	10974
	PPARCH	552	11993

1.1.3 Explanations, comparisons and comments

As it can be observed, the `optimize_registers` command makes the FPU significantly faster at the cost of an enlargement of the complexity. On the other side, the command `compile_ultra` manages to obtain the smallest area slightly improving also the performance with respect to `compile` command. As expected, the CSA implementation is slower than the PPARCH, but the latter occupies more area. Even the slowest PPARCH implementation seen during lectures (Ladner-Fischer) leads to better performance than the CSA.

1.1.4 R8-MBE multiplier

The circuit implementing the R8-MBE is shown in Fig. 1.2.

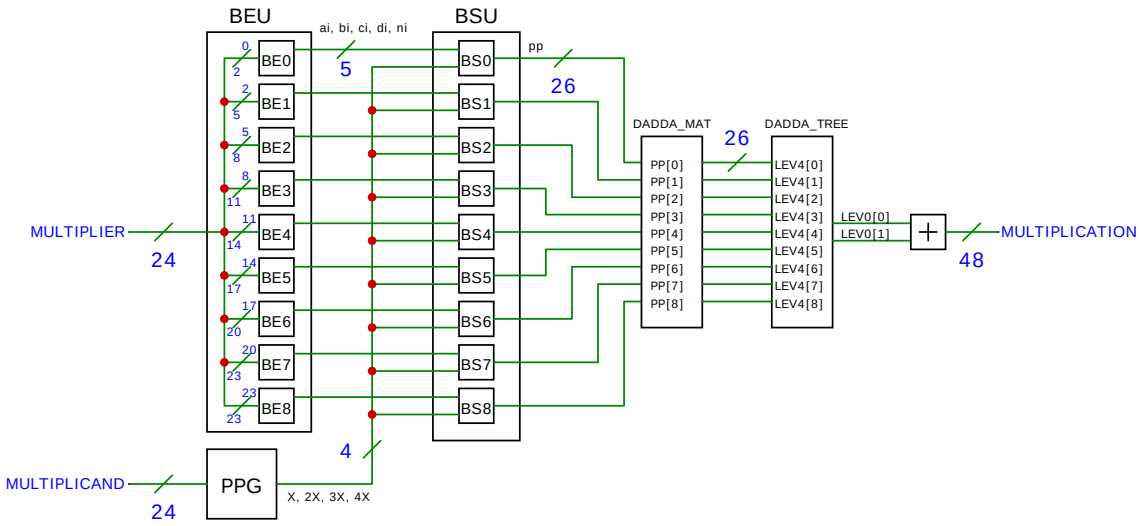

Figure 1.2: Schematic of the R8-MBE Multiplier.

The Dadda-like tree is shown in figure 1.3 with the required compressors. Moreover, figure 1.4 shows how sign extension has been simplified to avoid unnecessary compressors.

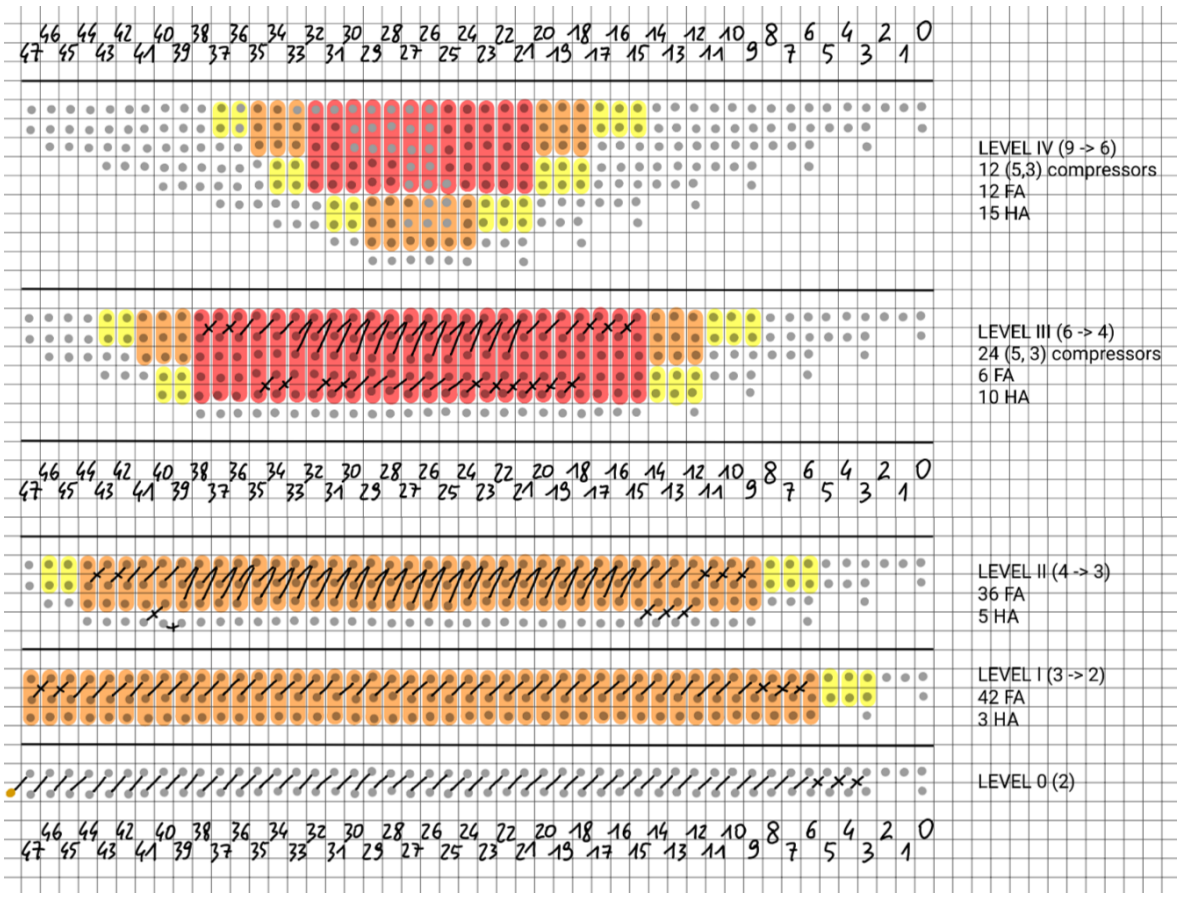

Figure 1.3: Dadda Tree design.

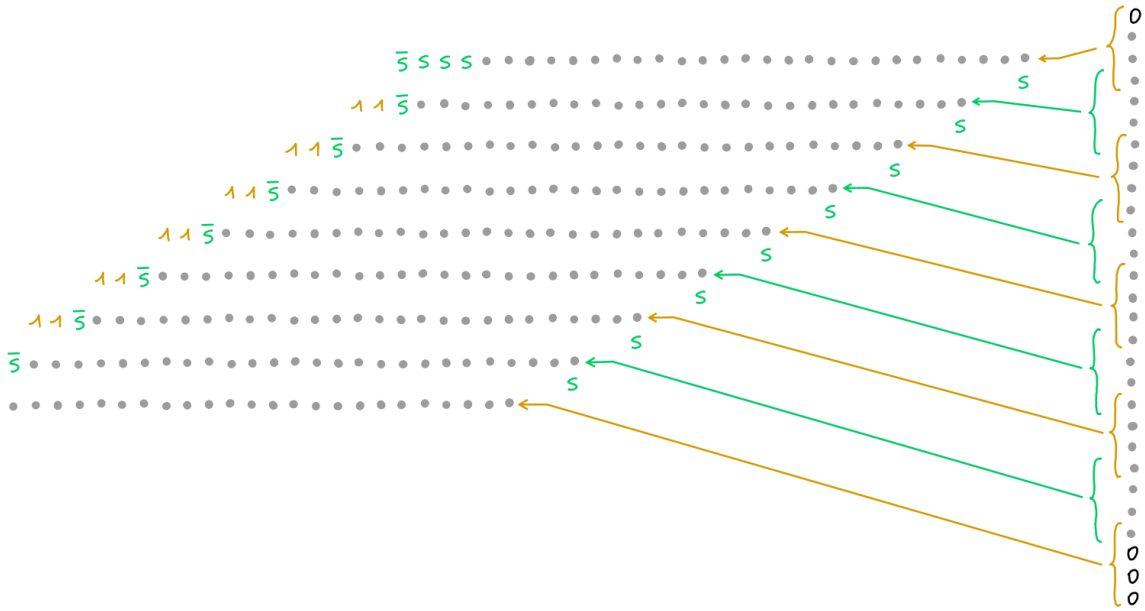

Figure 1.4: Simplification of extension bits to reduce compressors.

Overall, the number of resources instantiated is:

- (5,3) compressors = **36**.
- Full-Adders = **96**.
- Half-Adders = **33**.

Simulation

Standalone multiplier Figure 1.5 shows a snapshot of a simulation for the designed multiplier as a standalone block.

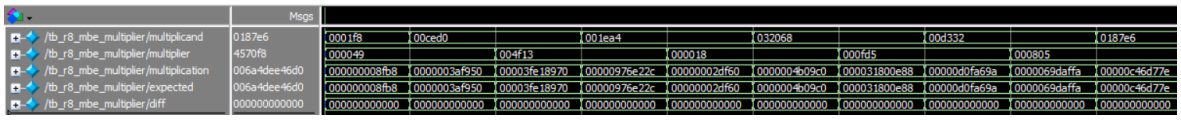

Figure 1.5: Radix-8 MBE Multiplier simulation as a standalone component.

Whole FPU Figure 1.6 shows a snapshot of a simulation for the designed multiplier included in the whole FPU.

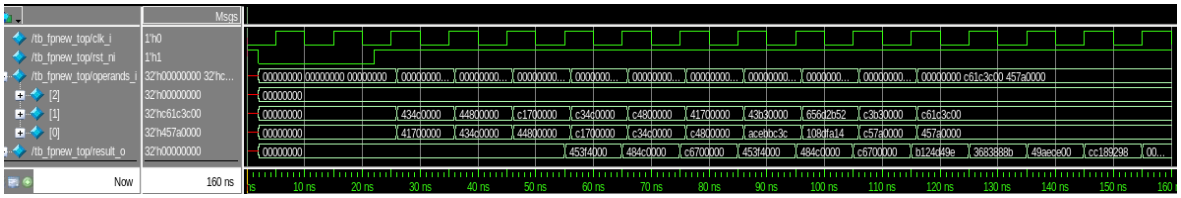

Figure 1.6: Radix-8 MBE Multiplier simulation as part of the FPU unit.

Synthesis

The results of the synthesis are shown in Table 1.3.

Table 1.3: Results of the synthesis

command	**maximum frequency** $f_{max}(MHz)$	**area** (μm^2)
compile_ultra	388	11044

The netlist generated by Design Compiler has been simulated. The results are shown in figure 1.7.

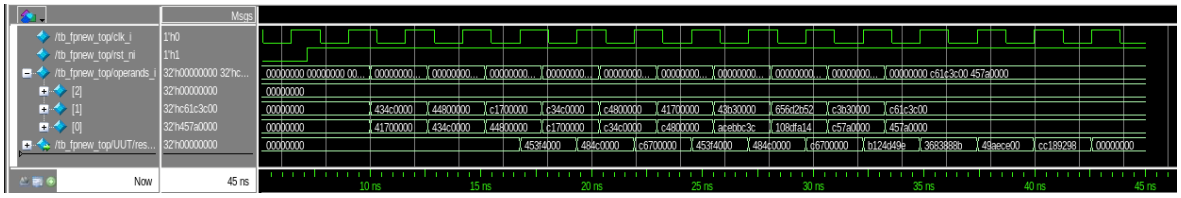

Figure 1.7: Simulation results of the netlist generated by Design Compiler.

Explanations, comparisons and comments

To clarify the role of every component of the R8-MBE Multiplier schematic, a description is provided:

PPG Module
The *Partial Product Generator* module takes as input the multiplicand, and provides as output the corresponding partial products; since for a R8-MBE Multiplier there are only four different multiplication factors (X, 2X, 3X, 4X) according to a generic input X, this module is designed with four outputs, each one representing one out of the four possible values.

BEU Module
The *Booth Encoding Unit* module is an array instantiation of *Booth Encoding* modules, each one takes a 4-bit wide input from the multiplier and provides as output 5 values describing the correspondent Booth codification: these "parameters" are necessary to select the correct partial product among all.

BSU Module
The *Booth Selector Unit* module, similarly to the BEU, is composed by multiple *Booth Selector* modules: each instance gets all the partial products and decides which one should be provided to the next stage; the selection depends on the Booth-encoded parameters generated by the respective Booth Encoding module.

DADDA_MAT Module
The *Dadda Mat* module takes all the partial products to be processed by the Dadda Tree and stores them in a temporary matrix-like structure called *tmpvect*, where it performs the necessary operations to:

1. assign the partial products respecting the 3-bit left shift between adjacent values.
2. rearrange the columns in the range [47:30] in order to do a "vertical flip" of the bits involved: this is an useful operation since after that, the relevant bits (the "dots") follows the same pattern used by the dot matrix in the Dadda Tree design.

Finally, the resulting structure is assigned to *lev4*, which represents the starting level of the Dadda Tree.

DADDA_TREE Module
The last module is the *Dadda Tree*, this works as a multioperand adder and compresses the nine input operands stored in *lev4*; at the end, two converted values are provided at the output and are added together by an adder, that delivers the multiplication.

In figure 1.4, *S* represents the *ni* signal provided from the Booth Encoding module, its value determines if the 2's complement of the respective partial product should be provided to Dadda Tree.

Finally, in figure 1.5, *expected* is the value to be compared with the actual value represented by *multiplication*, *diff* instead is the difference between the two values: since *diff* and is always zero, this demonstrates the correct behavior of the designed multiplier.

APPENDIX A

Reports

A.1 Timing Reports

A.1.1 Timing report #1 - *compile*

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 28 17:04:51 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_operands_q_reg
      [1][1][5]
              (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][67]
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_operands_q_reg[1][1][5]/CK (
      DFFR_X1)
                                                          0.00       0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_operands_q_reg[1][1][5]/Q (DFFR_X1
      )
                                                          0.08       0.08 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/operands_i[1][5] (
      fpnew_classifier_0_3)
                                                          0.00       0.08 f
```

```
37  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U22/ZN (INV_X1)
38                                                      0.02       0.11 r
39  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U19/ZN (NAND3_X1)
40                                                      0.04       0.14 f
41  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U23/ZN (NOR4_X2)
42                                                      0.07       0.21 r
43  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U7/ZN (AND4_X1)
44                                                      0.07       0.28 r
45  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U100/ZN (NOR2_X1)
46                                                      0.02       0.31 f
47  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/info_o[1][is_subnormal] (
        fpnew_classifier_0_3)
48                                                      0.00       0.31 f
49  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U305/ZN (INV_X1)
50                                                      0.02       0.33 r
51  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U304/ZN (NAND2_X1)
52                                                      0.03       0.36 f
53  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/CI (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_6)
54                                                      0.00       0.36 f
55  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U82/ZN (
        NOR2_X1)
56                                                      0.05       0.41 r
57  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U83/ZN (
        OAI21_X1)
58                                                      0.04       0.45 f
59  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U78/ZN (
        XNOR2_X1)
60                                                      0.06       0.51 r
61  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/SUM[1] (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_6)
62                                                      0.00       0.51 r
63  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U288/ZN (XNOR2_X1)
64                                                      0.06       0.58 r
65  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U287/ZN (XNOR2_X1)
66                                                      0.06       0.64 r
67  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1016/ZN (NAND2_X1)
68                                                      0.04       0.68 f
69  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/B[1] (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_6)
70                                                      0.00       0.68 f
71  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U75/ZN (OR2_X2)
72                                                      0.06       0.74 f
73  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U122/ZN (OAI21_X1)
74                                                      0.04       0.77 r
75  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U109/ZN (AOI21_X1)
76                                                      0.03       0.81 f
77  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U101/ZN (OAI21_X1)
78                                                      0.05       0.85 r
79  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U106/ZN (AOI21_X1)
80                                                      0.03       0.89 f
```

```
81  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U102/ZN (OAI21_X1)
82                                                      0.07       0.96 r
83  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U78/ZN (AOI21_X1)
84                                                      0.05       1.00 f
85  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U76/ZN (OAI21_X1)
86                                                      0.05       1.05 r
87  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U138/ZN (XNOR2_X1)
88                                                      0.06       1.12 r
89  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/DIFF[8] (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_6)
90                                                      0.00       1.12 r
91  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1023/ZN (INV_X1)
92                                                      0.03       1.14 f
93  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1024/ZN (NAND3_X1)
94                                                      0.04       1.18 r
95  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U210/ZN (NAND2_X1)
96                                                      0.04       1.22 f
97  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1037/ZN (OAI21_X1)
98                                                      0.04       1.26 r
99  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U32/ZN (NAND2_X1)
100                                                     0.08       1.34 f
101 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1038/ZN (INV_X1)
102                                                     0.06       1.40 r
103 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U503/Z (BUF_X1)
104                                                     0.04       1.44 r
105 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U229/Z (CLKBUF_X3)
106                                                     0.06       1.50 r
107 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U708/ZN (NAND2_X2)
108                                                     0.08       1.57 f
109 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U776/ZN (INV_X2)
110                                                     0.08       1.65 r
111 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1203/ZN (AOI22_X1)
112                                                     0.05       1.70 f
113 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1204/ZN (OAI211_X1)
114                                                     0.04       1.74 r
115 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U320/ZN (AND4_X1)
116                                                     0.07       1.81 r
117 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U205/ZN (NAND3_X1)
118                                                     0.03       1.84 f
119 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1445/ZN (OAI21_X1)
120                                                     0.05       1.89 r
121 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1448/ZN (OAI211_X1)
122                                                     0.05       1.93 f
123 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1449/ZN (NOR2_X1)
124                                                     0.04       1.98 r
125 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/CI (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_7)
126                                                     0.00       1.98 r
127 gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U909/ZN (AND2_X1)
128                                                     0.05       2.02 r
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U961/ZN (AOI21_X1)
                                                          0.03       2.06 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U932/ZN (OAI21_X2)
                                                          0.06       2.11 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U952/ZN (AOI21_X1)
                                                          0.04       2.15 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U955/ZN (OAI221_X4)
                                                          0.12       2.27 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1268/ZN (AOI21_X1)
                                                          0.04       2.31 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1266/Z (XOR2_X1)
                                                          0.07       2.39 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/SUM[49] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_7)
                                                          0.00       2.39 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/B[49] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                          0.00       2.39 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U372/ZN (NOR2_X2)
                                                          0.07       2.45 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U361/ZN (AND4_X2)
                                                          0.07       2.52 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U359/ZN (AND4_X2)
                                                          0.07       2.59 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U363/ZN (AND2_X2)
                                                          0.05       2.63 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U379/ZN (INV_X1)
                                                          0.03       2.67 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U642/ZN (NOR2_X1)
                                                          0.04       2.71 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U641/ZN (XNOR2_X1)
                                                          0.06       2.77 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/DIFF[67] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                          0.00       2.77 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1514/ZN (AOI22_X1)
                                                          0.03       2.80 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U90/ZN (NAND2_X1)
                                                          0.03       2.83 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][67]/D (DFFR_X2)
                                                          0.01       2.84 r
data arrival time                                                    2.84

clock MY_CLK (rise edge)                                  2.94       2.94
clock network delay (ideal)                               0.00       2.94
clock uncertainty                                        -0.07       2.87
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][67]/CK (DFFR_X2)
                                                          0.00       2.87 r
library setup time                                       -0.03       2.84
data required time                                                   2.84
-----------------------------------------------------------------------------
data required time                                                   2.84
data arrival time                                                   -2.84
-----------------------------------------------------------------------------
```

```
  slack (MET)                                                    0.00


1
```

A.1.2 Timing report #2 - *compile + optimize_registers*

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 28 18:54:22 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/MY_CLK_r_REG481_S1
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG222_S2
           (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                  Incr       Path
  -----------------------------------------------------------------------
  clock MY_CLK (rise edge)                               0.00       0.00
  clock network delay (ideal)                            0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/MY_CLK_r_REG481_S1/CK (DFFR_X1)
                                                         0.00       0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/MY_CLK_r_REG481_S1/QN (DFFR_X1)
                                                         0.07       0.07 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U94/ZN (INV_X1)
                                                         0.02       0.09 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U151/ZN (AOI21_X1)
                                                         0.05       0.14 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U134/ZN (OAI21_X1)
                                                         0.03       0.17 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U150/ZN (AOI21_X1)
                                                         0.06       0.23 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U157/ZN (OAI21_X1)
                                                         0.04       0.27 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U116/ZN (AOI21_X1)
                                                         0.06       0.32 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U129/ZN (XNOR2_X1)
                                                         0.07       0.39 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/DIFF[8] (
      fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_9)
                                                         0.00       0.39 r
```

```
51  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U577/ZN (AND2_X1)
52                                                      0.05       0.44 r
53  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U782/ZN (AND4_X2)
54                                                      0.06       0.50 r
55  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U536/ZN (OAI22_X1)
56                                                      0.04       0.54 f
57  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U352/ZN (OR2_X2)
58                                                      0.09       0.63 f
59  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U720/ZN (OR2_X1)
60                                                      0.08       0.71 f
61  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U412/ZN (AND2_X1)
62                                                      0.04       0.75 f
63  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1039/ZN (AOI22_X1)
64                                                      0.06       0.81 r
65  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U289/ZN (OAI221_X1)
66                                                      0.06       0.87 f
67  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1163/ZN (AOI22_X1)
68                                                      0.05       0.92 r
69  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1164/ZN (OAI211_X1)
70                                                      0.05       0.97 f
71  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1165/ZN (INV_X1)
72                                                      0.04       1.01 r
73  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1471/ZN (AOI22_X1)
74                                                      0.04       1.04 f
75  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/U1472/Z (XOR2_X1)
76                                                      0.07       1.12 f
77  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/B[10] (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_9)
78                                                      0.00       1.12 f
79  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U996/ZN (NOR2_X1)
80                                                      0.04       1.16 r
81  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1146/ZN (OAI21_X1)
82                                                      0.03       1.19 f
83  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1147/ZN (AOI21_X1)
84                                                      0.04       1.23 r
85  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1646/ZN (OAI21_X1)
86                                                      0.03       1.27 f
87  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1645/ZN (AOI21_X1)
88                                                      0.07       1.34 r
89  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U888/ZN (INV_X1)
90                                                      0.04       1.38 f
91  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U886/Z (BUF_X1)
92                                                      0.05       1.42 f
93  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1417/ZN (AOI21_X1)
94                                                      0.04       1.47 r
95  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1043/ZN (XNOR2_X1)
96                                                      0.04       1.51 f
97  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
        gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/SUM[21] (
        fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_9)
98                                                      0.00       1.51 f
```

```
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/B[21] (
      fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                          0.00       1.51 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U633/ZN (NOR2_X1)
                                                          0.05       1.56 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U375/ZN (NAND2_X1)
                                                          0.03       1.59 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U368/ZN (OR2_X2)
                                                          0.07       1.66 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U603/ZN (NOR2_X1)
                                                          0.05       1.71 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U620/ZN (NAND2_X1)
                                                          0.03       1.73 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG222_S2/D (DFFR_X1)
                                                          0.01       1.74 f
  data arrival time                                                  1.74

  clock MY_CLK (rise edge)                                1.85       1.85
  clock network delay (ideal)                             0.00       1.85
  clock uncertainty                                      -0.07       1.78
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG222_S2/CK (DFFR_X1)
                                                          0.00       1.78 r
  library setup time                                     -0.04       1.74
  data required time                                                 1.74
  -----------------------------------------------------------------------------
  data required time                                                 1.74
  data arrival time                                                 -1.74
  -----------------------------------------------------------------------------
  slack (MET)                                                        0.00


1
```

A.1.3 Timing report #3 - *compile_ultra*

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 28 19:34:07 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][34]
              (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/out_pipe_status_q_reg[1][UF]
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

```

```
Point                                                   Incr       Path
---------------------------------------------------------------------------
clock MY_CLK (rise edge)                                0.00       0.00
clock network delay (ideal)                             0.00       0.00
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][34]/CK (DFFR_X1)
                                                        0.00       0.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][34]/Q (DFFR_X1)
                                                        0.10       0.10 f
U2070/ZN (OR2_X1)                                       0.07       0.17 f
U1083/ZN (NOR2_X2)                                      0.06       0.23 r
U269/ZN (AND4_X1)                                       0.08       0.32 r
U55/ZN (AND2_X1)                                        0.06       0.38 r
U1081/ZN (AND3_X2)                                      0.08       0.45 r
U1098/ZN (NAND3_X1)                                     0.04       0.50 f
U277/ZN (OAI211_X1)                                     0.05       0.55 r
U2137/ZN (NAND2_X1)                                     0.05       0.59 f
U2173/ZN (INV_X1)                                       0.03       0.63 r
U2174/ZN (OAI21_X1)                                     0.03       0.65 f
U2179/ZN (AOI21_X1)                                     0.04       0.69 r
U2202/ZN (OAI21_X1)                                     0.03       0.72 f
U2205/ZN (NAND2_X1)                                     0.04       0.77 r
U2210/Z (MUX2_X1)                                       0.09       0.85 f
U2212/Z (MUX2_X1)                                       0.08       0.93 f
U2225/ZN (INV_X1)                                       0.03       0.96 r
U721/ZN (AND2_X2)                                       0.08       1.04 r
U72/ZN (INV_X1)                                         0.05       1.09 f
U2473/ZN (INV_X1)                                       0.11       1.20 r
U2294/ZN (NAND2_X1)                                     0.04       1.24 f
U2297/ZN (NAND4_X1)                                     0.05       1.29 r
U2298/ZN (NAND2_X1)                                     0.03       1.32 f
U164/ZN (AND4_X1)                                       0.05       1.37 f
U968/ZN (OAI211_X1)                                     0.05       1.42 r
U2385/ZN (NAND4_X1)                                     0.06       1.48 f
U947/ZN (AND4_X2)                                       0.07       1.55 f
U433/ZN (INV_X1)                                        0.05       1.60 r
U479/ZN (AND2_X1)                                       0.05       1.64 r
U1116/ZN (NOR2_X1)                                      0.02       1.67 f
U2580/ZN (OAI22_X1)                                     0.05       1.72 r
U2596/ZN (AND4_X1)                                      0.07       1.79 r
U2607/ZN (AND4_X1)                                      0.06       1.85 r
U2608/ZN (OAI21_X1)                                     0.04       1.89 f
U990/Z (BUF_X2)                                         0.06       1.95 f
U3395/ZN (NAND4_X1)                                     0.06       2.00 r
U3416/ZN (NAND2_X1)                                     0.04       2.05 f
U3459/ZN (NOR2_X1)                                      0.06       2.11 r
U3491/ZN (NAND2_X1)                                     0.03       2.15 f
U3492/ZN (NOR2_X1)                                      0.04       2.19 r
U395/ZN (NAND2_X1)                                      0.05       2.24 f
U3521/ZN (NOR2_X1)                                      0.05       2.29 r
U3522/ZN (XNOR2_X1)                                     0.04       2.33 f
U6478/ZN (INV_X1)                                       0.03       2.36 r
U6479/ZN (NAND4_X1)                                     0.04       2.40 f
U6480/ZN (NOR4_X1)                                      0.10       2.50 r
U6481/ZN (NAND2_X1)                                     0.03       2.53 f
U6483/ZN (NAND2_X1)                                     0.03       2.56 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/out_pipe_status_q_reg[1][UF]/D (DFFR_X2)
                                                        0.01       2.57 r
data arrival time                                                  2.57

clock MY_CLK (rise edge)                                2.67       2.67
clock network delay (ideal)                             0.00       2.67
clock uncertainty                                      -0.07       2.60
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/out_pipe_status_q_reg[1][UF]/CK (DFFR_X2)
                                                        0.00       2.60 r
library setup time                                     -0.03       2.57
data required time                                                 2.57
---------------------------------------------------------------------------
data required time                                                 2.57
data arrival time                                                 -2.57
---------------------------------------------------------------------------
```

```
  slack (MET)                                                    0.00


1
```

A.1.4 Timing report #4 - *CSA multiplier, compile + optimize_registers*

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 28 21:31:42 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: MY_CLK_r_REG444_S1
              (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: MY_CLK_r_REG339_S2
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                    Incr       Path
  --------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                 0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  MY_CLK_r_REG444_S1/CK (DFFR_X1)                          0.00       0.00 r
  MY_CLK_r_REG444_S1/Q (DFFR_X1)                           0.10       0.10 r
  U2026/ZN (NAND2_X1)                                      0.04       0.14 f
  U1748/ZN (INV_X1)                                        0.07       0.22 r
  U1734/ZN (NAND2_X1)                                      0.04       0.26 f
  U1339/Z (CLKBUF_X1)                                      0.09       0.35 f
  U2200/ZN (OAI22_X1)                                      0.08       0.43 r
  U2201/ZN (INV_X1)                                        0.03       0.46 f
  U2242/ZN (AOI22_X1)                                      0.06       0.52 r
  U2243/ZN (OAI221_X1)                                     0.05       0.58 f
  U2244/ZN (INV_X1)                                        0.04       0.61 r
  U2303/Z (MUX2_X1)                                        0.04       0.66 r
  U1566/ZN (AND2_X1)                                       0.05       0.71 r
  U2304/ZN (OAI222_X1)                                     0.05       0.76 f
  U2305/ZN (INV_X1)                                        0.05       0.81 r
  U2443/ZN (NOR3_X1)                                       0.03       0.84 f
  U2444/ZN (NAND4_X1)                                      0.03       0.87 r
  U2445/ZN (NOR4_X1)                                       0.03       0.90 f
  U2450/ZN (OAI221_X1)                                     0.06       0.95 r
  U1565/ZN (NOR2_X1)                                       0.03       0.98 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
       i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/CI (
       fpnew_top_DW01_add_15)
                                                           0.00       0.98 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
       i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U892/ZN (NAND2_X1)
                                                           0.05       1.04 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
       i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1069/ZN (INV_X1)
                                                           0.03       1.07 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
       i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1216/ZN (AOI21_X1)
                                                           0.05       1.12 r
```

```
59  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U688/ZN (OAI21_X1)
60                                                      0.04       1.16 f
61  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1249/ZN (AOI21_X1)
62                                                      0.06       1.22 r
63  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U704/ZN (OAI21_X1)
64                                                      0.04       1.26 f
65  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1172/ZN (AOI21_X1)
66                                                      0.06       1.32 r
67  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1274/ZN (OAI21_X1)
68                                                      0.04       1.36 f
69  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U523/CO (FA_X1)
70                                                      0.11       1.46 f
71  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U522/CO (FA_X1)
72                                                      0.11       1.57 f
73  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1287/ZN (AOI21_X1)
74                                                      0.06       1.63 r
75  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1286/ZN (OAI21_X1)
76                                                      0.04       1.67 f
77  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1222/ZN (INV_X1)
78                                                      0.03       1.70 r
79  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1221/ZN (OAI21_X1)
80                                                      0.04       1.74 f
81  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1080/ZN (AOI21_X1)
82                                                      0.05       1.79 r
83  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1144/ZN (INV_X1)
84                                                      0.03       1.82 f
85  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1143/ZN (AOI21_X1)
86                                                      0.05       1.86 r
87  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1097/ZN (INV_X1)
88                                                      0.03       1.89 f
89  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1111/ZN (AOI21_X1)
90                                                      0.06       1.95 r
91  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1285/ZN (OAI21_X1)
92                                                      0.04       1.99 f
93  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1272/ZN (AOI21_X1)
94                                                      0.05       2.05 r
95  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1284/ZN (OAI21_X1)
96                                                      0.04       2.09 f
97  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U701/ZN (AOI21_X1)
98                                                      0.06       2.15 r
99  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1131/ZN (OAI21_X1)
100                                                     0.04       2.19 f
101 add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U763/ZN (AOI21_X1)
102                                                     0.04       2.23 r
103 add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U680/ZN (INV_X1)
104                                                     0.03       2.26 f
105 add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1154/ZN (AOI21_X1)
106                                                     0.05       2.31 r
107 add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
        i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U751/ZN (XNOR2_X1)
```

```
                                                          0.06       2.37 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/SUM[37] (
      fpnew_top_DW01_add_15)
                                                          0.00       2.37 r
  MY_CLK_r_REG339_S2/D (DFFR_X1)                          0.01       2.38 r
  data arrival time                                                  2.38

  clock MY_CLK (rise edge)                                2.49       2.49
  clock network delay (ideal)                             0.00       2.49
  clock uncertainty                                      -0.07       2.42
  MY_CLK_r_REG339_S2/CK (DFFR_X1)                         0.00       2.42 r
  library setup time                                     -0.04       2.38
  data required time                                                 2.38
  -----------------------------------------------------------------------------
  data required time                                                 2.38
  data arrival time                                                 -2.38
  -----------------------------------------------------------------------------
  slack (MET)                                                        0.00


1
```

A.1.5 Timing report #5 - *PPARCH multiplier*, *compile + optimize_registers*

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 28 21:47:46 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/MY_CLK_r_REG523_S1
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG283_S2
           (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/MY_CLK_r_REG523_S1/CK (DFFR_X1)
                                                          0.00       0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/MY_CLK_r_REG523_S1/Q (DFFR_X1)
                                                          0.08       0.08 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U72/ZN (OR2_X2)
                                                          0.06       0.15 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U94/ZN (AOI21_X1)
                                                          0.05       0.20 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U151/ZN (OAI21_X1)
```

```
                                                          0.03       0.23 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U149/ZN (AOI21_X1)
                                                          0.04       0.27 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U130/Z (XOR2_X1)
                                                          0.08       0.35 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/DIFF[9] (fpnew_top_DW01_sub_6)
                                                          0.00       0.35 r
  U2501/ZN (INV_X1)                                       0.03       0.38 f
  U1810/ZN (OAI22_X1)                                     0.08       0.46 r
  U2512/ZN (NAND2_X1)                                     0.04       0.50 f
  U1624/Z (BUF_X1)                                        0.05       0.55 f
  U1790/ZN (OAI22_X1)                                     0.06       0.61 r
  U1794/ZN (INV_X1)                                       0.03       0.64 f
  U2675/ZN (AOI22_X1)                                     0.07       0.71 r
  U2676/ZN (OAI221_X1)                                    0.05       0.76 f
  U2677/ZN (INV_X1)                                       0.03       0.79 r
  U2737/Z (MUX2_X1)                                       0.05       0.84 r
  U1895/ZN (AND2_X1)                                      0.04       0.88 r
  U1759/ZN (OAI222_X1)                                    0.04       0.93 f
  U1828/ZN (INV_X1)                                       0.04       0.96 r
  U2836/Z (MUX2_X1)                                       0.08       1.04 f
  U2837/ZN (NAND2_X1)                                     0.04       1.08 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/B[13] (
      fpnew_top_DW01_add_12)
                                                          0.00       1.08 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1078/ZN (NOR2_X1)
                                                          0.03       1.11 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1019/ZN (NOR2_X1)
                                                          0.04       1.15 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1547/ZN (NAND2_X1)
                                                          0.03       1.18 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1562/ZN (OAI21_X1)
                                                          0.05       1.23 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1561/ZN (AOI21_X1)
                                                          0.03       1.26 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U923/ZN (OAI21_X1)
                                                          0.06       1.32 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1004/Z (BUF_X4)
                                                          0.07       1.39 r
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1566/ZN (AOI21_X1)
                                                          0.05       1.44 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1055/ZN (XNOR2_X1)
                                                          0.06       1.50 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/SUM[47] (
      fpnew_top_DW01_add_12)
                                                          0.00       1.50 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/B[47] (fpnew_top_DW01_sub_7)
                                                          0.00       1.50 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U524/ZN (NOR2_X1)
                                                          0.05       1.55 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U646/ZN (NAND2_X1)
                                                          0.03       1.58 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U378/ZN (NOR2_X1)
                                                          0.04       1.62 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U451/ZN (AND2_X1)
```

```
                                                          0.05       1.67 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U773/ZN (NAND2_X1)
                                                          0.03       1.69 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG283_S2/D (DFFS_X1)
                                                          0.01       1.70 f
  data arrival time                                                  1.70

  clock MY_CLK (rise edge)                                1.81       1.81
  clock network delay (ideal)                             0.00       1.81
  clock uncertainty                                      -0.07       1.74
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG283_S2/CK (DFFS_X1)
                                                          0.00       1.74 r
  library setup time                                     -0.04       1.70
  data required time                                                 1.70
  --------------------------------------------------------------------------
  data required time                                                 1.70
  data arrival time                                                 -1.70
  --------------------------------------------------------------------------
  slack (MET)                                                        0.00


1
```

A.1.6 Timing report #6 - *BOOTH multiplier*, *compile_ultra*

```
Information: Updating design information... (UID-85)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Dec 19 18:54:45 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_op_q_reg[1][0]
              (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][62]
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_op_q_reg[1][0]/CK (DFFR_X1)
                                                          0.00       0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_op_q_reg[1][0]/Q (DFFR_X1)
                                                          0.09       0.09 f
  U4778/ZN (OR2_X2)                                       0.07       0.16 f
  U3938/ZN (AND2_X1)                                      0.06       0.22 f
  U5550/ZN (AND2_X1)                                      0.05       0.26 f
  U7107/ZN (NOR2_X1)                                      0.05       0.31 r
  U7109/ZN (OAI21_X1)                                     0.04       0.35 f
```

```
  U3933/ZN (AOI21_X1)                                      0.06       0.40 r
  U4651/ZN (INV_X1)                                        0.04       0.45 f
  U7584/ZN (XNOR2_X1)                                      0.07       0.52 f
  U3679/ZN (INV_X1)                                        0.04       0.56 r
  U3681/ZN (INV_X1)                                        0.04       0.59 f
  U4075/ZN (INV_X1)                                        0.05       0.64 r
  U11710/ZN (OR2_X1)                                       0.04       0.68 r
  U11712/ZN (NAND2_X1)                                     0.02       0.71 f
  U11717/ZN (NOR4_X1)                                      0.08       0.79 r
  intadd_27/U4/S (FA_X1)                                   0.14       0.92 f
  U4661/CO (FA_X1)                                         0.10       1.02 f
  U4993/ZN (XNOR2_X1)                                      0.06       1.08 r
  U4991/ZN (XNOR2_X1)                                      0.06       1.14 r
  U8692/ZN (NAND2_X1)                                      0.03       1.18 f
  U5632/ZN (OR2_X1)                                        0.05       1.23 f
  U5631/ZN (AND2_X1)                                       0.04       1.27 f
  U6174/ZN (NAND2_X1)                                      0.03       1.30 r
  U8700/ZN (AOI21_X1)                                      0.03       1.33 f
  U8756/ZN (OAI21_X1)                                      0.05       1.38 r
  U8815/ZN (AOI21_X1)                                      0.04       1.42 f
  U3745/ZN (OAI21_X2)                                      0.06       1.48 r
  U4633/ZN (AOI21_X1)                                      0.03       1.52 f
  U6288/ZN (OAI21_X1)                                      0.05       1.57 r
  U4860/ZN (INV_X1)                                        0.03       1.60 f
  U9200/ZN (OAI21_X1)                                      0.05       1.65 r
  U9201/ZN (INV_X1)                                        0.03       1.68 f
  U6173/ZN (OAI21_X1)                                      0.04       1.73 r
  U6172/ZN (XNOR2_X1)                                      0.07       1.80 r
  U6317/ZN (XNOR2_X1)                                      0.08       1.87 r
  U6082/ZN (NOR2_X1)                                       0.03       1.91 f
  U6087/ZN (NOR2_X1)                                       0.04       1.94 r
  U9427/ZN (NAND2_X1)                                      0.03       1.97 f
  U5139/ZN (AND2_X1)                                       0.04       2.01 f
  U9430/ZN (OAI21_X1)                                      0.04       2.05 r
  U9431/ZN (AOI21_X1)                                      0.03       2.07 f
  U9432/ZN (OAI21_X1)                                      0.04       2.11 r
  U9463/ZN (NAND2_X1)                                      0.03       2.14 f
  U4758/ZN (AND2_X2)                                       0.04       2.18 f
  U4913/ZN (OR2_X2)                                        0.06       2.24 f
  U4948/ZN (NAND2_X1)                                      0.05       2.29 r
  U11331/ZN (NAND2_X1)                                     0.04       2.33 f
  U11333/ZN (NAND2_X1)                                     0.03       2.36 r
  U11334/ZN (XNOR2_X1)                                     0.05       2.41 r
  U11335/ZN (NAND2_X1)                                     0.03       2.44 f
  U11337/ZN (NAND3_X1)                                     0.03       2.47 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][62]/D (DFFR_X1)
                                                           0.01       2.48 r
  data arrival time                                                   2.48

  clock MY_CLK (rise edge)                                 2.58       2.58
  clock network delay (ideal)                              0.00       2.58
  clock uncertainty                                       -0.07       2.51
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][62]/CK (DFFR_X1)
                                                           0.00       2.51 r
  library setup time                                      -0.03       2.48
  data required time                                                  2.48
  ------------------------------------------------------------------------
  data required time                                                  2.48
  data arrival time                                                  -2.48
  ------------------------------------------------------------------------
  slack (MET)                                                         0.00


1
```

A.2 Area Reports

A.2.1 Area report #1 - *compile*

```
1
2  ****************************************
3  Report : area
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Nov 28 17:04:51 2022
7  ****************************************
8
9  Library(s) Used:
10
11     NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
           NangateOpenCellLibrary_typical_ecsm_nowlm.db)
12
13 Number of ports:                         3458
14 Number of nets:                        10738
15 Number of cells:                        7372
16 Number of combinational cells:          7003
17 Number of sequential cells:              297
18 Number of macros/black boxes:              0
19 Number of buf/inv:                      1759
20 Number of references:                     17
21
22 Combinational area:               8385.384002
23 Buf/Inv area:                     1120.923997
24 Noncombinational area:            1592.542052
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:      undefined  (Wire load has zero net area)
27
28 Total cell area:                  9977.926053
29 Total area:                 undefined
30 1
```

A.2.2 Area report #2 - *compile + optimize_registers*

```
1
2  ****************************************
3  Report : area
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Nov 28 18:54:22 2022
7  ****************************************
8
9  Library(s) Used:
10
11     NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
           NangateOpenCellLibrary_typical_ecsm_nowlm.db)
12
13 Number of ports:                         3391
14 Number of nets:                         9398
15 Number of cells:                        7363
16 Number of combinational cells:          6072
17 Number of sequential cells:              933
18 Number of macros/black boxes:              0
19 Number of buf/inv:                      1458
20 Number of references:                     14
21
22 Combinational area:               7198.225989
23 Buf/Inv area:                      871.948001
24 Noncombinational area:            4964.092160
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:      undefined  (Wire load has zero net area)
27
28 Total cell area:                 12162.318149
29 Total area:                 undefined
30 1
```

A.2.3 Area report #3 - *compile_ultra*

```
1
2  ****************************************
3  Report : area
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Nov 28 19:34:08 2022
7  ****************************************
8
9  Library(s) Used:
10
11     NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
           NangateOpenCellLibrary_typical_ecsm_nowlm.db)
12
13 Number of ports:                          160
14 Number of nets:                          7548
15 Number of cells:                         6956
16 Number of combinational cells:           6686
17 Number of sequential cells:               268
18 Number of macros/black boxes:               0
19 Number of buf/inv:                       1046
20 Number of references:                      47
21
22 Combinational area:               7765.071993
23 Buf/Inv area:                      588.658004
24 Noncombinational area:            1431.346046
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:      undefined  (Wire load has zero net area)
27
28 Total cell area:                  9196.418039
29 Total area:                 undefined
30 1
```

A.2.4 Area report #4 - *CSA multiplier, compile + optimize_registers*

```
1
2  ****************************************
3  Report : area
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Nov 28 21:31:42 2022
7  ****************************************
8
9  Library(s) Used:
10
11     NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
           NangateOpenCellLibrary_typical_ecsm_nowlm.db)
12
13 Number of ports:                          1097
14 Number of nets:                          7384
15 Number of cells:                         5879
16 Number of combinational cells:           5069
17 Number of sequential cells:               785
18 Number of macros/black boxes:               0
19 Number of buf/inv:                        944
20 Number of references:                      51
21
22 Combinational area:               6797.629995
23 Buf/Inv area:                      525.616003
24 Noncombinational area:            4176.732135
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:      undefined  (Wire load has zero net area)
27
28 Total cell area:                 10974.362130
29 Total area:                 undefined
30 1
```

A.2.5 Area report #5 - *PPARCH multiplier*, *compile + optimize_registers*

```
1
2  ****************************************
3  Report : area
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Nov 28 21:47:46 2022
7  ****************************************
8
9  Library(s) Used:
10
11     NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
           NangateOpenCellLibrary_typical_ecsm_nowlm.db)
12
13 Number of ports:                          939
14 Number of nets:                          7806
15 Number of cells:                         6651
16 Number of combinational cells:           5676
17 Number of sequential cells:               955
18 Number of macros/black boxes:               0
19 Number of buf/inv:                       1308
20 Number of references:                      54
21
22 Combinational area:               6912.275993
23 Buf/Inv area:                      784.434000
24 Noncombinational area:            5080.600164
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:      undefined  (Wire load has zero net area)
27
28 Total cell area:                 11992.876157
29 Total area:                 undefined
30 1
```

A.2.6 Area report #6 - *BOOTH multiplier*, *compile_ultra*

```
1
2  ****************************************
3  Report : area
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Dec 19 18:54:46 2022
7  ****************************************
8
9  Library(s) Used:
10
11     NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
           NangateOpenCellLibrary_typical_ecsm_nowlm.db)
12
13 Number of ports:                          160
14 Number of nets:                         10156
15 Number of cells:                         9794
16 Number of combinational cells:           9525
17 Number of sequential cells:               268
18 Number of macros/black boxes:               0
19 Number of buf/inv:                       1523
20 Number of references:                      52
21
22 Combinational area:               9617.761958
23 Buf/Inv area:                      875.938003
24 Noncombinational area:            1426.026046
25 Macro/Black Box area:                0.000000
26 Net Interconnect area:      undefined  (Wire load has zero net area)
27
28 Total cell area:                 11043.788004
29 Total area:                 undefined
30 1
```

A.3 Resources Reports

A.3.1 Resource report #1 - *CSA multiplier*, *compile + optimize_registers*

```
1
2  ****************************************
3  Report : resources
4  Design : fpnew_top
5  Version: S-2021.06-SP4
6  Date   : Mon Nov 28 21:31:42 2022
7  ****************************************
8
9  Resource Sharing Report for design fpnew_top in file ../src/fpnew_top.sv
10
11 ===============================================================================
12 |          |              |            | Contained     |                      |
13 | Resource | Module       | Parameters | Resources     | Contained Operations |
14 ===============================================================================
15 | r448     | DW01_cmp2    | width=3    |               | gen_operation_groups[0].i_opgroup_block/
       i_arbiter/gt_208_G4 |
16 |              |                         |
17 |          |              |            |               | gen_operation_groups[0].i_opgroup_block/
       i_arbiter/lte_209_G4 |
18 | r449     | DW01_cmp2    | width=3    |               | gen_operation_groups[1].i_opgroup_block/
       i_arbiter/gt_208_G4 |
19 |              |                         |
20 |          |              |            |               | gen_operation_groups[1].i_opgroup_block/
       i_arbiter/lte_209_G4 |
21 | r450     | DW01_cmp2    | width=3    |               | gen_operation_groups[2].i_opgroup_block/
       i_arbiter/gt_208_G4 |
22 |              |                         |
23 |          |              |            |               | gen_operation_groups[2].i_opgroup_block/
       i_arbiter/lte_209_G4 |
24 | r451     | DW01_cmp2    | width=3    |               | gen_operation_groups[3].i_opgroup_block/
       i_arbiter/gt_208_G4 |
25 |              |                         |
26 |          |              |            |               | gen_operation_groups[3].i_opgroup_block/
       i_arbiter/lte_209_G4 |
27 | r452     | DW01_cmp2    | width=2    |               | i_arbiter/gt_208_G4  |
28 |          |              |            |               | i_arbiter/lte_209_G4 |
29 | r482     | DW01_add     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/add_285 |
30 | r490     | DW01_sub     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/sub_293 |
31 | r492     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/gt_295 |
32 | r494     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/lte_302 |
33 | r496     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/lte_305 |
34 | r498     | DW01_sub     | width=7    |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/sub_306 |
35 | r500     | DW02_mult    | A_width=24 |               | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/mult_325 |
36 |
37 |          |              | B_width=24 |               |                      |
38 | r502     | DW_rightsh   | A_width=100 |              | gen_operation_groups[0].i_opgroup_block/
       gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
       i_fma/srl_349 |
39 |
40 |          |              | SH_width=7 |               |                      |
41 | r504     | DW01_add     | width=77   |               | add_1_root_gen_operation_groups[0].
       i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
       lane_instance.i_fma/add_368_2 |
```

```
| r506     | DW01_sub     | width=76   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_372 |
| r508     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510 |
| r510     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510_2 |
| r516     | DW_cmp       | width=12   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_512 |
| r518     | DW01_add     | width=7    |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_514 |
| r524     | DW01_add     | width=7    |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_519 |
| r526     | DW_leftsh    | A_width=77 |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sll_530 |
|          |              | SH_width=7 |               |                       |
| r528     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gt_547 |
| r530     | DW01_inc     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_542 |
| r532     | DW01_dec     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_549 |
| r534     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_576 |
| r536     | DW01_add     | width=31   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/i_fpnew_rounding/add_63 |
| r1264    | DW01_add     | width=10   |               |
    add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1266    | DW01_sub     | width=10   |               |
    sub_2_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1268    | DW01_add     | width=10   |               |
    add_0_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1988    | DW01_sub     | width=11   |               | sub_1_root_gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512 |
| r1990    | DW01_inc     | width=12   |               | add_0_root_gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512 |
| r2710    | DW01_sub     | width=10   |               | sub_1_root_gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
| r2712    | DW01_inc     | width=10   |               | add_0_root_gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_515 |
================================================================================


Implementation Report
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|                    |                  | Current            | Set            |
| Cell               | Module           | Implementation     | Implementation |
================================================================================
| add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2 |
|                    | DW01_add         | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372 |
|                    | DW01_sub         | pparch (area,speed)                 |
```

```
| add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                  | DW01_inc         | pparch (speed)     |                |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                  | DW01_sub         | pparch (speed)     |                |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/i_fpnew_rounding/add_63 |
|                  | DW01_add         | pparch (area,speed)                 |
| add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
|                  | DW01_add         | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293 |
|                  | DW01_sub         | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325 |
|                  | DW02_mult        | csa                | csa            |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_542 |
|                  | DW01_inc         | rpl                |                |
==============================================================================

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```

A.3.2 Resource report #2 - *PPARCH multiplier, compile + optimize_registers*

```

****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Mon Nov 28 21:47:46 2022
****************************************

Resource Sharing Report for design fpnew_top in file ../src/fpnew_top.sv

==============================================================================
|          |              |            | Contained     |                        |
| Resource | Module       | Parameters | Resources     | Contained Operations |
==============================================================================
| r449     | DW01_cmp2    | width=3    |               | gen_operation_groups[0].i_opgroup_block/
    i_arbiter/gt_208_G4 |
|              |                       |
|          |              |            |               | gen_operation_groups[0].i_opgroup_block/
    i_arbiter/lte_209_G4 |
| r450     | DW01_cmp2    | width=3    |               | gen_operation_groups[1].i_opgroup_block/
    i_arbiter/gt_208_G4 |
|              |                       |
|          |              |            |               | gen_operation_groups[1].i_opgroup_block/
    i_arbiter/lte_209_G4 |
| r451     | DW01_cmp2    | width=3    |               | gen_operation_groups[2].i_opgroup_block/
    i_arbiter/gt_208_G4 |
|              |                       |
|          |              |            |               | gen_operation_groups[2].i_opgroup_block/
    i_arbiter/lte_209_G4 |
| r452     | DW01_cmp2    | width=3    |               | gen_operation_groups[3].i_opgroup_block/
    i_arbiter/gt_208_G4 |
|              |                       |
|          |              |            |               | gen_operation_groups[3].i_opgroup_block/
    i_arbiter/lte_209_G4 |
| r453     | DW01_cmp2    | width=2    |               | i_arbiter/gt_208_G4  |
|          |              |            |               | i_arbiter/lte_209_G4 |
| r483     | DW01_add     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_285 |
| r491     | DW01_sub     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_293 |
| r493     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
```

```
    i_fma/gt_295 |
| r495     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_302 |
| r497     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_305 |
| r499     | DW01_sub     | width=7    |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_306 |
| r501     | DW02_mult    | A_width=24 |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/mult_325 |
|          |              | B_width=24 |               |                       |
| r503     | DW_rightsh   | A_width=100 |              | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/srl_349 |
|          |              | SH_width=7 |               |                       |
| r505     | DW01_add     | width=77   |               | add_1_root_gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_368_2 |
| r507     | DW01_sub     | width=76   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_372 |
| r509     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510 |
| r511     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/lte_510_2 |
| r517     | DW_cmp       | width=12   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_512 |
| r519     | DW01_add     | width=7    |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_514 |
| r525     | DW01_add     | width=7    |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_519 |
| r527     | DW_leftsh    | A_width=77 |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sll_530 |
|          |              | SH_width=7 |               |                       |
| r529     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gt_547 |
| r531     | DW01_inc     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/add_542 |
| r533     | DW01_dec     | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/sub_549 |
| r535     | DW_cmp       | width=10   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/gte_576 |
| r537     | DW01_add     | width=31   |               | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.
    i_fma/i_fpnew_rounding/add_63 |
| r1265    | DW01_add     | width=10   |               |
    add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1267    | DW01_sub     | width=10   |               |
    sub_2_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1269    | DW01_add     | width=10   |               |
    add_0_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1989    | DW01_sub     | width=11   |               | sub_1_root_gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/add_512 |
```

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| r1991    | DW01_inc     | width=12   |               | add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_512 |
| r2711    | DW01_sub     | width=10   |               | sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
| r2713    | DW01_inc     | width=10   |               | add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
===============================================================================


Implementation Report
===============================================================================
|                    |                  | Current            | Set            |
| Cell               | Module           | Implementation     | Implementation |
===============================================================================
| add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2 |
|                    | DW01_add         | pparch (area,speed)                 |
| add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                    | DW01_inc         | pparch (speed)     |                |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                    | DW01_sub         | pparch (speed)     |                |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/i_fpnew_rounding/add_63 |
|                    | DW01_add         | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325 |
|                    | DW02_mult        | pparch (speed)     | pparch         |
|                    |                  | mult_arch: benc_radix4              |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372 |
|                    | DW01_sub         | pparch (speed)     |                |
| add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
|                    | DW01_add         | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293 |
|                    | DW01_sub         | pparch (area,speed)                 |
===============================================================================

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