Advanced Design for Signal Integrity and Compliance

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IBM Deutschland Research & Development GmbH

Overview:

- Biggest Server Lab Outside The US
- Founded: 1953
- Employees:
  ca. 1.300
- Location: Böblingen

Key Competencies:

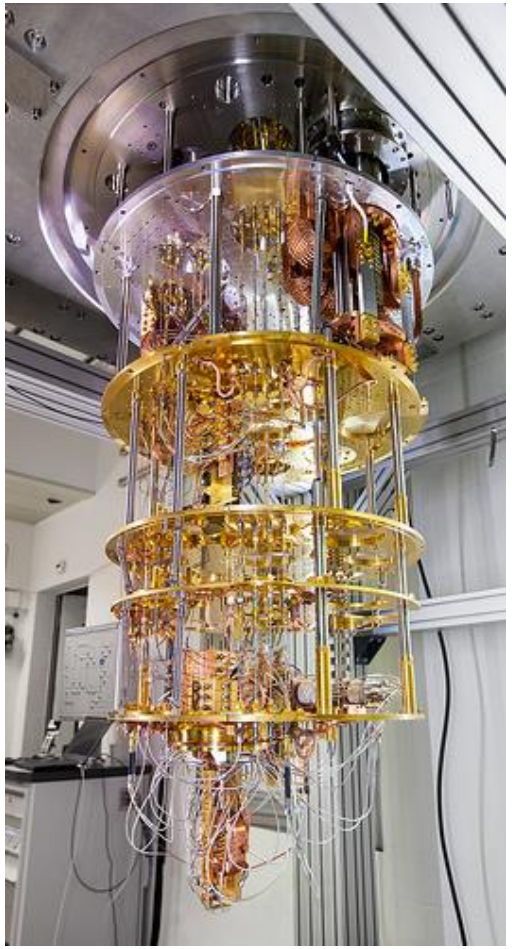
- Hardware
- Firmware
- OS
- Software
- Cloud

We Are Working On:

IBM POWER Server

IBM z Server
Linux on Z, z/OS, ZaaS

IBM Storage Products



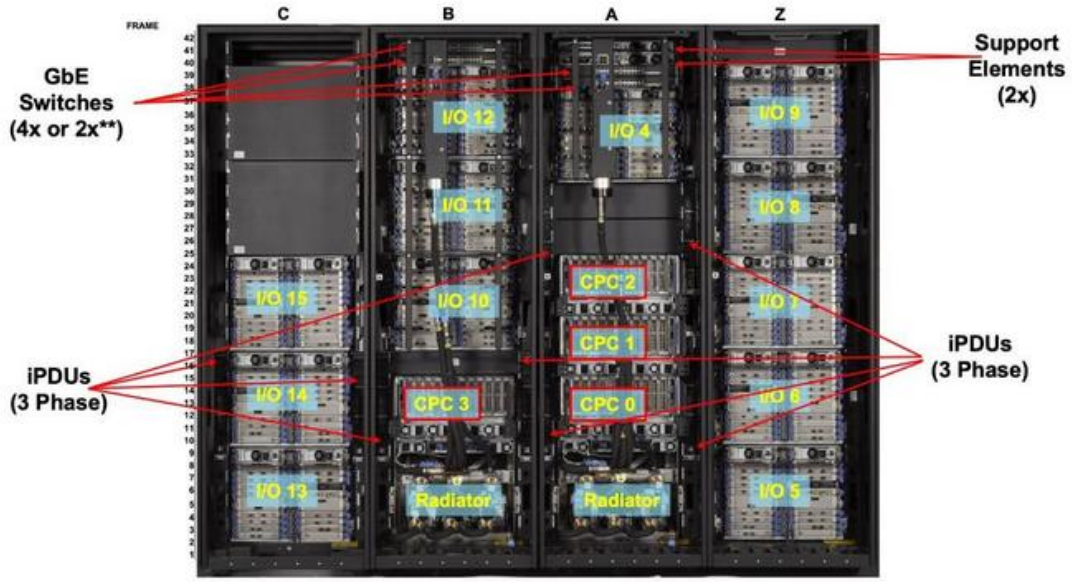
IBM Quantum Computer

Agenda

- Why is Signal Integrity and Power Integrity essential for designing modern computers
  - How does a high end server look like
  - How is this SI class related to real problems and daily business of a SI or PI engineer in development
    - Modeling and Simulation
  - Technology trends in packaging

Today’s Challenges in High End Servers

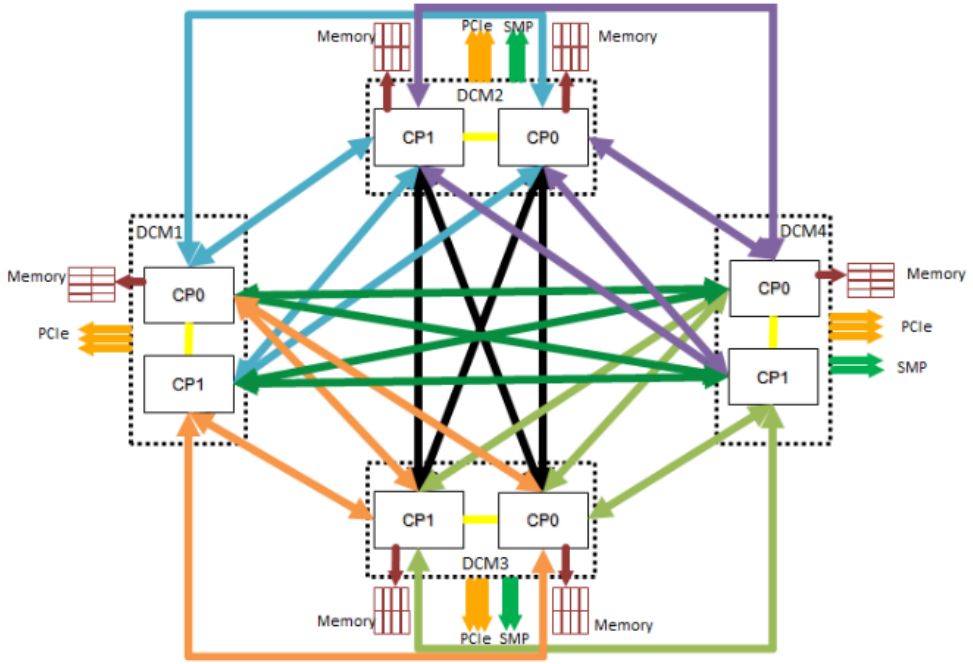
- System Architecture Design
- Chip Design
- SCM/MCM (Single/Multi Chip Module) Design
- PCB (Printed Circuit Board) Design
- Signal Integrity
- Power Integrity
- Mechanical Design
- Thermal Design
- RAS (Reliablity and Service)
- EMC (Electromagnetic compatibility)
- …

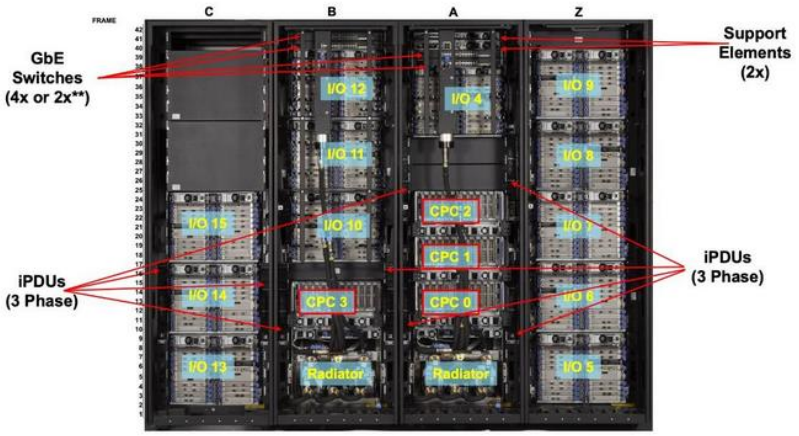


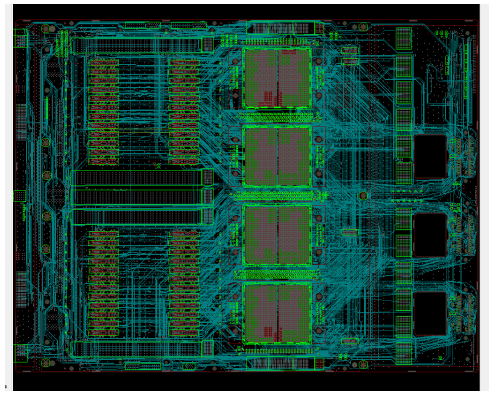
Drawer Architecture

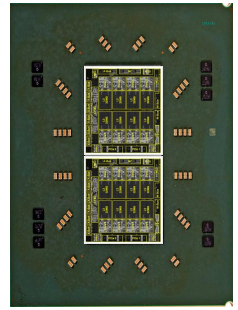
- Low latency MBUS on DCM with 226 GB/s
- Fully connected XBUS on the drawer to all other chips with 47 GB/s
- Redundant SMP to each drawer with 70 GB/s
- 48 Memory Dimms 12.8 GB/s for each Dimm
  - RAIM redundancy for group of 8 (102 GB/s)
- 12 IO slots with Gen 4 PCIE at 32 GB/s

Bandwidths are given for single direction only (double the numbers for tx+rx)



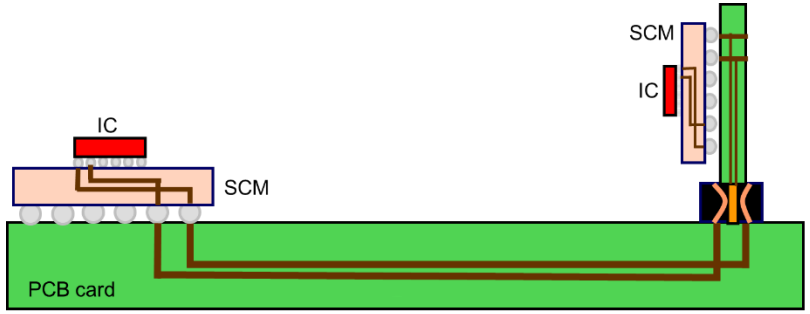




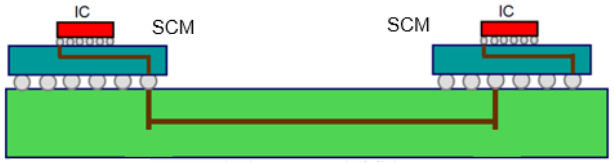


Basic Topolgies of High Speed Nets

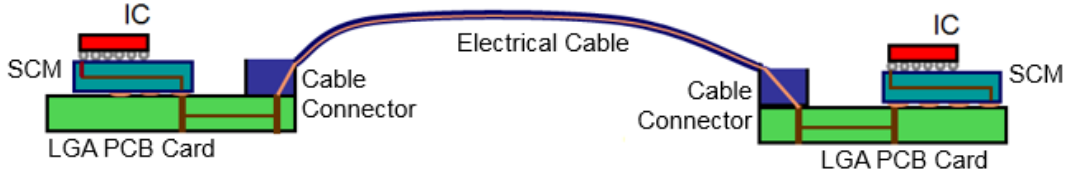
On MCM Signal Connection



On Drawer Memory Signal Connection



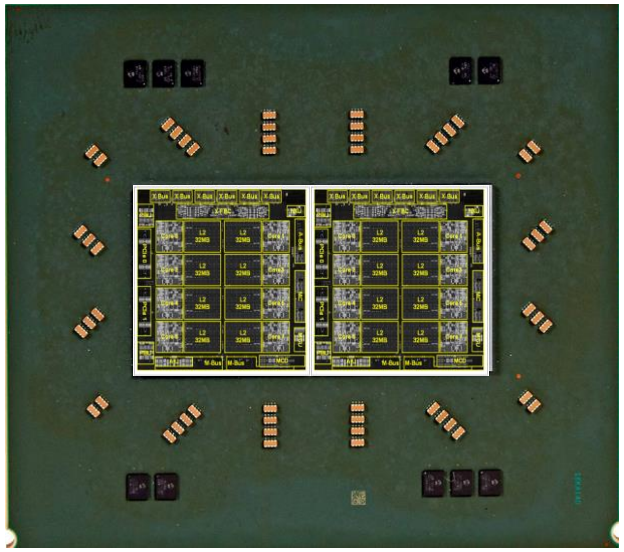
On Drawer Signal Connection

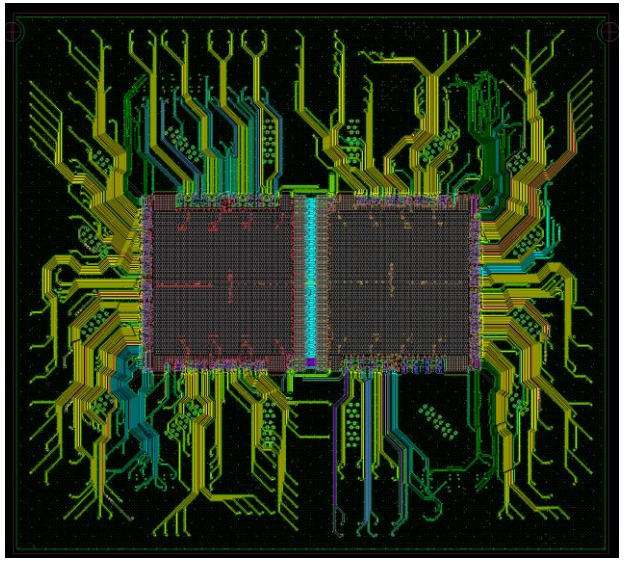


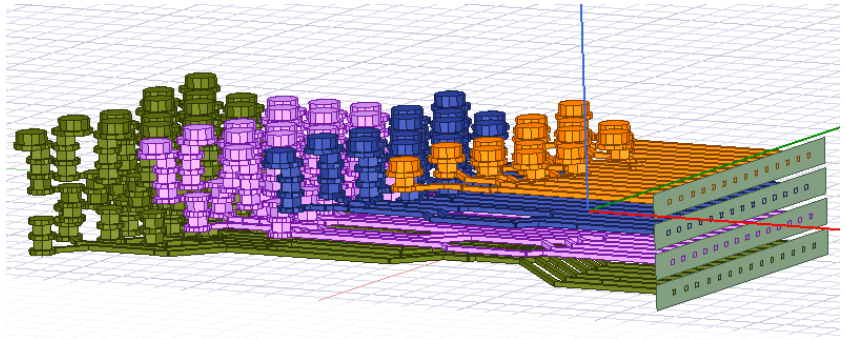
Drawer to Drawer Signal Connection

DCM and Chip

- 8 processor cores running at 5.2GHz in 7nm technology
- 1060 mm^2 chip area with 22.5 Billion transistors per DCM
  - Digital modeling
  - Analog modeling for IOs, PLL, voltage regulators
- Dual Chip Module 79.0 mm x 71.5 mm
- MBUS with 1388 data lanes at 2.6Gb/s
- Synchronous chip operation

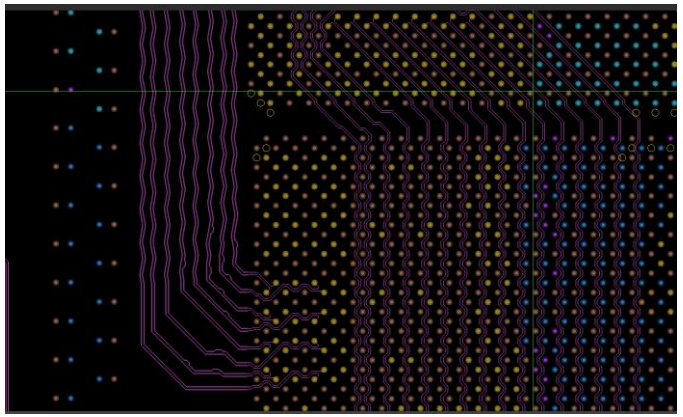


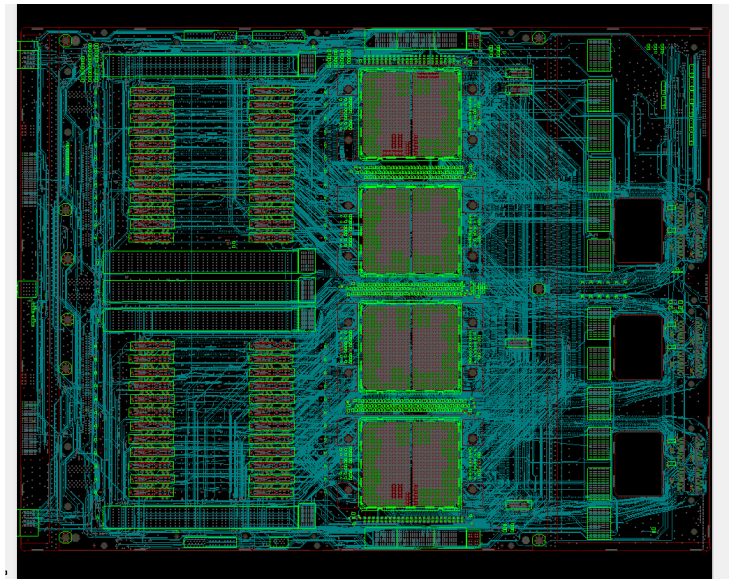




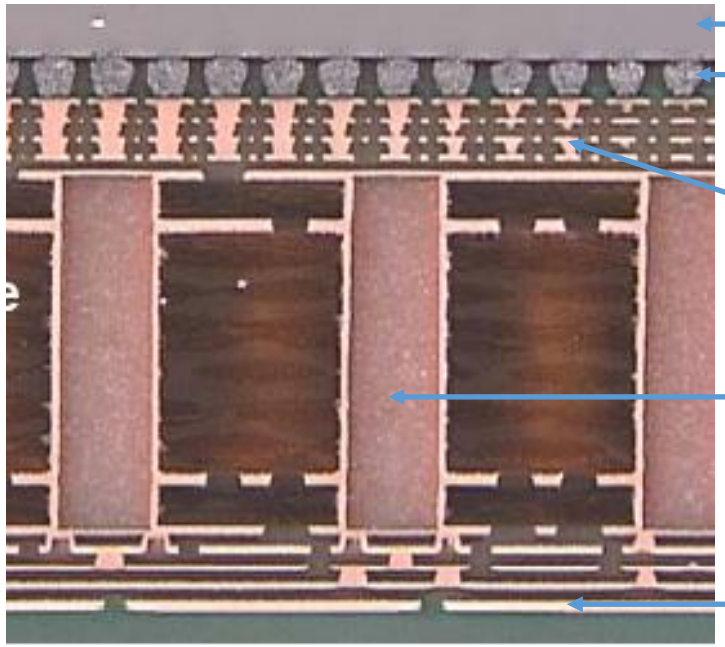
Processor Board

- 40 layer PCB (12S26P2MP) at 434 mm x 486 mm
- Trace lengths 1177 m
- 26918 Vias
- LGA with 4753 IOs at 1.5mm interstitial for Processor DCM
- Redundant 4000 W max power capability
- 20 voltage domains
- Redundant water cooling of processors





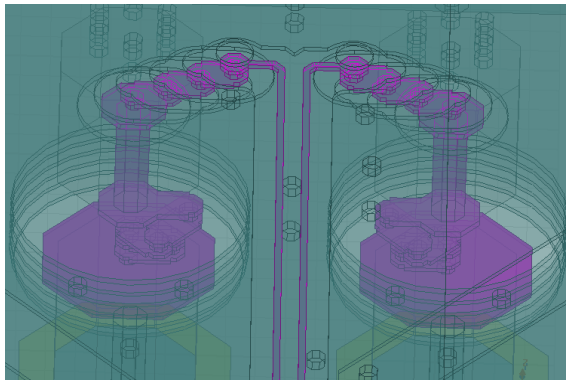
Chip Substrate Modeling

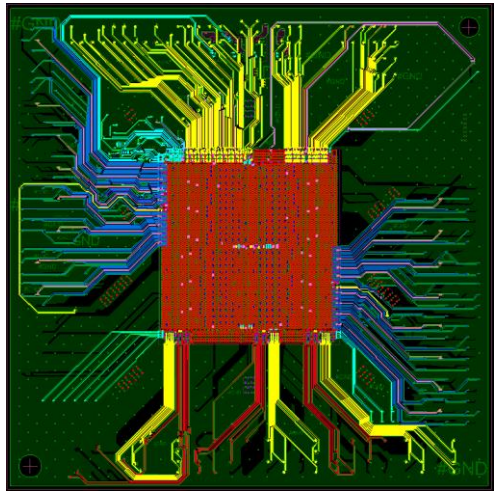


chip
C4
Top layers
uVia

RFP: Resin filled PTH
(plated through hole)

Bottom layers
BSM (bottom surface metal)



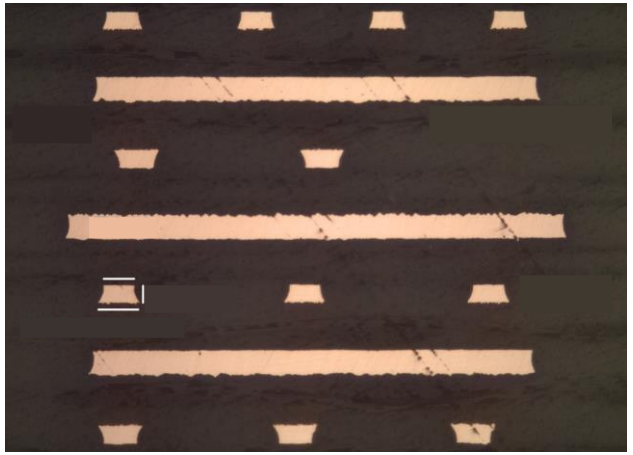


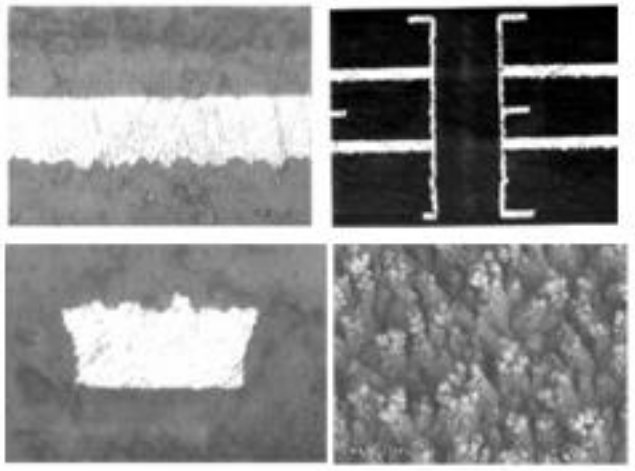
Power delivery: Current per plane, u-via, RFP or LGA
Signal integrity: impedance, shielding and spacing for minimizing cross talk, ...

Processor Board Cross Section

Cross section:

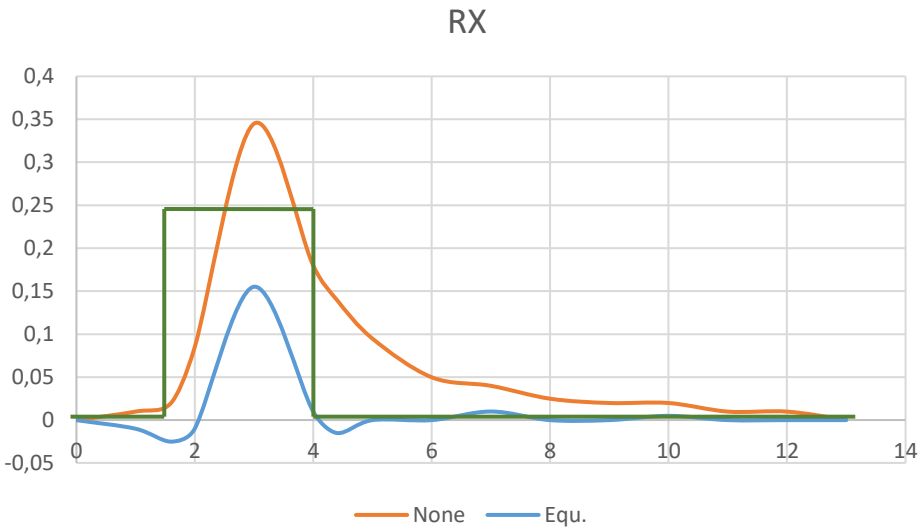
- **Underetching leads to nonrectangular lines**
- **Copper smoothness important for skin effect due to increasing attenuation**
- **Material choice depending on attenuation budget**
  - **Standard loss material**
  - **Low loss material**
  - **Ultra low loss material**
- **Hybrid designs for cost reduction**





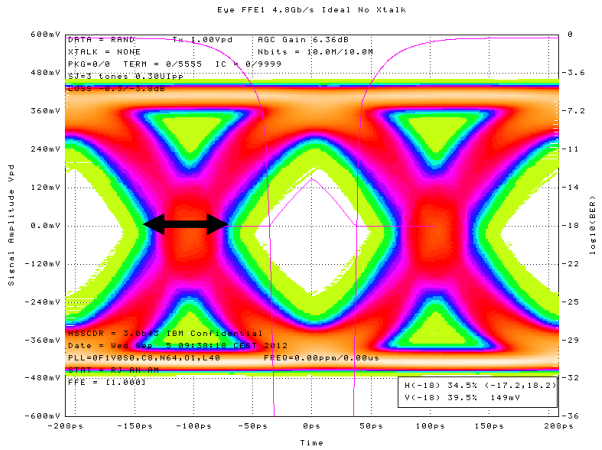
IO Compensation Techniques

- **TX Side**
  - FFE (Feedback Forward Equalization)
    - Amplifies or weakens the output level depending
    - on the previous pattern
  - Boost
    - Small output level increase for a short bit time



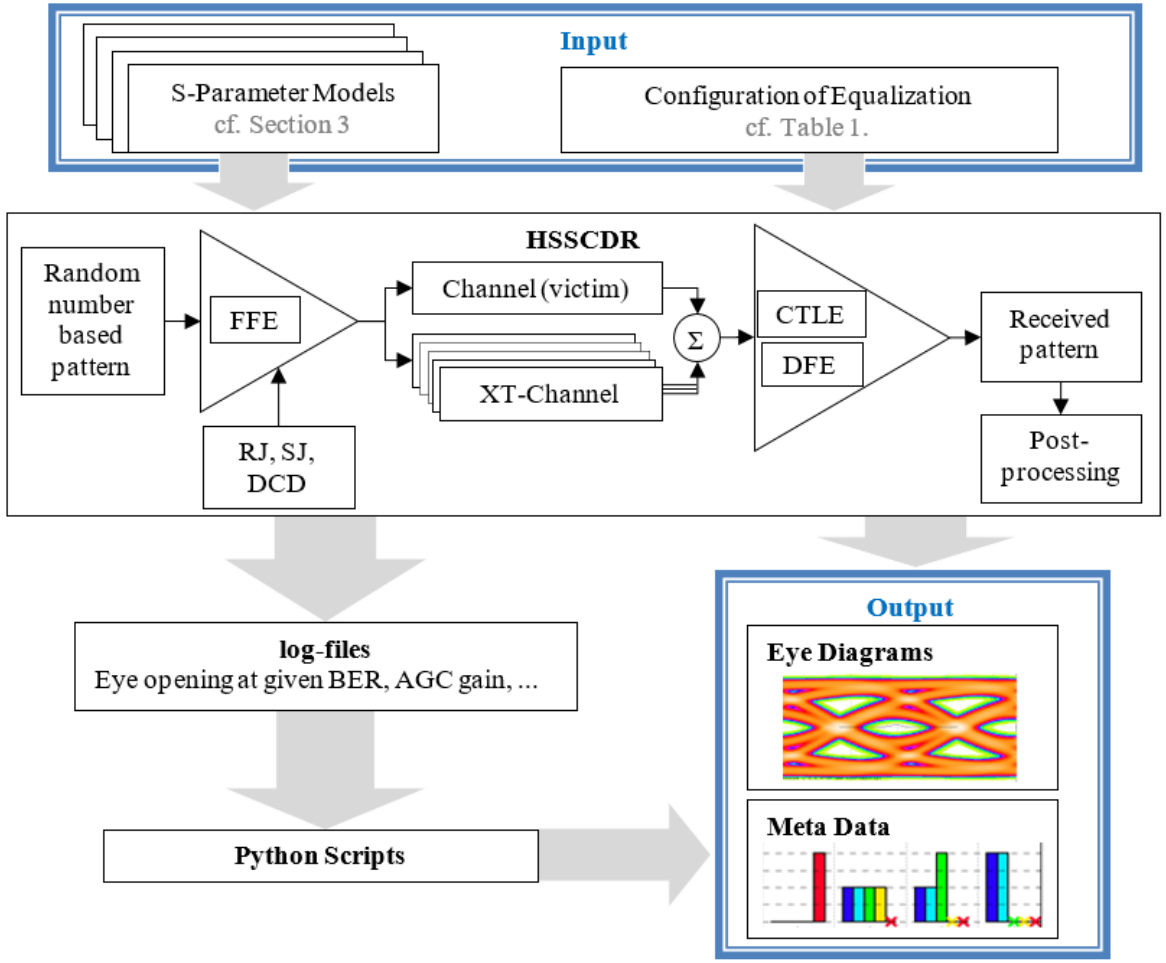
- **RX Side**
  - DFE (Decision Feedback Equalization)
    - Moves the RCV threshold level depending on the previous pattern
  - CTLE (Continuous Time Linear Equalization or Peaking)
    - Linear frequency bandpass filter to compensate for the channel transfer function
    - represents the inverse filter function of the channel
    - „no notches“ in the transfer function

Jitter

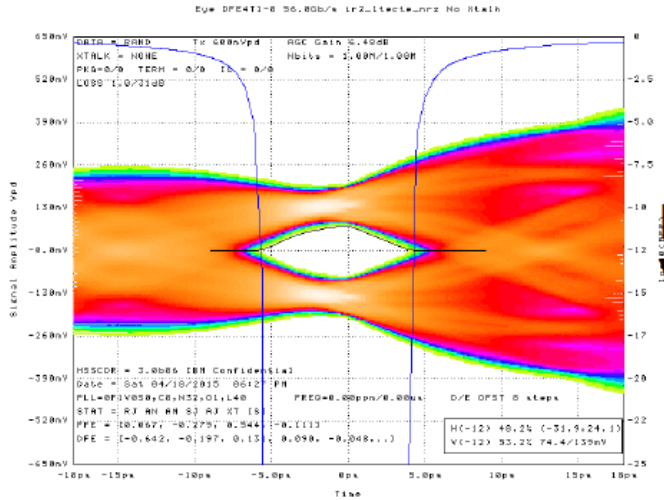


- Jitter is defined as the variation of the signal edges crossing the center of the eye
- Jitter can be caused by
  - Duty cycle distortions of clock signals
  - Power noise
  - Wiring Skew
  - ISI
  - Different Rise/Fall transitions

Simulation Flow



Signal Integrity



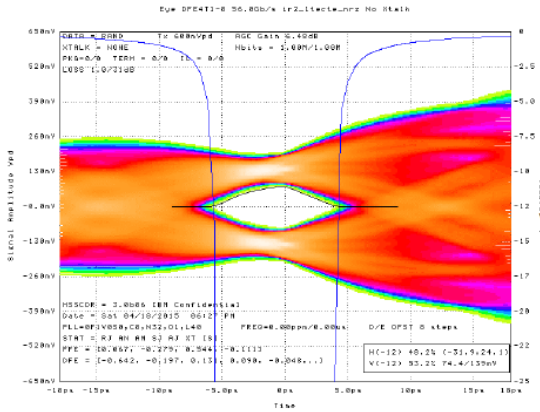
BER=10^{-12}

H: 48%
V: 74mV

ISI only

Equalizer:
CTLE
FFE: 5 taps
DFE: 12 taps

Signal Integrity



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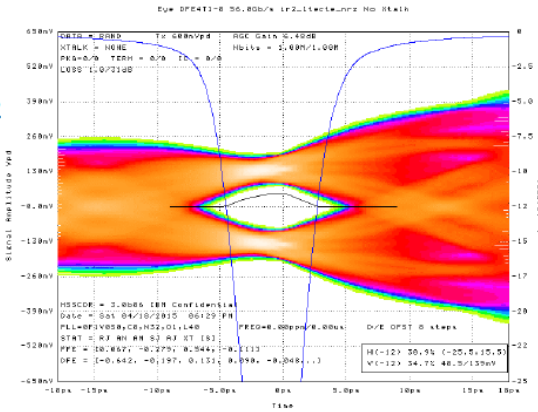
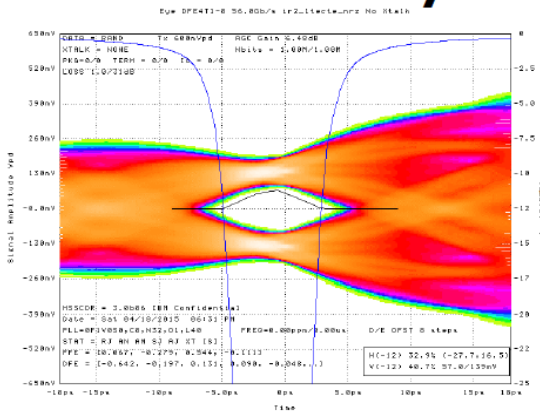
ISI only



H: 31%
V: 49mV

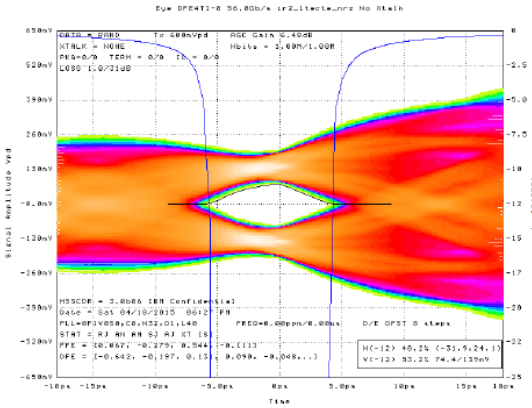
+Noise



H: 33%
V: 57mV

+Jitter

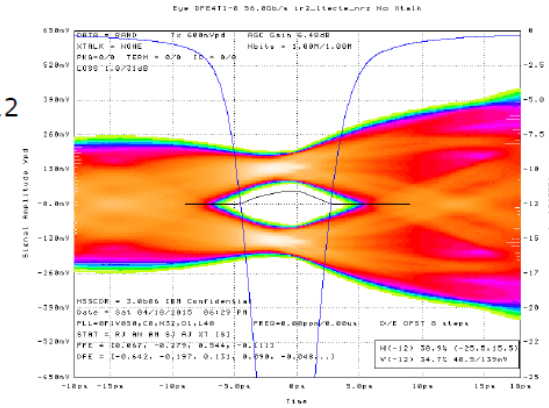
Signal Integrity



BER=10^{-12}

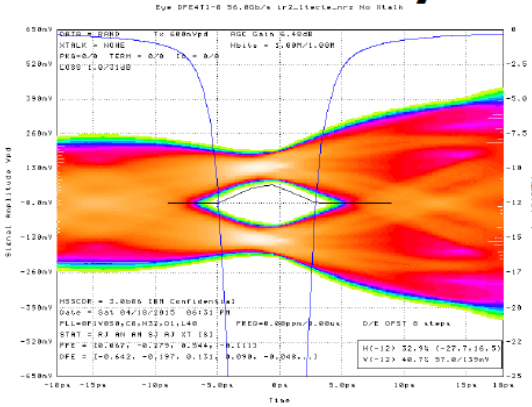
H: 48%
V: 74mV

ISI only



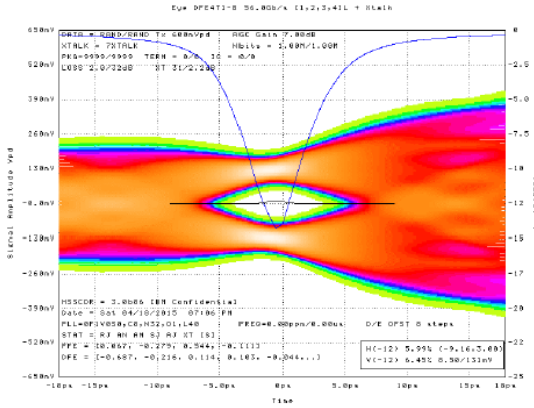
H: 31%
V: 49mV

+Noise



H: 33%
V: 57mV

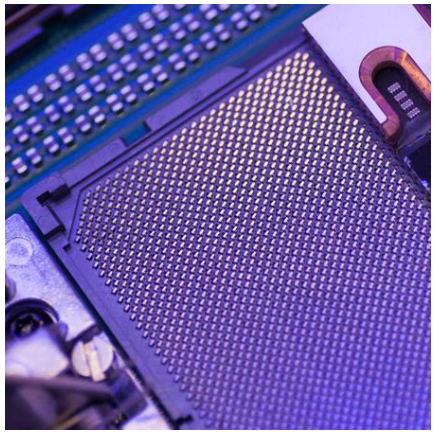
+Jitter



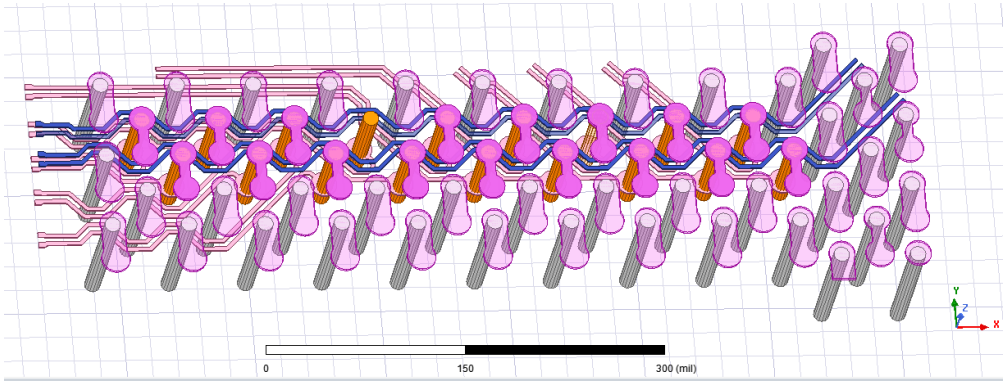
H: 6%
V: 9mV

+Noise+Jitter+X-talk

Signal Integrity – Impedance Discontinuities

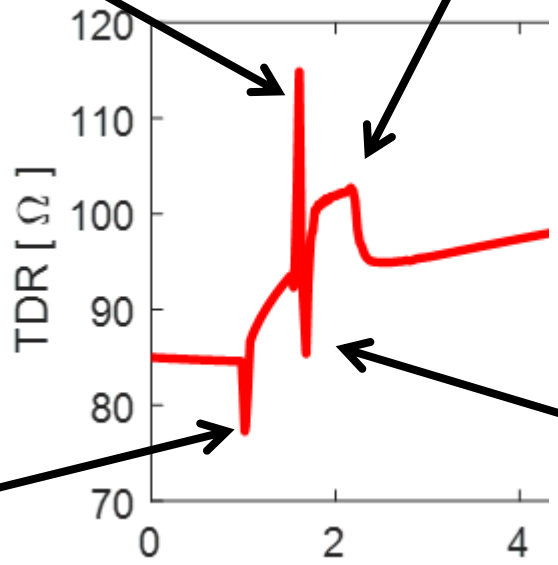


Socket pin



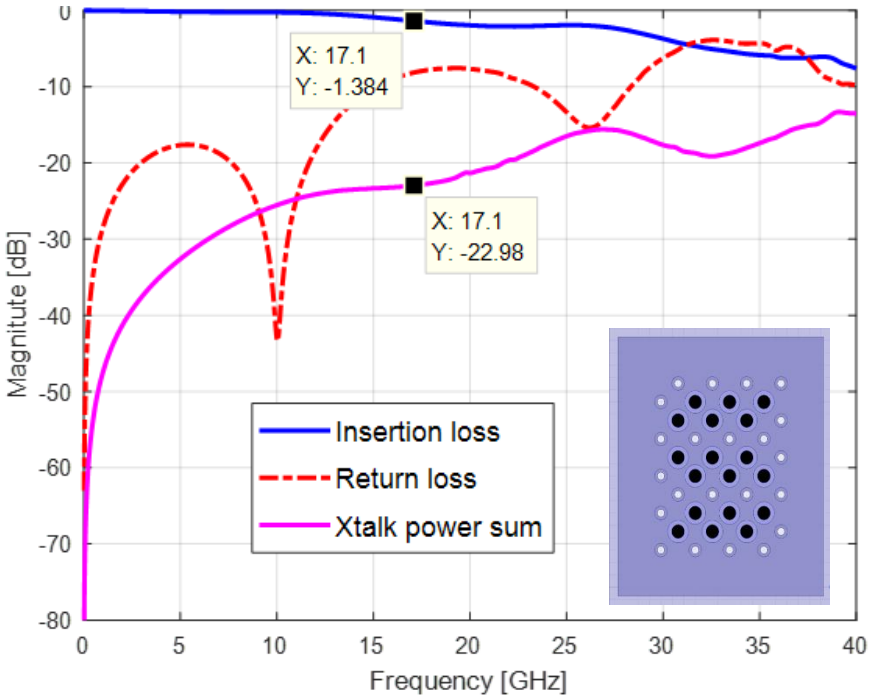
Module escape

C4 escape

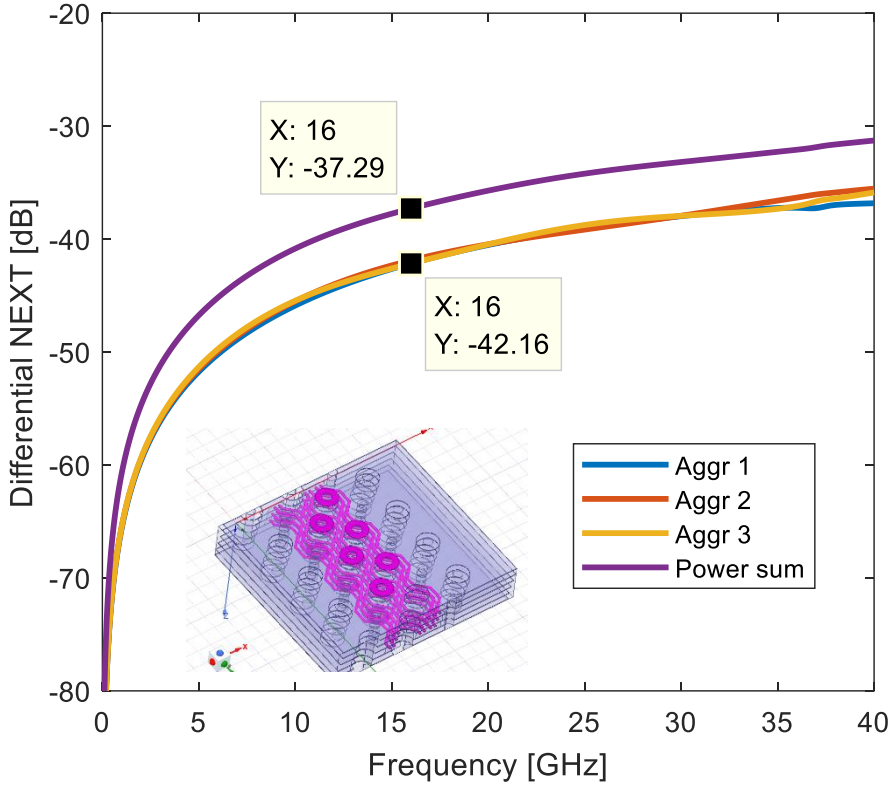


Though hole via

Signal Integrity - Crosstalk



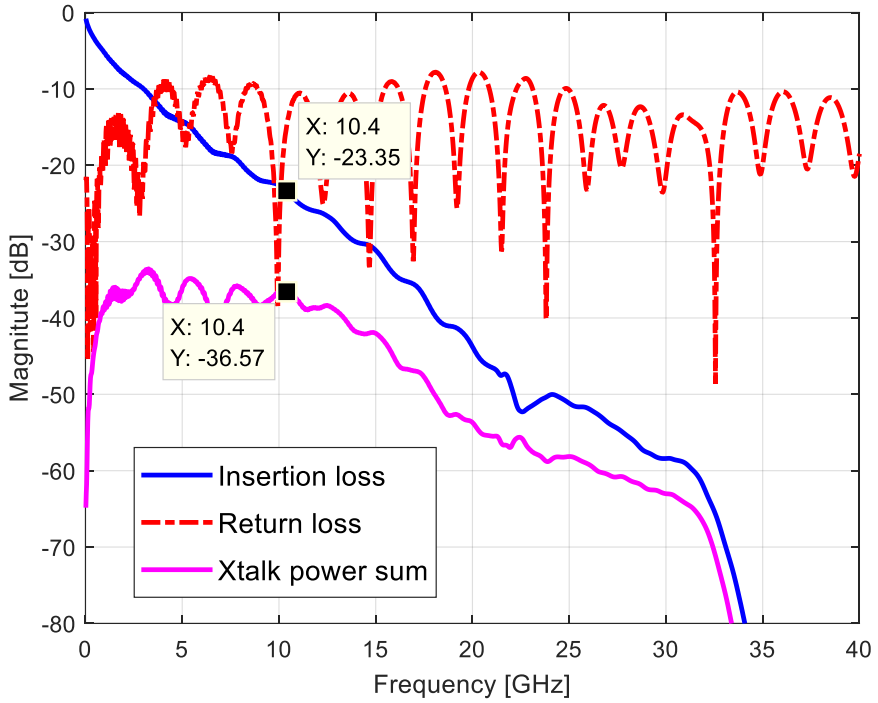
Via far-end crosstalk from 8 neighbors

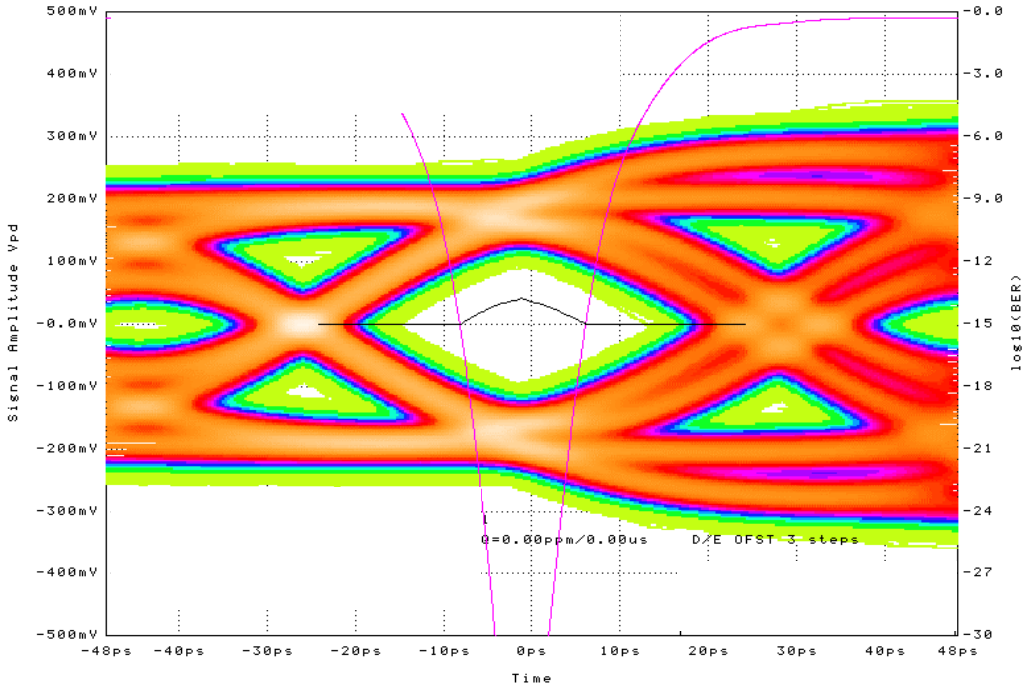


Via to trace near-end crosstalk

Most significant crosstalk sources are the vertical connections.

Running XBUS at 20.8 Gbps





Insertion Loss @10.4GHz = 23.4 dB

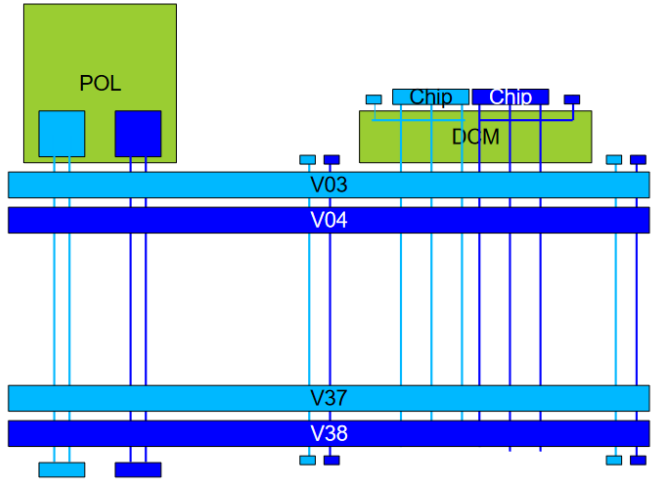
Signal to Crosstalk Ratio @10.4GHz = 13.2 dB

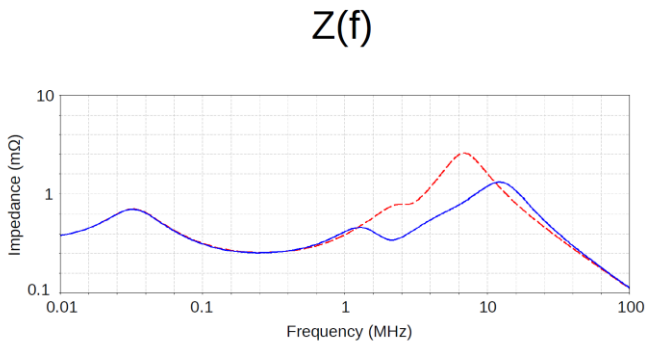
Heye = 29.3%, Veye = 41mV

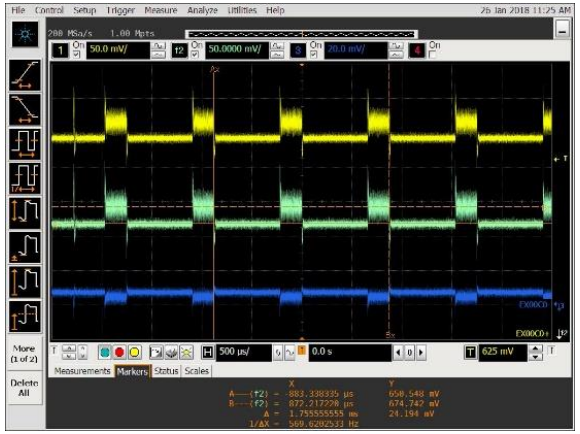
- TX: FFE (Feed-Forward Equalization)
- RX: DFE (Decision Feedback Equalization)
- RX: CTLE (Continuous Time Linear Equalization)

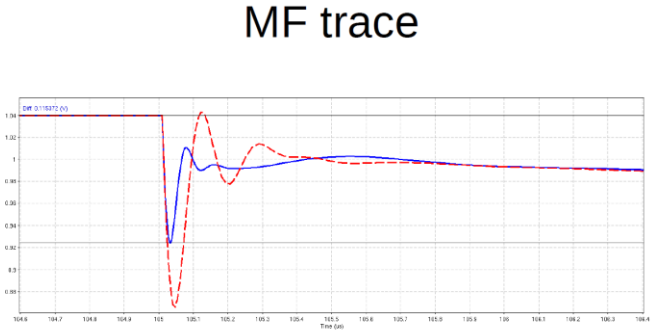
Power Integrity

- Challenges
  - 12V PSUs, 4000W
  - DCM up to 480W
  - 240A per chip
  - Delta I ~120 A within nanoseconds
  - Limited voltage tolerances
  - Physically fitting capacitors
  - Z(f) = 0
- Decoupling Importance
  - Device functionality
  - Device reliability
  - Yield vs power vs performance
- Trends
  - Integrated/embedded capacitors
  - Advanced power management





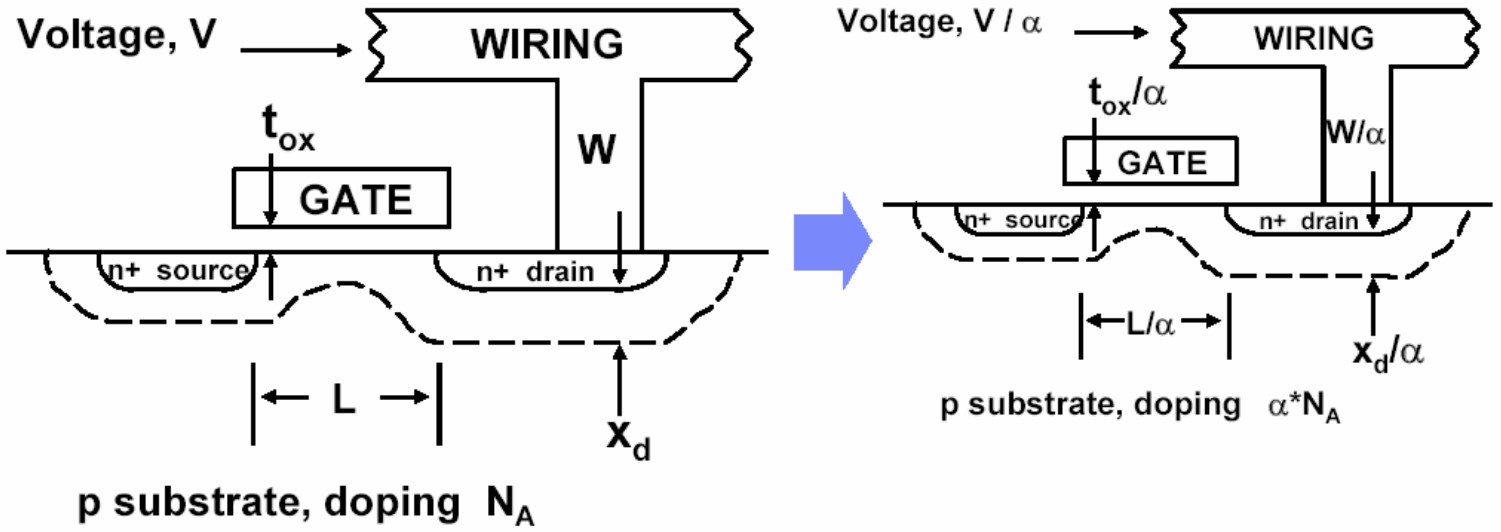




CMOS Scaling

Transistor Scaling

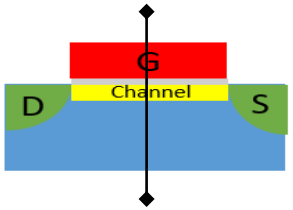
Dennard, et al., 1974



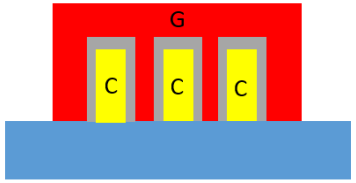
RESULTS:

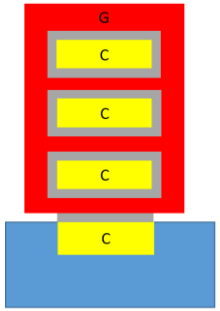
Higher Density:	α^2
Higher Speed:	α
Lower Power:	$1/\alpha^2$
per circuit	
Power Density:	Constant

Chip Technology



- Continued shrinking of transistor geometries in chip technologies
  - Traditional FET (> ~22nm)
  - FinFET (~22nm, ... ~5nm)
  - Nanosheets with Gate-All-Around (~3nm, ...)
    - ~50% less power, 45% area improvement, 30% performance improvement

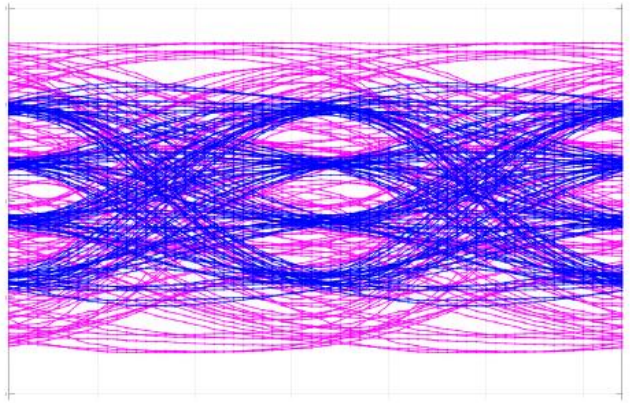




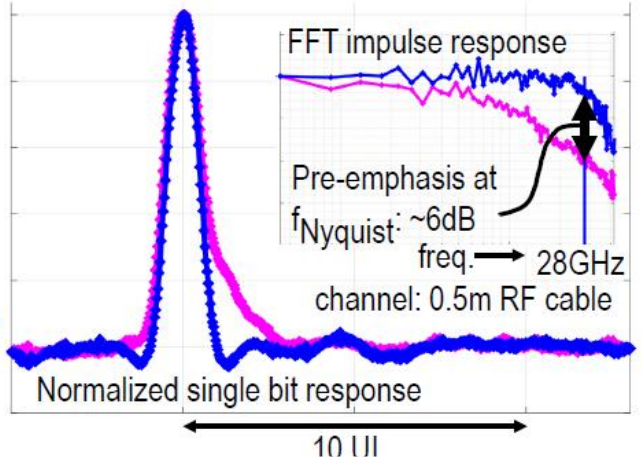
May 15, 2019 by Yongjoo Jeon, https://news.samsung.com/global/editorial-making-semiconductor-history-contextualizing-samsungs-latest-transistor-technology

High Speed IO Trends

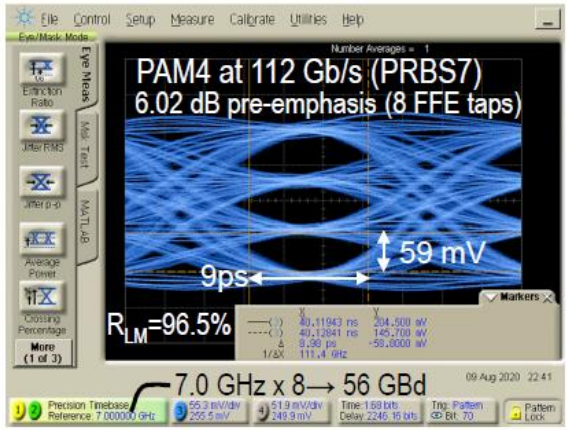
Exemplary deconvolution at 56 GBd

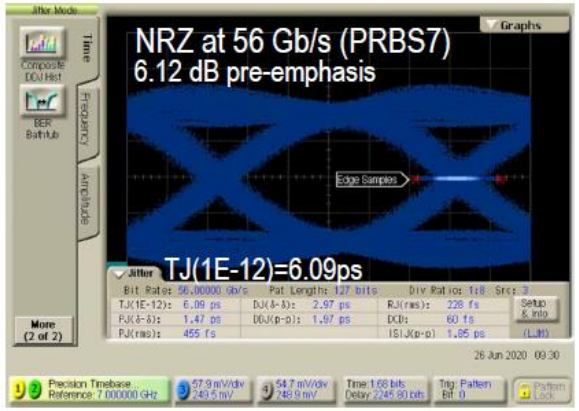


Sampled scope data processed with Octave



pink: unequalized,
blue: equalized

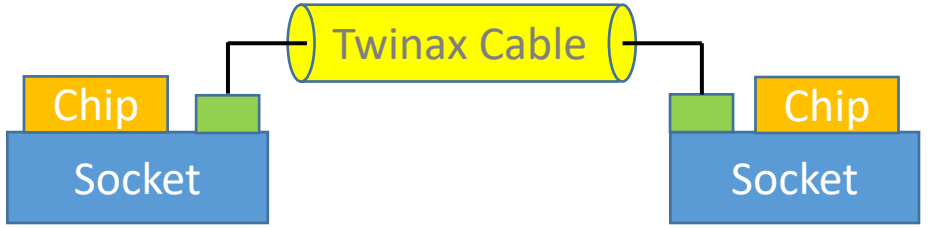


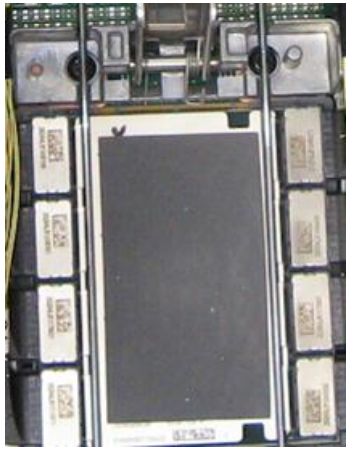


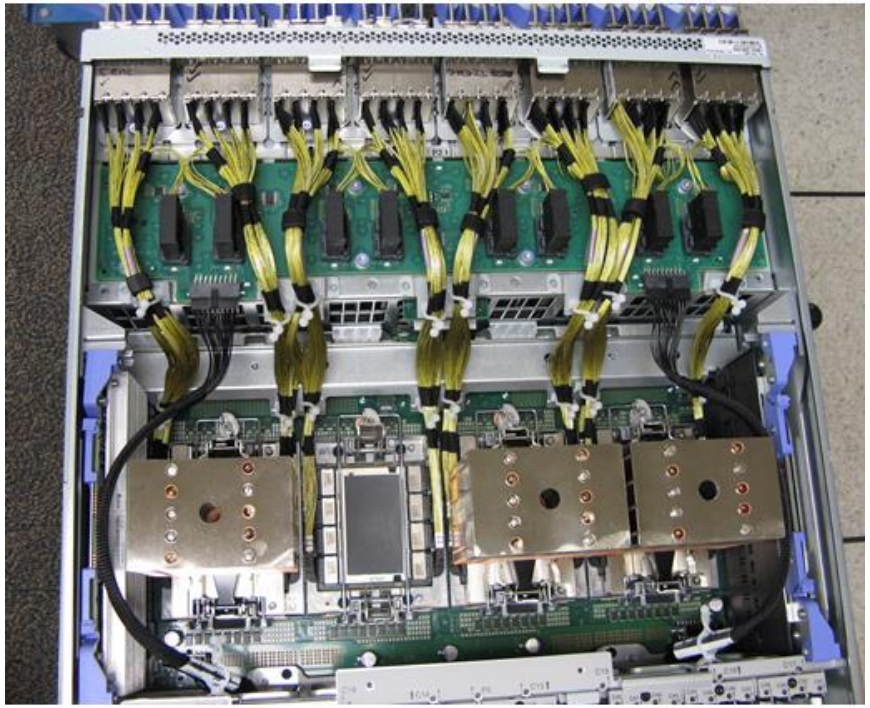
ISSCC 2021, Marcel Kossel & others, An 8b DAC-based SST TX using metal gate resistors with 1.4pJ/b efficiency at 112Gb/s PAM4 and 8-taps FFE in 7nm CMOS

System Integration Technologies

Electrical cabling between chip carriers
- Bypass loss and crosstalk of PCB
- Better shielding properties
- High speeds at low costs







Summary

- SI and PI are essential for enabling high data bandwidths
  - Requires detailed modeling and simulation techniques
  - Si class should give you an better imagination about the job of a SI/PI development engineer
- Technology and bandwidth scaling will continue and provide increased performance
  - Nanotechnology will lead to denser devices requiring more detailed modeling
  - High speed IOs will continue to increase speed
  - Heterogeneous system integration will continue to get increased importance
- The future for packaging engineers is bright