

Advanced Design for Signal Integrity and Compliance

Stefano Grivet-Talocia, Paolo Manfredi
Dept. Electronics and Telecommunications
Politecnico di Torino, Italy

stefano.grivet@polito.it, paolo.manfredi@polito.it

IBM z16

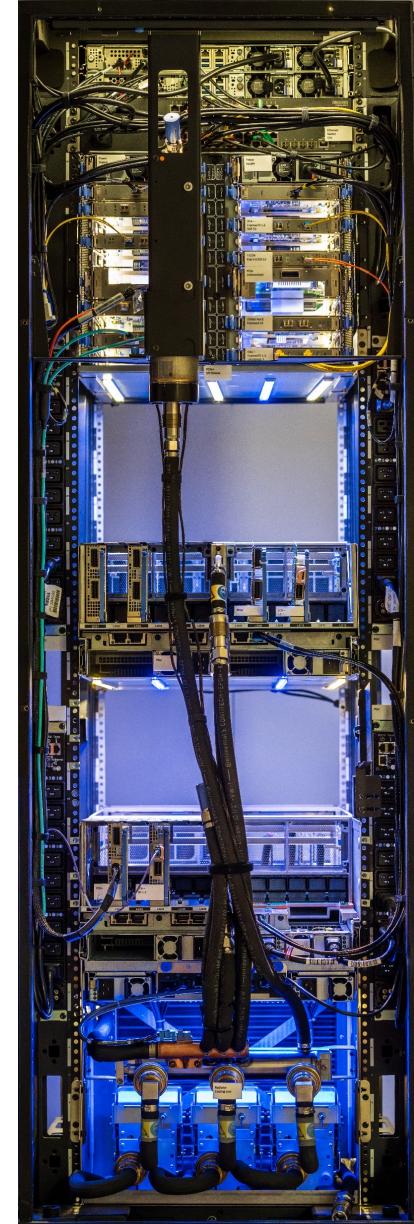
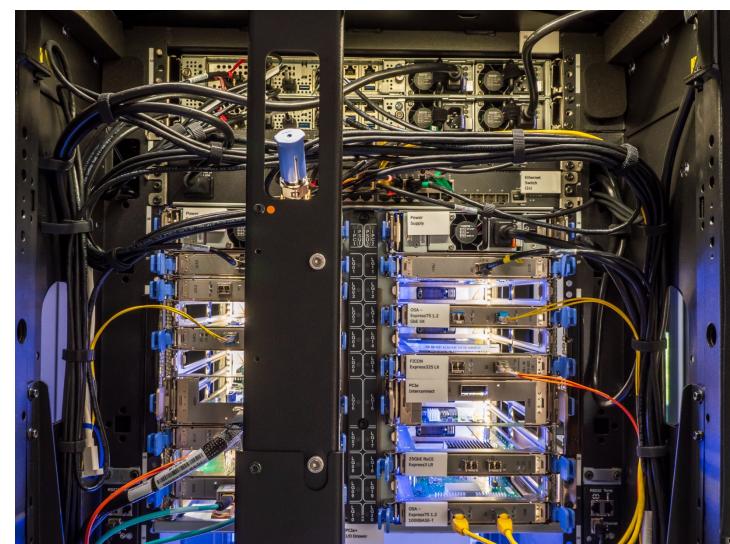
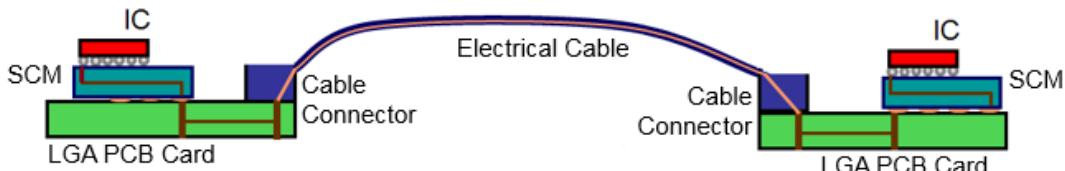
Signal Integrity Testcase

Courtesy: Xiaomin Duan, Hubert Harrer, IBM R&D Germany

Stefano Grivet-Talocia, Paolo Manfredi
Dept. Electronics and Telecommunications
Politecnico di Torino, Italy

stefano.grivet@polito.it, paolo.manfredi@polito.it

The IBM z16 Mainframe System

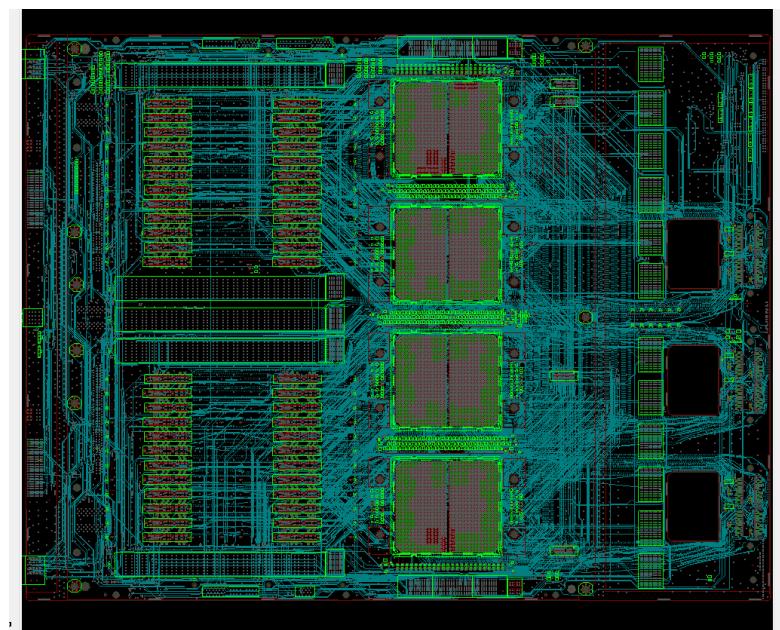


Source: IBM

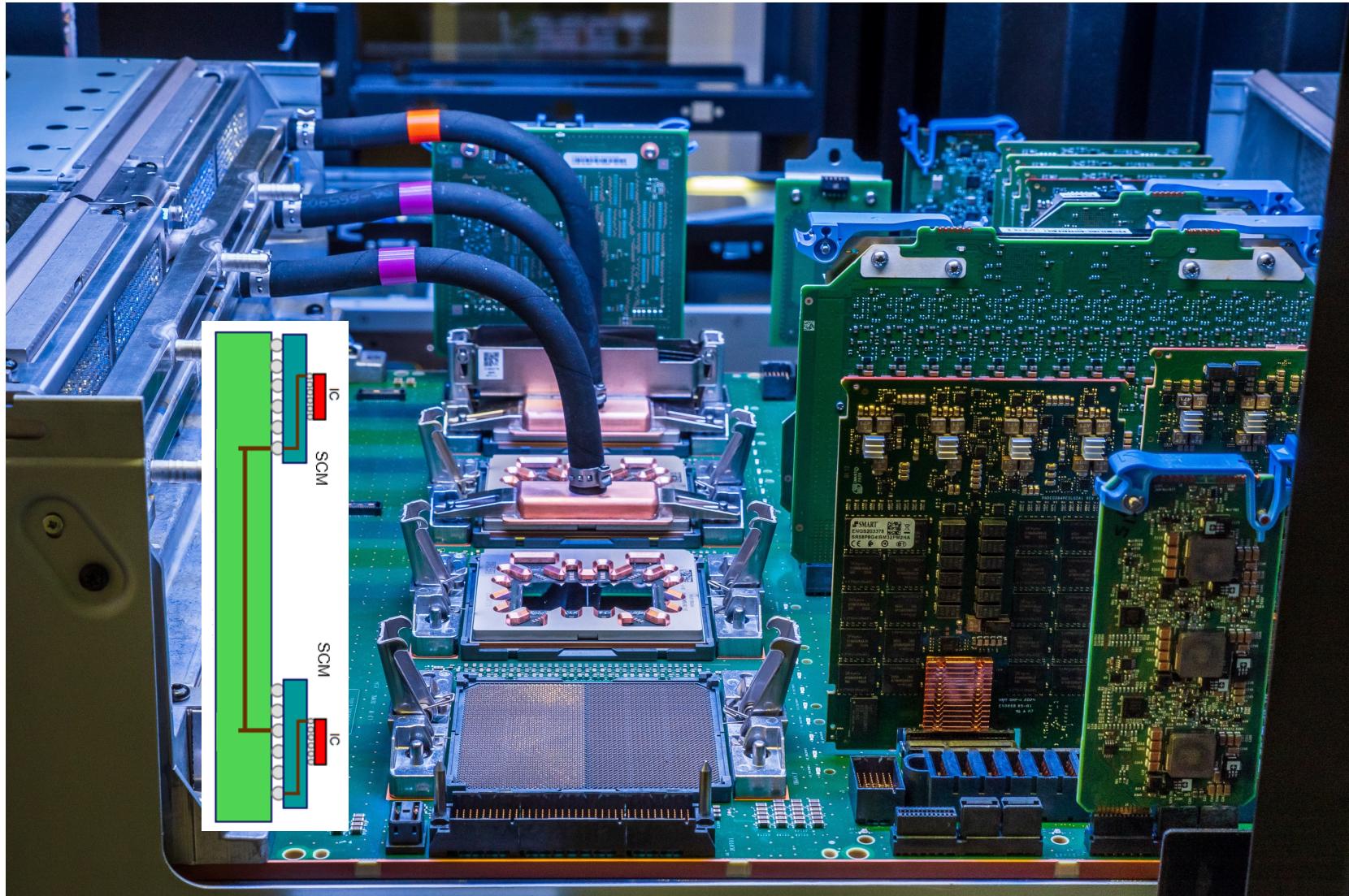
The IBM z16 Mainframe System



Source: IBM

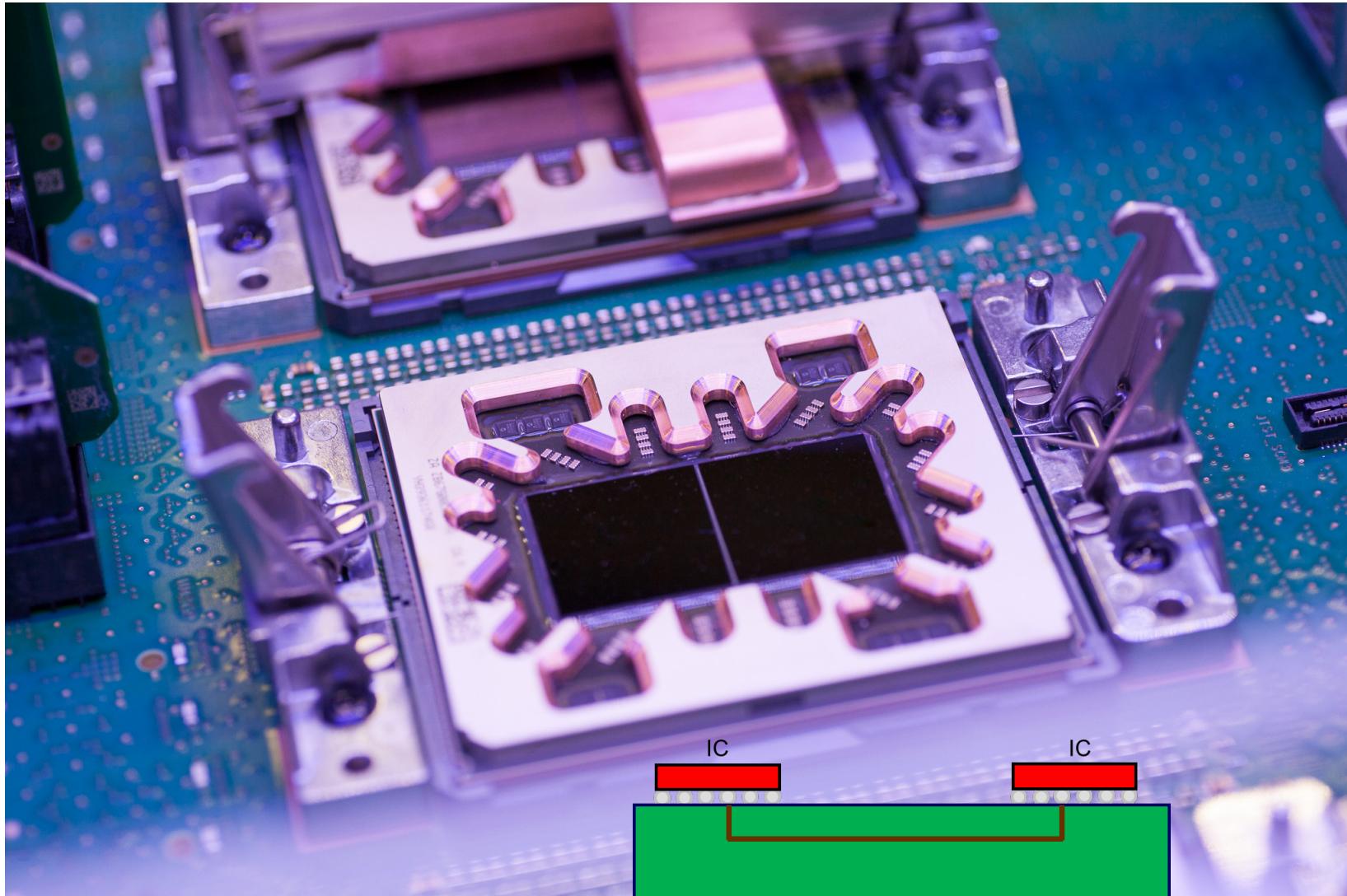


The IBM z16 Mainframe System



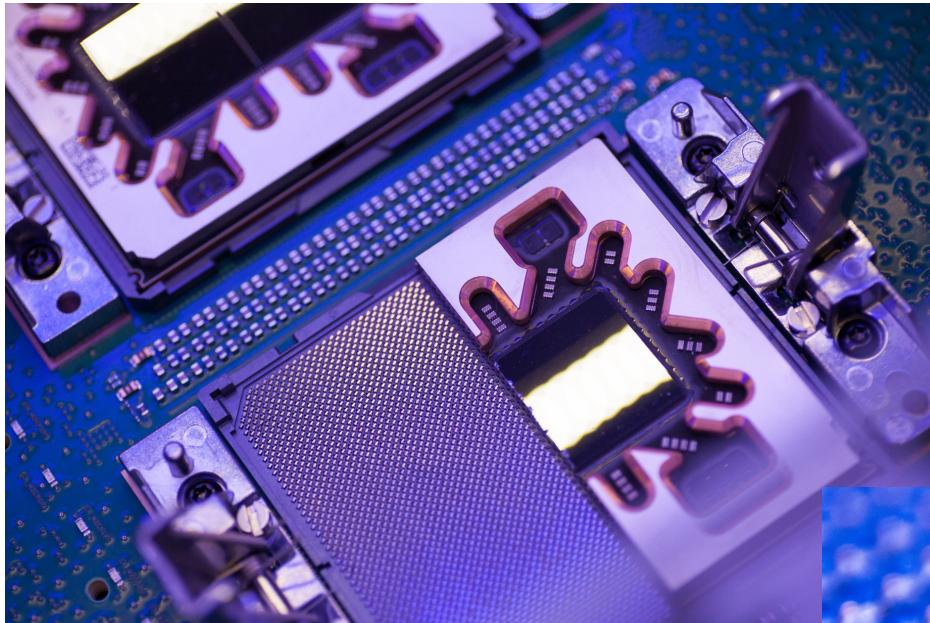
Source: IBM

The IBM z16 Mainframe System

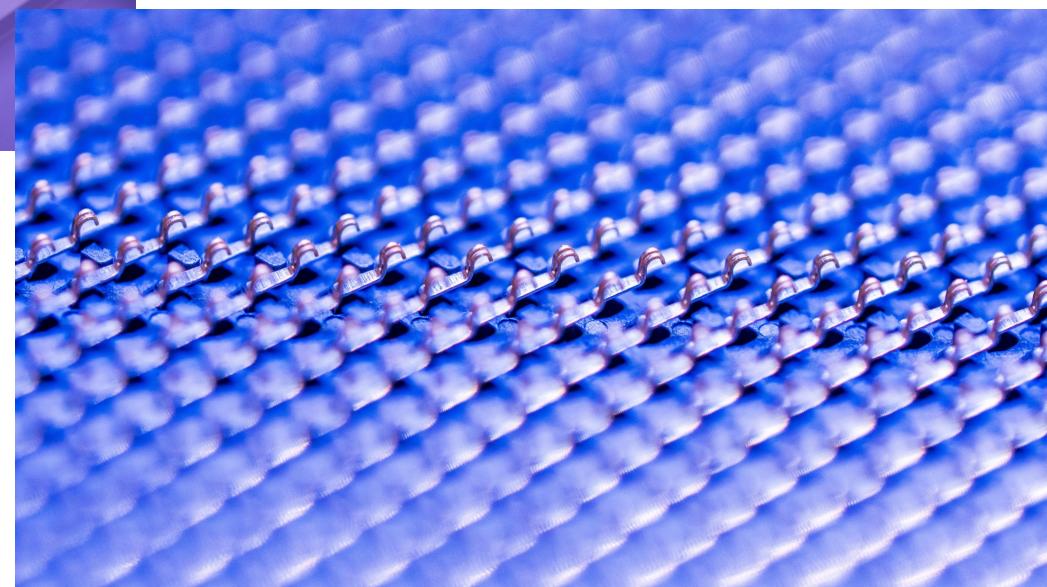


Source: IBM

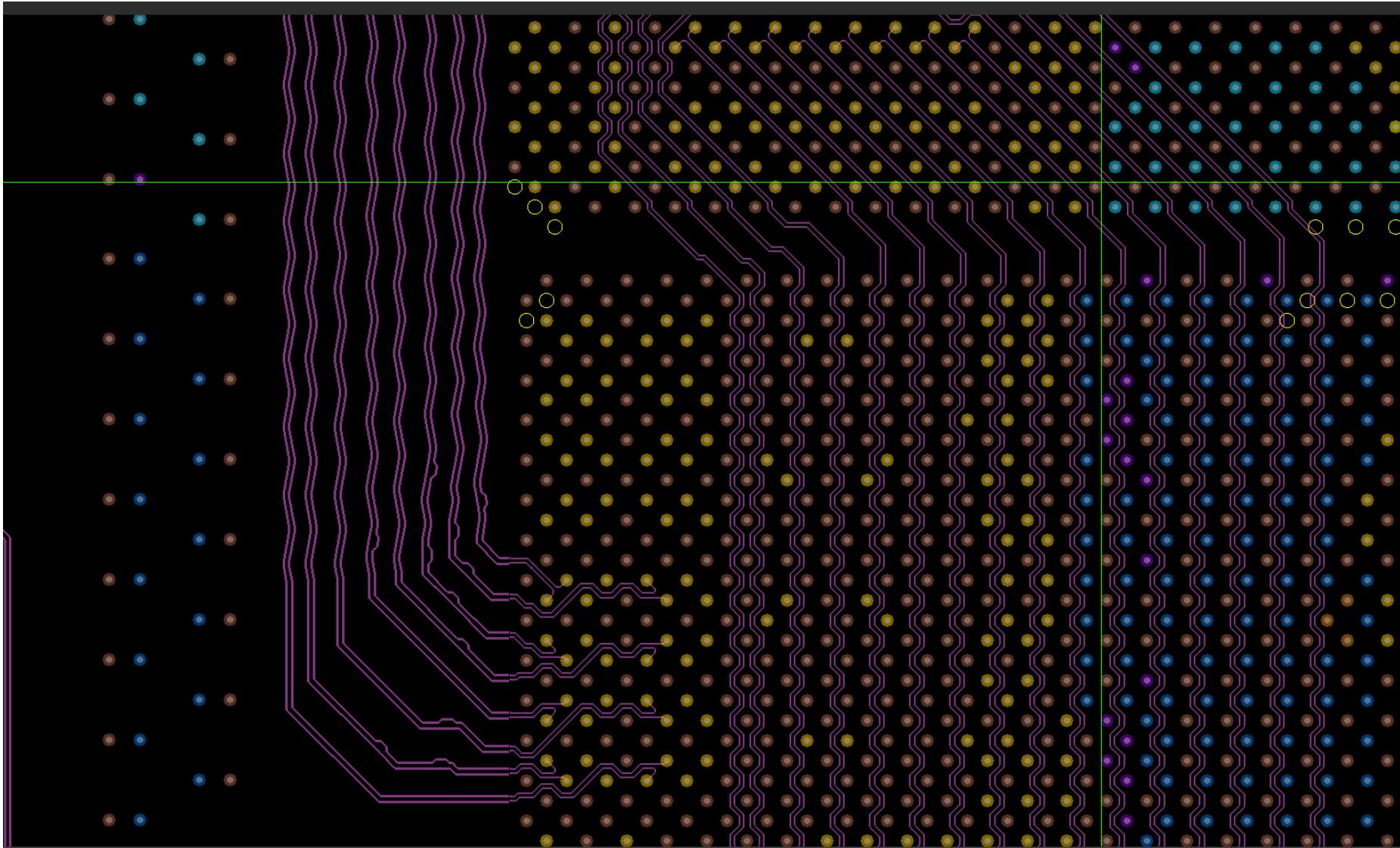
The IBM z16 Mainframe System



Source: IBM



The IBM z16 Mainframe System



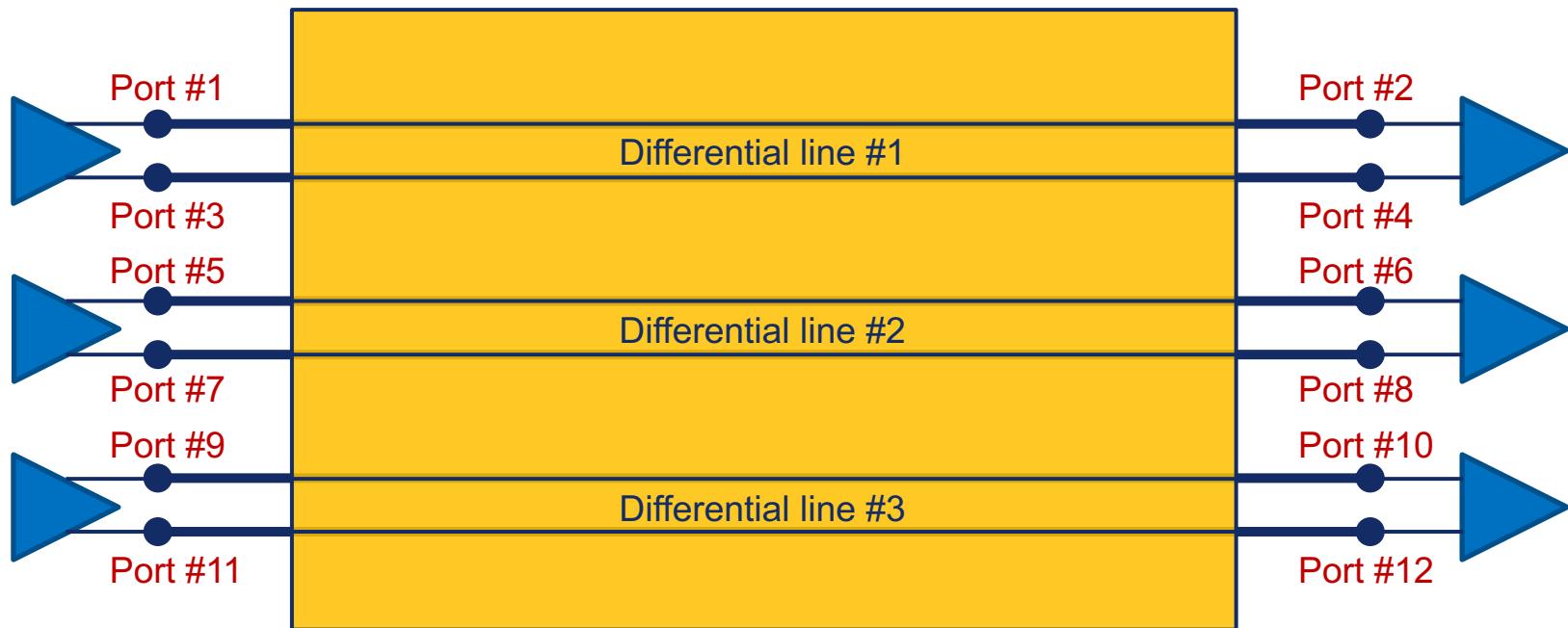
Source: IBM

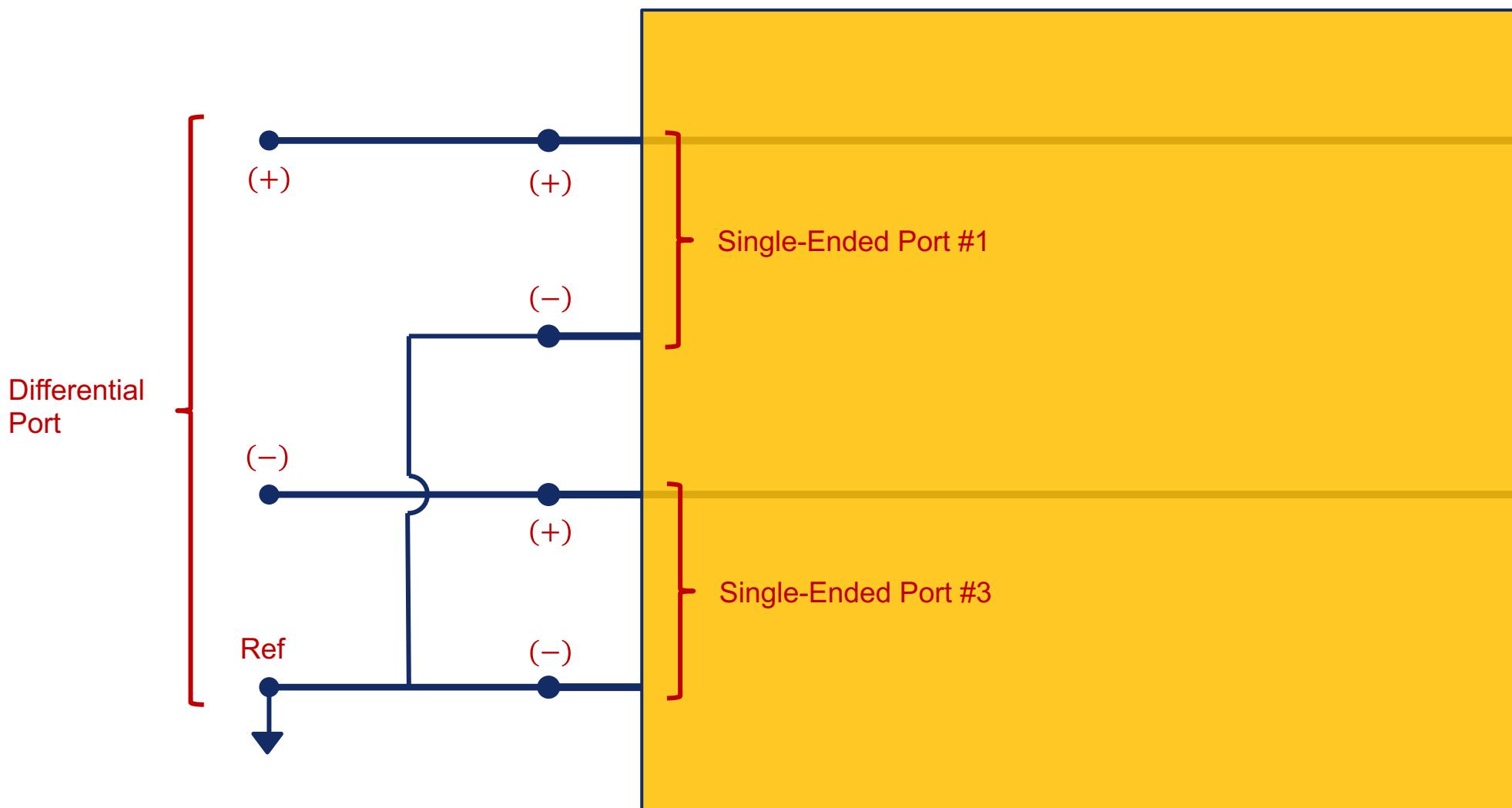
Three coupled differential lines for two different topologies

- Chip-to-chip path routed through module
- Chip-to-chip path routed through package and board
- Various interconnect length and material configurations
- Electrical models available for all parts (from real design!)

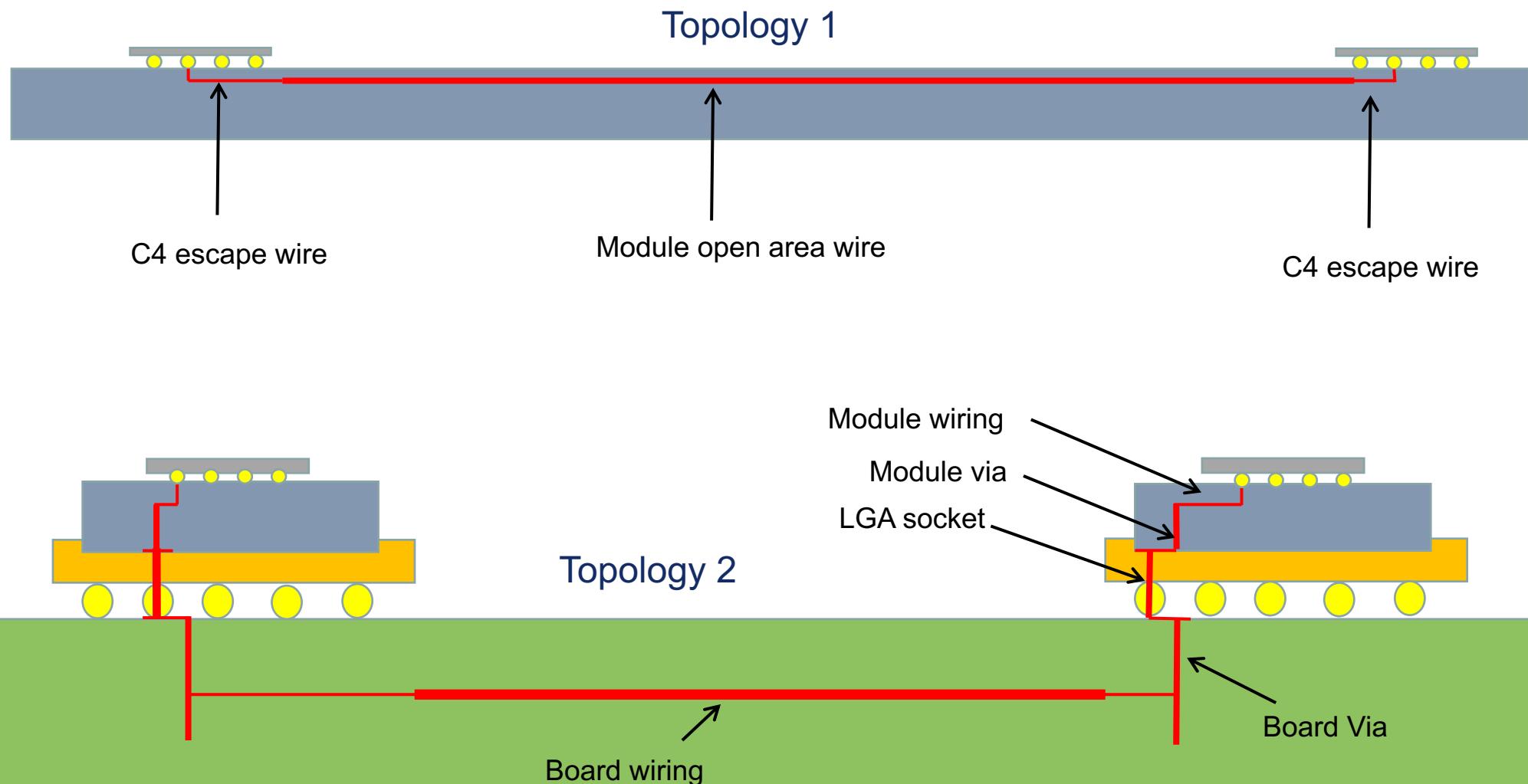
Objectives

- Perform frequency-domain and time-domain analysis
- Investigate influence of material and interconnect length
- Investigate effects of via stubs
- Experiment with equalization schemes: TX-FFE, RX-CTLE and RX-DFE
 - improving eye diagram and push transmission to higher speed
- All simulations to be done in LTSPICE and MATLAB

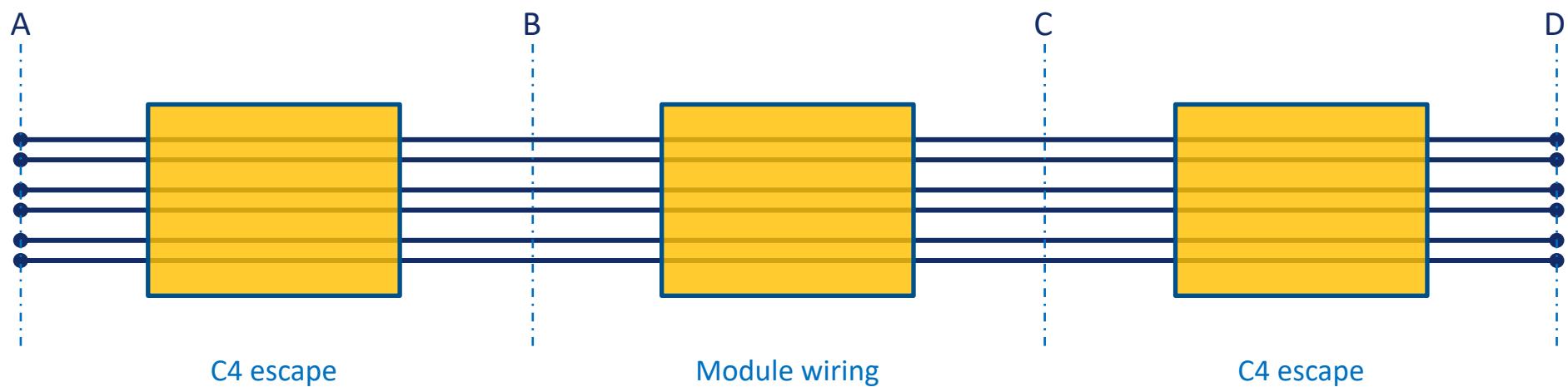
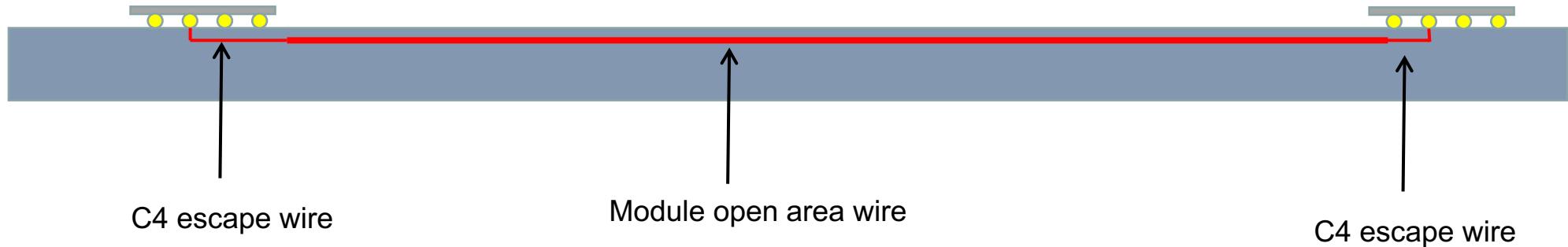




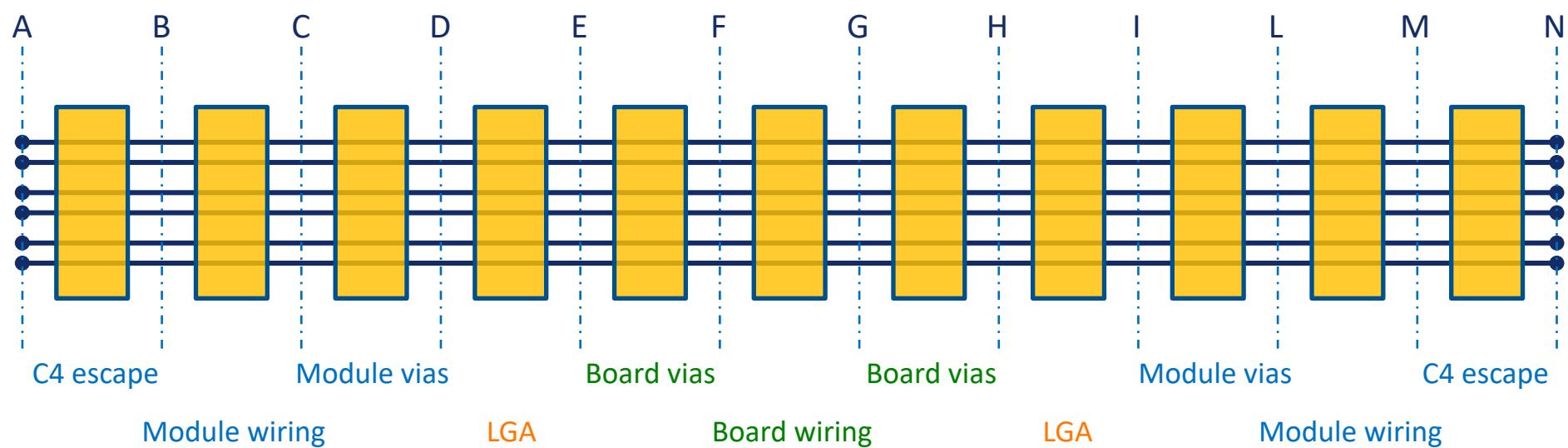
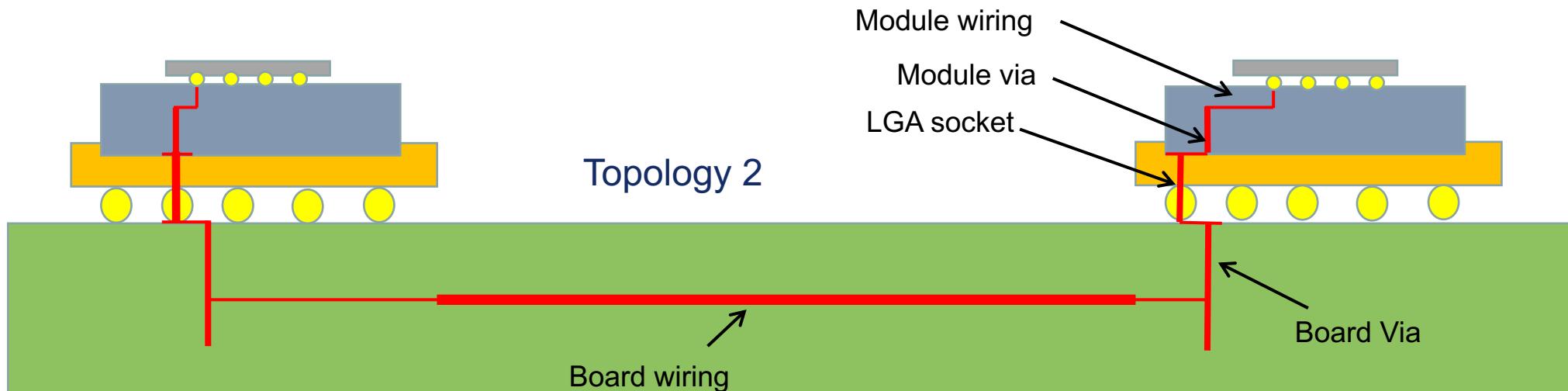
The testcases

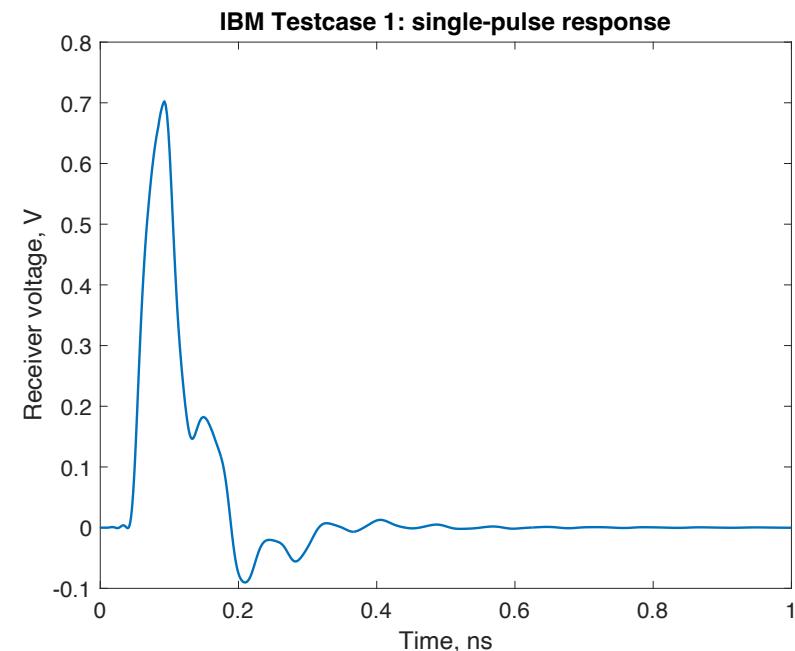
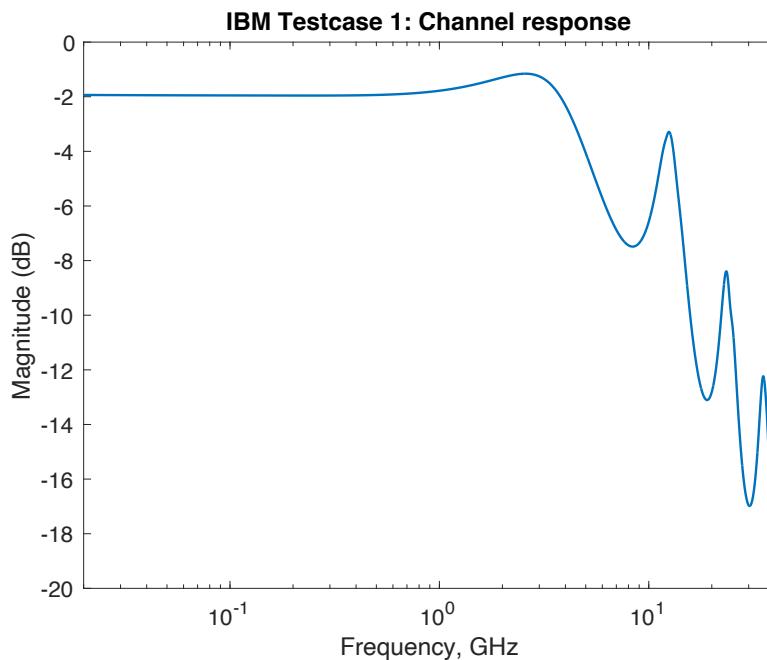


The testcase: topology 1



The testcase: topology 2



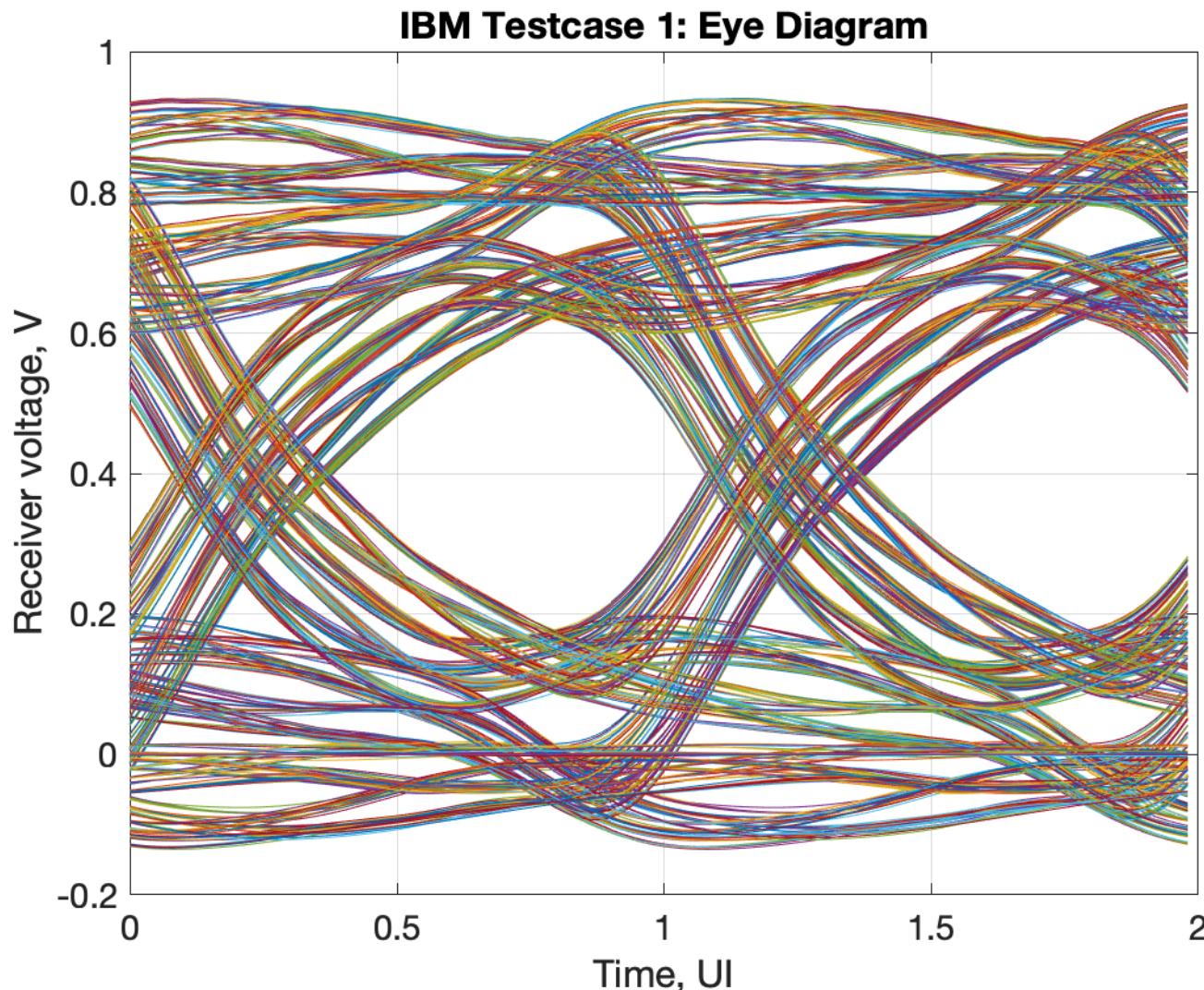


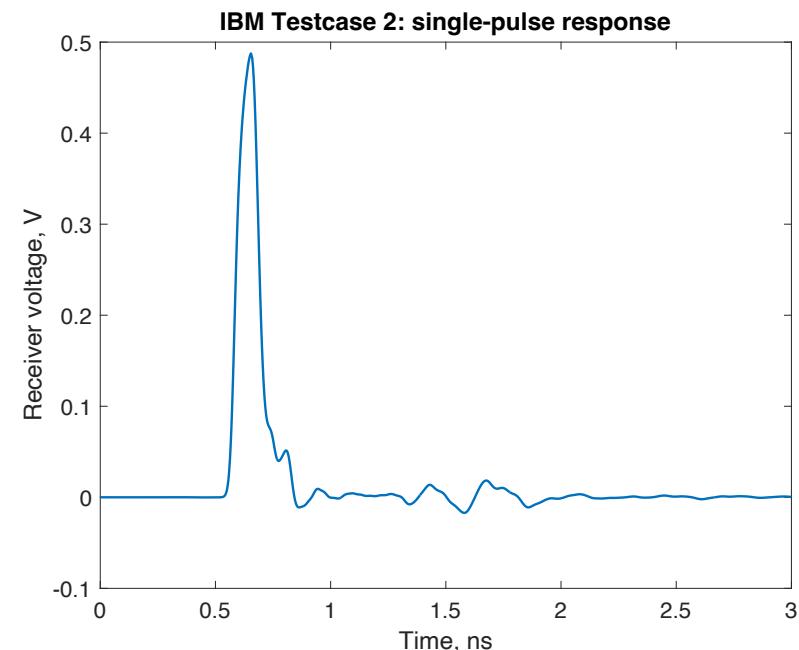
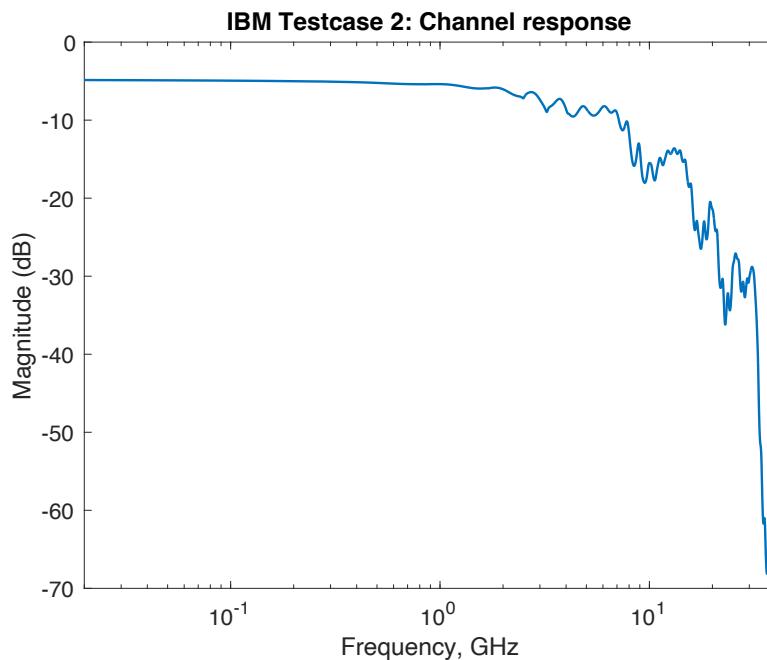
Channel configuration (for illustration only): high-loss, 5mm module length

Driver: 20Ω differential resistance, 1V differential swing

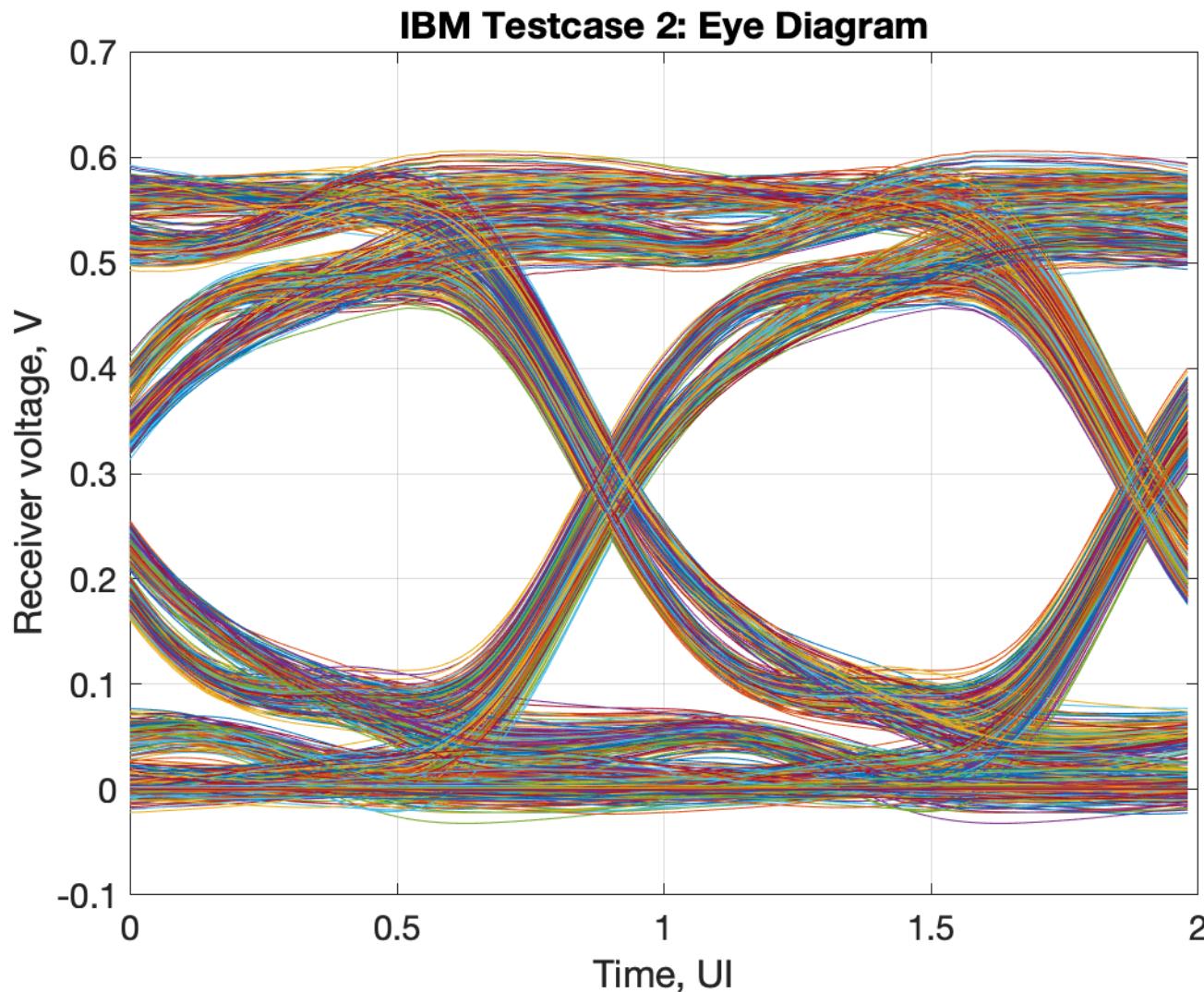
Receiver: differential 85Ω and 0.4pF

Pulse: 50ps duration, 10ps rise time (20Gbps data rate)





Channel configuration (for illustration only): high-loss, 5mm module length, backdrilled PCB vias
Driver: 60Ω differential resistance, 1V differential swing
Receiver: differential 85Ω and 0.4pF
Pulse: 100ps duration, 10ps rise time (10Gbps data rate)



Testcase material provided

SPICE netlists for both topologies (master netlist files)

`ibm_topology_1.cir, ibm_topology_2.cir`

SPICE drivers to evaluate channel response and pulse response

`ibm_topology_*_AC.cir, ibm_topology_*_TRAN.cir`

Frequency responses of all interconnects (all 12-port, Touchstone format)

`*.s12p`

SPICE models of all interconnects (all 12-port, computed by IdEM)

`subckt_1_*.cir, ..., subckt_15_*.cir`

IdEM workspace with all data and models

`workspace_all_models.idem.mat`

Disclaimer: all data representative of geometry, materials and technology, but not necessarily related to the actual product

- Evaluate and plot channel responses (AC) and pulse responses (TRAN)
 - For both topologies
 - For various configurations of the channels (effects of losses and via stubs)
 - Change termination capacitance and driver resistance and observe channel and pulse responses
 - Change pulse width (data rate)
 - Estimate Xtalk
 - For topology 2: set a target data rate 5Gbps and 10Gbps
 - Evaluate eye diagrams at both data rates for bare channel
 - Test various configurations (low/high loss and with/without stubs)
 - Choose the most promising channel configuration
 - Design an appropriate equalization scheme to achieve target data rate (free to select TX-FFE, CTLE, DFE and their combinations)
 - What is the highest data rate that you can achieve?
 - Document methods and results in a written report