Integrated Systems Architectures

Design of a RISC-V-lite processor
Assignment

1 Assignment

The output of this lab is the following:

1. Design in VHDL or in SystemVerilog the RISC-V-lite processor with the requirements described in the lab description document.
2. Verify the correct behaviour of the processor by running the C program (*minv*), which is available on "Portale della didattica".
3. Synthesize the HDL and verify that the netlist still behaves as your RTL description.
   When launching the `elaborate` command, log the output on a file and check **all** the messages.
   In particular, check that all the memory elements are flip-flops (except for the SSRAM).
   If you have one or more latches, modify your RTL.
4. Modify the architecture by adding support for the execution of encrypted code.
5. Repeat the previous steps (verify and synthesize).