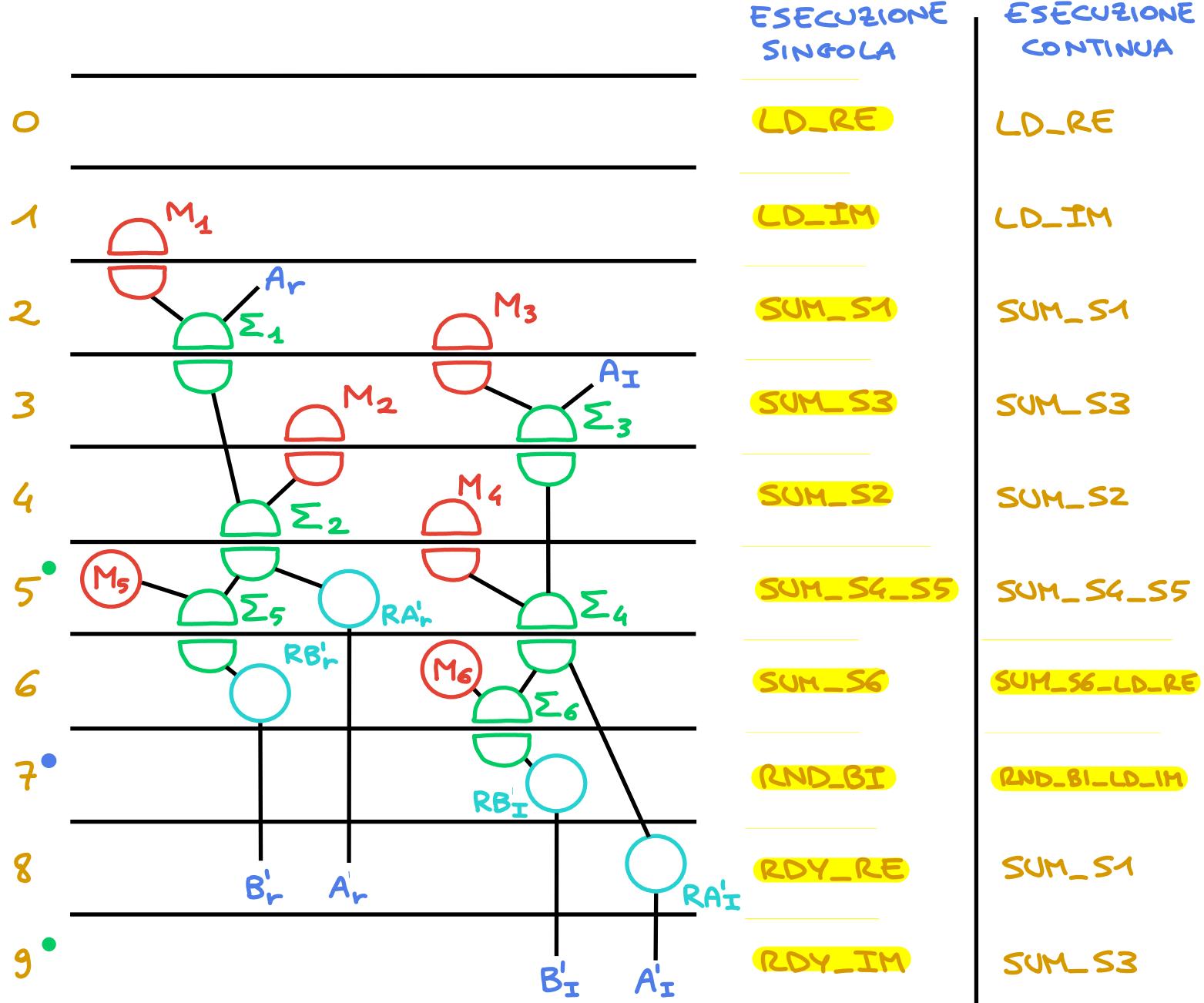


BUTTERFLY DESIGN

CONTROL DATA FLOW GRAPH



← CICLO SENSIBILE A START

← CICLO CHE FORNISCE DONE

12 STATI TOTALI

	I	II	III	IV	V	VI	VII	VIII	IX
Ar	0 4	0 5	0 4	0 5	0 4		0 4	0 4	0 4
Ai		0 5	0 5	0 5	0 5	0 5		0 5	0 5
B _r	0 6	0 6				0 6	0 6		
B _i		0 7	0 7	0 7			0 7	0 7	0 7
W _r	0 8	0 8	0 8	0 8			0 8	0 8	0 8
W _i	0 9	0 9	0 9				0 9	0 9	0 9
M ₁	0								
M ₂			0						
M ₃		0							
M ₄				0					
M ₅									
M ₆									
Σ_1		0	0 2						
Σ_2				0					
Σ_3			0	0 2					
Σ_4					0	0 2	0 2		
Σ_5					0				
Σ_6						0			
R _{A'} _r					0 0	0 0	0 0		
R _{B'} _r						0 1	0 1		
R _{A'} _I							0 3		
R _{B'} _I							0 3	0 3	

10 REGISTRI IN
TOTALE NEL DF

CONTROL UNIT DESIGN

DEFAULT VALUES

tutti i segnali a '0'

LD_RE

le(4)

le(6)

SUM_S6

sel_int(0)

le(1)

le(2)

sel_in

sel_mux01

sel_mux3

sub_add_n(1)

LD_IM

le(5)

le(7)

RND_BI -> done

le(3)

sel_mux3

SUM_S1

sel_int(2)

le(2)

sel_mux3 = 2

RDY_RE

le(2)

sel_mux3 = 2

SUM_S3

sel_int(0)

sel_int(1)

sel_int(2)

le(2)

sel_in

sel_out

RDY_IM <- start

le(8)

le(9)

sel_out

SUM_S6_LD_RE

sel_int(0)

le(1)

le(2)

sel_in

sel_mux01

sel_mux3

sub_add_n(1)

le(4)

le(6)

SUM_S2

sel_int(1)

le(2)

sel_in

sel_mux2

sub_add_n(0)

SUM_S4_S5 <- start

le(0)

sel_mux01

sel_mux2

sub_add_n(1)

RND_BI_LD_IM -> done

le(3)

sel_mux3

le(5)

le(7)

DIAGRAMMA DEGLI STATI

In grigio ci sono stati inutilizzati.

STATO PRESENTE	START	STATO FUTURO
0000 - RDY_IM	0	0000 - RDY_IM
	1	0001 - LD_RE
0001 - LD_RE	-	0010 - LD_IM
0010 - LD_IM	-	0011 - SUM_S1
0011 - SUM_S1	-	0100 - SUM_S3
0100 - SUM_S3	-	0101 - SUM_S2
0101 - SUM_S2	-	0110 - SUM_S4_S5
0110 - SUM_S4_S5	0	1000 - SUM_S6
	1	1001 - SUM_S6_LD_RE
0111	-	0000 - RDY_IM
1000 - SUM_S6	-	1010 - RND_BI
1001 - SUM_S6_LD_RE	-	1011 - RND_BI_LD_IM
1010 - RND_BI	-	1100 - RDY_RE
1011 - RND_BI_LD_IM	-	0011 - SUM_S1
1100 - RDY_RE	-	0000 - RDY_IM
1101	-	0000 - RDY_IM
1110	-	0000 - RDY_IM
1111	-	0000 - RDY_IM

PROGRAMMAZIONE uROM

STATO PRESENTE	CU_SEL_IN	CU_SEL_INT	CU_SEL_OUT	CU_LE	CU_SEL_MUX01	CU_SEL_MUX2	CU_SEL_MUX3	CU_SUB_ADD_N	CU_DONE
0000 - RDY_IM	0	000	1	0000000011	0	0	00	00	0
0001 - LD_RE	0	000	0	0000101000	0	0	00	00	0
0010 - LD_IM	0	000	0	0000010100	0	0	00	00	0
0011 - SUM_S1	0	001	0	0010000000	0	0	10	00	0
0100 - SUM_S3	1	111	1	0010000000	0	0	00	00	0
0101 - SUM_S2	1	010	0	0010000000	0	1	00	10	0
0110 - SUM_S4_S5	0	000	0	1000000000	1	1	00	01	0
0111	0	000	0	0000000000	0	0	00	00	0
1000 - SUM_S6	1	100	0	0110000000	1	0	01	01	0
1001 - SUM_S6_LD_RE	1	100	0	0110101000	1	0	01	01	0
1010 - RND_BI	0	000	0	0001000000	0	0	01	00	1
1011 - RND_BI_LD_IM	0	000	0	0001010100	0	0	01	00	1
1100 - RDY_RE	0	000	0	0010000000	0	0	10	00	0
1101	0	000	0	0000000000	0	0	00	00	0
1110	0	000	0	0000000000	0	0	00	00	0
1111	0	000	0	0000000000	0	0	00	00	0

PROGRAMMAZIONE PLA

START è il segnale di stato, S il bit di CC, LSB il bit di stato con peso più basso e X l'uscita della PLA.
La PLA è un multiplexer con START e LSB agli ingressi e S selettore.

STATO PRESENTE	S	X
0000 - RDY_IM	1	START
0001 - LD_RE	0	LSB
0010 - LD_IM	0	LSB
0011 - SUM_S1	0	LSB
0100 - SUM_S3	0	LSB
0101 - SUM_S2	0	LSB
0110 - SUM_S4_S5	1	START
0111	0	LSB
1000 - SUM_S6	0	LSB
1001 - SUM_S6_LD_RE	0	LSB
1010 - RND_BI	0	LSB
1011 - RND_BI_LD_IM	0	LSB
1100 - RDY_RE	0	LSB
1101	0	LSB
1110	0	LSB
1111	0	LSB