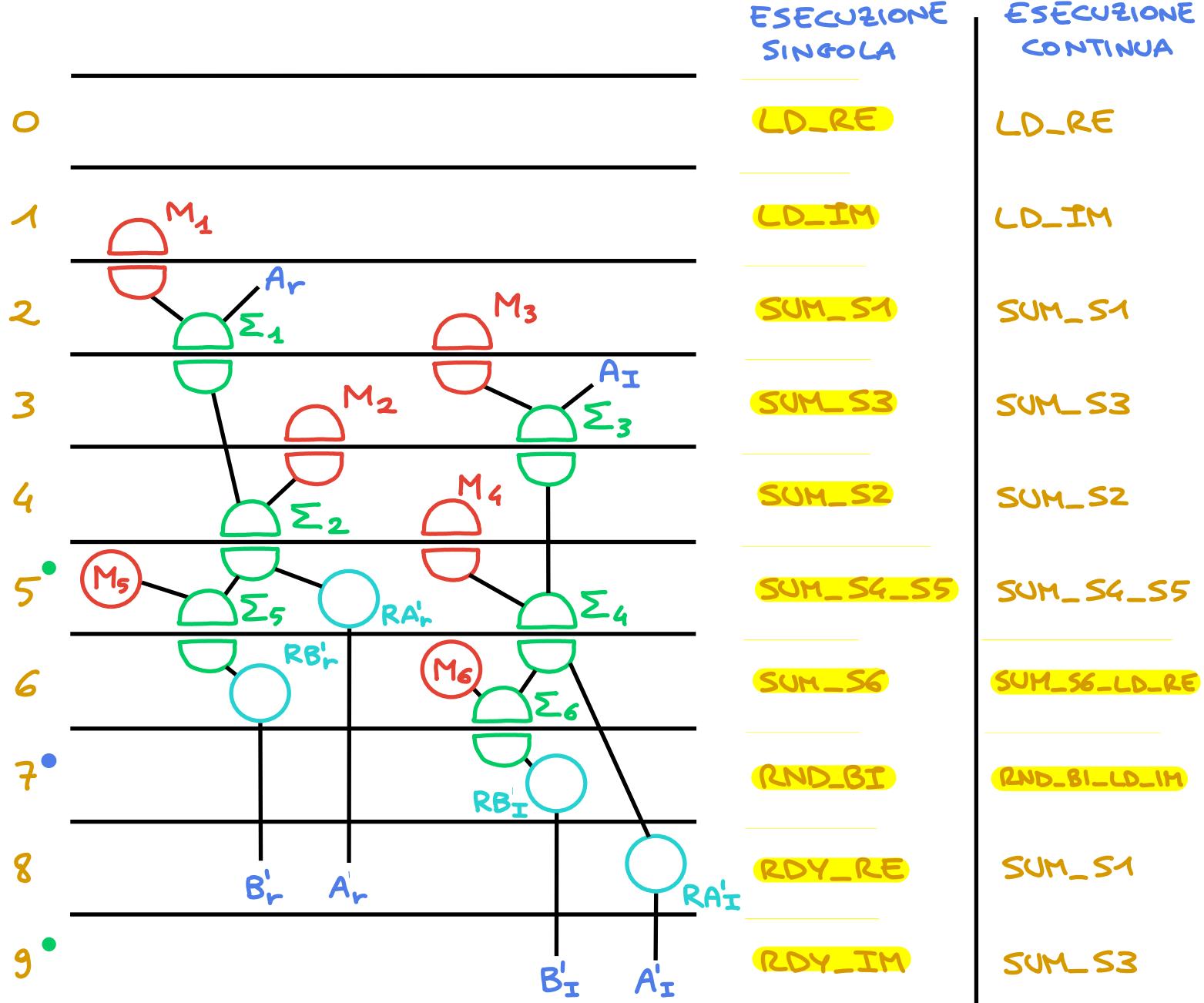


# BUTTERFLY DESIGN

## CONTROL DATA FLOW GRAPH



● ← CICLO SENSIBILE A START

● ← CICLO CHE FORNISCE DONE

12 STATI TOTALI

	I	II	III	IV	V	VI	VII	VIII	IX
Ar	0 4	0 5	0 4	0 5	0 4		0 4	0 4	0 4
Ai		0 5	0 5	0 5	0 5	0 5		0 5	0 5
B <sub>r</sub>	0 6	0 6				0 6	0 6		
B <sub>i</sub>		0 7	0 7	0 7			0 7	0 7	0 7
W <sub>r</sub>	0 8	0 8	0 8	0 8			0 8	0 8	0 8
W <sub>i</sub>	0 9	0 9	0 9				0 9	0 9	0 9
M <sub>1</sub>	0								
M <sub>2</sub>			0						
M <sub>3</sub>		0							
M <sub>4</sub>				0					
M <sub>5</sub>									
M <sub>6</sub>									
$\Sigma_1$		0	0 2						
$\Sigma_2$				0					
$\Sigma_3$			0	0 2					
$\Sigma_4$					0	0 2	0 2		
$\Sigma_5$					0				
$\Sigma_6$						0			
R <sub>A'</sub> <sub>r</sub>					0 0	0 0	0 0		
R <sub>B'</sub> <sub>r</sub>						0 1	0 1		
R <sub>A'</sub> <sub>I</sub>								0 3	0 3
R <sub>B'</sub> <sub>I</sub>								0 2	0 3

10 REGISTRI IN  
TOTALE NEL DF

# CONTROL UNIT DESIGN

## DEFAULT VALUES

tutti i segnali a '0'

## LD\_RE

le(4)  
le(6)

## LD\_IM

le(5)  
le(7)

## SUM\_S1

sel\_int(2)  
le(2)  
sel\_mux3 = 2

## SUM\_S3

sel\_int(0)  
sel\_int(1)  
sel\_int(2)  
le(2)  
sel\_in  
sel\_out

## SUM\_S2

sel\_int(1)  
le(2)  
sel\_in  
sel\_mux2

## SUM\_S4\_S5 <- start

le(0)  
sel\_mux01  
sel\_mux2

## SUM\_S6

sel\_int(0)  
le(1)  
le(2)  
sel\_in  
sel\_mux01  
sel\_mux3

## RND\_BI -> done

le(3)  
sel\_mux3

## RDY\_RE

le(2)  
sel\_mux3 = 2

## RDY\_IM <- start

le(8)  
le(9)  
sel\_out

## SUM\_S6\_LD\_RE

sel\_int(0)  
le(1)  
le(2)  
sel\_in  
sel\_mux01  
sel\_mux3  
le(4)  
le(6)

## RND\_BI\_LD\_IM -> done

le(3)  
sel\_mux3  
le(5)  
le(7)

## DIAGRAMMA DEGLI STATI

In grigio ci sono stati inutilizzati.

STATO PRESENTE	START	STATO FUTURO
0000 - RDY_IM	0 1	0000 - RDY_IM 0001 - LD_RE
0001 - LD_RE	-	0010
0010 - LD_IM	-	0011
0011 - SUM_S1	-	0100
0100 - SUM_S3	-	0101
0101 - SUM_S2	-	0110
0110 - SUM_S4_S5	0 1	1000 - SUM_S6 1001 - SUM_S6_LD_RE
0111	-	0000
1000 - SUM_S6	-	1010
1001 - SUM_S6_LD_RE	-	1011
1010 - RND_BI	-	1100
1011 - RND_BI_LD_IM	-	0011
1100 - RDY_RE	-	0000
1101	-	0000
1110	-	0000
1111	-	0000

## PROGRAMMAZIONE uROM

CC composto da 1 bit (S), se attivo sono in RDY\_IM o SUM\_S4\_S5.

STATO PRESENTE	CU_SEL_IN	CU_SEL_INT	CU_SEL_OUT	CU_LE	CU_SEL_MUX01	CU_SEL_MUX2	CU_SEL_MUX3	CU_DONE
0000 - RDY_IM	0	000	1	0000000011	0	0	00	0
0001 - LD_RE	0	000	0	0000101000	0	0	00	0
0010 - LD_IM	0	000	0	0000010100	0	0	00	0
0011 - SUM_S1	0	001	0	0010000000	0	0	10	0
0100 - SUM_S3	1	111	1	0010000000	0	0	00	0
0101 - SUM_S2	1	010	0	0010000000	0	1	00	0
0110 - SUM_S4_S5	0	000	0	1000000000	1	1	00	0
0111	0	000	1	0000000011	0	0	00	0
1000 - SUM_S6	1	100	0	0110000000	1	0	01	0
1001 - SUM_S6_LD_RE	1	100	0	0110101000	1	0	01	0
1010 - RND_BI	0	000	0	0001000000	0	0	01	1
1011 - RND_BI_LD_IM	0	000	0	0001010100	0	0	01	1
1100 - RDY_RE	0	000	0	0010000000	0	0	10	0
1101	0	000	1	0000000011	0	0	00	0
1110	0	000	1	0000000011	0	0	00	0
1111	0	000	1	0000000011	0	0	00	0

## PROGRAMMAZIONE PLA

START è il segnale di stato, S il bit di CC, LSB il bit di stato con peso più basso e X l'uscita della PLA.  
La PLA è un multiplexer con START e LSB agli ingressi e S selettore.

STATO PRESENTE	S	X
0000 - RDY_IM	1	START
0001 - LD_RE	0	LSB
0010 - LD_IM	0	LSB
0011 - SUM_S1	0	LSB
0100 - SUM_S3	0	LSB
0101 - SUM_S2	0	LSB
0110 - SUM_S4_S5	1	START
0111	0	LSB
1000 - SUM_S6	0	LSB
1001 - SUM_S6_LD_RE	0	LSB
1010 - RND_BI	0	LSB
1011 - RND_BI_LD_IM	0	LSB
1100 - RDY_RE	0	LSB
1101	0	LSB
1110	0	LSB
1111	0	LSB