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AutoRRAM: An Agile RRAM Compiler Featuring Simultaneous Layout/Netlist Generation and Cross-Technology Migration

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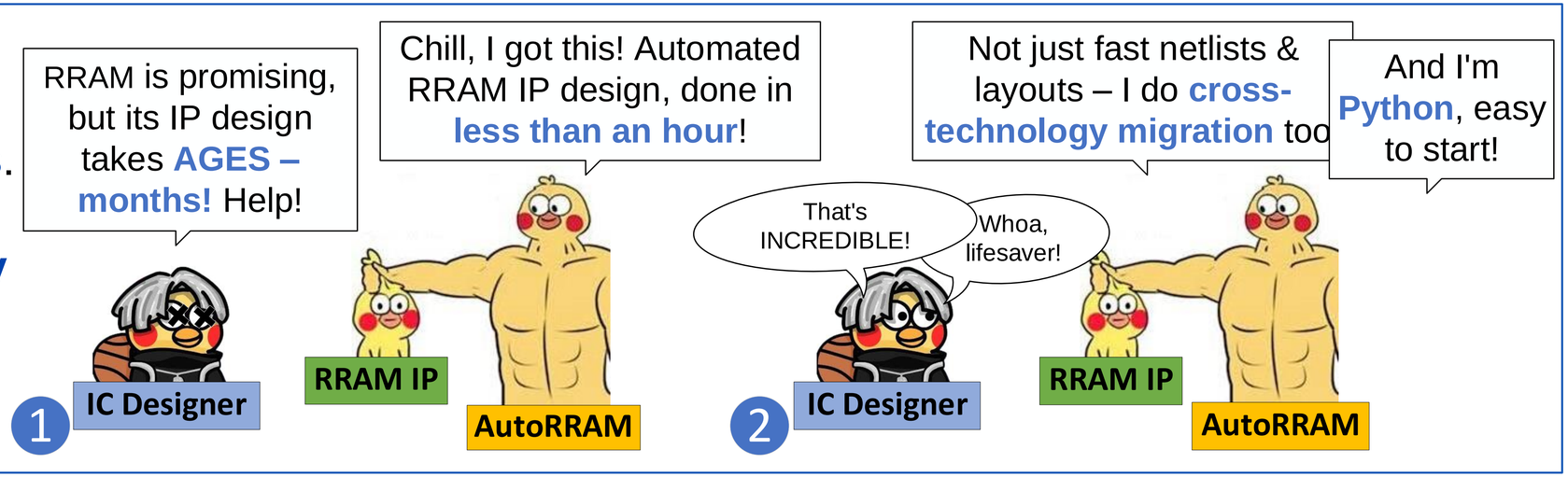
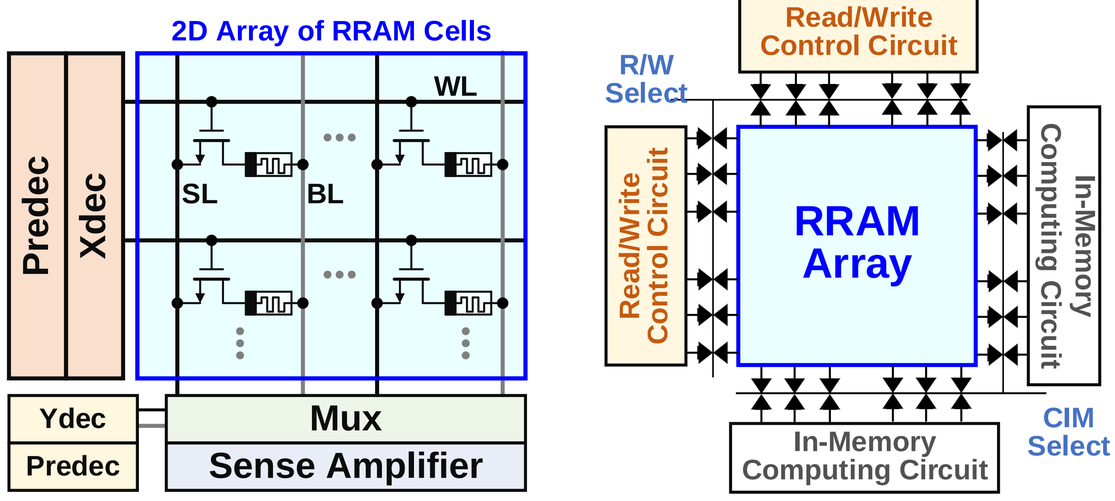
Introduction

- Simultaneous Layout/Netlist generation in **tens of minutes**.
- The first RRAM compiler that supports **process technology migration** using Virtual PDK.
- The first reported **Python-based** agile RRAM compiler.



RRAM IP Architecture



(a) Array with peripherals. (b) Storage/CIM mode switching.

Fig. 1. RRAM IP Schematics.

- **Fundamental design based on 40nm commercial RRAM technology**, featuring an RRAM array, X-axis Decoder, Y-axis Decoder, Multiplexer, and Pre-decoder (Fig. 1(a)).
- **Architecture incorporating transmission gates for mode switching**, enabling signal gating of read/write circuitry and in-memory computing operations with user-customizable design configurations (Fig. 1(b)).

Framework

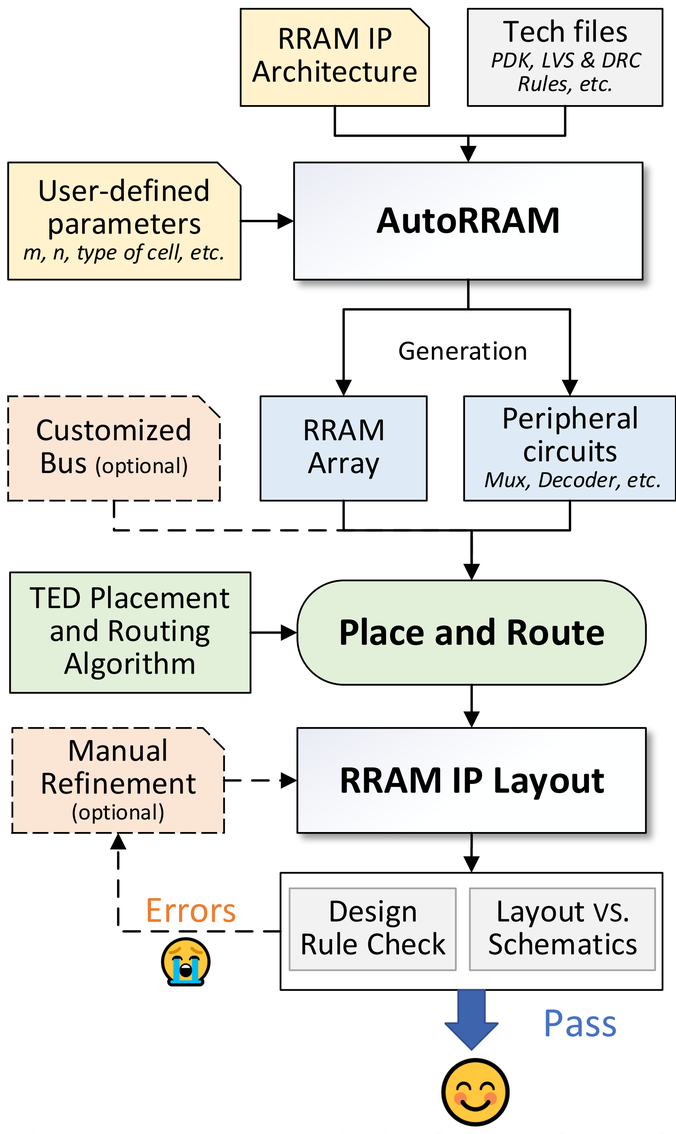


Fig. 2. AutoRRAM compilation framework overview

- **User-Driven Design.** Configures RRAM IP from user-specified templates/parameters.
- **Automated Layout.** Automated high-performance P&R (TED platform) generates the complete IP layout.
- **Integrated Verification.** Built-in LVS/DRC checks with tech files ensures a correct, fabrication-ready output.

Implementation

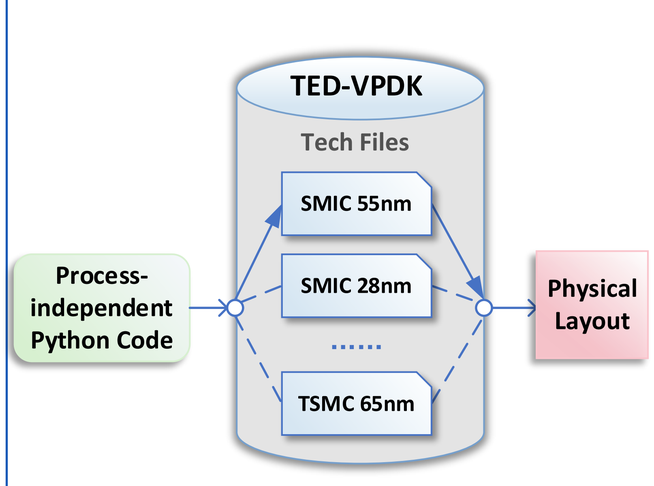


Fig. 3. Virtual PDK.

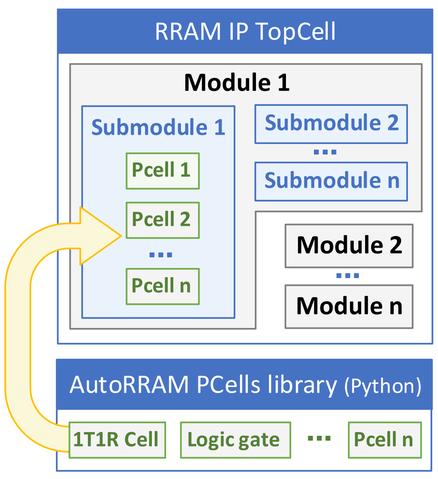
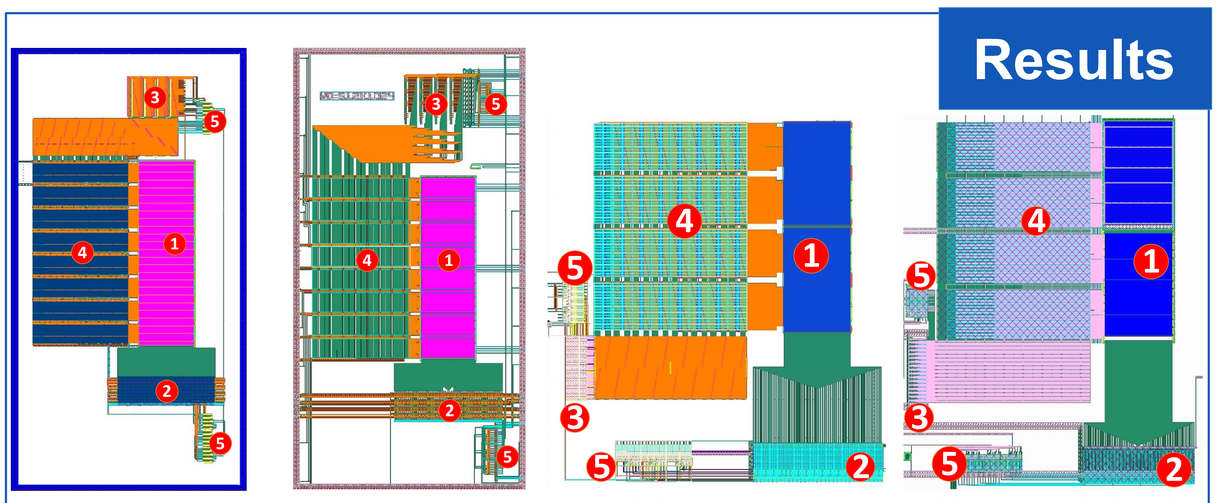


Fig. 4. Parametric Implementation.

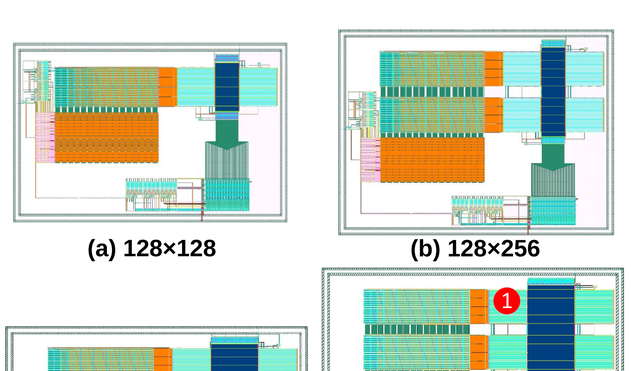
- **Cross-Technology Migration:** A Virtual PDK adapts process-independent code to specific technologies by interpreting diverse tech files for design translation, layout adjustments, and standard cell equivalence (Fig. 3).
- **Parametric Implementation:** Reusable, Python-implemented Parametric Cells (PCells)—like 1T1R units and logic gates—are hierarchically combined to efficiently construct top-level cell designs (Fig. 4).

Results



(a) AutoRRAM (SMIC 28nm) (b) Custom designed (SMIC 28nm) (c) AutoRRAM (SMIC 55nm) (d) Custom designed (SMIC 55nm)

Fig. 5. AutoRRAM vs. custom layouts. 1: array, 2: xdec, 3: ydec, 4: mux, 5: predec.



(a) 128×128 (b) 128×256 (c) 256×256 (d) 256×512

Fig. 6. AutoRRAM-generated RRAM IPs. 1: Y-axis transmission gate, 2: X-axis transmission gate.

Tabel I. RRAM Compiler Comparison

RRAM Compilers	[1]	[2]	AutoRRAM
Programming Language	Cadence SKILL	Cadence SKILL	Python
Cross Process Technology	✗	✗	✓
Mode Switching	✗	✗	✓

[1] A ReRAM memory compiler with layout-precise performance evaluation. S3S, 2019.
[2] An open-source RRAM compiler. NEWCAS, 2022.

AutoRRAM is the first Python RRAM compiler, also first for process migration, supporting mode switching between storage and CIM.

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