PD9982 Module (CS0202/1 displays)

Overview

The PD9982 module is used to transmit data to CS0202/1 unicode/emoji displays. The CS0202/1 displays can display any unicode character. Data bytes are queued for transmission to the display in a 7-byte `transmission buffer` and transmitted over a serial bus to the `pre-display buffer` on the display. In order to show data on the display, a special command can be sent over the bus (controlled by ctrl reg). This will shift the UTF-16 characters from the `pre-display buffer` to the actual display. This operation will clear the `pre-display buffer`. In order to guarantee data integrity a CRC (CRC-8/LTE) should be calculated - based on bytes that were queued for transmission - and appended at the end of the `transmission buffer`, (see Checksum chapter for more details). If the receiver was not ready for receiving data it will only receive a subset of the data and report the number of bytes successfully read.

The module can be accessed and controlled by two memory-mapped registers. The `PD_CTRL` (control) register and the `PD_STS` (status) registers each occupy one byte consecutively. Futhermore, the `transmission buffer (PD_TR_BUF)` is also memory-mapped and is followed by the `PD_CRC_BUF` on the next consecutive byte. In other words, order in memory is as follows: PD_CTRL | PD_STS | PD_TR_BUF | PD_CRC_BUF.

Data encoding

The module requires input data on the `transmission buffer` to be UTF-16-LE encoded. Internally the module uses UTF-8 representation and it will output UTF-8 characters.

Registers

Control register (PD_CTRL)

The control register is used to indicate how many bytes are written to `PD_TR_BUF`. See the following table for detail.

Bit num	7	6	5	4	3	2	1	0
	ERR_RST	X	X	X	WRT_CNT	WRT_CNT	WRT_CNT	X

X = Reserved

Bit 7 ERR_RST (Error Reset): This bit is used to reset the `ERR_IND` bit of `PD_STS`. When 1 is written to this bit **AND all other bits in the control register is 0** the module will exit the error-state and will continue processing data. *Note*: This bit will automatically be set to 0 once the `ERR_IND` bit is 0.

Bit 6:4 Reserved: These bits are reserved and should not be written.

Bit 3:1 WRT_CNT (Write Count): These bits should be written to indicate the number of bytes (0-7) written to `PD_TR_BUF` for transmission. These bits are scanned every `Operation Cycle` and if any bit is 1 the transmission will start and `OP_STS` will be set to 1.

Bit 0 Reserved: This bit is reserved and should not be written.

Status Register (PD_STS)

Bit num	7	6	5	4	3	2	1	0
	ERR_IND	TR_CNT	TR_CNT	TR_CNT	X	STRT	X	OP_STS

X = Reserved

Bit 7 ERR_IND (Crc Error Indication): This bit is used to indicate that the provided CRC didn't match CRC of the data. This means that no data was transmitted. The content of `PD_TR_BUF` and `PD_CRC_BUF` is undefined when this bit is set to 1. To indicate error recovery write 1 to the `ERR_RST` bit.

Bit 6:4 TR_CNT (Write Count): These bits are set when OP_STS goes from 1 to 0. This is indicates the number of bytes that was actually transmitted.

Bit 3 Reserved: This bit is reserved and should not be read - contents are undefined.

Bit 2 STRT (Started): This bit indicates that the module has been started and the display has been initialized.

Bit 1 Reserved: This bit is reserved and should not be read - contents are undefined.

Bit 0 OP_STS (Operation Status): This bit is set to 1 if any data is detected during the start of an `Operation Cycle`. While this bit is 1 the `PD_TR_BUF` and `PD_CRC_BUF` must not be written. Once data has been transmitted (or partially transmitted) this bit will be set to 0.

Buffers

Transmission Buffer (PD_TR_BUF)

This buffer can be used to write bytes that should be transmitted to the display. The buffer can contain up to 7 bytes of data.

CRC Buffer (PD_CRC_BUF)

This buffer contain one byte. When data has been written to `PD_TR_BUF` a checksum of the bytes that should be transmitted should be calculated (see checksum).

Checksum

The checksum should be calculated on the CRC8/LTE format.

Circular buffer

The PD9982 module has an internal circular buffer where the bytes transmitted over the 'Transmission Buffer' are stored. This buffer can store up to 64 bytes of data.

Operation

Operation Cycle

The module has an operation cycle of approx 50ms. Every cycle the `WRT_CNT` segment of `PD_CTRL` will be scanned and if any bit is set to 1 a transmission will be initiated. However since the `pre-disply buffer` is limited the text also needs to be shifted to the actual display before the buffer has been filled (the buffer is circular so any overflow will overwrite previously recieved data) see 'Circular Buffer'. This is done byte setting `PD_CTRL` to the special value `0xF1` (`11110001b`). This command has priority over initiating a transmission and will start shifting text to the display and convert data stored in its circular buffer from UTF16 to UTF8. During this process the bit `OP_STS` of `PD_CTRL` will be set to 1.

Library

The recommended way to use the PD9982 Module is to use the driver-library that provides access to the registers and buffers. For more details on the functions in the library see the `pd9982_driver.h`.