Assignment 1: Fibonacci

- Design
  - Code up the Fibonacci module in SystemVerilog
  - Use the 2-process method
  - Implement using a FSM with at most 2-3 states
  - Make sure to clock all output signals
- Simulation
  - Run the simulation with the provided testbench in Modelsim
  - Add 2 or more additional test vectors to the testbench
  - Create a fibonacci_sim.do file that compiles the SystemVerilog files, sets up the wave form, and runs the simulation.
  - Verify your algorithm generates the correct output
  - Get total simulation cycle count
- Synthesize the design
  - Synthesize the design with Synplify Premier, targeting the Cyclone IV-E
  - Get resource utilization including:
    - Logic Elements
    - Registers
    - Memory
    - Multipliers
- Submit a PDF file with simulation and synthesis results with the following:
  - Simulation results:
    - Clock cycle count
    - Errors reported (if any)
  - Synthesis results (some might not apply):
    - Maximum frequency
    - Registers / LUTs / Logic Elements
    - Memory utilization
    - Multipliers (DSPs)
    - Worst path (timing analysis)
    - Schematic architecture (RTL)

Zip up your SystemVerilog files and fibonacci_sim.do file, and submit it on Canvas. I should be able to simply type "do fibonacci_sim.do" in Modelsim to run your simulation and verify it is correct.