## 1.1 add

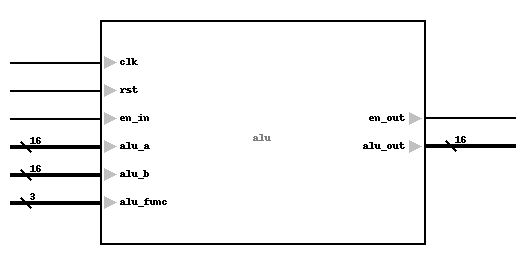


表x add模块

表x add模块端口表

|  |  |  |  |
| --- | --- | --- | --- |
| 信号名 | 位宽(bit) | I/O | 描述 |
| a | 32 | I |  |
| b | 32 | I |  |
| sum | 32 | O |  |
| overflow | 1 | O |  |

## 1.2 alu

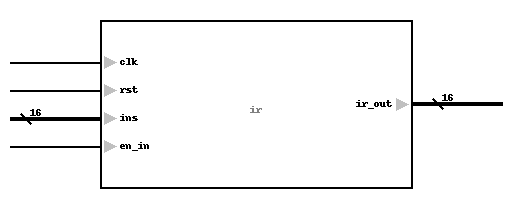


表x alu模块

表x alu模块端口表

|  |  |  |  |
| --- | --- | --- | --- |
| 信号名 | 位宽(bit) | I/O | 描述 |
| clk | 1 | I |  |
| rst | 1 | I |  |
| en\_in | 1 | I |  |
| alu\_a | 16 | I |  |
| alu\_b | 16 | I |  |
| alu\_func | 3 | I |  |
| en\_out | 1 | O |  |
| alu\_out | 16 | O |  |

## 1.3 ir

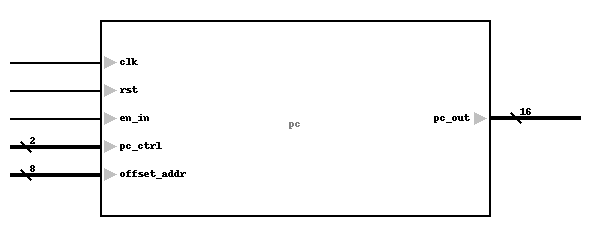


表x ir模块

表x ir模块端口表

|  |  |  |  |
| --- | --- | --- | --- |
| 信号名 | 位宽(bit) | I/O | 描述 |
| clk | 1 | I |  |
| rst | 1 | I |  |
| ins | 16 | I |  |
| en\_in | 1 | I |  |
| ir\_out | 16 | O |  |

## 1.4 pc

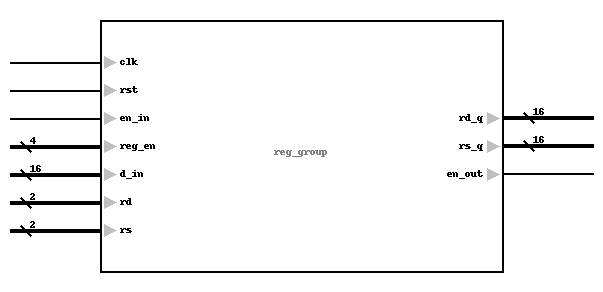


表x pc模块

表x pc模块端口表

|  |  |  |  |
| --- | --- | --- | --- |
| 信号名 | 位宽(bit) | I/O | 描述 |
| clk | 1 | I |  |
| rst | 1 | I |  |
| en\_in | 1 | I |  |
| pc\_ctrl | 2 | I |  |
| offset\_addr | 8 | I |  |
| pc\_out | 16 | O |  |

## 1.5 reg\_group



表x reg\_group模块

表x reg\_group模块端口表

|  |  |  |  |
| --- | --- | --- | --- |
| 信号名 | 位宽(bit) | I/O | 描述 |
| clk | 1 | I |  |
| rst | 1 | I |  |
| en\_in | 1 | I |  |
| reg\_en | 4 | I |  |
| d\_in | 16 | I |  |
| rd | 2 | I |  |
| rs | 2 | I |  |
| rd\_q | 16 | O |  |
| rs\_q | 16 | O |  |
| en\_out | 1 | O |  |