MCP4725

12-Bit Digital-to-Analog Converter with EEPROM Memory in SOT-23-6

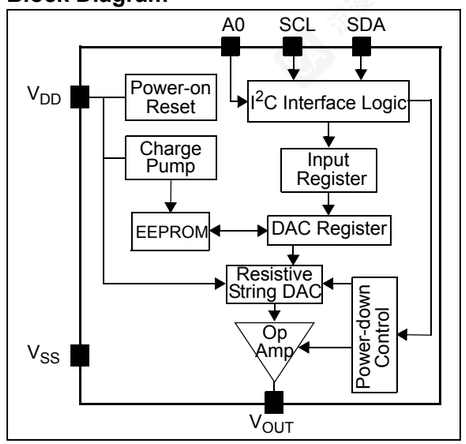
Features

- 12-Bit Resolution
- On-Board Non-Volatile Memory (EEPROM)
- ±0.2 LSB DNL (typical)
- External A0 Address Pin
- Normal or Power-Down Mode
- Fast Settling Time: 6 µs (typical)
- External Voltage Reference (V_{DD})
- Rail-to-Rail Output
- Low Power Consumption
- Single-Supply Operation: 2.7V to 5.5V
- I^2C^{TM} Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) Modes
- Small 6-lead SOT-23 Package
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Closed-Loop Servo Control
- Low Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems

Block Diagram



DESCRIPTION

The MCP4725 is a low-power, high accuracy, single channel, 12-bit buffered voltage output Digital-to-Analog Convertor (DAC) with non-volatile memory (EEPROM). Its on-board precision output amplifier allows it to achieve rail-to-rail analog output swing.

The DAC input and configuration data can be programmed to the non-volatile memory (EEPROM) by the user using I^2C interface command. The non-volatile memory feature enables the DAC device to hold the DAC input code during power-off time, and the DAC output is available immediately after power-up. This feature is very useful when the DAC device is used as a supporting device for other devices in the network.

The device includes a Power-On-Reset (POR) circuit to ensure reliable power-up and an on-board charge pump for the EEPROM programming voltage. The DAC reference is driven from V_{DD} directly. In power-down mode, the output amplifier can be configured to present a known low, medium, or high resistance output load.

The MCP4725 has an external A0 address bit selection pin. This A0 pin can be tied to V_{DD} or V_{SS} of the user's application board.

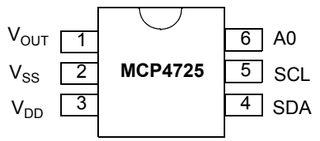
The MCP4725 has a two-wire I^2C™ compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

The MCP4725 is an ideal DAC device where design simplicity and small footprint is desired, and for applications requiring the DAC device settings to be saved during power-off time.

The device is available in a small 6-pin SOT-23 package.

Package Type

SOT-23-6



MCP4725

12 位数模转换器，带 EEPROM 存储器，采用 SOT-23-6 封装

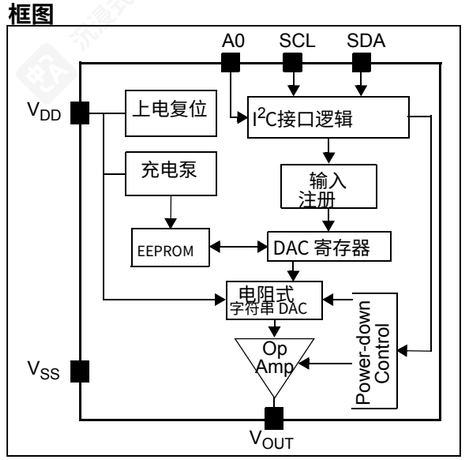
特性

- 12位分辨率
- 板载非易失性存储器（EEPROM）
- ±0.2 LSB DNL (典型)
- 外部A0地址引脚
- 正常或掉电模式
- 快速建立时间：6 µs (典型)
- 外部电压参考 (VDD)
- 轨到轨输出
- 低功耗
- 单电源供电：2.7V 至 5.5V
- I^2CTM 接口：
  - 八个可用地址
  - 标准（100kbps）、快速（400 kbps）和高速（3.4 Mbps）模式
- 小型 6 引脚 SOT-23 封装
- 扩展温度范围：-40°C至 +125°C

应用

- 设定点或偏移量微调
- 传感器校准
- 闭环伺服控制
- 低功耗便携式测量仪器
- PC外设
- 数据采集系统

框图



描述

MCP4725是一款低功耗、高精度、单通道、12位缓冲电压输出数模转换器(DAC)，具有非易失性存储器(EEPROM)。其板载精密输出放大器允许它实现轨到轨的模拟输出摆幅。

DAC输入和配置数据可以通过I^2C接口命令由用户编程到非易失性存储器(EEPROM)中。非易失性存储器特性使DAC设备能够在断电期间保持DAC输入代码，并在上电后立即提供DAC输出。当DAC设备用作网络中其他设备的外围设备时，此特性非常有用。

该设备包含一个上电复位（POR）电路，以确保可靠的启动，并提供一个板载充电泵为EEPROM编程电压供电。DAC参考电压直接由VDD驱动。在关断模式下，输出放大器可以配置为呈现已知的低、中或高阻值输出负载。

MCP4725具有一个外部A0地址选择引脚。该A0引脚可以连接到用户应用板的VDD或VSS。

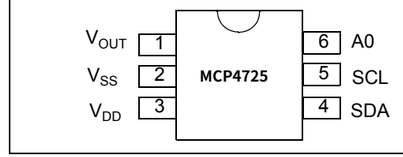
MCP4725具有一个兼容I^2CTM的双线串行接口，支持标准（100 kHz）、快速（400 kHz）或高速（3.4 MHz）模式。

MCP4725是一款理想的DAC设备，适用于需要设计简单和紧凑封装的应用，并且要求DAC设备设置在断电时能够保存的应用。

该设备采用小型6引脚SOT-23封装。

封装类型

SOT-23-6



NOTES:

MCP4725

注意：

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....6.5V
All inputs and outputs w.r.t V_{SS} .....–0.3V to V_{DD}+0.3V
Current at Input Pins .....±2 mA
Current at Supply Pins .....±50 mA
Current at Output Pins .....±25 mA
Storage Temperature .....-65°C to +150°C
Ambient Temp. with Power Applied .....-55°C to +125°C
ESD protection on all pins ..... ≥ 6 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF, T_A = -40°C to +125°C. Typical values are at +25°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Supply Current	I_{DD}	—	210	400	µA	Digital input pins are grounded, Output pin (V_{OUT}) is not connected (unloaded), Code = 000h
Power-Down Current	I_{DDP}	—	0.06	2.0	µA	V_{DD} = 5.5V
Power-On-Reset Threshold Voltage	V_{POR}	—	2	—	V	
DC Accuracy						
Resolution	n	12	—	—	Bits	Code Range = 000h to FFFh
INL Error	INL	—	±2	±14.5	LSB	**Note 1**
DNL	DNL	-0.75	±0.2	±0.75	LSB	**Note 1**
Offset Error	V_{OS}		0.02	0.75	% of FSR	Code = 000h
Offset Error Drift	ΔV_{OS}/°C	—	±1	—	ppm/°C	-45°C to +25°C
		—	±2	—	ppm/°C	+25°C to +85°C
Gain Error	G_E	-2	-0.1	2	% of FSR	Code = FFFh, Offset error is not included.
Gain Error Drift	ΔG_E/°C	—	-3	—	ppm/°C	
Output Amplifier						
Phase Margin	p_M	—	66	—	Degree(°)	C_L = 400 pF, R_L = ∞
Capacitive Load Stability	C_L	—	—	1000	pF	R_L = 5 kΩ, **Note 2**
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	15	24	mA	V_{DD} = 5V, V_{OUT} = Grounded
Output Voltage Settling Time	T_S	—	6	—	µs	**Note 3**

Note 1: Test Code Range: 100 to 4000.
2: This parameter is ensure by design and not 100% tested.
3: Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.
4: Logic state of external address selection pin (A0 pin).

1.0 电气特性

绝对最大额定值 †

VDD.6.5V 所有输入和输出相对于VSS .....–0.3V 至 VDD+0.3V 输入引脚处的电流.±2 mA 电源引脚处的电流.±50 mA

输出引脚当前值.±25 mA 存储温度.-65°C至+150°C 带电源时的环境温度 .....-55°C至+125°C

所有引脚的ESD保护 ..... ≥ 6 kV HBM, ≥ 400V MM 最大结温（TJ）.+150°C

† 注意：超过“最高额定值”列出的应力值可能永久损坏设备。这仅是应力额定值，不意味着设备在本文规范的操作列表中指示的这些或其他任何条件下能正常工作。长时间暴露在最高额定值条件下可能会影响设备可靠性

电气特性

电气规格：除非另有说明，所有参数适用于VDD = + 2.7V至5.5V、VSS = 0V、R_L = 5 kΩ从VOUT至V_{SS}、C_L = 100 pF、T_A = -40°C至+125°C。典型值在+25°C时。

参数	Sym	Min	Typ	Max	单位	条件
电源要求						
工作电压	V_{DD}	2.7		5.5	V	
电源电流	I_{DD}	—	210	400	µA	数字输入引脚接地，输出引脚（VOUT）未连接（未负载），代码 = 000h
掉电电流	I_{DDP}	—	0.06	2.0	µA	VDD = 5.5V
上电复位阈值电压	V_{POR}	—	2	—	V	
直流精度						
分辨率	n	12	—	—	Bits	代码范围 = 000h 至 FFFh
INL 错误	INL	—	±2	±14.5	LSB	**注释 1**
DNL	DNL	-0.75	±0.2	±0.75	LSB	**注释 1**
偏移错误	V_{OS}		0.02	0.75	% 的 FSR	代码 = 000h
偏移误差漂移	ΔVOS/°C	—	±1	—	ppm/°C	-45°C 至 +25°C
		—	±2	—	ppm/°C	+25°C 至 +85°C
增益误差	G_E	-2	-0.1	2	FSR 的百分比	代码 = FFFh ，偏移误差不包含在内。
增益误差漂移	ΔGE/°C	—	-3	—	ppm/°C	
输出放大器						
相位裕度	p_M	—	66	—	度(°)	CL = 400 pF, RL = ∞
电容负载稳定性	C_L	—	—	1000	pF	RL = 5 kΩ, 注释2
压摆率	SR	—	0.55	—	V/µs	
短路电流	I_{SC}	—	15	24	mA	V_{DD} = 5V, V_{OUT} = 接地
输出电压稳定 Time	T_S	—	6	—	µs	**注意 3**

注意 1： 测试代码范围：100 至 4000。
2： 该参数由设计保证，未经 100% 测试。
3： 在满量程范围中，当代码从 1/4 变为 3/4（400h 至 C00h）时，最终值在最终值 LSB 的 1/2 范围内。
4： 外部地址选择引脚（A0引脚）的逻辑状态。

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF, T_A = -40°C to +125°C. Typical values are at +25°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Up Time	T_{PU}	—	2.5	—	µs	V_{DD} = 5V
		—	5	—	µs	V_{DD} = 3V Exit Power-down Mode, (Started from falling edge of ACK pulse)
DC Output Impedance	R_{OUT}	—	1	—	Ω	Normal mode (V_{OUT} to V_{SS})
		—	1	—	kΩ	Power-Down Mode 1 (V_{OUT} to V_{SS})
		—	100	—	kΩ	Power-Down Mode 2 (V_{OUT} to V_{SS})
		—	500	—	kΩ	Power-Down Mode 3 (V_{OUT} to V_{SS})
Supply Voltage Power-up Ramp Rate for EEPROM loading	V_{DD_RAMP}	1	—	—	V/ms	Validation only.
Dynamic Performance						
Major Code Transition Glitch		—	45	—	nV-s	1 LSB change around major carry (from 800h to 7FFh) (**Note 2)**
Digital Feedthrough		—	<10	—	nV-s	**Note 2**
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	$0.7V_{DD}$	—	—	V	
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	$0.3V_{DD}$	V	
Input High Voltage (A0 Pin)	$V_{A0\text{-}Hi}$	$0.8V_{DD}$	—	—		**Note 4**
Input Low Voltage (A0 Pin)	$V_{A0\text{-}IL}$	—	—	$0.2V_{DD}$		**Note 4**
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = A0 = V_{SS} or SCL = SDA = A0 = V_{DD}
Pin Capacitance	C_{PIN}	—	—	3	pF	**Note 2**
EEPROM						
EEPROM Write Time	TWRITE	—	25	50	ms	
Data Retention		—	200	—	Years	At +25°C, **(Note 2)**
Endurance		1	—	—	Million Cycles	At +25°C, **(Note 2)**

Note 1: Test Code Range: 100 to 4000.

2: This parameter is ensure by design and not 100% tested.

3: Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.

4: Logic state of external address selection pin (A0 pin).

MCP4725

电气特性 (续)

电气 S p规格：除非另有说明 , all p参数 a pply at V_{DD} = + 2.7V 至 5.5V，VSS = 0V，R_L = 5 kΩ 从 VOUT 至 Vss，C_L = 100 pF，T_A = -40°C 至 +125°C。典型值在 +25°C 时。

参数	Sym	Min	Typ	Max	单位	条件
启动时间	T_{PU}	—	2.5	—	µs	VDD = 5V
		—	5	—	µs	VDD = 3V 退出掉电模式，(从ACK脉冲下降沿启动)
直流输出阻抗	R_{OUT}	—	1	—	Ω	正常模式 (VOUT至VSS)
		—	1	—	kΩ	掉电模式1 (VOUT至VSS)
		—	100	—	kΩ	掉电模式2 (VOUT至VSS)
		—	500	—	kΩ	掉电模式3 (VOUT至VSS)
EEPROM 加载的电源电压上电斜率	VDD RAMP_	1	—	—	V/ms	仅验证。
动态性能						
主要代码转换毛刺		—	45	—	nV-s	主要区域附近1 LSB变化传输（从800h到7FFh）（注2）
数字馈通		—	<10	—	nV-s	**注2**
数字接口						
输出低电压	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
输入高电压（SDA和SCL引脚）	V_{IH}	0.7VDD	—	—	V	
输入低电压（SDA和SCL引脚）	V_{IL}	—	—	0.3VDD	V	
输入高电压（A0引脚）	VA0-高	0.8VDD	—	—		**注意4**
输入低电压（A0引脚）	VA0-IL	—	—	0.2VDD		**备注 4**
输入泄漏	I_{LI}	—	—	±1	µA	SCL = SDA = A0 = VSS 或 SCL = SDA = A0 = V DD
引脚电容	C_{PIN}	—	—	3	pF	**备注 2**
EEPROM						
EEPROM 写入时间	TWRITE	—	25	50	ms	
数据保持		—	200	—	年	**在 +25°C 时，（注 2）**
耐久性		1	—	—	百万循环	**在 +25°C 下，(注 2)**

注 1：测试代码范围：100 至 4000。

2: 此参数由设计保证，并非100%经过测试。

3: 在代码从1/4变化到3/4（400h到C00h）的全量程范围内，最终值偏差在1/2 LSB以内。

4: 外部地址选择引脚（A0引脚）的逻辑状态。

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	190.5	—	°C/W	

温度特性

电气规格：除非另有说明，VDD = +2.7V 至 +5.5V，VSS =GND。						
参数	**Sym**	**Min**	**Typ**	**Max**	**单位**	**条件**
温度范围						
指定温度范围	T_A	-40	—	+125	°C	
工作温度范围	T_A	-40	—	+125	°C	
存储温度范围	T_A	-65	—	+150	°C	
热封装电阻						
热阻，6L-SOT-23	θ_{JA}	—	190.5	—	°C/W	

NOTES:

MCP4725

备注：

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

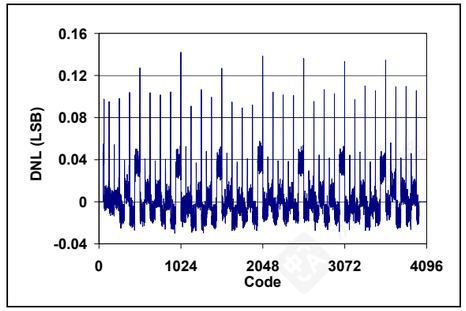


FIGURE 2-1: *DNL vs. Code (V_{DD} = 5.5V).*

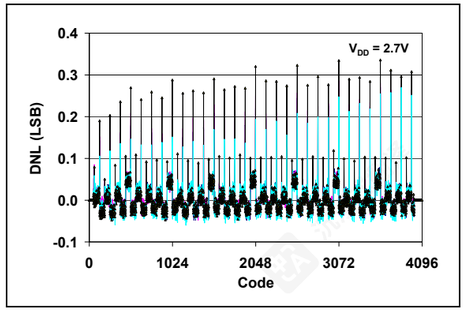


FIGURE 2-4: *DNL vs. Code and Temperature (T_A = -40°C to +125°C).*

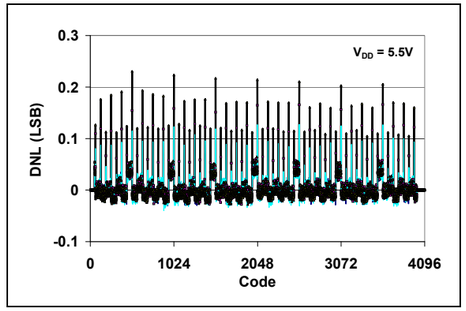


FIGURE 2-2: *DNL vs. Code and Temperature (T_A = -40°C to +125°C).*

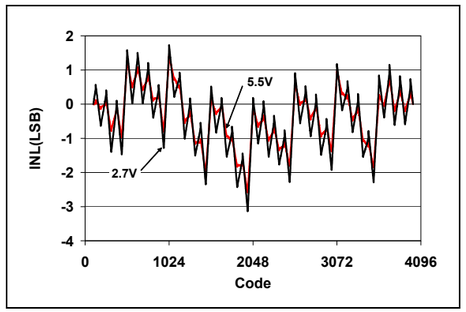


FIGURE 2-5: *INL vs. Code.*

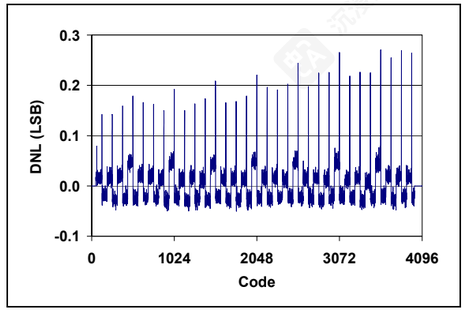


FIGURE 2-3: *DNL vs. Code (V_{DD} = 2.7V).*

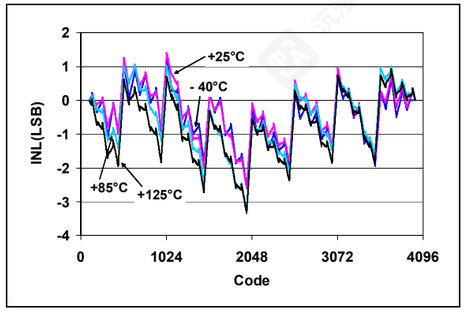


FIGURE 2-6: *INL vs. Code and Temperature (V_{DD} = 5.5V).*

2.0 典型性能曲线

注意：本说明之后提供的图表和表格是基于有限样本量的统计汇总，仅供信息参考。此处列出的性能指标未经测试或保证。在某些图表或表格中，所呈现的数据可能超出指定工作范围（例如，超出指定电源范围），因此也超出保证范围。

注意：除非另有说明，TA = +25°C，VDD = +5.0V，VSS = 0V，RL = 5 kΩ 至 VSS，CL = 100 pF。

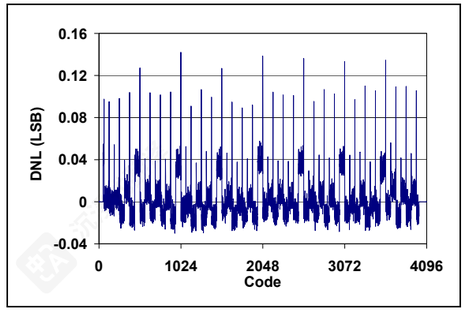


图 2-1: DNL 与代码关系 (VDD = 5.5V)。

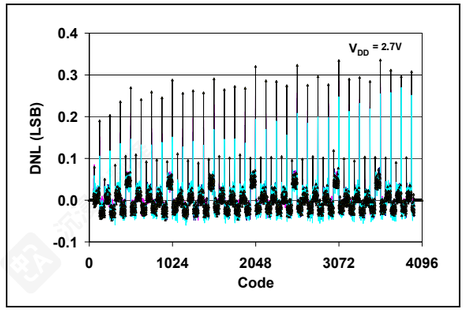


图2-4: DNL 与 Code 和温度 (TA = -40°C 至 +125°C)。

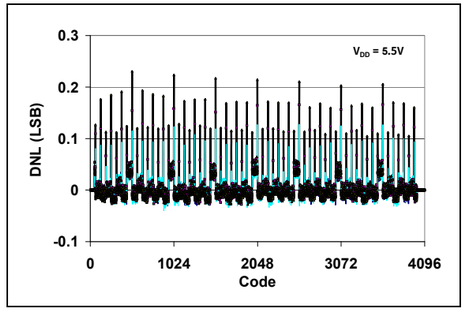


图2-2: DNL与代码和温度（TA =-40°C至 +125°C）。

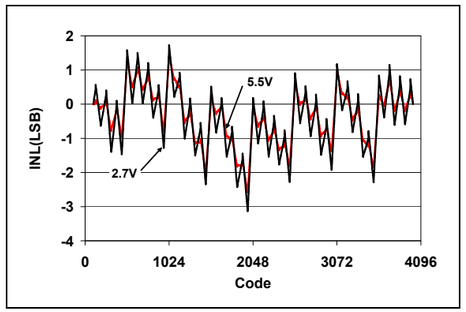


图 2-5: INL 与 Code。

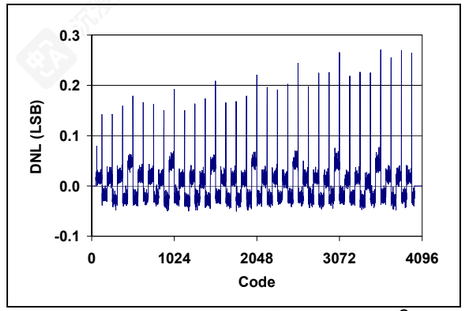


图2-3: DNL与代码（VDD = 2.7V）。

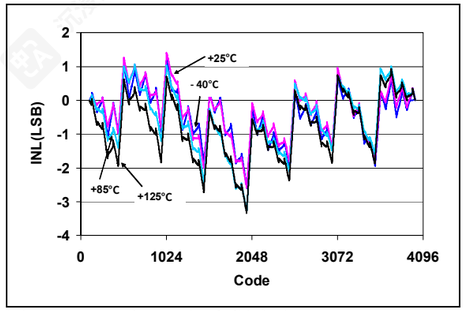


图 2-6: INL 与 Code 和温度 (VDD = 5.5V)。

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

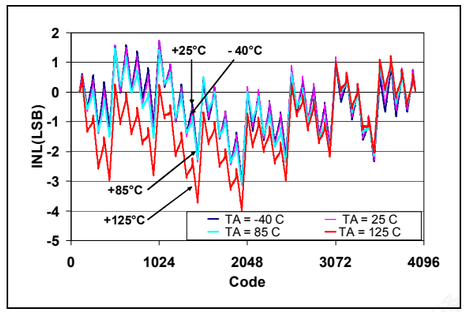


FIGURE 2-7: *INL vs. Code and Temperature (V_{DD} = 2.7V).*

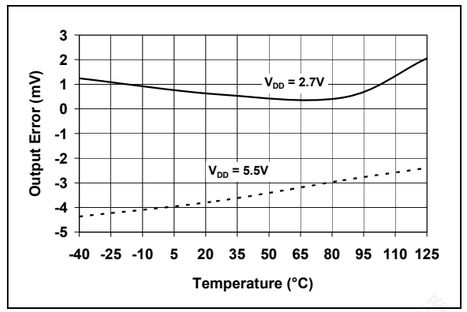


FIGURE 2-10: *Output Error vs. Temperature (Code = 4000d).*

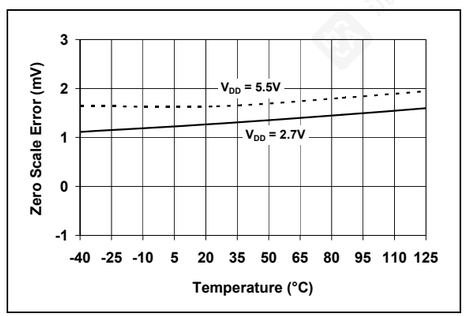


FIGURE 2-8: *Zero Scale Error vs. Temperature (Code = 000d).*

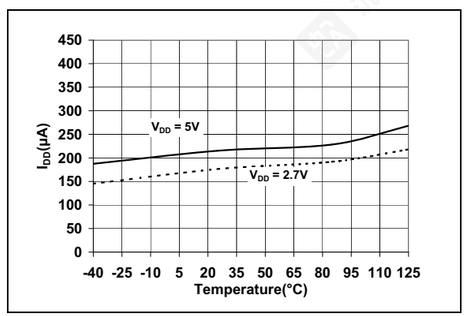


FIGURE 2-11: *I_{DD} vs. Temperature.*

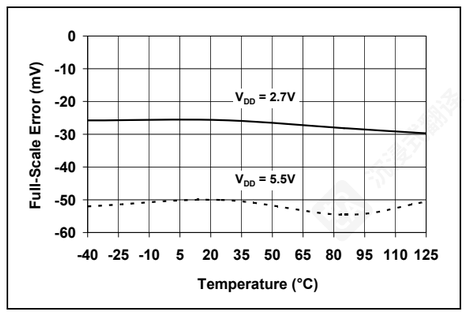


FIGURE 2-9: *Full Scale Error vs. Temperature (Code = 4095d).*

注意：除非另有说明，TA = +25°C，VDD = +5.0V，VSS = 0V，RL = 5 kΩ 至 VSS，CL = 100 pF。

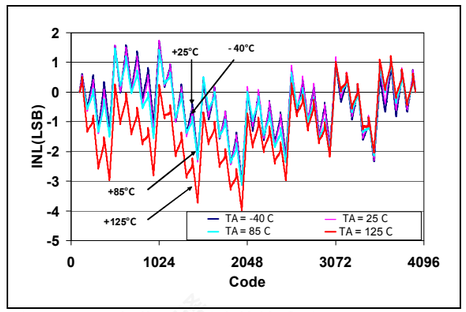


图2-7：INL 与代码和温度的关系（ VDD = 2.7V）。

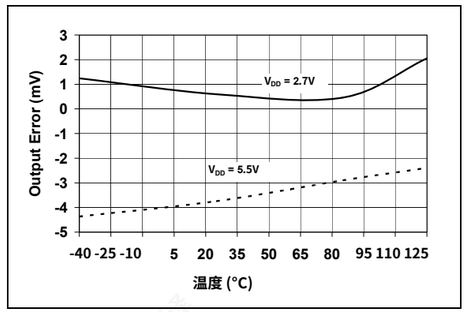


图2-10： 输出误差与温度（代码 = *4000*d）。

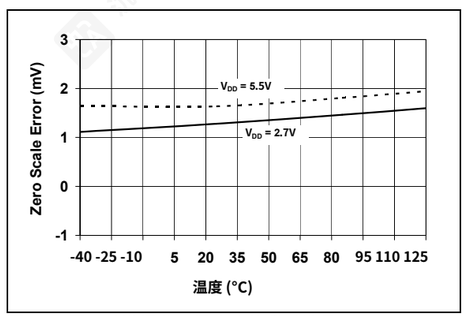


图2-8：零点校准误差与温度的关系（代码 = *000* d）。

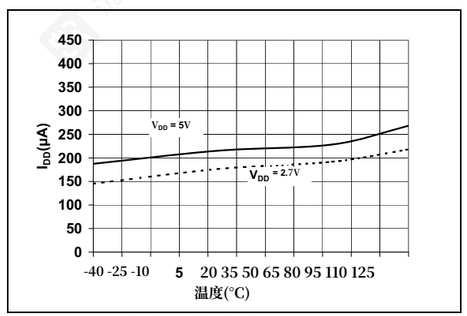


图2-11：IDD与温度的关系。

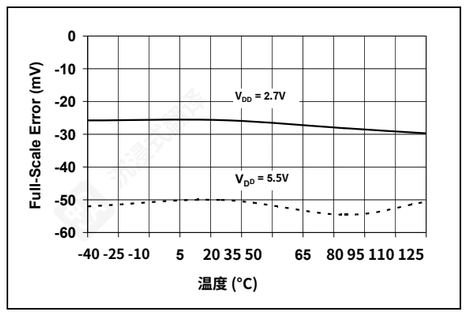


图2-9： 全尺度误差与温度（代码 = *4095*d）。

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

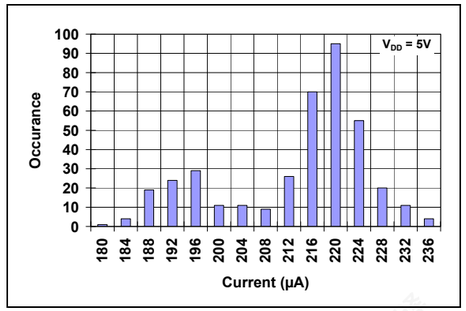


FIGURE 2-12: *I_{DD} Histogram .*

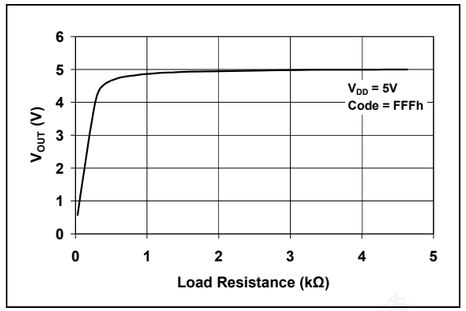


FIGURE 2-15: *V_{OUT} vs. Resistive Load.*

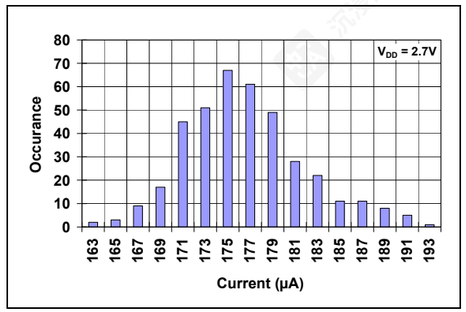


FIGURE 2-13: *I_{DD} Histogram.*

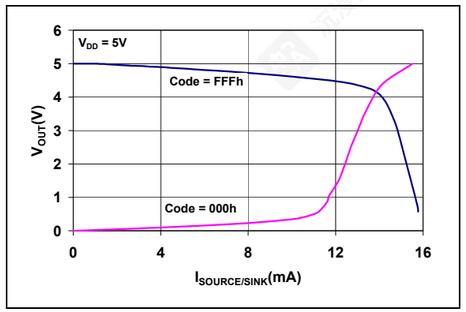


FIGURE 2-16: *Source and Sink Current Capability.*

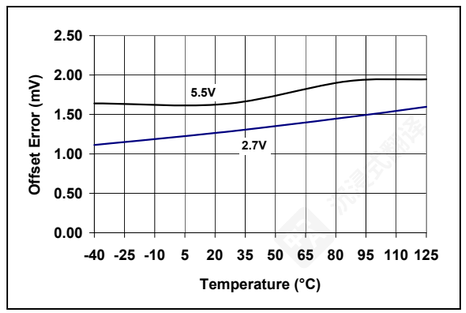


FIGURE 2-14: *Offset Error vs. Temperature and V_{DD}.*

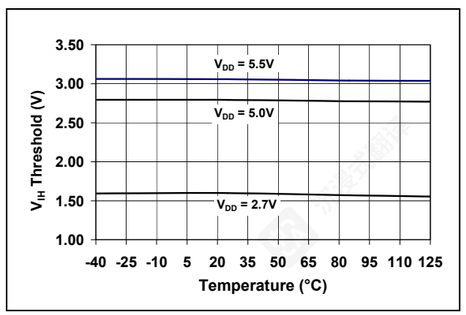


FIGURE 2-17: *V_{IN} High Threshold vs. Temperature and V_{DD}.*

注意：除非另有说明，TA = +25°C，VDD = +5.0V，VSS = 0V，RL = 5 kΩ 至 VSS，CL = 100 pF。

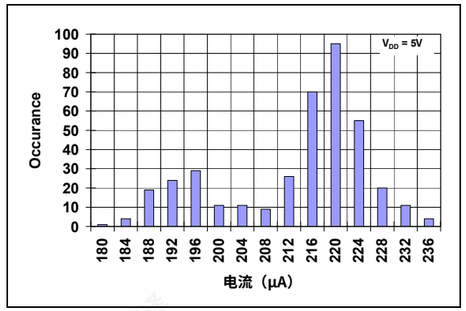


图 2-12: IDD 直方图。

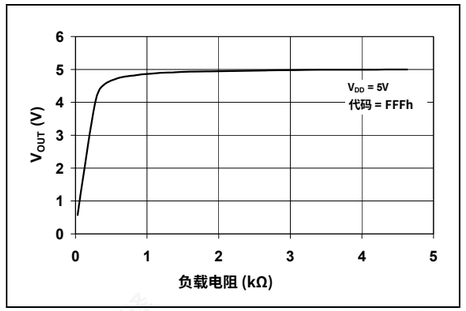


图2-15: VOUT与阻性负载的关系。

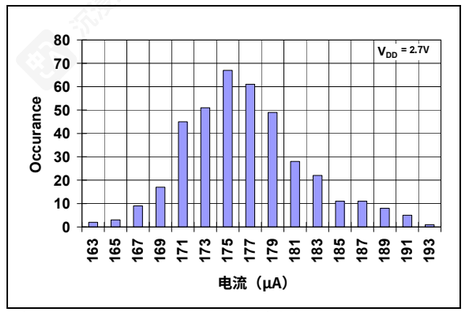


图2-13: IDD直方图。

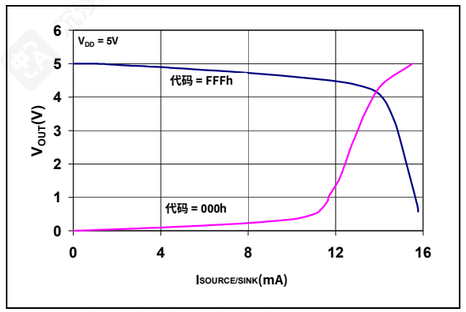


图2-16：源极和漏极电流能力。

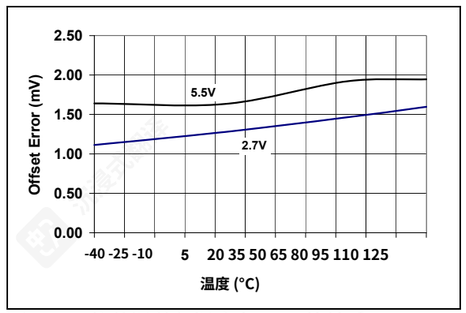


图2-14：偏移误差与温度和VDD的关系。

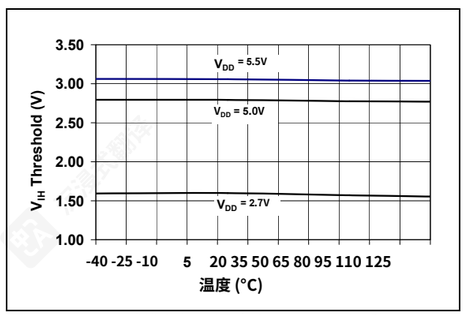


图2-17：VIN高阈值与温度和VDD的关系。

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

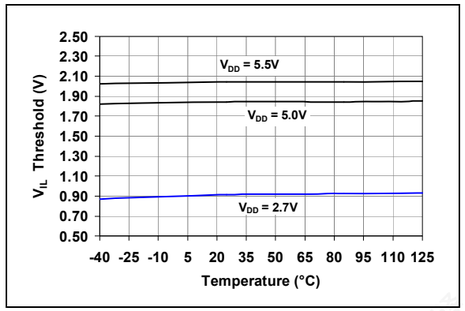


FIGURE 2-18: *V_{IN} Low Threshold vs. Temperature and V_{DD}.*

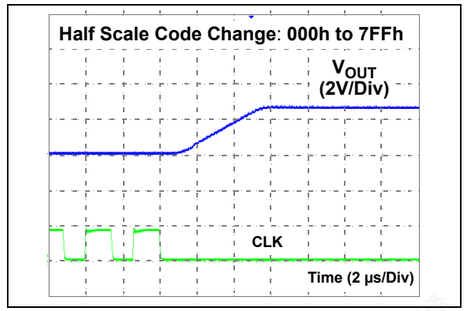


FIGURE 2-21: *Half Scale Settling Time.*

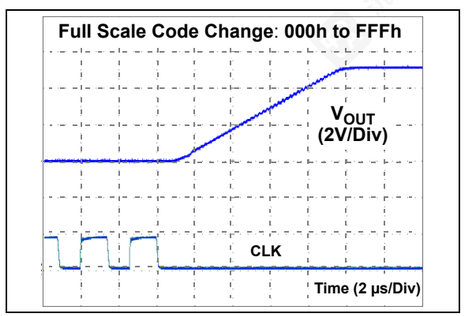


FIGURE 2-19: *Full Scale Settling Time.*

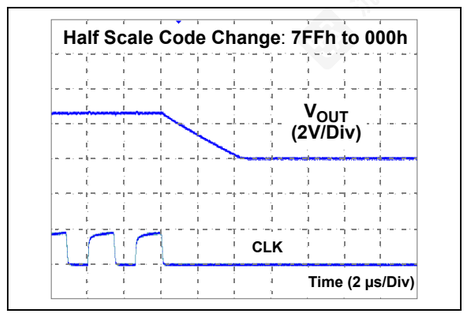


FIGURE 2-22: *Half Scale Settling Time.*

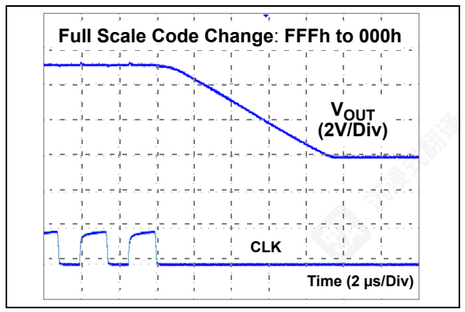


FIGURE 2-20: *Full Scale Settling Time.*

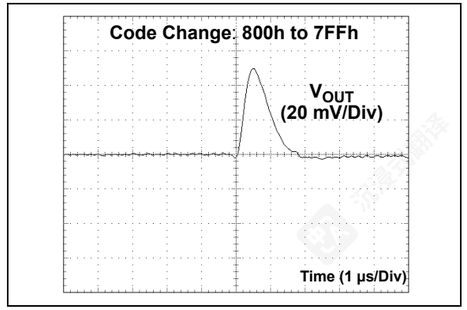


FIGURE 2-23: *Code Change Glitch.*

注意：除非另有说明，TA = +25°C，VDD = +5.0V，VSS = 0V，RL = 5 kΩ 至 VSS，CL = 100 pF。

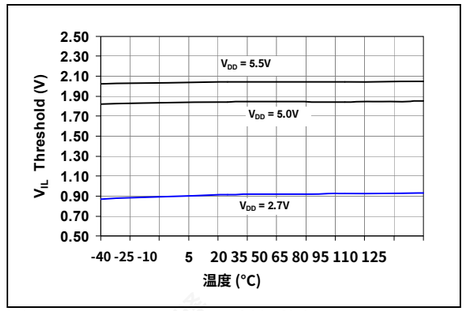


图2-18: VIN低阈值与温度和VDD

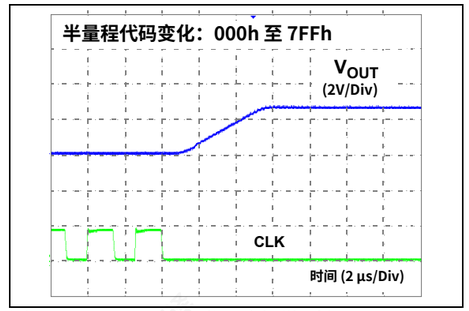


图2-21: 半尺度沉降时间。

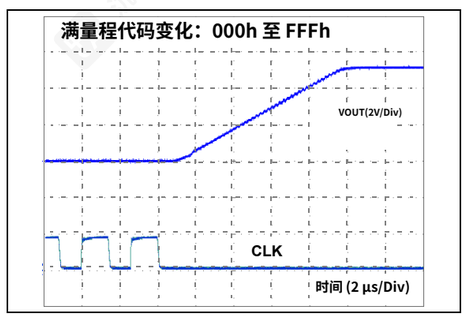


图2-19: 满量程建立时间。

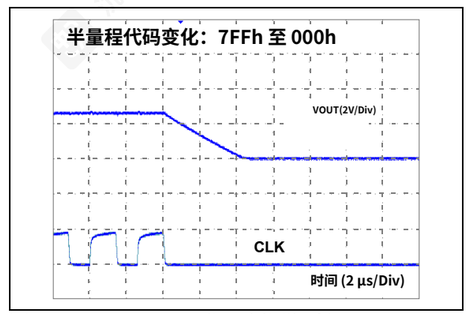


图2-22: 半尺度沉降时间。

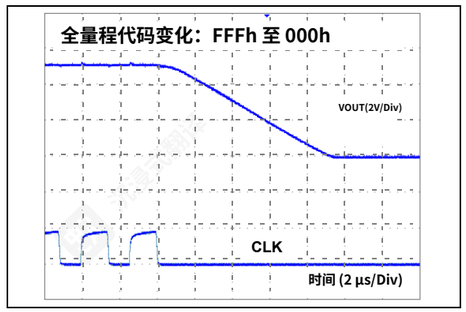


图2-20: 满量程建立时间。

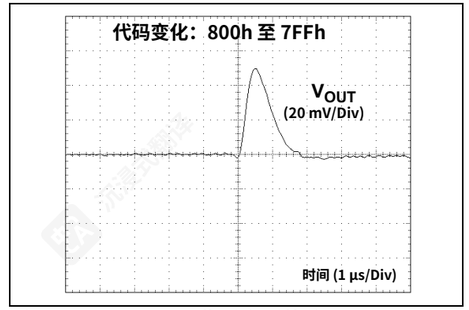


图2-23: 代码变更故障。

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

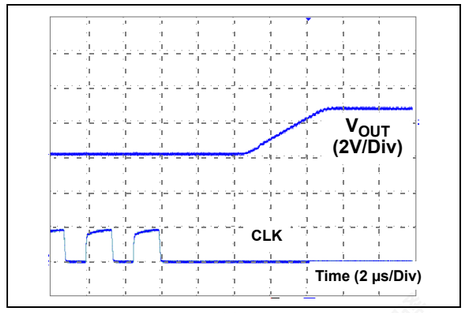


FIGURE 2-24: *Exiting Power Down Mode.*

注意：除非另有说明，TA = +25°C，VDD = +5.0V，VSS = 0V，RL = 5 kΩ 至 VSS，CL = 100 pF。

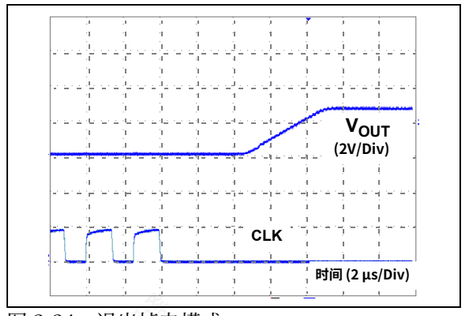


图 2-24：退出掉电模式。

NOTES:.

备注：.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP4725 SOT-23	Name	Description
1	V_{OUT}	Analog Output Voltage
2	V_{SS}	Ground Reference
3	V_{DD}	Supply Voltage
4	SDA	I^2C Serial Data
5	SCL	I^2C Serial Clock Input
6	A0	I^2C Address Bit Selection pin (A0 bit). This pin can be tied to V_{SS} or V_{DD}, or can be actively driven by the digital logic levels. The logic state of this pin determines what the A0 bit of the I^2C address bits should be.

3.1 Analog Output Voltage (V_{OUT})

V_{OUT} is an analog output voltage from the DAC device. DAC output amplifier drives this pin with a range of V_{SS} to V_{DD}.

3.2 Supply Voltage (V_{DD} or V_{SS})

V_{DD} is the power supply pin for the device. The voltage at the V_{DD} pin is used as the supply input as well as the DAC reference input. The power supply at the V_{DD} pin should be clean as possible for a good DAC performance.

This pin requires an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in application boards. The supply voltage (V_{DD}) must be maintained in the 2.7V to 5.5V range for specified operation.

V_{SS} is the ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC register and EEPROM data. The SDA pin is an open-drain N-chan nel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin. Except for START and STOP conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 7.0 "I^2C Serial Interface Communication"** for more details of I^2C Serial Interface communication.

3.4 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP4725 acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP4725 occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 7.0 "I^2C Serial Interface Communication"** for more details of I^2C Serial Interface communication.

3.5 Device Address Selection Pin (A0)

This pin is used to select the A0 address bit by the user. The user can tie this pin to V_{SS} (logic '0'), or V_{DD} (logic '1'), or can be actively driven by the digital logic levels, such as the I^2C Master Output. See **Section 7.2 "Device Addressing"** for more details of the address bits.

3.0 引脚描述

引脚的描述列于表 3-1 中。

表3-1：引脚功能表

MCP4725 SOT-23	Name	描述
1	V_{OUT}	模拟输出电压
2	V_{SS}	接地参考
3	V_{DD}	供电电压
4	SDA	I^2C串行数据
5	SCL	I^2C串行时钟输入
6	A0	I^2C地址位选择引脚（A0位）。该引脚可以连接到VSS或VDD，也可以由数字逻辑电平主动驱动。该引脚的逻辑状态决定了I^2C地址位中的A0位应该是何值。

3.1 模拟输出电压 (VOUT)

V_{OUT} 是来自DAC设备的模拟输出电压。DAC输出放大器以VSS到VDD的范围驱动此引脚。

3.2 电源电压（VDD或VSS）

VDD是设备的电源引脚。电压
此引脚需要一个约0.1 µF（陶瓷）的旁路电容接地。此外，建议并联一个10 µF的电容（钽电容）以进一步衰减应用板上存在的高频噪声。电源电压（VDD）必须在2.7V至5.5V的范围内才能正常工作。

VSS是设备的接地引脚和电流返回路径。用户必须通过低阻抗连接将VSS引脚连接到地平面。如果应用PCB（印刷电路板）中有模拟接地路径，强烈建议将VSS引脚连接到模拟接地路径，或在电路板的模拟接地平面上隔离。

VSS是设备的接地引脚和电流返回路径。用户必须通过低阻抗连接将VSS引脚连接到地平面。如果应用PCB（印刷电路板）中有模拟接地路径，强烈建议将VSS引脚连接到模拟接地路径，或在电路板的模拟接地平面上隔离。

3.3 串行数据引脚 (SDA)

SDA是I^2C接口的串行数据引脚。SDA引脚用于写入或读取DAC寄存器和EEPROM数据。SDA引脚是一个开漏N通道驱动器。因此，它需要从VDD线到SDA引脚一个上拉电阻。除START和STOP条件外，SDA引脚上的数据在时钟的高电平期间必须保持稳定。SDA引脚的高电平或低电平状态只能在SCL引脚上的时钟信号为低电平时改变。有关I^2C串行接口通信的更多详细信息，请参阅第7.0节“I^2C串行接口通信”。

3.4 串行时钟引脚 (SCL)

SCL 是 I^2C 接口的串行时钟引脚。MCP4725 仅作为从设备工作，其 SCL 引脚只接受外部串行时钟。主设备的输入数据在 SCL 时钟的上升沿被移入 SDA 引脚，而 MCP4725 的输出则发生在 SCL 时钟的下降沿。SCL 引脚是一个开漏 N 沟道驱动器。因此，它需要从 VDD 线到 SCL 引脚的一个上拉电阻。有关 I^2C 串行接口通信的更多详细信息，请参阅第 7.0 节“I^2C 串行接口通信”。

3.5 设备地址选择引脚 (A0)

此引脚用于用户选择 A0 地址位。用户可以将此引脚连接到 VSS（逻辑‘0’），或 VDD（逻辑‘1’），或者可以被数字逻辑电平主动驱动，例如 I^2C 主机输出。有关地址位更详细的信息，请参阅第 7.2 节“设备寻址”。

NOTES:

注意：

4.0 TERMINOLOGY

4.1 Resolution

The resolution is the number of DAC output states that divide the full scale range. For the 12-bit DAC, the resolution is 2^{12} or the DAC code ranges from 0 to 4095.

4.2 LSB

The least significant bit or the ideal voltage difference between two successive codes.

EQUATION 4-1:

$$LSB_{Ideal} = \frac{V_{REF}}{2^n} = \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{2^n - 1}$$

Where:

V_{REF} = The reference voltage = V_{DD} in the MCP4725. This V_{REF} is the ideal full scale voltage range

n = The number of digital input bits. (n = 12 for MCP4725)

4.3 Integral Nonlinearity (INL) or Relative Accuracy

INL error is the maximum deviation between an actual code transition point and its corresponding ideal transition point (straight line). Figure 2-5 shows the INL curve of the MCP4725. The end-point method is used for the calculation. The INL error at a given input DAC code is calculated as:

EQUATION 4-2:

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

V_{Ideal} = Code*LSB

V_{OUT} = The output voltage measured at the given input code

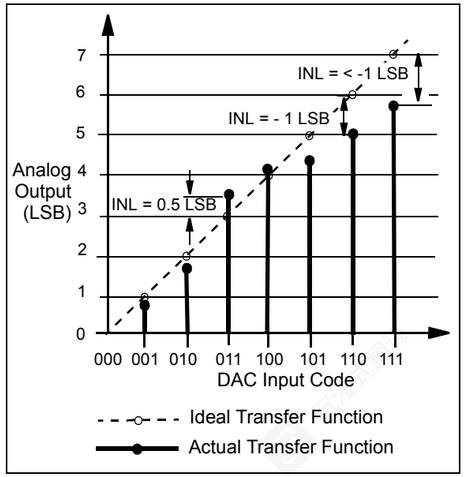


FIGURE 4-1: *INL Accuracy.*

4.4 Differential Nonlinearity (DNL)

Differential nonlinearity error (Figure 4-2) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSB. A DNL error of zero would imply that every code is exactly 1 LSB wide. If the DNL error is less than 1 LSB, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

EQUATION 4-3:

$$DNL = \frac{\Delta V_{OUT} - LSB}{LSB}$$

Where:

ΔV_{OUT} = The measured DAC output voltage difference between two adjacent input codes.

4.0 术语

4.1 分辨率

分辨率是DAC输出状态的数量，用于划分满量程范围。对于12位DAC，分辨率是2^12，即DAC代码范围从0到4095。

4.2 LSB

最低有效位或两个连续代码之间的理想电压差。

公式 4-1：

$$LSB_{Ideal} = \frac{V_{REF}}{2^n} = \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{2^n - 1}$$

其中：

V_{REF} = MCP4725 中的参考电压 = VDD。此 VREF 是理想的满量程电压范围

n = 数字输入位数。 (n = 12 for MCP4725)

4.3 积分非线性度（INL）或相对精度

INL 误差是指实际代码转换点与其对应的理想转换点（直线）之间的最大偏差。图 2-5 显示了 MCP4725 的 INL 曲线。计算采用端点法。给定输入 DAC 代码处的 INL 误差计算如下：

公式 4-2：

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

其中：

$V_{理想}$ = 代码*LSB

V_{OUT} = 在测量给定的输入代码

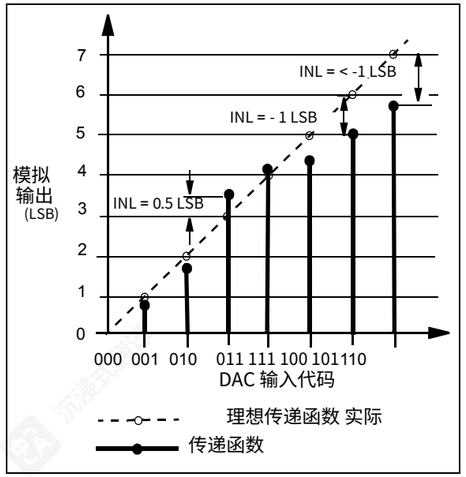


图4-1: INL精度。

4.4 差分非线性度（DNL）

差分非线性误差（图4-2）是实际传递函数中码之间步长的度量。码之间的理想步长为1 LSB。零DNL误差意味着每个码的宽度正好是1 LSB。如果DNL误差小于1 LSB，DAC保证输出单调且无缺失码。任意两个相邻码之间的DNL误差计算方法如下：

公式4-3：

$$DNL = \frac{\Delta V_{OUT} - LSB}{LSB}$$

其中：

ΔV_{OUT} = 两个相邻输入代码之间测量的DAC输出电压差。

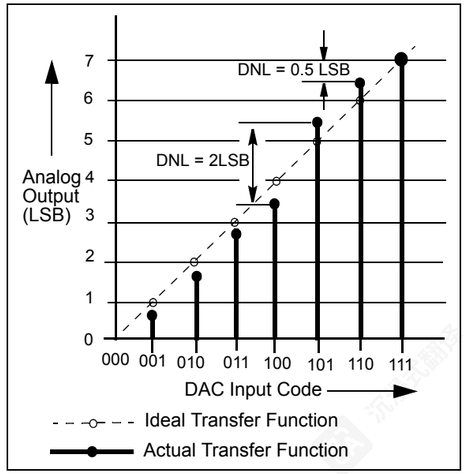


FIGURE 4-2: *DNL Accuracy.*

4.5 Offset Error

Offset error (Figure 4-3) is the deviation from zero voltage output when the digital input code is zero. This error affects all codes by the same amount. In the MCP4725, the offset error is not trimmed at the factory. However, it can be calibrated by software in application circuits.

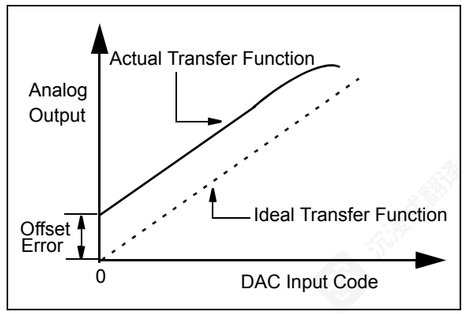


FIGURE 4-3: *Offset Error.*

4.6 Gain Error

Gain error (see Figure 4-4) is the difference between the actual full scale output voltage from the ideal output voltage on the transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full scale range (% of FSR) or in LSB.

In the MCP4725, the gain error is not calibrated at the factory and most of the gain error is contributed by the output op amp saturation near the code range beyond 4000. For the applications which need the gain error specification less than 1% maximum, the user may consider using the DAC code range between 100 and 4000 instead of using full code range (code 0 to 4095). The DAC output of the code range between 100 and 4000 is much linear than full scale range (0 to 4095). The gain error can be calibrated by software in applications.

4.7 Full Scale Error (FSE)

Full scale error (Figure 4-4) is the sum of offset error plus gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh).

EQUATION 4-4:

$$FSE = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

V_{Ideal} = $(V_{REF})\ (1 - 2^{-n}) - V_{OFFSET}$

V_{REF} = The reference voltage. $V_{REF} = V_{DD}$ in the MCP4725

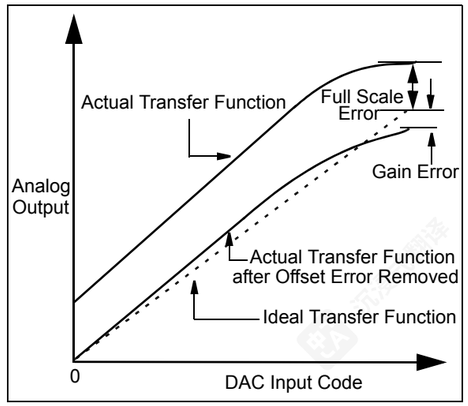


FIGURE 4-4: *Gain Error and Full Scale Error.*

4.8 Gain Error Drift

Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C.

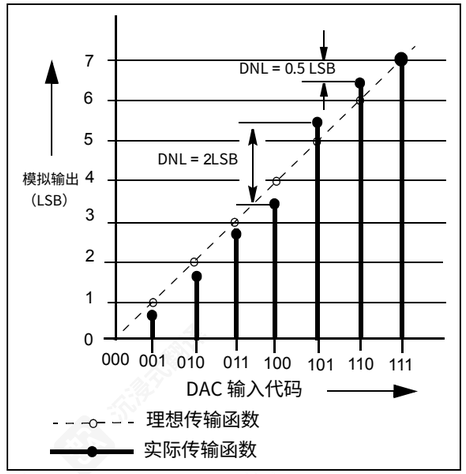


图4-2: DNL精度。

4.5 偏移误差

失调误差（图4-3）是指数字输入码为零时偏离零电压输出的偏差。该误差以相同量影响所有码。在MCP4725中，失调误差在工厂不进行校准。但在应用电路中可以通过软件进行校准。

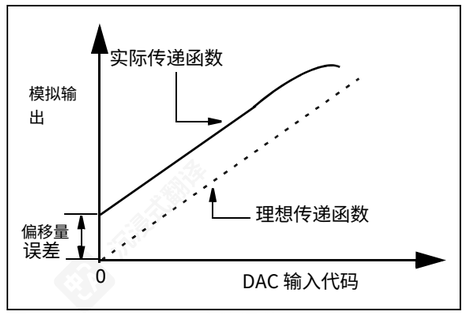


图4-3: 偏移误差。

4.6 增益误差

增益误差（见图4-4）是指实际满量程输出电压与转移特性曲线上的理想输出电压之间的差值。增益误差是在抵消偏移误差后计算的，即满量程误差减去偏移误差。

增益误差表示实际传递函数的斜率与理想传递函数的斜率匹配的程度。增益误差通常以满量程范围百分比（% FSR）或LSB表示。

在MCP4725中，增益误差在工厂未校准，大部分增益误差是由代码范围超过4000时输出运算放大器饱和引起的。对于需要增益误差规格小于1%最大值的应用，用户可以考虑使用100到4000的DAC代码范围，而不是使用全代码范围（0到4095）。100到4000的代码范围的DAC输出比0到4095的满量程范围线性度更高。增益误差可以在应用中通过软件校准。

4.7 满量程误差（FSE）

满量程误差（见图4-4）是偏移误差与增益误差之和。它是理想输出电压与所有位设置为1（DAC输入代码 = FFFh）时的测量DAC输出电压之间的差值。

公式 4-4：

$$FSE = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

其中：

VIdeal = (VREF) (1 - 2-n) - VOFFSET

V_{REF} = 参考电压。VREF = VDD 在 MCP4725 中

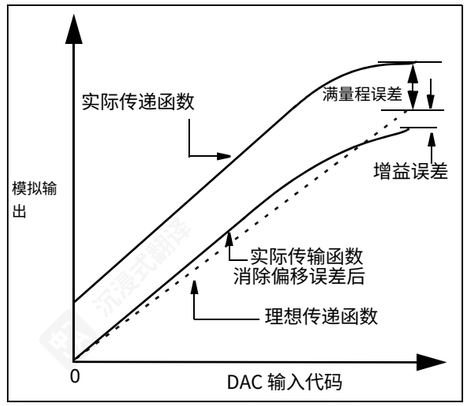


图 4-4: 增益误差和满量程误差。

4.8 增益误差漂移

增益误差漂移是指由于环境温度变化导致的增益误差的变化。增益误差漂移通常以 ppm/oC 表示。

4.9 Offset Error Drift

Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/^{o}C.

4.10 Settling Time

The Settling time is the time delay required for the DAC output to settle to its new output value from the start of code transition, within specified accuracy. In the MCP4725, the settling time is a measure of the time delay until the DAC output reaches its final value (within 0.5 LSB) when the DAC code changes from 400h to C00h.

4.11 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec. and is measured when the digital code is changed by 1 LSB at the major carry transition (Example: 011...111 to 100... 000, or 100... 000 to 011 ... 111).

4.12 Digital Feedthrough

Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. It is specified in nV-Sec. and is measured with a full scale change on the digital input pins (Example: 000... 000 to 111... 111, or 111... 111 to 000... 000). The digital feedthrough is measured when the DAC is not being written to the register.

4.9 偏移误差漂移

失调误差漂移是指由于环境温度变化导致的失调误差的变化。失调误差漂移通常以 ppm/oC 表示。

4.10 建立时间

建立时间是指DAC输出从代码转换开始到达到其新输出值所需的时间延迟，且需在指定精度范围内。在MCP4725中，建立时间是衡量DAC代码从400h变化到C00h时，DAC输出达到最终值（误差在0.5 LSB以内）所需的时间延迟。

4.11 主要代码转换毛刺

主要代码转换毛刺是指当DAC寄存器中的代码状态发生变化时，注入到DAC模拟输出端的脉冲能量。通常以nV-秒为单位指定其面积，并在数字代码在主要进位转换时变化1 LSB时进行测量（例如：011...111到100...000，或100...000到011...111）。

4.12 数字馈通

数字馈通是指设备数字输入引脚耦合导致的模拟输出端出现的故障。它被规定在nV-Sec.中，并通过数字输入引脚的全量程变化进行测量（例如：000... 000到111... 111，或111... 111到000... 000）。当DAC未被写入寄存器时测量数字馈通。

NOTES:

备注：

5.0 GENERAL DESCRIPTION

The MCP4725 is a single channel buffered voltage output 12-bit DAC with non-volatile memory (EEPROM). The user can store configuration register bits (2 bits) and DAC input data (12 bits) in non-volatile EEPROM (14 bits) memory.

When the device is powered on first, it loads the DAC code from the EEPROM and outputs the analog output accordingly with the programmed settings. The user can reprogram the EEPROM or DAC register any time.

The device uses a resistor string architecture. DAC's output is buffered with a low power precision amplifier. This output amplifier provides low offset voltage and low noise, as well as rail-to-rail output. The amplifier can also provide high source currents (V_{OUT} pin to V_{SS}).

The DAC can be configured to normal or power saving power-down mode by setting the configuration register bits.

The device uses a two-wire I^2C compatible serial interface and operates from a single power supply ranging from 2.7V to 5.5V.

5.1 Output Voltage

The input coding to the MCP4725 device is unsigned binary. The output voltage range is from 0V to V_{DD}. The output voltage is given in Equation 5-1:

EQUATION 5-1:

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{4096}$$

Where:

V_{REF} = V_{DD}

D_n = Input code

5.1.1 OUTPUT AMPLIFIER

The DAC output is buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to **Section 1.0 "Electrical Characteristics"** for range and load conditions.

The output amplifier can drive the resistive and high capacitive loads without oscillation. The amplifier can provide maximum load current as high as 25 mA which is enough for most of a programmable voltage reference applications.

5.1.2 DRIVING RESISTIVE AND CAPACITIVE LOADS

The MCP4725 output stage is capable of driving loads up to 1000 pF in parallel with 5 kΩ load resistance. Figure 2-15 shows the V_{OUT} vs. Resistive Load. V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ.

5.2 LSB SIZE

One LSB is defined as the ideal voltage difference between two successive codes. (see Equation 4-1). Table 5-1 shows an example of the LSB size over full scale range (V_{DD}).

TABLE 5-1: LSB SIZES FOR MCP4725 (EXAMPLE)

Full Scale Range (V_{DD})	LSB Size	Condition
3.0V	0.73 mV	3V / 4096
5.0V	1.22 mV	5V / 4096

5.3 Voltage Reference

The MCP4725 device uses the V_{DD} as its voltage reference. Any variation or noises on the V_{DD} line can affect directly on the DAC output. The V_{DD} needs to be as clean as possible for accurate DAC performance.

5.4 Reset Conditions

In the Reset conditions, the device uploads the EEPROM data into the DAC register. The device can be reset by two independent events: (a) by POR or (b) by I^2C General Call Reset Command.

The factory default settings for the EEPROM prior to shipment are shown in Table 5-3 (set for a middle scale output). The user can rewrite or read the DAC register or EEPROM anytime after the Power-On-Reset event.

5.4.1 POWER-ON-RESET

The device's internal Power-On-Reset (POR) circuit ensures that the device powers up in a defined state.

If the power supply voltage is less than the POR threshold (V_{POR} = 2V, typical), all circuits are disabled and there will be no DAC output. When the V_{DD} increases above the V_{POR}, the device takes a reset state. During the reset period, the device uploads all configuration and DAC input codes from EEPROM. The DAC output will be the same as for the value last stored in the EEPROM. This enables the device returns to the same state that it was at the last write to the EEPROM before it was powered off.

5.0 概述

MCP4725 是一款单通道缓冲电压输出 12 位 DAC，具有非易失性存储器（EEPROM）。用户可以在非易失性 EEPROM （14 位）存储器中存储配置寄存器位（2 位）和 DAC 输入数据（12 位）。

设备首次上电时，会从 EEPROM 加载 DAC 代码，并根据编程设置输出相应的模拟输出。用户可以随时重新编程 EEPROM 或 DAC 寄存器。

该设备采用电阻串架构。DAC的输出通过低功耗精密放大器进行缓冲。该输出放大器提供低失调电压、低噪声，以及轨到轨输出。该放大器还可以提供高源电流（VOUT引脚到VSS）。

通过设置配置寄存器位，可以将DAC配置为正常模式或省电模式。

该设备使用兼容I^2C的两线串行接口，并工作在2.7V至5.5V的单电源下。

5.1 输出电压

MCP4725设备的输入编码为无符号二进制。输出电压范围为0V至VDD。输出电压由公式5-1给出：

公式5-1：

$$V_{OUT} = \frac{V_{REF} \times D_n}{4096}$$

其中：

V_{REF} = V_{DD}

D_n = 输入代码

5.1.1 输出放大器

DAC 输出通过一个低功耗、高精度的 CMOS 放大器进行缓冲。该放大器提供低失调电压和低噪声。输出级使设备能够在接近电源轨的输出电压下工作。有关范围和负载条件，请参阅第 1.0 节“电气特性”。

输出放大器可以在不振荡的情况下驱动阻性和大电容负载。该放大器可提供高达 25 mA 的最大负载电流，足以满足大多数可编程电压基准应用的需求。

5.1.2 驱动阻性和容性负载

MCP4725 输出级能够驱动并联 5 kΩ 负载电阻的 1000 pF 负载。图 2-15 展示了 VOUT 与阻性负载的关系。当负载电阻在 3.5 kΩ 以下时，VOUT 会缓慢下降。

5.2 LSB 尺寸

一个 LSB 定义为两个连续代码之间的理想电压差
在两个连续代码之间 .(参见公式4-1) .
表5-1显示了在完整量程范围（VDD）下的LSB大小示例。

表5-1：MCP4725的LSB大小（示例）

满量程范围（VDD）	LSB Size	条件
3.0V	0.73 mV	3V / 4096
5.0V	1.22 mV	5V / 4096

5.3电压参考

MCP4725器件使用VDD作为其电压
参考VDD线上的任何变化或噪声都会直接影响DAC输出。
为了获得准确的DAC性能，VDD需要尽可能干净。

5.4 复位条件

在复位条件下，设备将EEPROM数据上传到DAC寄存器。
设备可以
被复位b y 两个 p独立事件： (a) 由 POR 或 (b) 由 I^2C通用复位命令。

发货前 EEPROM 的工厂默认设置如表 5-3 所示（设置为中间量程输出）。用户可以在 Power-On-Reset 事件之后随时重写或读取 DAC 寄存器
或 EEPROM 在 Power-On-Reset 事件之后任何时候 .

5.4.1 上电复位

设备的内部上电复位 (POR) 电路确保设备以定义的状态上电。

如果电源电压低于上电复位阈值（VPOR = 2V，典型值），所有电路将被禁用和
不会有DAC输出VPOR时，设备进入复位状态。在复位期间，设备会从EEPROM中上传所有配置和DAC输入代码。DAC输出将与EEPROM中最后存储的值相同。这使设备能够恢复到断电前最后一次写入EEPROM时的状态。

5.4.2 V_{DD} RAMP RATE AND EEPROM

The MCP4725 uploads the EEPROM data to the DAC register during power-up sequence. However, if the V_{DD} ramp rate is too slow (<1 V/ms), the device may not be able to load the EEPROM data to the DAC register. Therefore, the DAC output that is corresponding to the current EEPROM data may not available to the output pin. It is highly recommended to send a General Call Reset Command (see **Section 7.3.1 "General call reset"**) after power-up. This command will reset the device at a stable V_{DD} and make the DAC output available immediately using the EEPROM data.

5.5 Normal and Power-Down Modes

The device has two modes of operation: Normal mode and power-down mode. The mode is selected by programming the power-down bits (PD1 and PD0) in the Configuration register. The user can also program the two power-down bits in non-volatile EEPROM memory.

When the normal mode is selected, the device operates a normal digital-to-analog conversion. If the power-down mode is selected, the device enters a power saving condition by shutting down most of the internal circuits. During the power-down mode, all internal circuits except the I^2C interface are disabled and there is no data conversion event, and no V_{OUT} is available. The device also switches the output stage from the output of the amplifier to a known resistive load. The value of the resistive load is determined by the state of the power-down bits (PD1 and PD0). Table 5-2 shows the outcome of the power-down bit and the resistive load.

During the power-down mode, the device draws about 60 nA (typical). Although most of internal circuits are shutdown, the serial interface remains active in order to receive the I^2C command.

The device exits the power-down mode immediately when (a) it receives a new write command for normal mode or (b) it receives an I^2C General Call Wake-Up Command.

When the DAC operation mode is changed from power-down to normal mode, the output settling time takes less than 10 µs, but greater than the standard Active mode settling time (6 µs, typical).

TABLE 5-2: POWER-DOWN BITS

PD1	PD0	Function
0	0	Normal Mode
0	1	1 kΩ resistor to ground (1)
1	0	100 kΩ resistor to ground (1)
1	1	500 kΩ resistor to ground (1)

Note 1: In the power-down mode: V_{OUT} is off and most of internal circuits are disabled.

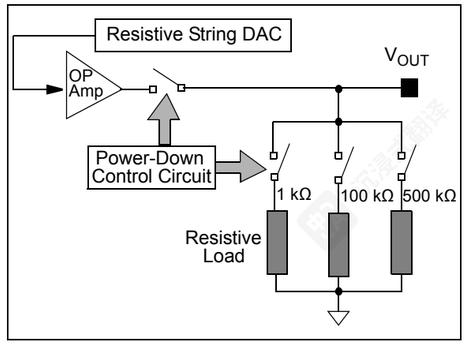


FIGURE 5-1: *Output Stage for Power-Down Mode.*

5.4.2 VDD RAMP RATE 和 EEPROM

MCP4725在上电序列期间将EEPROM数据上传到DAC寄存器。但如果VDD斜升速率过慢（<1 V/ms），设备可能无法将EEPROM数据加载到DAC寄存器。因此，当前EEPROM数据对应的DAC输出可能无法出现在输出引脚上。强烈建议在上电后发送通用复位命令（参见第7.3.1节“通用复位”）。该命令将在稳定的VDD下复位设备，并立即使用EEPROM数据使DAC输出可用。

5.5 正常模式和掉电模式

该设备有两种工作模式：正常模式和掉电模式。模式由配置寄存器中的掉电位（PD1和PD0）选择。用户也可以在非易失性EEPROM存储器中编程这两个掉电位。

当选择正常模式时，设备执行正常的数模转换。如果选择掉电模式，设备通过关闭大部分内部电路进入省电状态。在掉电模式下，除I^2C接口外所有内部电路均被禁用，没有数据转换事件，且无VOUT输出。设备还将输出级从放大器输出切换到已知阻性负载。阻性负载的值由掉电位（PD1和PD0）的状态决定。表5-2显示了掉电位和阻性负载的结果。

在掉电模式下，设备约消耗60 nA（典型值）。虽然大部分内部电路已关闭，但串行接口保持激活状态以接收I^2C命令。

当设备接收到（a）正常模式的新的写命令或（b）I^2C通用唤醒命令时，会立即退出掉电模式。

当 DAC 工作模式从掉电模式切换到正常模式时，输出建立时间小于 10 µs，但大于标准主动模式建立时间（典型值为 6 µs）。

表 5-2：掉电位

PD1	PD0	功能
0	0	普通模式
0	1	1 kΩ 电阻接地（1）
1	0	100 kΩ 电阻接地（1）
1	1	500 kΩ 电阻接地（1）

注意 1： 在掉电模式下：VOUT 断电且大部分内部电路已禁用 .

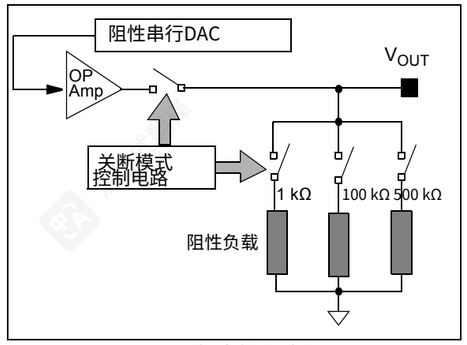


图 5-1: 掉电模式输出级。

5.6 Non-Volatile EEPROM Memory

The MCP4725 device has a 14-bit wide EEPROM memory to store configuration bit (2 bits) and DAC input data (12 bits). These bits are readable and re-writable with I^2C interface commands. The device has an on-chip charge pump circuit to write the EEPROM memory bits without using an external program voltage.

The EEPROM writing operation is initiated when the device receives an EEPROM write command (C2 = 0, C1 = 1, C0 = 1). The configuration and writing data bits are transferred to the EEPROM memory block. A status bit, RDY/$\overline{BSY}$, stays low during the EEPROM writing and goes high as the write operation is completed. While the RDY/$\overline{BSY}$ bit is low (during the EEPROM writing), any new write command is ignored (for EEPROM or DAC register). Table 5-3 shows the EEPROM bits and factory default settings. Table 5-4 shows the DAC input register bits of the MCP4725.

TABLE 5-3: EEPROM MEMORY AND FACTORY DEFAULT SETTINGS (TOTAL NUMBER OF BITS: 14 BITS)

Bit Name	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Power-Down Select (2 bits)		DAC Input Data (12 bits)											
Factory Default Value	0	0 (1)	1 (2)	0	0	0	0	0	0	0	0	0	0	0

Note 1: See Table 5-2 for details.

2: Bit D11 = '1' (while all other bits are "0") enables the device to output 0.5 * V_{DD} (= middle scale output).

TABLE 5-4: DAC REGISTER

Bit Name	C2	C1	C0	RDY/$\overline{BSY}$	POR	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Command Type			(1)		Power-Down Select		Data (12 bits)											

Note 1: Write EEPROM status indication bit (0:EEPROM write is not completed. 1:EEPROM write is complete.)

5.6 非易失性EEPROM存储器

MCP4725设备具有一个14位宽的EEPROM存储器，用于存储配置位（2位）和DAC输入数据（12位）。这些位可通过I^2C接口命令进行读取和重写。该设备内置了一个电荷泵电路，可以在不使用外部程序电压的情况下写入EEPROM存储器位。

EEPROM 写入操作在设备接收到 EEPROM 写入命令（C2 = 0, C1 = 1, C0 = 1）时启动。配置和写入数据位被传输到 EEPROM 内存块。状态位 RDY/BSY 在 EEPROM 写入期间保持低电平，写入操作完成时变为高电平。当 RDY/BSY 位为低（EEPROM 写入期间），任何新的写入命令都会被忽略（针对 EEPROM 或 DAC 寄存器）。表 5-3 显示了 EEPROM 位和工厂默认设置。表 5-4 显示了 MCP4725 的 DAC 输入寄存器位。

表 5-3：EEPROM存储器和工厂默认设置（总位数：14位）

Bit Name	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit 功能	关机 选择 (2 位)		DAC 输入数据 (12 位)											
工厂默认值	0	0 (1)	1 (2)	0	0	0	0	0	0	0	0	0	0	0

注释1：详情请参见表5-2。

2: 位D11 = '1'（其他所有位均为"0"）使设备能够输出0.5 * VDD (= 中间量程输出)。

表 5-4：DAC寄存器

Bit Name	C2	C1	C0	RDY/$\overline{BSY}$	POR	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit 功能	命令类型			(1)		电源-向下选择		数据（12位）											

注释1： 写入EEPROM状态指示位（0：EEPROM写入未完成。1：EEPROM写入完成。）

NOTES:

注意：

6.0 THEORY OF OPERATION

When the device is connected to the I²C bus line, the device is working as a slave device. The Master (MCU) can write/read the DAC input register or EEPROM using the I²C interface command. The MCP4725 device address contains four fixed bits (1100 = device code) and three address bits (A2, A1, A0). The A2 and A1 bits are hard-wired during manufacturing, and A0 bit is determined by the logic state of A0 pin. The A0 pin can be connected to V_{DD} or V_{SS}, or actively driven by digital logic levels.

The following sections describe the communication protocol to send or read the data code and write/read the EEPROM using the I²C interface. See **Section 7.0 "I²C Serial Interface Communication"**.

6.1 Write Commands

The write commands are used to load the configuration bits and DAC input code to the DAC register, or to write to the EEPROM of the device. The write command types are defined by using three write command type bits (C2, C1, C0). Table 6-2 shows the write command types and their functions. There are three command types for the MCP4725. The four "reserved" commands in Table 6-2 are for future use. The MCP4725 ignores the "reserved" commands. Write command protocol examples are shown in Figure 6-1 and Figure 6-2.

The input data code is coded as shown in Table 6-1. The MSB of the data is always transmitted first and the format is unipolar binary.

TABLE 6-1: INPUT DATA CODING

Input Code	Nominal Output Voltage (V)
111111111111 (FFFh)	V_{DD} - 1 LSB
111111111110 (FFEh)	V_{DD} - 2 LSB
000000000010 (002h)	2 LSB
000000000001 (001h)	1 LSB
000000000000 (000h)	0

6.1.1 WRITE COMMAND FOR FAST MODE (C2 = 0, C1 = 0, C0 = X, X = DON'T CARE)

The fast write command is used to update the DAC register. The data in the EEPROM of the device is not affected by this command. This command updates Power-Down mode selection bits (PD1 and PD0) and 12 bits of the DAC input code in the DAC register. Figure 6-1 shows an example of the fast write command for the MCP4725 device.

6.1.2 WRITE COMMAND FOR DAC INPUT REGISTER (C2 = 0, C1 = 1, C0 = 0)

In MCP4725, this command performs the same function as the Fast Mode command in **Section 6.1.1 "Write Command for Fast mode (C2 = 0, C1 = 0, C0 = X, X = Don't Care)"**. Figure 6-2 shows the write command protocol for the MCP4725.

As shown in Figure 6-2, the D11 - D0 bits in the third and fourth bytes are DAC input data. The last 4 bits (X, X, X, X) in the fourth byte are don't care bits.

The device executes the Master's write command after receiving the last byte (4th byte). The Master can send a STOP bit to terminate the current sequence, or send a Repeated START bit followed by an address byte. If the device receives three data bytes continuously after the 4th byte, it updates from the 2nd to the 4th data bytes with the last three input data bytes.

The contents of the register are updated at the end of the 4th byte. The device ignores any partially received data bytes if the I²C communication with the Master ends before completing the 4th byte.

6.1.3 WRITE COMMAND FOR DAC INPUT REGISTER AND EEPROM (C2 = 0, C1 = 1, C0 = 1)

When the device receives this command, it (a) loads the configuration and data bits to the DAC register, and (b) also writes the EEPROM. When the device is writing the EEPROM, the RDY/BSY bit goes low and stays low until the EEPROM write operation is completed. The state of the RDY/BSY bit can be monitored by a read command. Figure 6-2 shows the details of the this write command protocol and Figure 6-3 shows the details of the read command.

6.0 工作原理

当设备连接到 I²C 总线时，设备作为从设备工作。主设备（MCU）可以使用 I²C 接口命令写入/读取 DAC 输入寄存器或 EEPROM。MCP4725 设备地址包含四位固定位（ 1100 = 设备代码）和三位地址位（A2、A1、A0）。A2 和 A1 位在制造时已固定，A0 位由 A0 引脚的逻辑电平决定。A0 引脚可以连接到 VDD 或 VSS，或由数字逻辑电平主动驱动。

以下部分描述了使用 I²C 接口发送/读取数据代码以及写入/读取 EEPROM 的通信协议。参见第 7.0 节 "I²C 串行接口通信"。

6.1 编写命令

写入命令用于将配置位和DAC输入代码加载到DAC寄存器，或写入设备的EEPROM。写入命令类型由三个写入命令类型位（C2、C1、C0）定义。表6-2显示了写入命令类型及其功能。MCP4725有三种命令类型。表6-2中的四个"保留"命令用于未来使用。MCP4725会忽略"保留"命令。写入命令协议示例显示在图6-1和图6-2中。

输入数据代码如表6-1所示。数据的主位（MSB）总是首先传输，格式为单极性二进制。

表6-1：输入数据编码

输入代码	标称输出电压 (V)
111111111111 (FFFh)	VDD - 1 LSB
111111111110 (FFEh)	VDD - 2 LSB
000000000010 (002h)	2 LSB
000000000001 (001h)	1 LSB
000000000000 (000h)	0

6.1.1 快速模式写入命令（C2 = 0、C1 = 0、C0 =X、X = DON' T CARE）

快速写入命令用于更新DAC寄存器。该命令不会影响设备EEPROM中的数据。此命令会更新DAC寄存器中的掉电模式选择位（PD1和PD0）以及12位DAC输入代码。图6-1展示了MCP4725设备的快速写入命令示例。

6.1.2 DAC输入寄存器写入命令（C2 = 0、C1 = 1、C0 = 0）

在MCP4725中，此命令与第6.1.1节"快速模式写命令(C**2 = 0**, C**1 = 0**, C**0 =**X, X **=**无关位)"中的快速模式命令执行相同的功能。图6-2显示了MCP4725的写命令协议。

如图6-2所示，第三和第四字节的D11 - D0位是DAC输入数据。第四字节中的最后4位(X, X, X, X)是无关位。

设备在接收到最后一个字节(第4个字节)后执行主机的写命令。主机可以发送停止位来终止当前序列，或发送重复启动位后跟一个地址字节。如果设备在第4个字节后连续接收到三个数据字节，它会用最后三个输入数据字节更新第2到第4个数据字节。

寄存器的内容在第四个字节结束时更新。如果与主机的I²C通信在完成第四个字节之前结束，设备会忽略任何部分接收的数据字节。

6.1.3 写入DAC输入寄存器和EEPROM命令（C2 = 0, C1 = 1, C0 = 1）

当设备接收此命令时 , it (a) 加载配置DAC寄存器的配置和数据位，以及（b）还写入EEPROM。当设备正在写入EEPROM时，RDY/BSY位会置低，并保持低电平直到EEPROM写入操作完成。RDY/BSY位的状态可以通过读命令进行监控。图6-2显示了此写入命令协议的详细信息，图6-3显示了读命令的详细信息。

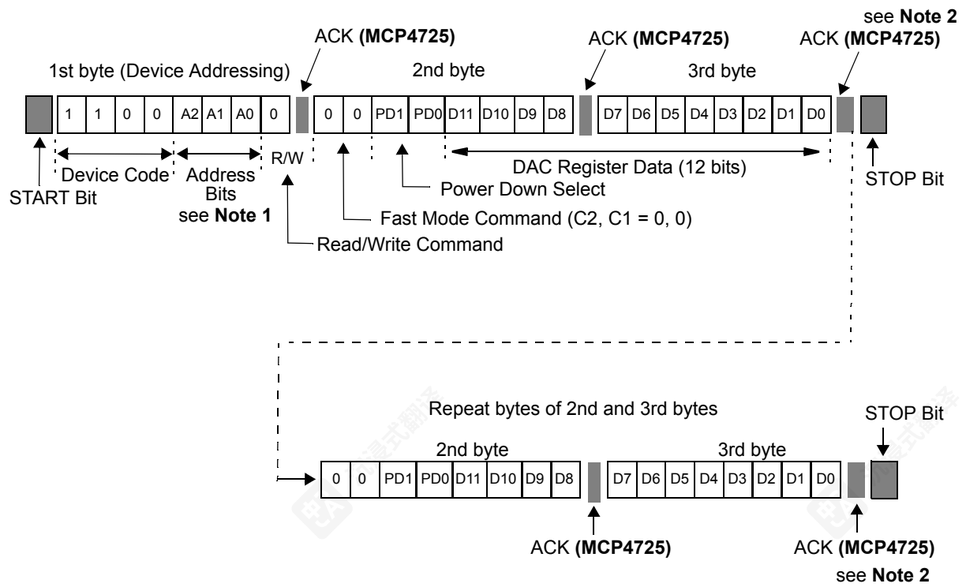
TABLE 6-2: WRITE COMMAND TYPE

C2	C1	C0	Command Name	Function
0	0	X	Fast Mode	This command is used to change the DAC register. EEPROM is not affected
0	0	X	“	“
0	1	0	Write DAC Register	Load configuration bits and data code to the DAC Register
0	1	1	Write DAC Register and EEPROM	(a) Load configuration bits and data code to the DAC Register and (b) also write the EEPROM
1	0	0	Reserved	Reserved for future use
1	0	1	Reserved	Reserved for future use
1	1	0	Reserved	Reserved for future use
1	1	1	Reserved	Reserved for future use

Note 1: X = Dont’ Care. Fast Mode does not use C0 bit.

2: The MCP4725 ignores the “Reserved” commands.

Write DAC Register using Fast Mode Write Command: (C2, C1) = (0, 0)



Note 1: A2 and A1 bits are programmed at the factory by hard-wired, and A0 bit is determined by the logic state of A0 pin.

2: The device updates V_{OUT} at the falling edge of the ACK pulse of the 3rd byte.

FIGURE 6-1: *Fast Mode Write Command.*

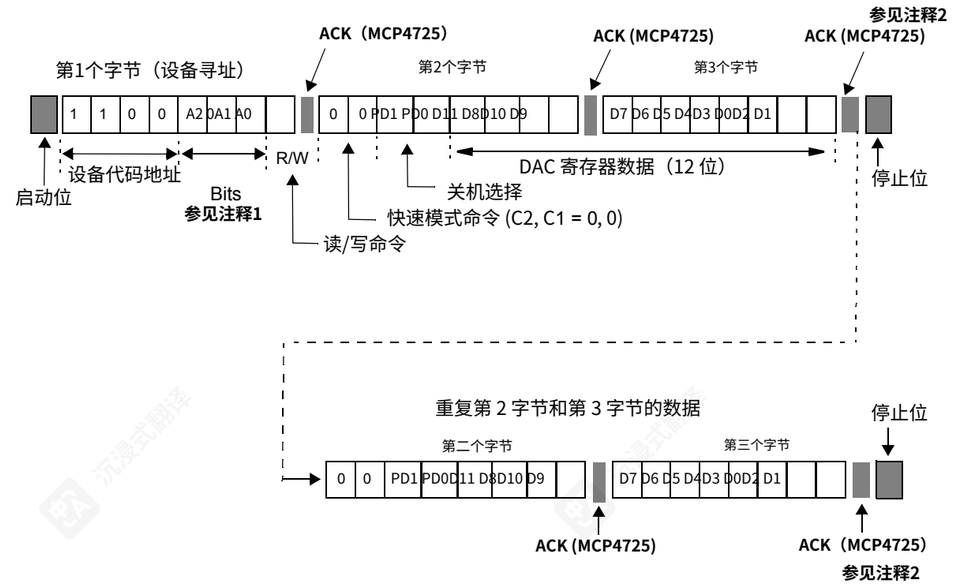
表6-2：写入命令类型

C2	C1	C0	命令名称	功能
0	0	X	快速模式	此命令用于更改DAC寄存器。EEPROM不受影响 影响
0	0	X	“	“
0	1	0	写入DAC寄存器	将配置位和数据代码加载到DAC寄存器
0	1	1	写入DAC寄存器并 EEPROM	(a) 将配置位和数据代码加载到DAC寄存器并 (b) 同时写入EEPROM
1	0	0	保留	保留供将来使用
1	0	1	保留	保留用于未来使用
1	1	0	保留	保留用于未来使用
1	1	1	保留	保留用于未来使用

注意 1：X = 不关心。快速模式不使用 C0 位。

2: MCP4725 会忽略“保留”指令。

使用快速模式写入命令写入 DAC 寄存器：(C2, C1) = (0, 0)



注释1： A2 和 A1 位由工厂通过硬件编程设置，而 A0 位由 A0 引脚的逻辑状态决定确定。

2: 该设备在第三个字节的ACK脉冲下降沿更新VOUT。

图 6-1：快速模式写入命令。

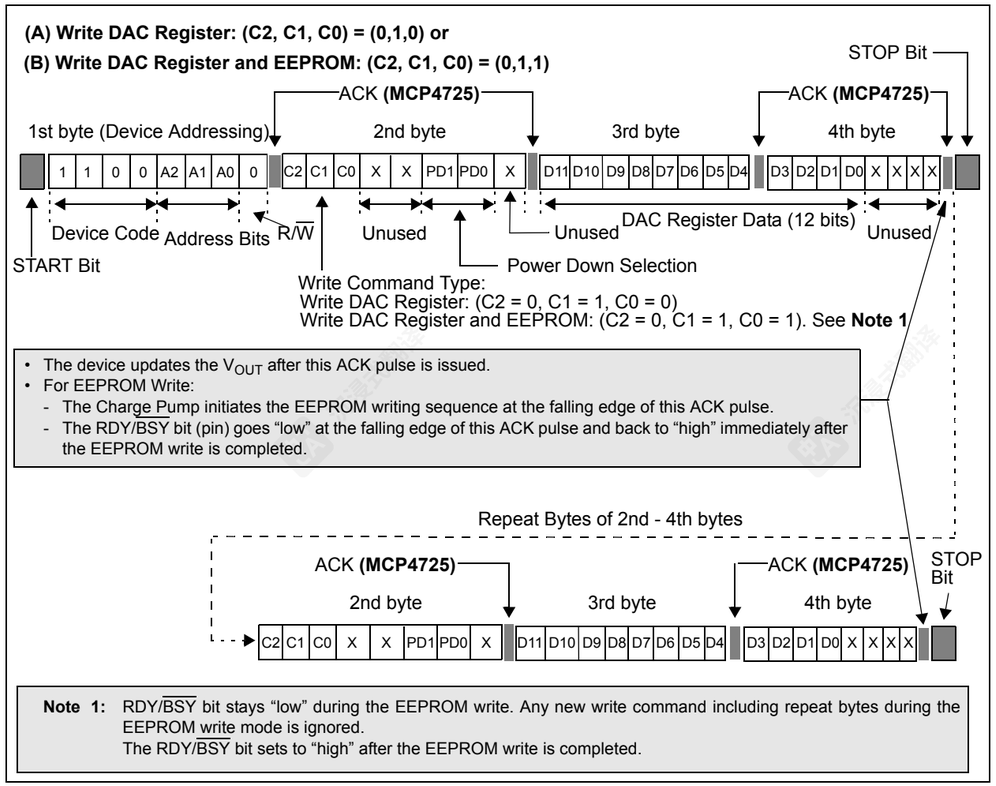


FIGURE 6-2: *Write Commands for DAC Input Register and EEPROM.*

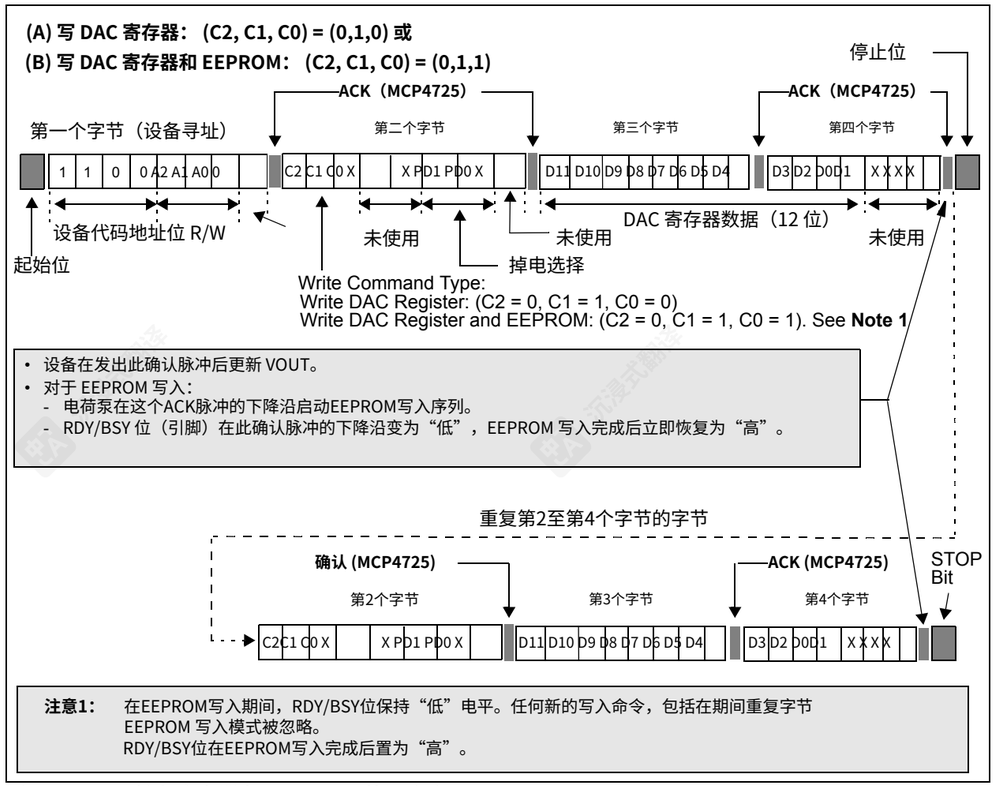
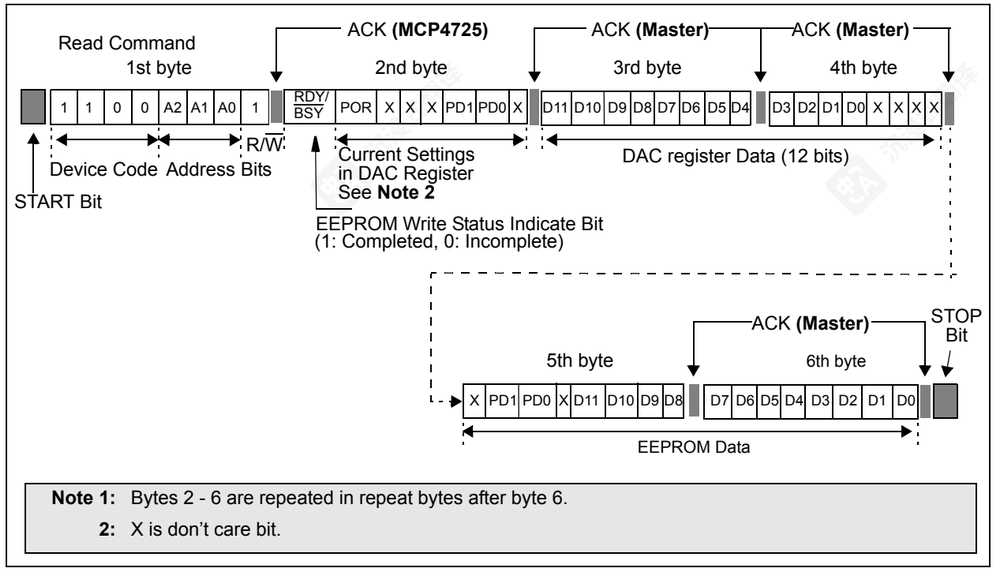


图 6-2：DAC 输入寄存器和 EEPROM 的写命令

6.2 READ COMMAND

If the R/$\overline{W}$ bit is set to a logic “high”, then the device outputs on SDA pin, the DAC register and EEPROM data. Figure 6-3 shows an example of reading the register and EEPROM data. The 2nd byte in Figure 6-3 indicates the current condition of the device operation. The RDY/$\overline{BSY}$ bit indicates EEPROM writing status. The RDY/$\overline{BSY}$ bit stays low during EEPROM writng and high when the writing is completed.

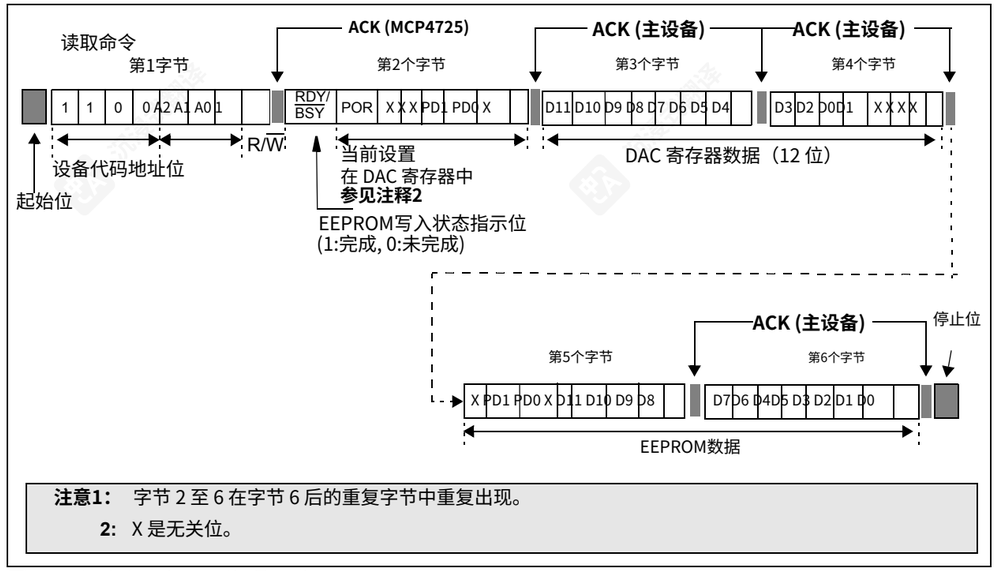


Note 1: Bytes 2 - 6 are repeated in repeat bytes after byte 6.
2: X is don’t care bit.

FIGURE 6-3: *Read Command and Output Data Format.*

6.2 读取命令

如果R/W位被置为逻辑“高”，则设备会在SDA引脚、DAC寄存器和EEPROM数据上输出。图6-3展示了读取寄存器和EEPROM数据的示例。图6-3中的第2个字节指示了设备当前的工作状态。RDY/BSY位表示EEPROM写入状态。在EEPROM写入期间，RDY/BSY位保持低电平，写入完成后变为高电平。



注意1： 字节 2 至 6 在字节 6 后的重复字节中重复出现。
2: X 是无关位。

图6-3：读取命令和输出数据格式

7.0 I²C SERIAL INTERFACE COMMUNICATION

7.1 OVERVIEW

The MCP4725 device uses a two-wire I²C serial interface that can operate on a standard, fast or high speed mode. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions. The MCP4725 device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. An example of hardware connection diagram is shown in Figure 8-1. Communication is initiated by the master (microcontroller) which sends the START bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits, and the R/$\overline{W}$ bit. The device code for the MCP4725 device is `1100`.

When the device receives a read command (R/W = `1`), it transmits the contents of the DAC input register and EEPROM. A non-acknowledge (NAK) or repeated START bit can be transmitted at any time. See Figure 6-3 for the read operation example. If writing to the device (R/W = `0`), the device will expect write command type bits in the following byte. See Figure 6-1 and Figure 6-2 for the write operation examples.

The MCP4725 supports all three I²C operating modes:

- Standard Mode: bit rates up to 100 kbit/s
- Fast Mode: bit rates up to 400 kbit/s
- High Speed Mode (HS mode): bit rates up to 3.4 Mbit/s

Refer to the Phillips I²C document for more details of the I²C specifications.

7.2 Device Addressing

The address byte is the first byte received following the START condition from the master device. The first part of the address byte consists of a 4-bit device code which is set to `1100` for the MCP4725. The device code is followed by three address bits (A2, A1, A0) which are programmed as follows:

- The choice of A2 and A1 bits are provided by the customer as part of the ordering process. These bits are then programmed (hard-wired) during manufacturing
- The A2 and A1 are programmed to '`00`' (default), if not requested by customer
- A0 bit is determined by the logic state of A0 pin. The A0 pin can be tied to V_{DD} or V_{SS}, or can be actively driven by digital logic levels. The advantage of using the A0 pin is that the users can control the A0 bit on their application PCB circuit and also two identical MCP4725 devices can be used on the same bus line.

When the device receives an address byte, it compares the logic state of the A0 pin with the A0 address bit received before responding with the acknowledge bit. The logic state of the A0 pin needs to be set prior to the interface communication.

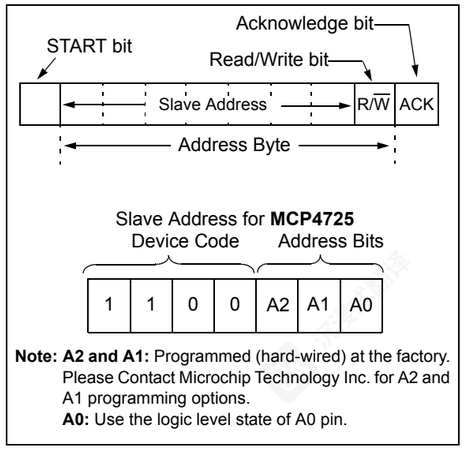


FIGURE 7-1: *Device Addressing.*

7.0 I²C串行接口通信

7.1 概述

MCP4725设备使用一个双线I²C串行接口，可以在标准、快速或高速模式下工作。将数据发送到总线上的设备定义为发送器，而接收数据的设备定义为接收器。总线必须由一个主设备控制，该设备生成串行时钟（SCL）、控制总线访问并生成启动和停止条件。MCP4725设备作为从设备工作。主设备和从设备都可以作为发送器或接收器工作，但主设备决定激活哪种模式。图8-1显示了硬件连接图的一个示例。通信由主设备（微控制器）启动，它发送启动位，然后发送从设备地址字节。第一个传输的字节始终是包含设备代码、地址位和R/W位的从设备地址字节。MCP4725设备的设备代码是1100。

当设备接收到读命令（R/W = `1`）时，它会传输DAC输入寄存器和EEPROM的内容。任何时候都可以传输非应答（NAK）或重复起始位。有关读操作示例，请参见图6-3。如果向设备写入（R/W = `0`），设备将在下一个字节中期望写入命令类型位。有关写操作示例，请参见图6-1和图6-2。

MCP4725支持所有三种I²C操作模式：

- 标准模式：波特率高达100 kbit/s
- 快速模式：波特率高达400 kbit/s
- 高速模式（HS模式）：波特率高达3.4 Mbit/s

请参考Phillips I²C文档，以获取更多关于I²C规范的信息。

7.2 设备寻址

地址字节是主设备发出START条件后接收的第一个字节。地址字节的第一部分由一个4位设备码组成，对于MCP4725，该设备码设置为1100。设备码后面跟着三个地址位（A2、A1、A0），它们按以下方式编程：

- A2 和 A1 位的选用由客户在订购过程中提供。这些位在生产过程中被编程（硬接）
- 如果客户没有提出要求，A2 和 A1 位会被编程为 '00'（默认值）
- A0 位由 A0 引脚的逻辑状态决定。A0 引脚可以连接到 VDD 或 VSS，也可以由数字逻辑电平主动驱动。使用 A0 引脚的优点是用户可以在他们的应用 PCB 电路中控制 A0 位，并且两个相同的 MCP4725 设备可以用于同一总线线上。

当设备接收到一个地址字节时，它会将 A0 引脚的逻辑状态与之前接收到的 A0 地址位进行比较，并在响应时发送确认位。A0 引脚的逻辑状态需要在接口通信之前设置。

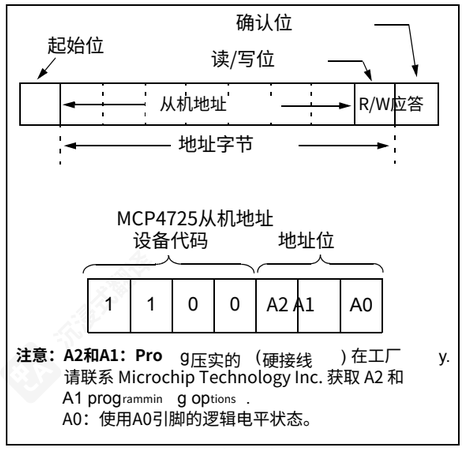


图7-1： 设备寻址。

7.3 General Call

The MCP4725 device acknowledges the general call address (0x00 in the first byte). The meaning of the general call address is always specified in the second byte (see Figure 7-2). The I²C specification does not allow to use "00000000" (00h) in the second byte. Please refer to the Phillips I²C document for more details of the General Call specifications. The MCP4725 supports the following general calls:

7.3.1 GENERAL CALL RESET

The general reset occurs if the second byte is "00000110" (06h). At the acknowledgement of this byte, the device will abort current conversion and perform an internal reset similar to a power-on-reset (POR). Immediately after this reset event, the device uploads the contents of the EEPROM into the DAC register.

7.3.2 GENERAL CALL WAKE-UP

If the second byte is "00001001" (09h), the device will reset the power-down bits. After receiving this command, the power-down bits of the DAC register are set to a normal operation (PD1, PD2 = 0,0). The power-down bit settings in EEPROM are not affected.

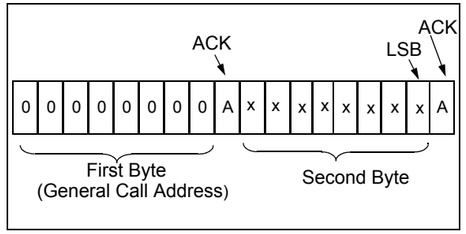


FIGURE 7-2: *General Call Address Format.*

7.4 High-Speed (HS) Mode

The I²C specification requires that a high-speed mode device must be 'activated' to operate in high-speed (3.4 Mbit/s) mode. This is done by sending a special address byte of 00001XXX following the START bit. The XXX bits are unique to the high-speed (HS) mode Master. This byte is referred to as the high-speed (HS) Master Mode Code (HSMMC). The MCP4725 device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode and can communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I²C modes, please refer to the Phillips I²C specification.

7.5 I²C BUS CHARACTERISTICS

The I²C specification defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined using Figure 7-3.

7.5.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

7.5.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition.

All commands must be preceded by a START condition.

7.5.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

7.5.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

7.3 一般呼叫

MCP4725设备响应通用呼叫地址（第一个字节为0x00）。通用呼叫地址的含义始终在第二个字节中指定（见图7-2）。I²C规范不允许在第二个字节中使用"00000000"（00h）。请参考Philips I²C文档获取通用呼叫规范的更多详细信息。MCP4725支持以下通用呼叫：

7.3.1 一般呼叫复位

如果第二个字节是"00000110"（06h），则会发生一般复位。在该字节确认后，设备将中止当前转换并执行类似于上电复位（POR）的内部复位。复位事件发生后，设备会将EEPROM的内容上传到DAC寄存器。

7.3.2 一般呼叫唤醒

如果第二个字节是"00001001"（09h），设备将重置掉电位。接收到此命令后，DAC寄存器的掉电位将被设置为正常工作（PD1、PD2 = 0、0）。EEPROM中的掉电位设置不受影响。

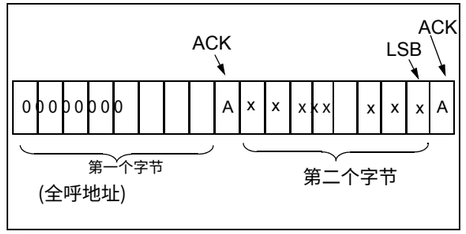


图7-2: 一般呼叫地址格式。

7.4 高速（HS）模式

I²C规范要求高速模式设备必须被"激活"才能以高速（3.4 Mbit/s）模式运行。这是通过在START位之后发送一个特殊的地址字节00001XXX来完成的。XXX位是高速（HS）模式主机的唯一标识。该字节被称为高速（HS）主机模式代码（HSMMC）。MCP4725设备不响应此字节。但是，在接收到此命令后，设备将切换到HS模式，并且可以在SDA和SCL线上以高达3.4 Mbit/s的速度通信。设备将在下一个STOP条件时退出HS模式。

有关HS模式或其他I²C模式的更多信息，请参阅飞利浦I²C规范。

7.5 I²C 总线特性

I²C规范定义了以下总线协议：

- 数据传输只能在总线不忙时启动。
- 在数据传输过程中，每当时钟线为高电平时，数据线必须保持稳定。当时钟线为高电平时数据线发生变化，将被解释为启动或停止条件。

因此，根据图7-3定义了以下总线条件。

7.5.1 总线不忙 (A)

数据和时钟线均保持高电平。

7.5.2 启动数据传输 (B)

在时钟 (SCL) 保持高电平的情况下，SDA线从高电平到低电平的跳变将确定一个启动条件。
所有命令都必须以一个START条件开始。

7.5.3 停止数据传输 (C)

SDA线在时钟 (SCL) 为高电平时从低电平到高电平的跳变确定一个STOP条件。所有操作都必须以一个STOP条件结束。

7.5.4 数据有效 (D)

在START条件之后，当数据线在时钟信号的高电平期间保持稳定时，数据线的状态表示有效数据。

数据线上的数据必须在时钟信号的低电平期间改变。每个数据位对应一个时钟脉冲。

每次数据传输都以一个启动条件开始，并以一个停止条件结束。

7.5.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must send an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave.

In this case, the slave (MCP4725) will leave the data line HIGH to enable the master to generate the STOP condition.

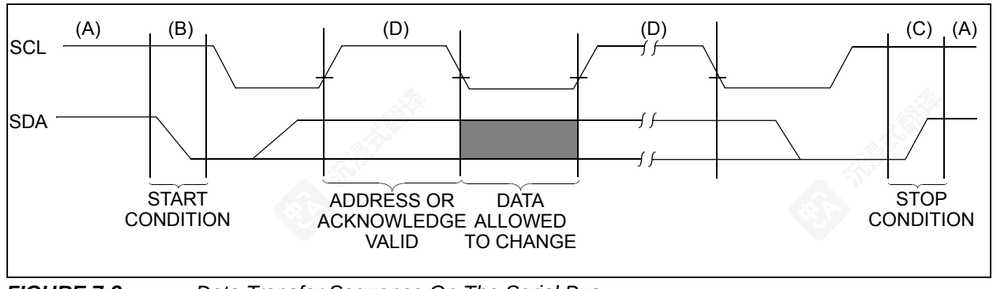


FIGURE 7-3: *Data Transfer Sequence On The Serial Bus.*

7.5.5 确认应答

每台接收设备在被寻址时，必须在接收每个字节后生成一个应答信号。主设备必须生成一个与该应答位相关的额外时钟脉冲。

进行确认应答的设备，必须在应答时钟脉冲期间将 SDA 线路拉低，使 SDA 线路在应答相关时钟脉冲的高电平期间保持稳定低电平。

课程中，建立时间和保持时间必须加以考虑。在读取期间，主设备必须通过不在最后一位已从从设备时钟输出的字节上生成确认位，来向从设备发送数据结束信号。在这种情况下，从设备（MCP4725）将使数据线保持高电平，以使主设备能够生成停止条件。

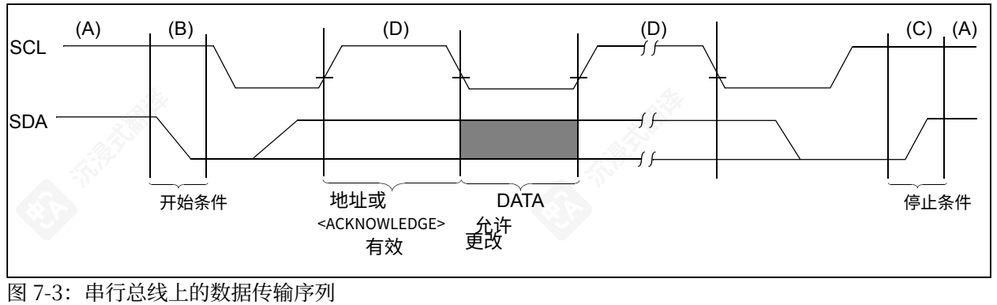


图 7-3：串行总线上的数据传输序列

TABLE 7-1: I²C SERIAL TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +85°C, V_{DD} = +2.7V to +5.0V, V_{SS} = 0V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Standard Mode						
Clock frequency	f_{SCL}	0	—	100	kHz	
Clock high time	T_{HIGH}	4000	—	—	ns	
Clock low time	T_{LOW}	4700	—	—	ns	
SDA and SCL rise time	T_R	—	—	1000	ns	From V_{IL} to V_{IH} **(Note 1)**
SDA and SCL fall time	T_F	—	—	300	ns	From V_{IH} to V_{IL} **(Note 1)**
START condition hold time	$T_{HD:STA}$	4000	—	—	ns	After this period, the first clock pulse is generated.
(Repeated) START condition setup time	$T_{SU:STA}$	4700	—	—	ns	
Data hold time	$T_{HD:DAT}$	0	—	3450	ns	**Note 3**
Data input setup time	$T_{SU:DAT}$	250	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	4000	—	—	ns	
Output valid from clock	T_{AA}	0	—	3750	ns	**Notes 2 and 3**
Bus free time	T_{BUF}	4700	—	—	ns	Time between START and STOP conditions.
Fast Mode						
Clock frequency	T_{SCL}	0	—	400	kHz	
Clock high time	T_{HIGH}	600	—	—	ns	
Clock low time	T_{LOW}	1300	—	—	ns	
SDA and SCL rise time	T_R	20 + 0.1Cb	—	300	ns	From V_{IL} to V_{IH} **(Note 1)**
SDA and SCL fall time	T_F	20 + 0.1Cb	—	300	ns	From V_{IH} to V_{IL} **(Note 1)**
START condition hold time	$T_{HD:STA}$	600	—	—	ns	After this period, the first clock pulse is generated
(Repeated) START condition setup time	$T_{SU:STA}$	600	—	—	ns	
Data hold time	$T_{HD:DAT}$	0	—	900	ns	**Note 4**
Data input setup time	$T_{SU:DAT}$	100	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	600	—	—	ns	
Output valid from clock	T_{AA}	0	—	1200	ns	**Notes 2 and 3**
Bus free time	T_{BUF}	1300	—	—	ns	Time between START and STOP conditions.

Note 1: This parameter is ensured by characterization and not 100% tested.

2: This specification is not a part of the I2C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (OR T_R).

3: If this parameter is too short, it can create an unintended START or STOP condition to other devices on the same bus line. If this parameter is too long, Clock Low time (T_{LOW}) can be affected.

4: For Data Input: This parameter must be longer than t_{SP}. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
For Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

5: All timing parameters in high-speed modes are tested at V_{DD} = 5V.

表7-1：I²C串行时序规范

电气规格：除非另有说明，所有限值均针对TA = -40至+85°C、VDD = +2.7V至+5.0V、VSS = 0V进行规定。						
参数	**Sym**	**Min**	**Typ**	**Max**	**单元**	**条件**
标准模式						
时钟频率	f_{SCL}	0	—	100	kHz	
时钟高电平时间	THIGH	4000	—	—	ns	
低电平保持时间	T_{LOW}	4700	—	—	ns	
SDA 和 SCL 上升时间	T_R	—	—	1000	ns	**从 VIL 到 VIH（注 1）**
SDA 和 SCL 下降时间	T_F	—	—	300	ns	**从 VIH 到 VIL（注 1）**
起始条件保持时间	THD:STA	4000	—	—	ns	在此期间，第一个时钟脉冲被生成。
(重复) 启动条件 建立时间	TSU:STA	4700	—	—	ns	
数据保持时间	THD:DAT	0	—	3450	ns	**注意3**
数据输入设置时间	TSU:DAT	250	—	—	ns	
停止条件设置时间	TSU:STO	4000	—	—	ns	
自时钟输出有效	T_{AA}	0	—	3750	ns	**备注2和3**
公交车空闲时间	T_{BUF}	4700	—	—	ns	START和STOP之间的时间 条件。
快速模式						
时钟频率	T_{SCL}	0	—	400	kHz	
时钟高电平时间	THIGH	600	—	—	ns	
时钟低电平时间	T_{LOW}	1300	—	—	ns	
SDA 和 SCL 上升时间	T_R	20 + 0.1Cb	—	300	ns	**从VIL到VIH（注1）**
SDA和SCL的下降时间	T_F	20 + 0.1Cb	—	300	ns	**从VIH到VIL（注1）**
起始条件保持时间	THD:STA	600	—	—	ns	在此期间之后，第一个时钟脉冲被生成
(重复) 启动条件 建立时间	TSU:STA	600	—	—	ns	
数据保持时间	$T_{HD:DAT}$	0	—	900	ns	**Note 4**
数据输入设置时间	TSU:DAT	100	—	—	ns	
停止条件设置时间	TSU:STO	600	—	—	ns	
输出有效时钟	T_{AA}	0	—	1200	ns	**笔记 2 和 3**
巴士空闲时间	T_{BUF}	1300	—	—	ns	START 和 STOP 之间的时间 条件。

Note 1: 该参数通过特性分析得到保证，而非100%测试。

2: 本规范不是 I2C 规范的一部分。本规范等同于数据保持时间 (THD:DAT) 加 SDA 下降 (或上升) 时间：TAA = THD:DAT + TF (OR TR)。

3: 如果此参数太短，可能会在总线线上的其他设备上创建意外的 START 或 STOP 条件。如果此参数太长，时钟低电平时间 (TLOW) 可能会受到影响。

4: 对于数据输入：此参数必须比tSP更长。如果此参数过长，可能会影响数据输入设置（TSU:DAT）或时钟低电平时间（TLOW）。

用于数据输出：该参数是有特征，并通过测试TAA参数间接进行测试

5: 高速模式下的所有时序参数均在V_{DD} = 5V进行测试。

TABLE 7-1: I²C SERIAL TIMING SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +85°C, V_{DD} = +2.7V to +5.0V, V_{SS} = 0V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
High Speed Mode (Note 5)						
Clock frequency	f_{SCL}	0	—	3.4	MHz	C_b = 100 pF
		0	—	1.7	MHz	C_b = 400 pF
Clock high time	T_{HIGH}	60	—	—	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		120	—	—	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
Clock low time	T_{LOW}	160	—	—	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		320	—	—	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
SCL rise time **(Note 1)**	$T_{R:SCL}$	—	—	40	ns	From V_{IL} to V_{IH}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	80	ns	From V_{IL} to V_{IH}, C_b = 400 pF, f_{SCL} = 1.7 MHz
SCL fall time **(Note 1)**	$T_{F:SCL}$	—	—	40	ns	From V_{IH} to V_{IL}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	80	ns	From V_{IH} to V_{IL}, C_b = 400 pF, f_{SCL} = 1.7 MHz
SDA rise time **(Note 1)**	$T_{R:DAT}$	—	—	80	ns	From V_{IL} to V_{IH}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	160	ns	From V_{IL} to V_{IH}, C_b = 400 pF, f_{SCL} = 1.7 MHz
SDA fall time **(Note 1)**	$T_{F:DAT}$	—	—	80	ns	From V_{IH} to V_{IL}, C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	160	ns	From V_{IH} to V_{IL}, C_b = 400 pF, f_{SCL} = 1.7 MHz
Data hold time **(Note 4)**	$T_{HD:DAT}$	0	—	70	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		0	—	150	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
Output valid from clock **(Notes 2 and 3)**	T_{AA}	—	—	150	ns	C_b = 100 pF, f_{SCL} = 3.4 MHz
		—	—	310	ns	C_b = 400 pF, f_{SCL} = 1.7 MHz
START condition hold time	$T_{HD:STA}$	160	—	—	ns	After this period, the first clock pulse is generated
START (Repeated) condition setup time	$T_{SU:STA}$	160	—	—	ns	
Data input setup time	$T_{SU:DAT}$	10	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	160	—	—	ns	

Note 1: This parameter is ensured by characterization and not 100% tested.

2: This specification is not a part of the I2C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (OR T_R).

3: If this parameter is too short, it can create an unintended START or STOP condition to other devices on the same bus line. If this parameter is too long, Clock Low time (T_{LOW}) can be affected.

4: For Data Input: This parameter must be longer than t_{SP}. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
For Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

5: All timing parameters in high-speed modes are tested at V_{DD} = 5V.

表 7-1：I²C 串行时序规格（续）

电气规格：除非另有说明，所有限值均针对 TA = -40 至 +85°C、VDD = +2.7V 至 +5.0V、VSS = 0V 进行规定。						
参数	**Sym**	**Min**	**Typ**	**Max**	**单位**	**条件**
高速模式（注意 5）						
时钟频率	f_{SCL}	0	—	3.4	MHz	Cb = 100 pF
		0	—	1.7	MHz	Cb = 400 pF
时钟高电平时间	THIGH	60	—	—	ns	Cb = 100 pF, fSCL = 3.4 MHz
		120	—	—	ns	Cb = 400 pF, fSCL = 1.7 MHz
时钟低电平时间	T_{LOW}	160	—	—	ns	Cb = 100 pF, fSCL = 3.4 MHz
		320	—	—	ns	Cb = 400 pF, fSCL = 1.7 MHz
SCL 上升时间 **(注 1)**	$T_{R:SCL}$	—	—	40	ns	从 V_{IL} to V_{IH}, Cb = 100 pF, fSCL = 3.4 MHz
		—	—	80	ns	从 V_{IL} to V_{IH}, Cb = 400 pF, fSCL = 1.7 MHz
SCL 下降时间 **(注 1)**	$T_{F:SCL}$	—	—	40	ns	来自 V_{IH} to V_{IL}, Cb = 100 pF, fSCL = 3.4 MHz
		—	—	80	ns	来自 V_{IH} to V_{IL}, Cb = 400 pF, fSCL = 1.7 MHz
SDA 上升时间 **(注 1)**	TR: DAT	—	—	80	ns	从 VIL 到 VIH，Cb = 100 pF，fSCL = 3.4 MHz
		—	—	160	ns	从 V_{IL} to V_{IH}, Cb = 400 pF，fSCL = 1.7 MHz
SDA 下降时间 **(注1)**	TF: DAT	—	—	80	ns	从VIH到VIL，Cb = 100 pF，fSCL = 3.4 MHz
		—	—	160	ns	从 V_{IH} to V_{IL}, Cb = 400 pF，fSCL = 1.7 MHz
数据保持时间 **(注4)**	THD:DAT	0	—	70	ns	Cb = 100 pF, fSCL = 3.4 MHz
		0	—	150	ns	Cb = 400 pF, fSCL = 1.7 MHz
输出在时钟有效 **(注释2和3)**	T_{AA}	—	—	150	ns	Cb = 100 pF, fSCL = 3.4 MHz
		—	—	310	ns	Cb = 400 pF, fSCL = 1.7 MHz
START条件保持时间	THD:STA	160	—	—	ns	在此期间，第一个时钟脉冲生成
START（重复）条件设置时间	TSU:STA	160	—	—	ns	
数据输入设置时间	TSU:DAT	10	—	—	ns	
停止条件设置时间	TSU:STO	160	—	—	ns	

Note 1: 该参数由特性化验证确保，而非100%测试。

2: 本规范并非I2C规范的一部分。本规范等同于数据保持时间（THD:DAT）。
加上SDA下降（或上升）时间：TAA = THD:DAT + TF（或TR）.

3: 如果该参数太短，可能会在总线线上对其他设备创建意外的START或STOP条件。如果该参数太长，时钟低电平时间（TLOW）可能会受影响。

4: 对于数据输入：该参数必须比tSP长。如果该参数太长，数据输入建立时间（TSU:DAT）或时钟低电平时间（TLOW）可能会受影响。

用于数据输出：该参数具有特征，并通过测试TAA参数间接进行测试

5: 高速模式下的所有时序参数均在V_{DD} = 5V进行测试。

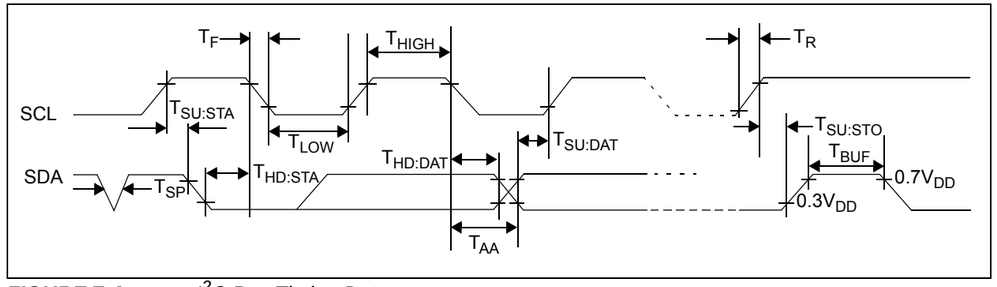


FIGURE 7-4: *I^2C Bus Timing Data.*

MCP4725

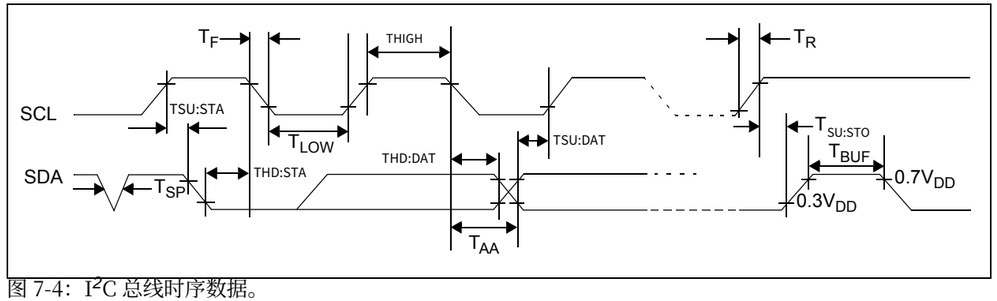


图 7-4：I^2C 总线时序数据。

© 2009 Microchip Technology Inc.

8.0 TYPICAL APPLICATIONS

The MCP4725 device is one of Microchip's latest DAC device family with non-volatile EEPROM memory. The device is a general purpose resistive string DAC intended to be used in applications where a precision, and low power DAC with moderate bandwidth is required.

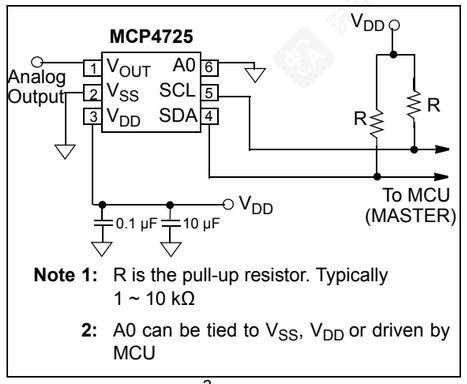
Since the device includes non-volatile EEPROM memory, the user can use this device for applications that require the output to return to the previous set-up value on subsequent power-ups.

Applications generally suited for the MCP4725 device family include:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery Powered)
- Motor Speed Control

8.1 Connecting to I²C BUS using Pull-Up Resistors

The SCL and SDA pins of the MCP4725 are open-drain configurations. These pins require a pull-up resistor as shown in Figure 8-1. The value of these pull-up resistors depends on the operating speed (standard, fast, and high speed) and loading capacitance of the I^2C bus line. Higher value of pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long bus line or high number of devices connected to the bus, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for standard and fast modes, and less than 1 kΩ for high speed mode.



Note 1: R is the pull-up resistor. Typically 1 ~ 10 kΩ

2: A0 can be tied to V_{SS}, V_{DD} or driven by MCU

FIGURE 8-1: *I^2C Bus Interface Connection with A0 pin tied to V_{SS}.*

Two devices with the same A2 and A1 address bits can be connected to the same I^2C bus by utilizing the A0 address pin (Example: A0 pin of device A is tied to V_{DD}, and the other device's pin is tied to V_{SS}).

8.1.1 DEVICE CONNECTION TEST

The user can test the presence of the MCP4725 on the I^2C bus line without performing the data conversion. This test can be achieved by checking an acknowledge response from the MCP4725 after sending a read or write command. Here is an example using Figure 8-2:

(a) Set the R/$\overline{W}$ bit "HIGH" in the address byte.

(b) If the MCP4725 is connected to the I^2C bus line, it will then acknowledge by pulling SDA bus LOW during the ACK clock and then release the bus back to the I^2C Master.

(c) A STOP or repeated START bit can then be issued from the Master and I^2C communication can continue.

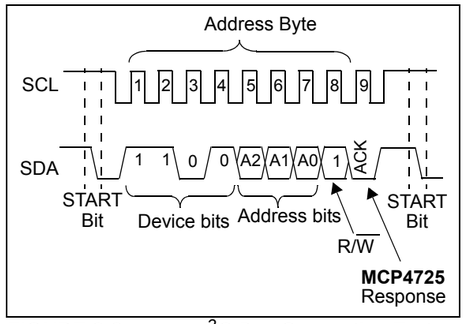


FIGURE 8-2: *I^2C Bus Connection Test.*

8.0 典型应用

MCP4725 设备是 Microchip 最新 DAC 设备家族中的一款，配备非易失性 EEPROM 存储器。该设备是一款通用电阻串 DAC，旨在用于需要高精度、低功耗且带宽适中的应用。

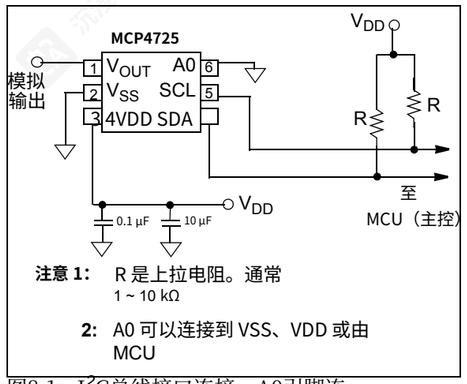
由于该设备包含非易失性EEPROM存储器，用户可以使用此设备用于需要在后续上电时恢复到先前设置值的输出应用。

适用于MCP4725设备系列的典型应用包括：

- 设置点或偏移量修剪
- 传感器校准
- 便携式仪器（电池供电）
- 电机速度控制

8.1 使用上拉电阻连接到I²C总线

MCP4725的SCL和SDA引脚是开漏配置。这些引脚需要像图8-1所示的那样接上上拉电阻。这些上拉电阻的阻值取决于I^2C总线线的运行速度（标准、快速和高速）和负载电容。上拉电阻的阻值越高，功耗越低，但会增加总线上的信号转换时间（更高的RC时间常数），因此可能会限制总线的运行速度。另一方面，阻值较低的电阻功耗较高，但允许更高的运行速度。如果总线线由于总线线较长或连接到总线上的设备数量较多而具有更高的电容，则需要使用较小的上拉电阻来补偿较长的RC时间常数。对于标准和快速模式，上拉电阻通常选择在1 kΩ到10 kΩ的范围内，而对于高速模式则应小于1 kΩ。



注意 1: R 是上拉电阻。通常 1 ~ 10 kΩ

2: A0 可以连接到 VSS、VDD 或由 MCU

图8-1：I^2C总线接口连接，A0引脚连接到VSS。

可以通过使用A0地址引脚将具有相同A2和A1地址位的两个设备连接到同一I^2C总线（示例：设备A的A0引脚连接到VDD，另一个设备的引脚连接到VSS）。

8.1.1 设备连接测试

用户可以在不执行数据转换的情况下测试 I^2C 总线线路上是否存在 MCP4725。此测试可以通过发送读或写命令后检查 MCP4725 的应答响应来实现。以下是使用图 8-2 的示例：

(a) 在地址字节中设置 R/W 位为“高”电平。

(b) 如果 MCP4725 连接到 I^2C 总线线路，它将通过在应答时钟期间将 SDA 总线拉低来应答，然后释放总线回到 I^2C 主机。

(c) 主机可以发出停止或重复启动位，I^2C 通信可以继续。

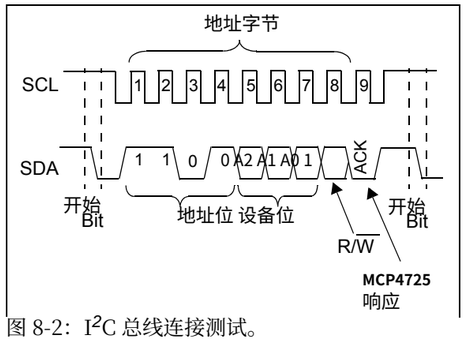


图 8-2：I^2C 总线连接测试。

8.2 Using Non-Volatile EEPROM Memory

The user can store the DAC input code (12 bits) and power-down configuration bits (2 bits) in the internal non-volatile EEPROM memory using the I^2C write command. The user can also read the EEPROM data using the I^2C read command. When the device is first powered after power is shut down, the device uploads the EEPROM contents to the DAC register automatically and provides the DAC output immediately. This feature is very useful in applications where the DAC device is used to provide set point or calibration data for other devices in the application system. The DAC will not lose the important system operational parameters due to the system power failure incidents. See **Section 5.6 "Non-Volatile EEPROM Memory"** for more details of the non-volatile EEPROM memory.

8.3 Power Supply Considerations

The power supply to the device is used for both V_{DD} and DAC reference voltage. Any noise induced on the V_{DD} line can affect on the DAC performance. Typical application will require a bypass capacitor in order to filter out high frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm).

The power source should be as clean as possible. If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the MCP4725 should reside on the analog plane.

8.4 Layout Considerations

Inductively-coupled AC transients and digital switching noise from other devices can affect on DAC performance and DAC output signal integrity. Careful board layout will minimize these effects. Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the MCP4725 is capable of providing. Particularly harsh environments may require shielding of critical signals. Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors of the MCP4725 should be terminated to the analog ground plane.

8.5 Application Examples

The MCP4725 is a rail-to-rail output DAC designed to operate with a V_{DD} range of 2.7V to 5.5V. Its output amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of an external buffer for most applications.

8.5.1 DC SET POINT OR CALIBRATION

A common application for the MCP4725 is a digitally-controlled set point or a calibration of variable parameters such as sensor offset or bias point. Example 8-1 shows an example of the set point setting. Since the MCP4725 is a 12-bit DAC and uses the V_{DD} supply as a reference source, it provides a V_{DD}/4096 of resolution per step.

8.2 使用非易失性 EEPROM 存储器

用户可以使用 I^2C 写命令将 DAC 输入代码（12 位）和掉电配置位（2 位）存储在内部非易失性 EEPROM 存储器中。用户还可以使用 I^2C 读命令读取 EEPROM 数据。设备在断电后首次上电时，会自动将 EEPROM 内容上传到 DAC 寄存器并提供 DAC 输出。此功能在 DAC 设备用于向应用系统中的其他设备提供设定点或校准数据的应用中非常有用。由于系统断电事件，DAC 不会丢失重要的系统运行参数。有关非易失性 EEPROM 存储器的更多详细信息，请参阅第 5.6 节“非易失性 EEPROM 存储器”。

8.3 电源注意事项

设备的电源既用于 VDD 也用于 DAC 基准电压。VDD 线上的任何噪声都会影响 DAC 性能。典型应用需要在 VDD 线上放置旁路电容以滤除高频噪声。噪声可能由电源的走线引入，也可能由 DAC 输出变化引起。旁路电容有助于最小化这些噪声源对信号完整性的影响。图 8-1 展示了在 VDD 线上并联使用两个旁路电容（一个 10 µF 钽电容和一个 0.1 µF 陶瓷电容）的示例。这些电容应尽可能靠近 VDD 引脚放置（距离在 4 mm 以内）。

电源应尽可能纯净。如果应用电路具有独立的数字和模拟电源，MCP4725 的 VDD 和 VSS 引脚应位于模拟平面上。

8.4 布局注意事项

感性耦合的交流瞬变和其他设备的数字开关噪声会影响 DAC 性能和 DAC 输出信号完整性。仔细的电路板布局将最大限度地减少这些影响。台架测试表明，采用低电感接地平面、隔离输入、隔离输出和适当去耦的多层电路板对于实现 MCP4725 所能提供的性能至关重要。在特别恶劣的环境下，可能需要对关键信号进行屏蔽。建议使用独立的数字和模拟接地平面。在这种情况下，MCP4725 的 VSS 引脚和 VDD 电容的接地引脚应连接到模拟接地平面。

8.5 应用实例

MCP4725 是一款轨到轨输出 DAC，设计用于在 2.7V 至 5.5V 的 VDD 范围内工作。其输出放大器足够强大，可以直接驱动常见的低信号负载，因此对于大多数应用而言，无需外部缓冲器即可消除成本和尺寸问题。

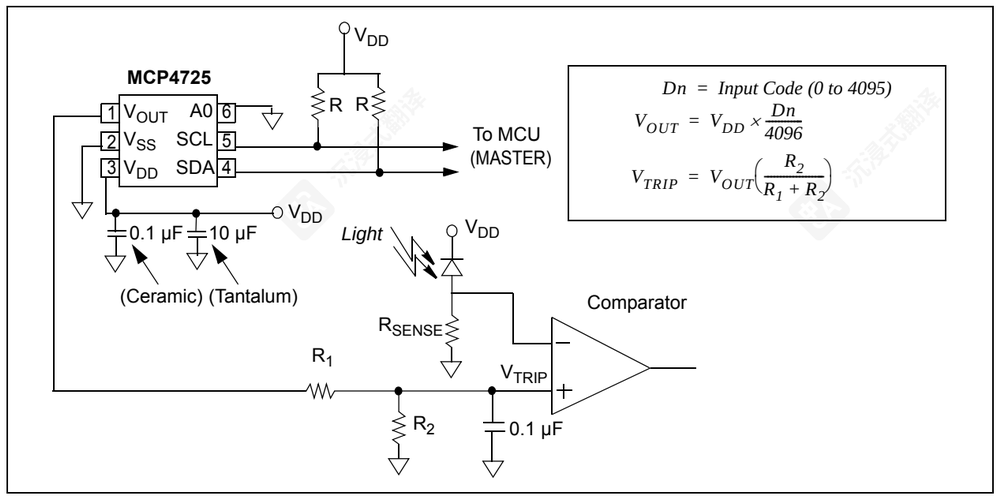
8.5.1 直流设定点或校准

MCP4725 的一个常见应用是数字控制的设定点或对传感器偏移、偏置点等可变参数进行校准。示例 8-1 展示了设定点设置的例子。由于 MCP4725 是一个 12 位 DAC，并使用 VDD 供电作为参考源，因此它每一步提供 VDD/4096 的分辨率。

8.5.2 DECREASING THE OUTPUT STEP SIZE

Calibrating the threshold of a diode, transistor or resistor may require a very small step size in the DAC output voltage. These applications may require about 200 µV of step resolution within 0.8V of range.

One method of achieving this small step resolution is using a voltage divider at the DAC output. An example is shown in Example 8-1. The step size of the DAC output is scaled down by the factor of the ratio of the voltage divider. Note that the bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

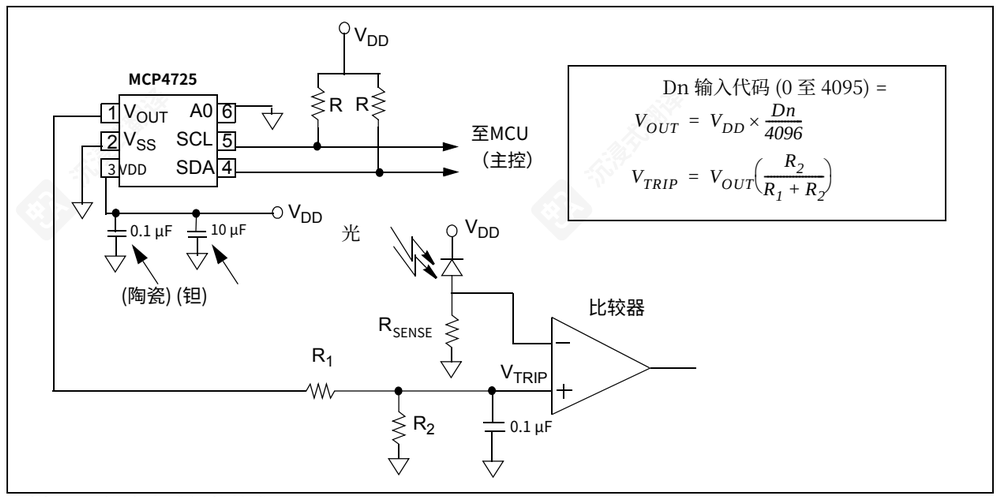


EXAMPLE 8-1: *Set Point Or Threshold Calibration.*

8.5.2 减小输出步进大小

校准二极管、晶体管或电阻的阈值可能需要 DAC 输出电压非常小的步长。这些应用可能需要在 0.8V 的范围内实现约 200 µV 的步长分辨率。

一种实现这种小步分辨率的方法是在 DAC 输出端使用分压器。示例 8-1 显示了这种情况。DAC 的步进大小输出根据分压比进行缩放。请注意，分压器输出端的旁路电容在衰减DAC输出噪声和环境感应噪声方面起着关键作用。

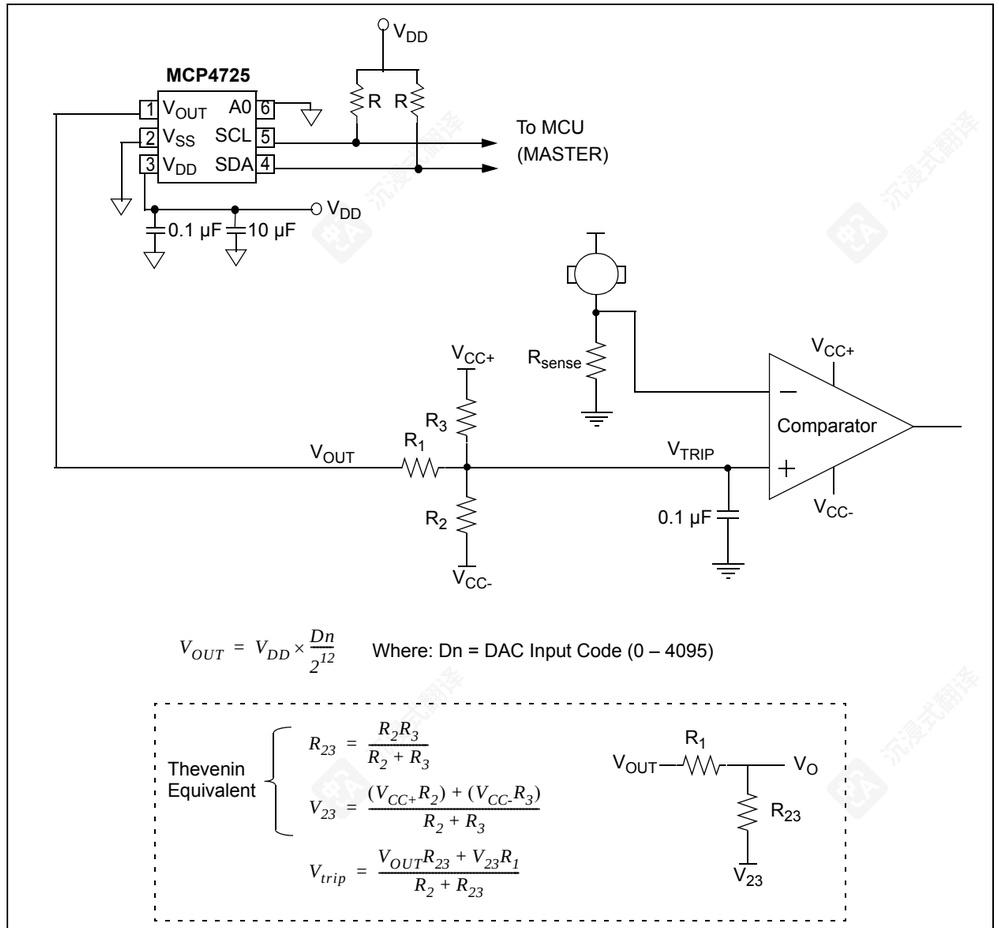


示例 8-1：设定点或阈值校准

8.5.3 BUILDING A “WINDOW” DAC

Some sensor applications require very high resolution around the set point or threshold voltage.

Example 8-2 shows an example of creating a “window” around the threshold using a voltage divider network with a pull-up and pull-down resistor. In the circuit, the output voltage range is scaled down, but its step resolution is increased greatly.



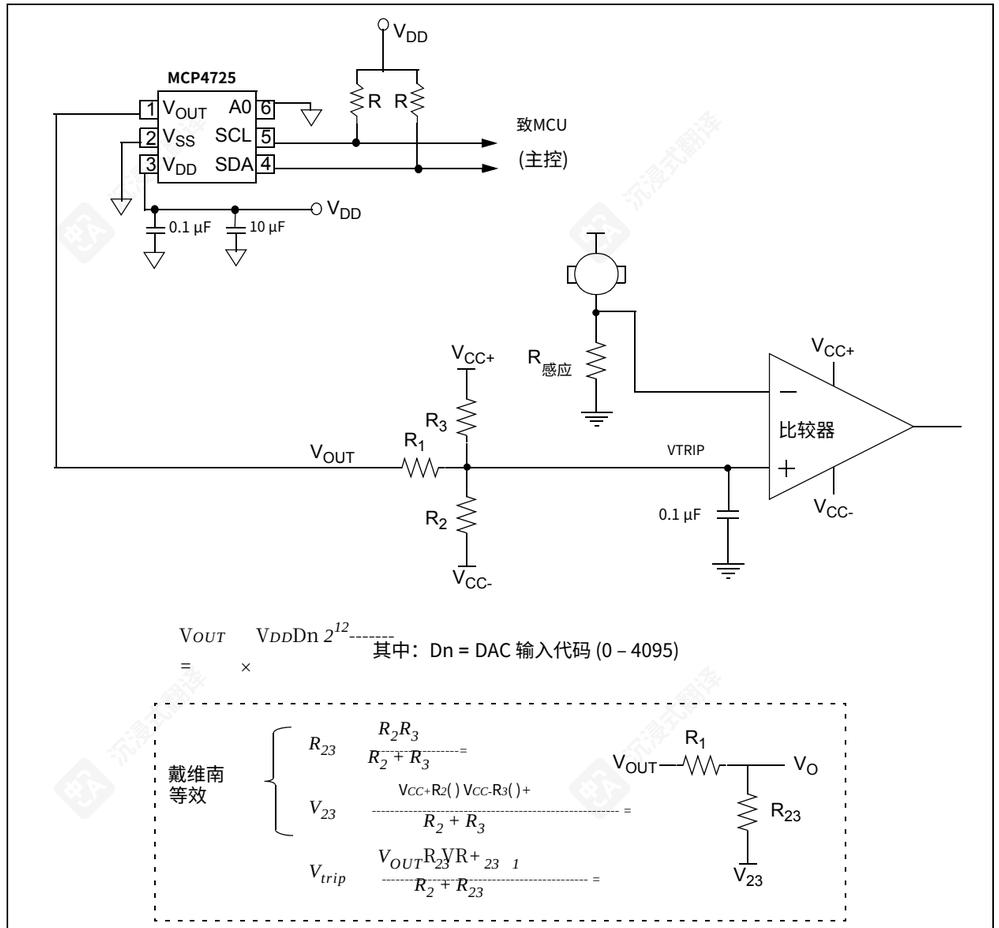
$$V_{OUT} = V_{DD} \times \frac{Dn}{2^{12}}$$ Where: Dn = DAC Input Code (0 – 4095)

EXAMPLE 8-2: *Single-Supply “Window” DAC.*

8.5.3 构建一个“窗口”DAC

某些传感器应用需要在设定点或阈值电压附近实现非常高的分辨率。

示例 8-2 展示了如何使用带有上拉和下拉电阻的分压器网络在阈值周围创建一个“窗口”。在该电路中，输出电压范围被缩小，但其步进分辨率大大提高。



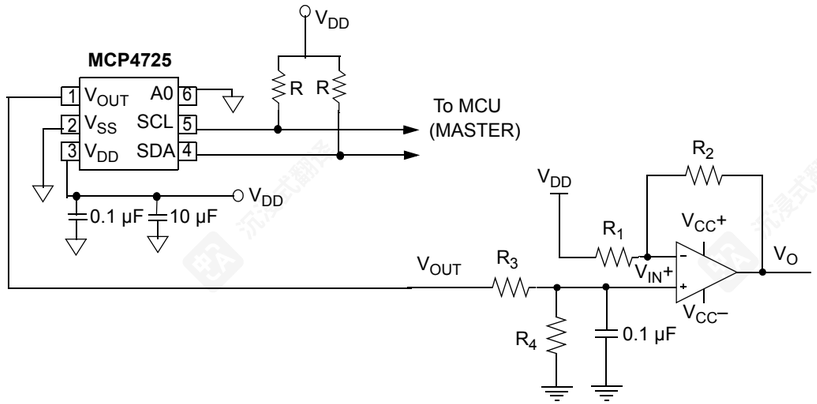
$$V_{OUT} = V_{DD} \times \frac{Dn}{2^{12}}$$ 其中：Dn = DAC 输入代码 (0 – 4095)

示例8-2: 单电源“窗口”DAC

8.5.4 BIPOLAR OPERATION

Bipolar operation is achievable using the MCP4725 by using an external operational amplifier (op amp). This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Example 8-3 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R_4 can be tied to V_{DD} (= V_{REF}) instead of V_{SS}, if a higher offset is desired. Note that a pull-up to V_{DD} could be used, instead of R_4, if a higher offset is desired.



$$V_{OUT} = V_{DD} \times \frac{Dn}{2^{12}}$$ Where: Dn = DAC Input Code (0 – 4095)

$$V_{IN+} = \frac{V_{OUT} R_4}{R_3 + R_4}$$

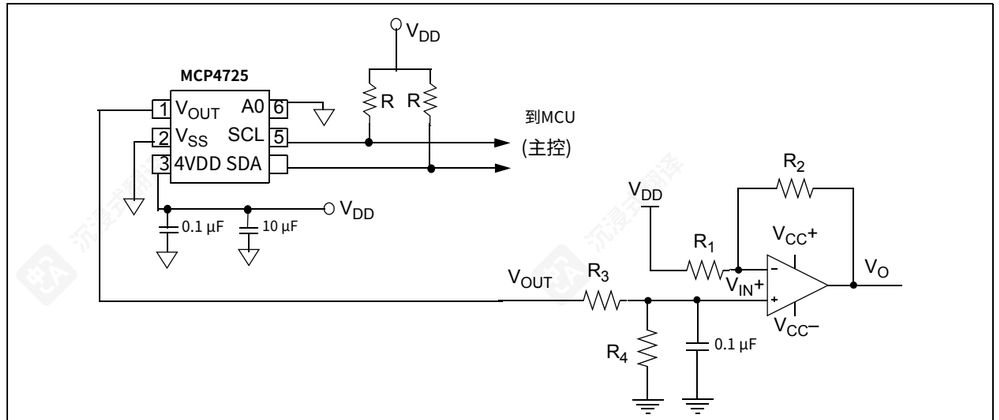
$$V_O = V_{IN+}\left(1 + \frac{R_2}{R_1}\right) - V_{DD}\left(\frac{R_2}{R_1}\right)$$

EXAMPLE 8-3: *Digitally-Controlled Bipolar Voltage Source.*

8.5.4 双极性操作

通过使用外部运算放大器（op amp），MCP4725 可以实现双极性操作。这使得通用型 DAC 能够利用其成本和可用性优势，满足几乎任何所需的输出电压范围、电源和噪声性能。

示例 8-3 展示了一个简单的双极性电压源配置。R1 和 R_2 允许选择增益，而 R_3 和 R_4 将 DAC 的输出偏移到选定值。请注意，如果需要更高的偏移量，R_4 可以连接到 V_{DD} (= V_{REF}) 而不是 VSS。请注意，如果需要更高的偏移量，可以使用上拉到 VDD，而不是 R_4。



$$V_{OUT} = V_{DD} \times \frac{Dn}{2^{12}}$$ 其中：Dn = DAC 输入代码 (0 – 4095)

$$V_{IN+} \quad \frac{V_{OUT} R_4}{R_3 + R_4} =$$

$$V_O = V_{IN+}\left(1 \quad \frac{R_2}{R_1}\right) V - \quad DD_{R1} \frac{R_2}{\quad}$$

示例8-3： 数字控制双极性电压源。

8.5.4.1 Design a Bipolar DAC using Example 8-3

Some applications desires an output step magnitude of 1 mV with an output range of ±2.05V. The following steps explain the design solution:

1. Calculate the range: +2.05V – (-2.05V) = 4.1V.
2. Calculate the resolution needed:
   4.1V/1 mV = 4100 steps

   Note that 2^{12} = 4096 for 12-bit resolution.
3. The amplifier gain (R_2/R_1), multiplied by V_{DD}, must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values (R_1+R_2), the V_{DD} value must be selected first. If a V_{DD} of 4.1V is used, solve for the amplifier's gain by setting the DAC code to 0, knowing that the output needs to be -2.05V. The equation can be simplified to

$$\frac{-R_2}{R_1} = \frac{-2.05}{V_{DD}} = \frac{-2.05}{4.1} \rightarrow \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

4. Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot V_{DD})}{1.5 \cdot V_{DD}} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

8.5.4.1 使用示例8-3设计双极性DAC

某些应用需要输出步进幅度为 1 mV，输出范围为 ±2.05V。以下步骤说明了设计方案：

1. 计算范围：+2.05V – (-2.05V) = 4.1V.
2. 计算所需的分辨率：
   4.1V/1 mV = 4100 步进

   注意 2^{12} = 4096 用于12位分辨率。
3. 放大器增益 (R_2/R_1)，乘以VDD，必须等于所需的最低输出以实现双极性操作。由于通过选择电阻值 (R_1+R_2)可以实现任何增益，因此必须首先选择VDD值。如果使用4.1V的VDD，通过将DAC代码设置为0来求解放大器的增益，知道输出需要为-2.05V。该方程可以简化为

$$\frac{-R_2}{R_1} = \frac{-2.05}{V_{DD}} = \frac{-2.05}{4.1} \rightarrow \frac{R_2}{R_1} = \frac{1}{2}$$

如果R_1 = 20kΩ和R_2 = 10 kΩ，增益将为0.5。

4. 接下来，通过将DAC设置为4096来求解R3和R4，知道输出需要为 +2.05V。

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot V_{DD})}{1.5 \cdot V_{DD}} = \frac{2}{3}$$

如果 R_4 = 20 为 kΩ，那么 R_3 = 10 为 kΩ

8.5.5 PROGRAMMABLE CURRENT SOURCE

Example 8-3 illustrates an example how to convert the DAC voltage output to a digitally selectable current source by adding a voltage follower and a sensor register.

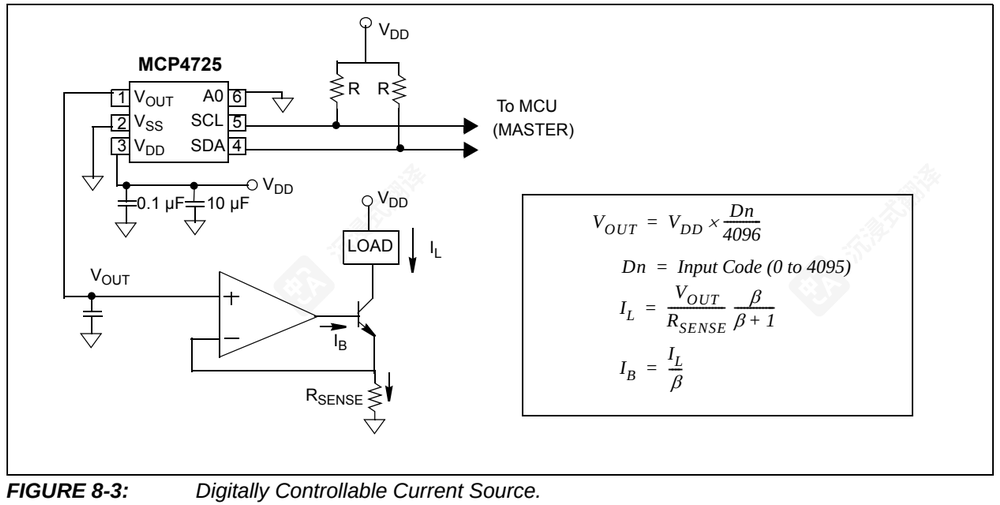


FIGURE 8-3: *Digitally Controllable Current Source.*

8.5.5 可编程电流源

示例 8-3 展示了如何通过添加一个电压跟随器和传感器寄存器，将 DAC 电压输出转换为数字可选电流源的一个实例。

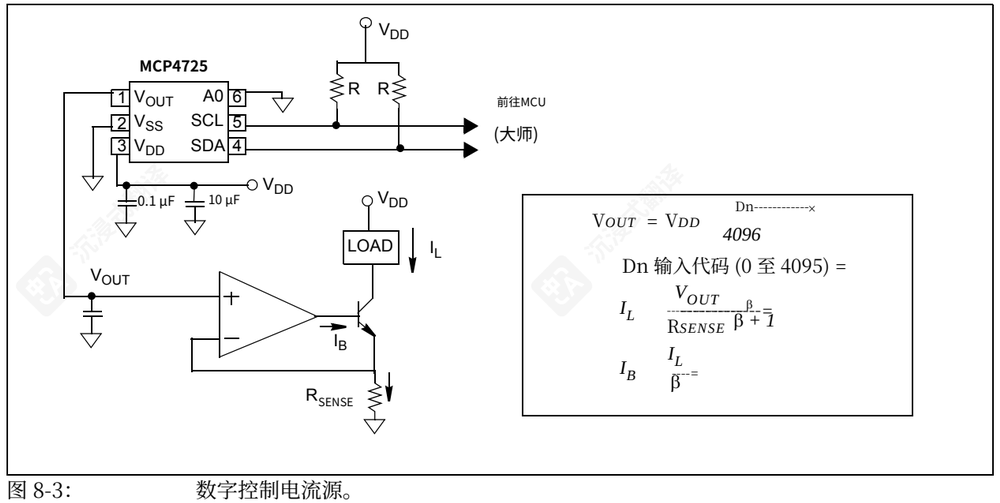


图 8-3: 数字控制电流源。

NOTES:

备注：

9.0 DEVELOPMENT SUPPORT

9.1 Evaluation & Demonstration Boards

The MCP4725 SOT-23-6 Evaluation Board is available from Microchip Technology Inc. This board works with Microchip's PICkit™ Serial Analyzer. The user can program the DAC input codes and EEPROM data, or read the programmed data using the easy to use PICkit Serial Analyzer with the Graphic User Interface software. Refer to www.microchip.com for further information on this product's capabilities and availability.

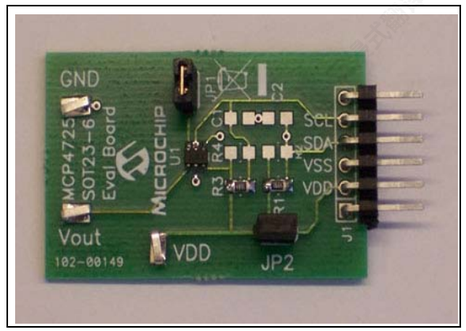


FIGURE 9-1: *MCP4725 SOT-23-6 Evaluation Board.*

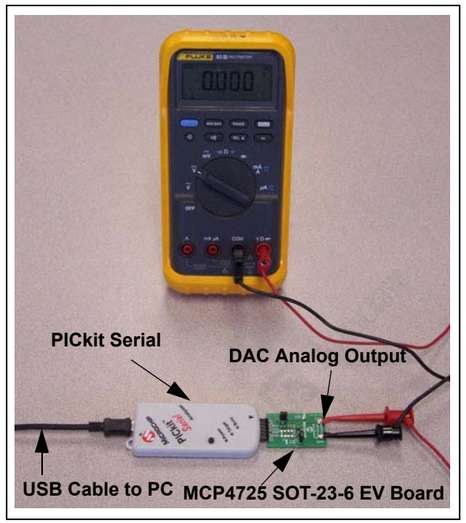


FIGURE 9-2: *Setup for the MCP4725 SOT-23-6 Evaluation Board with PICkit™ Serial Analyzer.*

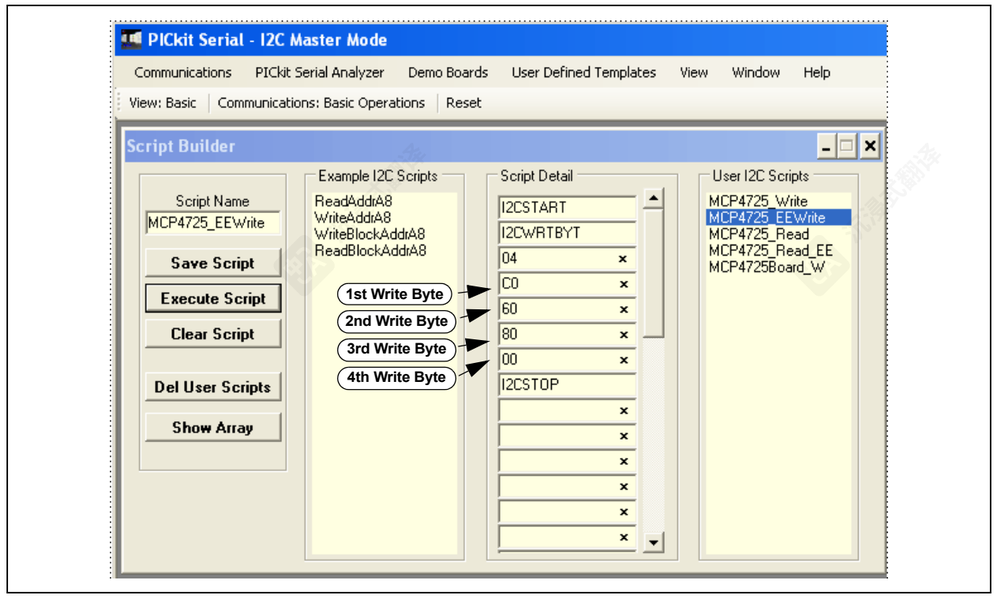


FIGURE 9-3: *Example of PICkit™ Serial User Interface.*

9.0 开发支持

9.1 评估与演示板

MCP4725 SOT-23-6 评估板可从 Microchip Technology Inc. 购得。该板与 Microchip 的 PICkitTM 串行分析器兼容。用户可通过易于使用的 PICkit 串行分析器和图形用户界面软件编程 DAC 输入代码和 EEPROM 数据，或读取已编程数据。有关该产品的功能和可用性的更多信息，请参阅 www.microchip.com。

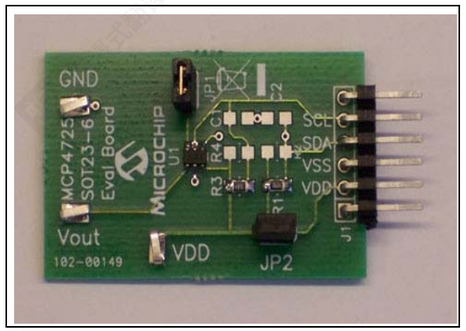


图 9-1: MCP4725 SOT-23-6 评估板。

图9-2：MCP4725 SOT-23-6评估板与PICkitTM串行分析器的设置。

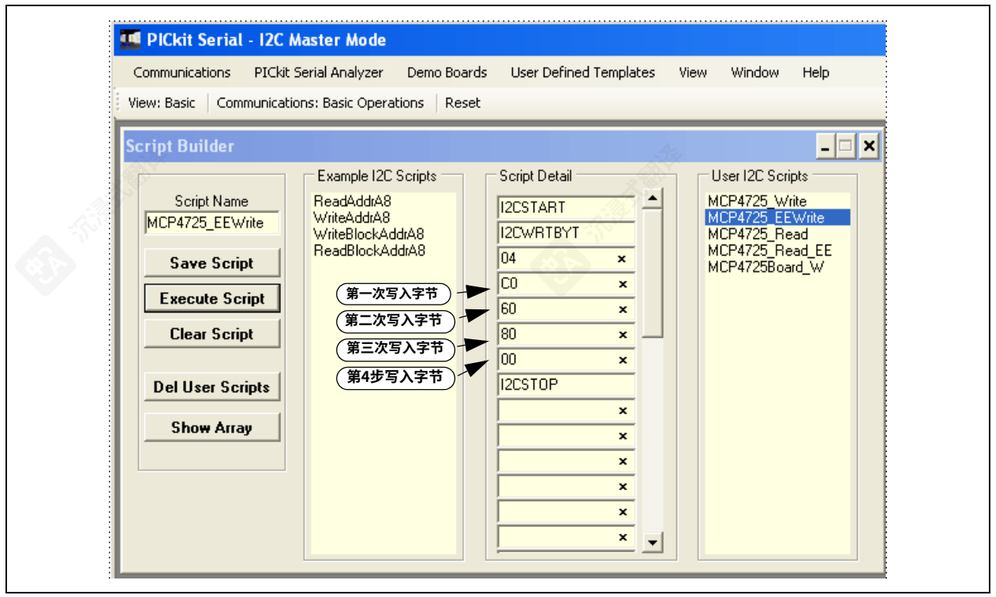


图9-3：PICkitTM串行用户界面示例。

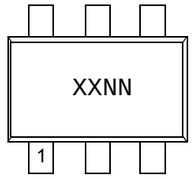
NOTES:

注意事项：

10.0 PACKAGING INFORMATION

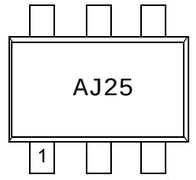
10.1 Package Marking Information

6-Lead SOT-23



Part Number	Address Option	Code
MCP4725A0T-E/CH	A0 (00)	AJNN
MCP4725A1T-E/CH	A1 (01)	APNN
MCP4725A2T-E/CH	A2 (10)	AQNN
MCP4725A3T-E/CH	A3 (11)	ARNN

Example



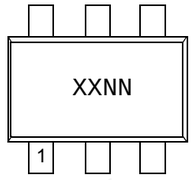
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10.0 包装信息

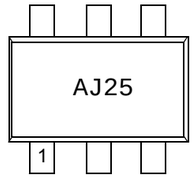
10.1 封装标记信息

6引脚SOT-23



部件编号	地址选项	Code
MCP4725A0T-E/CH	A0 (00)	AJNN
MCP4725A1T-E/CH	A1 (01)	APNN
MCP4725A2T-E/CH	A2 (10)	AQNN
MCP4725A3T-E/CH	A3 (11)	ARNN

示例

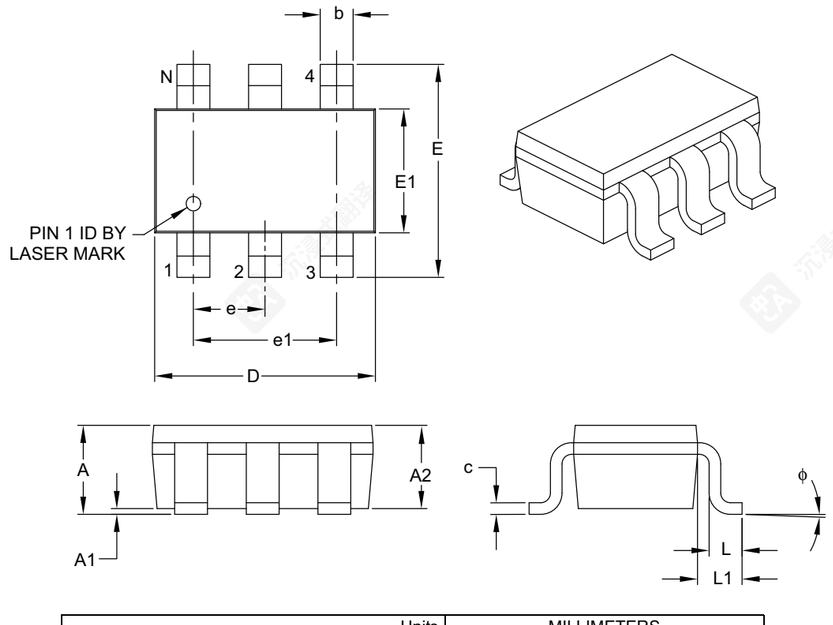


图例：	XX...X	客户特定信息
	Y	年代码（日历年最后一位）
	YY	年代码（日历年最后两位）
	WW	周代码（1月1日所在周为 ‘01’）
	NNN	字母数字追溯代码
	(e3)	无铅 JEDEC 标识符（适用于磨砂锡（Sn））
	*	此封**装對蓋餉**无铅 JEDEC 标识符（）将印在外包装上。 (e3)

注意： I 如果完整的 Microchip 部件编号无法在一行内标记，它将被延续到下一行，从而限制客户特定信息的可用字符数。
c字符数。

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

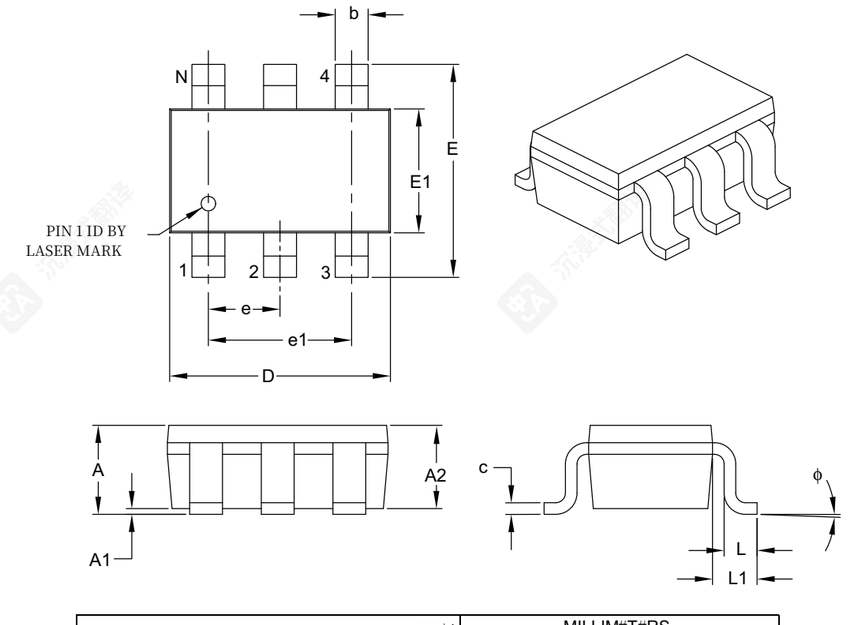
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

MCP4725

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: /or $he mo! $ c%rren$ package "ra.ing! , plea! e ! ee $he Microchip Packaging Speci&ica$ion loca$ e" a$h$$p,33….microchip.com/packaging



Uni$!		MILLIM#T#RS		
Dimen! ion Limi$!		MIN	NOM	MAX
6% ber o& Pin!	N		6	
Pi$ch	e		0.9) *SC	
7%$!i"e Lea" Pi$ch	e1		1.90 *SC	
7-erall :eigh$	A	0.90	–	1.4)
Mol"e" Package Thickne!!	A2	0.89	–	1.30
S$an"o&&	A1	0.00	–	0.1)
7-erall Wi"$h	E	2.20	–	3.20
Mol"e" Package Wi"$h	#1	1.30	–	1.80
7-erall Leng$h	D	2.70	–	3.10
/oo$ Leng$h	L	0.10	–	0.60
/oo$prin$	L1	0.3)	–	0.80
/oo$ Angle	ϕ	0°	–	30°
Lea" Thickne!!	c	0.08	–	0.26
Lea" Wi"$h	b	0.20	–	0.)1

Notes

1. Dimen! ion! D an" #1 "o no$ incl%"e mol" &la! h or pro$r%! ion! . Mol" &la! h or pro$r%! ion! ! hall no$ e’ cee" . 0.127 mm per ! i"e2. Dimen! ioning an" $olerancing per ASM# (14.)M.

*SC, *a!ic Dimen!ion. Theore$ically e’ ac$ -al%e !ho.n .i$ho%$ $olerance!.

Microchip Technology Drawing C04-028B

APPENDIX A: REVISION HISTORY

Revision D (June 2009)

The following is the list of modifications:

1. Added V_{DD_RAMP} parameter in **Section "ELECTRICAL CHARACTERISTICS"** and description in **Section 5.4.2 "V_{DD} Ramp Rate and EEPROM"**.

Revision C (November 2007)

The following is the list of modifications:

1. Corrected Address Options on Product Identification System page.

Revision B (October 2007)

The following is the list of modifications:

1. Added characterization graphs to document.
2. Numerous edits throughout.
3. Add new package marking address options. Updated package marking information and package outline drawings.
4. Added adress options to Product Identification System page.

Revision A (April 2007)

- Original Release of this Document.

附录 A：版本历史记录

版本 D（2009年6月）

以下为修改列表：

1. **在“电气特性”部分添加了 VDD_RAMP 参数，并在“VDD 斜坡速率和 EEPROM”部分（5.4.2 节）中添加了描述。**

修订版 C（2007 年 11 月）

以下是修改列表：

1. 修正地址选项 在产品识别系统页面。

修订版 B（2007 年 10 月）

以下为修改列表：

1. 为文档添加了角色化图表。
2. 全文进行了大量编辑。
3. 新增了新的包装标记地址选项。更新了包装标记信息和包装轮廓图。
4. 在产品识别系统页面添加了地址选项。

修订版A（2007年4月）

- 本文档的原始发布版本。

NOTES:

注释：

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	/XX
Device	Address Options	Tape and Reel	Temperature Range	Package

Device: MCP4725: Single Channel 12-Bit DAC w/EEPROM Memory

Address Options:

XX		A2	A1	A0
A0 *	=	0	0	External
A1	=	0	1	External
A2	=	1	0	External
A3	=	1	1	External

* Default option. Contact Microchip factory for other address options

Tape and Reel: T = Tape and Reel

Temperature Range: E = -40°C to +125°C

Package: CH = Plastic Small Outline Transistor (SOT-23-6), 6-lead

Examples:

a) MCP4725A0T-E/CH: Tape and Reel, Extended Temp., 6LD SOT-23 pkg. Address Option = A0

b) MCP4725A1T-E/CH: Tape and Reel, Extended Temp., 6LD SOT-23 pkg. Address Option = A1

c) MCP4725A2T-E/CH: Tape and Reel, Extended Temp., 6LD SOT-23 pkg. Address Option = A2

d) MCP4725A3T-E/CH: Tape and Reel, Extended Temp., 6LD SOT-23 pkg. Address Option = A3

产品识别系统

如需订购或获取信息（例如价格或交货信息），请咨询工厂或列出的销售办公室。

零件编号	XX	X	X	/XX
设备	地址选项	胶带和 Reel	温度范围	包装

设备： MCP4725： 单通道12位DAC带EEPROM内存

地址选项：

XX		A2	A1	A0
A0 *	=	0	0	外部
A1	=	0	1	外部
A2	=	1	0	外部
A3	=	1	1	外部

* 默认选项。请联系 Microchip 工厂获取其他地址选项

卷带包装： T = 卷带包装

温度范围： E = -40°C 至 +125°C

封装： CH = 塑料小型外型晶体管（SOT-23-6），6引脚

示例：

a) MCP4725A0T-E/CH: 带卷装，宽温范围，6LD SOT-23 封装。地址选项 = A0

b) MCP4725A1T-E/CH: 带卷装，宽温范围，6LD SOT-23 封装. 地址选项 = A1

c) MCP4725A2T-E/CH: 带卷，扩展温度，6LD SOT-23 封装. 地址选项 = A2

d) MCP4725A3T-E/CH: 带卷装，扩展温度，6LD SOT-23 封装。地址选项 = A3

NOTES:

备注：

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

请注意 Microchip 设备上代码保护功能的以下详细信息：

- 微芯产品符合其特定微芯数据表中所包含的规范。
- 微芯相信，其产品系列在按预期方式并在正常条件下使用时，是市场上同类产品中最安全的产品系列之一。
- 存在用于绕过代码保护功能的欺诈性甚至可能非法的方法。据我们所知，所有这些方法都需要以微芯数据表中规定的操作规范之外的方式使用微芯产品。很可能，实施这种行为的人是在从事知识产权盗窃。
- 微芯愿意与关注其代码完整性的客户合作。
- 微芯或任何其他半导体制造商都无法保证其代码的安全性。代码保护并不意味着我们保证产品是“无法破解的”。

代码保护在不断演进。微芯致力于持续改进其产品的代码保护功能。试图绕过微芯的代码保护功能可能违反《数字千年版权法案》。如果此类行为允许未经授权访问您的软件或其他受版权保护的作品，您可能有权根据该法案提起诉讼以获得救济。

商标

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

微芯科技已获得ISO/TS-16949:2002认证，覆盖其全球总部、设计及晶圆制造设施（位于亚利桑那州钱德勒和坦佩；俄勒冈州格雷沙姆；以及加利福尼亚州和印度的设计中心）。公司的质量体系流程和规范适用于其PIC® 微控制器、dsPIC® 数字信号控制器、KEELOQ® 跳码设备、串行EEPROM、微外围设备、非易失性存储器和模拟产品。此外，微芯科技在开发系统设计和制造方面的质量体系已获得ISO 9001:2000认证。

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4080

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

03/26/09

全球销售与服务

美洲

总部办公室 2355 West
Chandler Blvd. Chandler, AZ
85224-6199 电话：
480-792-7200 传真：
480-792-7277 技术支持：
http://support.
microchip.com 网址：
www.microchip.com

亚特兰大
Duluth, GA
电话：678-957-9614
传真：678-957-1455

波士顿 韦斯特伯勒,
MA
电话: 774-760-0087
传真: 774-760-0088

芝加哥 伊塔斯卡, IL
电话: 630-285-0071
传真: 630-285-0075

克利夫兰 独立镇, OH

电话: 216-447-0464
传真: 216-447-0643

达拉斯 艾迪森,
TX
电话：972-818-7423
传真：972-818-2924

底特律，Farmington
Hills，MI
电话：248-538-2250
传真：248-538-2260

Kokomo，
Kokomo，IN
电话：765-864-8360
传真：765-864-8387

洛杉矶
Mission Viejo, CA
电话：949-462-9523
传真：949-462-9608

Santa Clara
Santa Clara, CA
电话：408-961-6444
传真：408-961-6445

Toronto Mississauga,
Ontario, Canada 电话：
905-673-0699 传真：
905-673-6509

亚洲/太平洋

亚太区总部 3707-14，6号
楼37层，九龙湾
Gateway Harbour City，
香港 电话：
852-2401-1200 传真：
852-2401-3431

澳大利亚 - 悉尼 电话：
61-2-9868-6733 传真：
61-2-9868-6755

中国 - 北京 电话：
86-10-8528-2100 传真：
86-10-8528-2104

中国 - 成都 电话：
86-28-8665-5511 传真：
86-28-8665-7889

中国 - 香港特别行政区 电话：
852-2401-1200 传真：
852-2401-3431

中国 - 南京 电话：
86-25-8473-2460 传真：
86-25-8473-2470

中国 - 青岛 电话：
86-532-8502-7355 传真：
86-532-8502-7205

中国 - 上海 电话：
86-21-5407-5533 传真：
86-21-5407-5066

中国 - 沈阳 电话：
86-24-2334-2829 传真：
86-24-2334-2393

中国 - 深圳 电话：
86-755-8203-2660 传真：
86-755-8203-1760

中国 - 武汉 电话：
86-27-5980-5300 传真：
86-27-5980-5118

中国 - 厦门 电话：
86-592-2388138 传真：
86-592-2388130

中国 - 西安 电话：
86-29-8833-7252 传真：
86-29-8833-7256

中国 - 珠海 电话：
86-756-3210040 传真：
86-756-3210049

亚洲/太平洋

印度 - 班加罗尔 电话：
91-80-3090-4444 传真：
91-80-3090-4080

印度 - 新德里 电话：
91-11-4160-8631 传真：
91-11-4160-8632

印度 - 浦那 电话：
91-20-2566-1512 传真：
91-20-2566-1513

日本 - 横滨 电话：
81-45-471-6166 传真：
81-45-471-6122

韩国 - 大邱 电话：
82-53-744-4301 传真：
82-53-744-4302

韩国 - 首尔 电话：
82-2-554-7200
传真：82-2-558-5932 或
82-2-558-5934

马来西亚 - 吉隆坡 电话：
60-3-6201-9857 传真：
60-3-6201-9859

马来西亚 - 槟城 电话：
60-4-227-8870 传真：
60-4-227-4068

菲律宾 - 马尼拉 电话：
63-2-634-9065 传真：
63-2-634-9069

新加坡 电话：
65-6334-8870 传真：
65-6334-8850

台湾 - 新竹 电话：
886-3-6578-300 传真：
886-3-6578-370

台湾 - 高雄 电话：
886-7-536-4818 传真：
886-7-536-4803

台湾 - 台北 T
el 886 2 2500
: -- -6610 传真：
886-2-2508-0102

泰国 - 曼谷 电话：
66-2-694-1351 传真：
66-2-694-1350

欧洲

奥地利 - 维也纳 电话：
43-7242-2244-39 传真：
43-7242-2244-393

丹麦 - 哥本哈根 电话：
45-4450-2828 传真：
45-4485-2829

法国 - 巴黎 电话：
33-1-69-53-63-20 传真：
33-1-69-30-90-79

德国 - 慕尼黑 电话：
49-89-627-144-0 传真：
49-89-627-144-44

意大利 - 米兰 电话：
39-0331-742611 传真：
39-0331-466781 荷兰 - 杜
伦 电话：31-416-690399
传真：31-416-690340

西班牙 - 马德里 电话：
34-91-708-08-90 传真：
34-91-708-08-91

英国 - 沃金汉姆 电话：
44-118-921-5869 传真：
44-118-921-5820

03/26/09