CS 340

#4: Logic Gates, ISAs, and Instruction Sets

Computer Systems | Sept. 1, 2022 · Wade Fagen-Ulmschneider

Logic Gates and Truth Tables

We can begin to define the building blocks of the CPU by basic instructions with input bits and output bits through logical gates.

• By convention, you will see that the input bits are labeled A and **B** by default.

Logic Gate #1:

Logic Gate #2:

Logic Gate #3:

Logic Gate Challenge: A XOR B

We can also express this in a table known as a **truth table**:

Op.	Binary	Math	Example Value	es	
	Α	х	1100	110011	101
	В	у	1010	11	010
AND	A & B	ху			
OR	A B	x + y			
XOR	A ^ B	x XOR y			
NOT	!A	x '			

Truth Table: Half Adder

Α	В	A + B	<u>s</u> um	<u>C</u> ARRY

Truth Table for a Half Adder

Circuit Diagram for a "Half Adder":

Endl	44	A	ΩИ
HIIII	AΠ	а	er

Α	В	CARRY _{in}		SUM	CARRY _{out}

Truth Table for a Full Adder

Circuit Diagram for a "Full Adder":

Chaining Circuits Together:

Disadvantages:

Instruction	Set Architecture	(ISA)
-------------	-------------------------	-------

Every CPU has a set of commands it understands known as its Instruction Set Architecture or ISA. Two ISAs are **very** common:

1.

2.

An ISA defines the function of the hardware in the CPU.

CPU Registers

Each CPU core has an extremely limited number of _____ that are used for general purpose CPU operations:
• x64: 16 registers of 64 bits

- ARMv8: 31 registers of 64 bits

With very few exceptions ₋	

Instruction Sets

Every ISA defines a set of instructions that a CPU can execute:

Move:	MOV, XCHG, PUSH, POP,
Arithmetic (int):	ADD, SUB, MUL, DIV, NEG, CMP,
Logic:	AND, OR, XOR, SHR, SHL,
Control Flow:	JMP, LOOP, CALL, RET,
Synchronization:	LOCK,
Floating Point:	FADD, FSUB, FMUL, FDIV, FABS,

ARM processors have significantly fewer	instructions and are known
as	while x64 processors have a
greater set of instructions and known as	

Q: Advantages of RISC / CISC?

CPU Instruction in a Real Program

	04.c	gcc 04.c objdump -d ./a.out	
3	<pre>int main() {</pre>	f3 0f 1e fa endbr64 55 push %rbp 48 89 e5 mov %rsp,%rbp 48 83 ec 10 sub \$0x10,%rsp	
4	int a = 0;	c7 45 fc 00 00 00 00 movl \$0x0,-0x4(%rbp)
5	a = a + 3;	83 45 fc 03 addl \$0x3,-0x4(%rbp)
6	a = a - 2;	83 6d fc 02 sub1 \$0x2,-0x4(%rbp)
7	a = a * 4;	c1 65 fc 02 shll \$0x2,-0x4(%rbp)
8	a = a / 2;	8b 45 fc mov -0x4(%rbp),%ea 89 c2 mov %eax,%edx c1 ea 1f shr \$0x1f,%edx 01 d0 add %edx,%eax d1 f8 sar %eax 89 45 fc mov %eax,-0x4(%rbp	
9	a = a * 5;	8b 55 fc mov -0x4(%rbp),%ed 89 d0 mov %edx,%eax c1 e0 02 shl \$0x2,%eax 01 d0 add %edx,%eax 89 45 fc mov %eax,-0x4(%rbp)	
10	printf("Hi");	48 8d 3d f0 0d 00 00 lea 0xdf0(%rip),%r # 2004 <_IO_stdin_used+0x b8 00 00 00 00 mov \$0x0,%eax e8 42 fe ff ff callq 1060 <printf@pl< th=""><th>(4></th></printf@pl<>	(4>
11	a = a * 479;	8b 45 fc mov -0x4(%rbp),%ea 69 c0 df 01 00 00 imul \$0x1df,%eax,%e 89 45 fc mov %eax,-0x4(%rbp	eax

Program Counter (PC):

Operation Timings: