DAC YF

Adaptive Layout Decomposition with Graph Embedding Neural Networks

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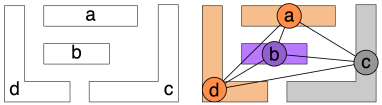
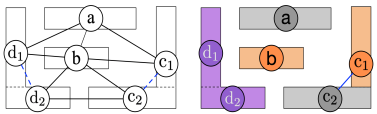
DESIGN AUTOMATION CONFERENCE
FROM CHIPS TO SYSTEMS – LEARN TODAY, CREATE TOMORROW

Layout decomposition

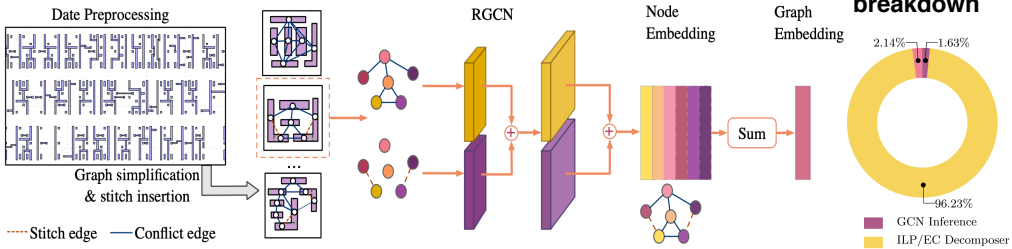


An example of the uncolorable case



An example of the stitch candidate and stitch

Graph Embedding Workflow by RGCN

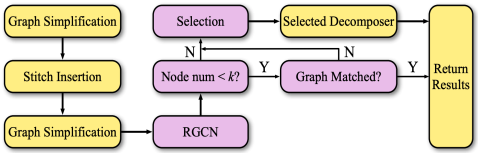


Runtime breakdown

Other methods

- ILP
  - Pros: Optimal
  - Cons: Bad runtime performance
- EC
  - Pros: High efficiency
  - Cons: Degradation of the solution quality
- Graph matching‡
  - Pros: Good performance in both efficiency and quality for small graphs
  - Cons: Graph library size is limited

Our framework



Decomposition results

Circuit	ILP				SDP				EC				RGCN			
	st#	cn#	cost	time (s)	st#	cn#	cost	time (s)	st#	cn#	cost	time (s)	st#	cn#	cost	time (s)
C432	4	0	0.4	0.486	4	0	0.4	0.016	4	0	0.4	0.005	4	0	0.4	0.007
C499	0	0	0	0.063	0	0	0	0.018	0	0	0	0.011	0	0	0	0.015
C880	7	0	0.7	0.135	7	0	0.7	0.021	7	0	0.7	0.010	7	0	0.7	0.014
C1355	3	0	0.3	0.121	3	0	0.3	0.024	3	0	0.3	0.011	3	0	0.3	0.015
C1908	1	0	0.1	0.129	1	0	0.1	0.024	1	0	0.1	0.017	1	0	0.1	0.031
C2670	6	0	0.6	0.158	6	0	0.6	0.044	6	0	0.6	0.035	6	0	0.6	0.046
C3540	8	1	1.8	0.248	8	1	1.8	0.086	8	1	1.8	0.032	8	1	1.8	0.038
C5315	9	0	0.9	0.226	9	0	0.9	0.106	9	0	0.9	0.039	9	0	0.9	0.049
C6288	205	1	21.5	5.569	203	4	24.3	0.648	203	5	25.3	0.151	205	1	21.5	0.154
C7552	21	1	3.1	0.872	21	1	3.1	0.157	21	1	3.1	0.071	21	1	3.1	0.111
S1488	2	0	0.2	0.147	2	0	0.2	0.031	2	0	0.2	0.013	2	0	0.2	0.016
S38417	54	19	24.4	7.883	48	25	29.8	1.686	54	19	24.4	0.329	54	19	24.4	0.729
S35932	40	44	48	13.692	24	60	62.4	5.130	46	44	48.6	0.868	40	44	48	1.856
S38584	117	36	47.7	13.494	108	46	56.8	4.804	116	37	48.6	0.923	117	36	47.7	1.840
S15850	97	34	43.7	11.380	85	46	54.5	4.320	100	34	44	0.864	97	34	43.7	1.792
average			12.893	3.640			15.727	1.141			13.267	0.225			12.893	0.448
ratio			1.000	1.000			1.220	0.313			1.029	0.062			1.000	0.123