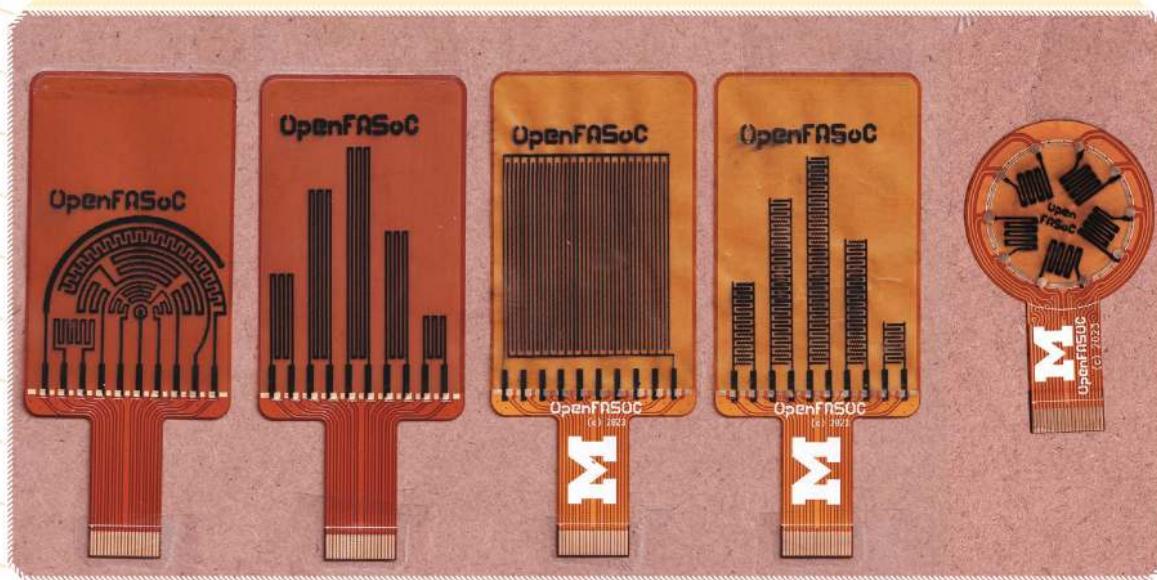


Anhang Li , Hongyi Wu , Madhulika Lingamguntla , Ashbir Aviat Fadila , Chan-Ho Kye , Arvind Balijepalli , Tim Ansell , Nigel J. Coburn , Sachin Nadig , and Mehdi Saligane 

Rapid Prototyping of Laser-Induced Graphene Sensors With Open-Source Silicon

Paving the Way for Low-Cost and Robust Flexible Wearable Sensing



THE IMAGE IS PHOTOGRAPHED BY ANHANG LI AT THE UNIVERSITY OF MICHIGAN.

Digital Object Identifier 10.1109/MSSC.2024.3380586

Date of current version: 25 June 2024



L

The open source hardware movement has made significant progress over the past few years.

Increasingly, more individuals are engaging with and participating in the open source chip design community, not only to design their chips with available open source tools but also to have their designs physically fabricated and returned to them for practical use. Companies like Google have sponsored physical chip fabrication runs over the past few years, such as OpenMPW, through semiconductor CMOS processes provided by Skywater (SKY130) and GlobalFoundries (GF180) [1]. When we consider the availability of open source chip design tools, a supportive community, reliable fabrication partners, financial sponsors, and a growing infrastructure of suppliers and educators, it becomes clear that a revolution in

chip design is an inevitable outcome. By leveraging existing resources provided by the open source community, this article presents the joint development of a new laser-induced graphene (LIG)-based sensor platform. The effort includes the design, fabrication, and testing of an AFE ASIC using open tools and the design and in-house fabrication of LIG sensors. The article presents the ASIC's design process and the fabricated chip's testing results. It demonstrates testing a wearable strain gauge LIG sensor and a temperature-sensitive LIG sensor using our AFE chip. The demonstration serves as an example of the potential to develop the sensing system into a multimodal flexible sensing platform.

LIG Sensor Design and Fabrication

Over the last two decades, graphene-based materials have attracted extensive attention because of their unique physical and chemical properties [2].

Compared to high-cost conventional methods of producing graphene, the LIG approach eliminates complex chemical synthesis steps and high-temperature processing. Additionally, the LIG approach is a quite straightforward one-step method to fabricate large-area graphene, especially for applications demanding precise custom-designed patterns on the surface of carbonaceous films [3].

LIG has a range of useful properties, such as high conductivity, a large surface area, and resistance to strain and corrosion [4]. Additionally, it can be functionalized to catalyze reactions or sense pressure, temperature, the intensity of magnetic fields, and the concentration of chemicals [4]. Consequently, it is exceptionally suitable for flexible and wearable electronics applications as a physical or electrochemical sensor [5], [6].

Polyimide Flexible PCB and Sensor Pattern Design

Our LIG sensors are integrated into polyimide flexible PCBs (FPCBs) that are designed to carry the sensor patterns. These FPCBs have flexible connectors that allow the LIG sensors to be connected to our AFE chip PCB for readout. The fabrication process for these FPCBs is standard and widely used in consumer electronics.

To expand the capability of a single sheet of LIG sensor, the layout is designed in such a way that sensor patterns serving different purposes are combined into one composite pattern. Figure 1 showcases two examples of LIG sensor patterns on circular and square FPCBs. These sensors include double-ended resistive and capacitive sensors for strain and temperature sensing and single-ended sensors that enable possible electrochemical sensing capabilities.

The resistive LIG sensors are sensitive to strain and temperature, which can be considered strain gauge sensors made of an emerging material. The LIG base strain gauge sensors promise high sensitivity, excellent repeatability, durability, and fast response times. Figure 1(a) shows a

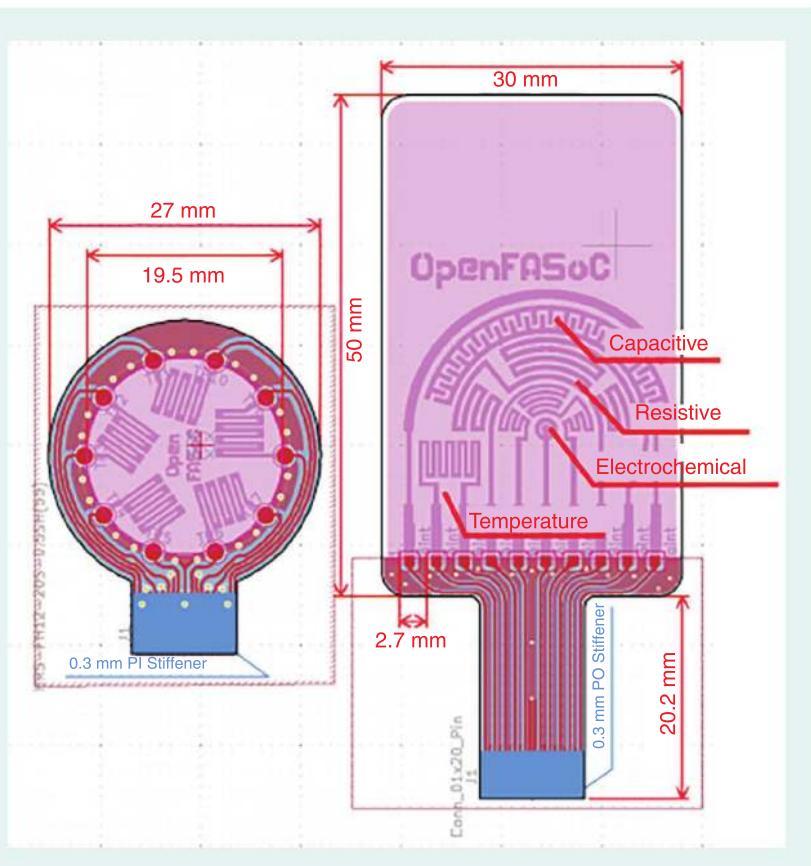


FIGURE 1: The layout designs for LIG sensors in KiCAD. The (a) penta-directional strain sensor and (b) composite multifunctional sensor. PI: polyimide; PO: polonium.

penta-direction strain sensor on the circular FPCB to detect strain and vibration from multiple directions. In addition to strain sensitivity, the LIG sensors are sensitive to temperature and humidity, allowing them to engage in various physical sensing applications. A similar mechanism operates for the capacitive LIG sensors as well. Moreover, due to the porous and 3D structures of the LIG sensors, they are also sensitive to specific chemical molecules when properly functionalized [5].

As opposed to having only resistive sensors, Figure 1(b) describes a composite multifunctional sensor on an FPCB, which could offer various kinds of physical and chemical sensing for wearable electronics. This work is a stepping stone for exciting future work where multiple-layer design could be implemented. Extra layers for fluidics could be fabricated above the LIG sensors to further expand functionality, including electrochemical and biomedical sensing capabilities.

LIG Sensor Fabrication and Application

Carbon dioxide (CO_2) infrared ray (IR) lasers stand as a common choice in LIG fabrication because they are cheap and quite efficient in carbonizing raw materials. At the same time, most substrates have large absorption in the medium- and far-IR wavelength regimes of CO_2 lasers, which allows fast and efficient carbonization [7]. Alternative lasers with shorter wavelengths, such as a 405-nm visible laser, are also explored to achieve higher resolution, but there are tradeoffs in terms of higher costs and larger irradiance requirements [8].

The width of the lines in our patterns varies from $200\ \mu\text{m}$ to 1 mm, so a CO_2 IR laser cutter is enough to meet the resolution. Figure 2(a) presents the schematics of the laser inducing on the FPCB and the LIG sensors under fabrication. The appropriate power, scan speed, and dpi we found to make the graphene induced successfully without burning through the FPCB are 6–9 W, 0.21–0.42 m/s, and 500–800,

respectively. Figure 2(b) displays fabricated samples.

Figure 3 examines two example scenarios for LIG sensor applications. The penta-direction strain/vibration

sensor can be employed to detect structural bending or vibration, while the composite sensor can serve for both human physical and electrochemical sensing.

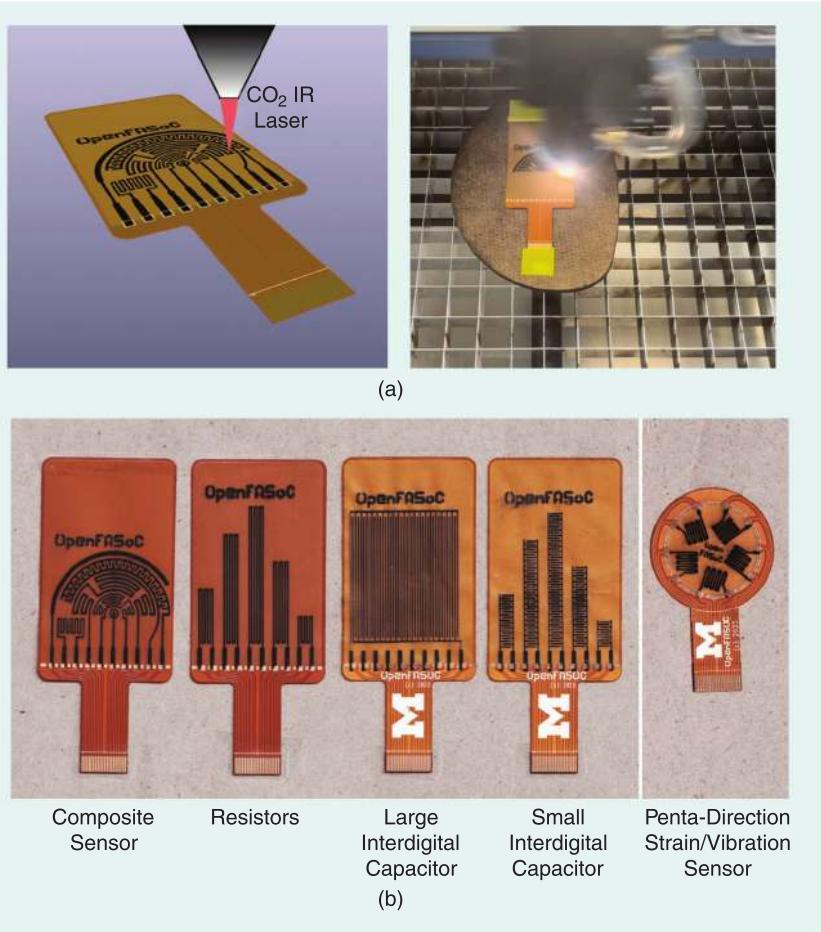


FIGURE 2: The (a) LIG sensor fabrication and (b) fabricated samples.

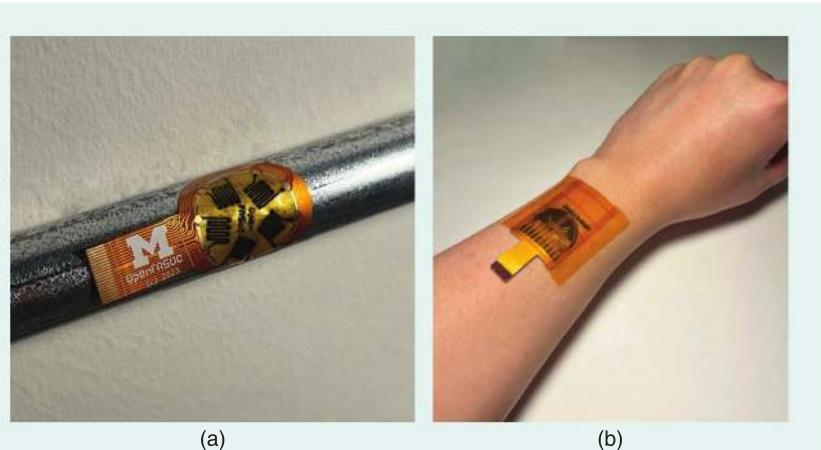


FIGURE 3: Intended applications of the LIG sensors. (a) A strain gauge for structure bending/vibration monitoring [9]. (b) A composite electrochemical sensor for human biometric measurements [4], [6].

Open Source AFE Sensor Readout

We utilized the open source analog electronics design automation (EDA) toolchain in GF180 to complete this project and pave the way for future tape out and the wider open source chip design community. Our FPCB LIG sensors were equipped with a flexible and generic readout AFE circuit,

significantly reducing costs by eliminating the need for expensive licenses associated with commercial tools. This approach aligns with the ethos of our multifunctional and low-cost sensors. Additionally, designers can take advantage of sponsored multiproject wafer shuttles, such as OpenMPW, to share high fabrication costs collec-

tively, which facilitates prototyping with limited resources.

The AFE chip integrates two operational amplifiers (OPAMPs), a SAR ADC, and a capacitive DAC (Figure 4). The OPAMPs and the SAR ADC are characterized and used as building blocks to build a testing platform to test the fabricated sensor. The following sections describe each component in detail. To facilitate reproducing our results and checking our design, we have published GDSII files, which are available for release on the GitHub repository [10].

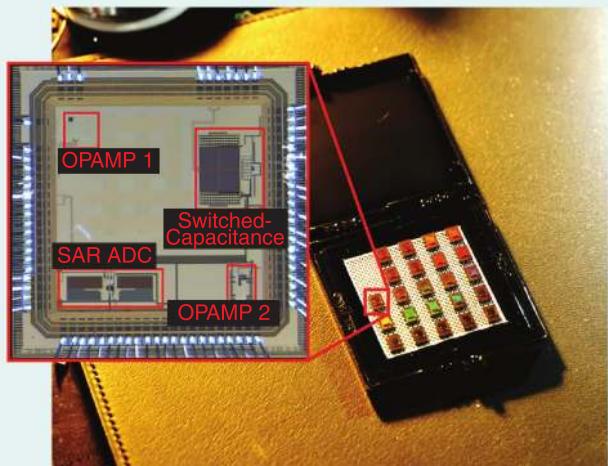
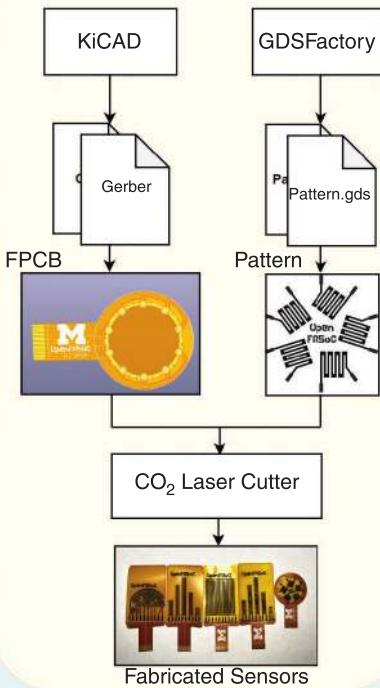
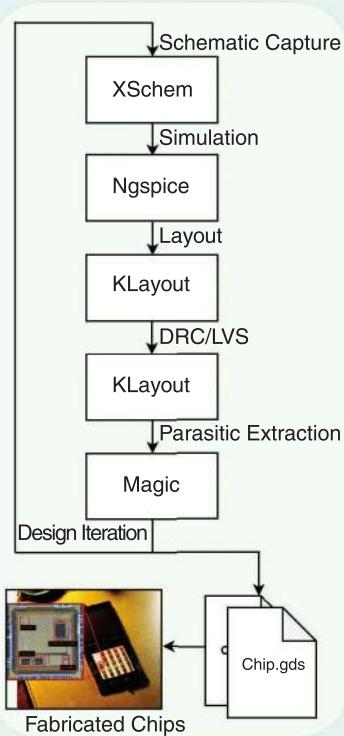


FIGURE 4: An annotated die shot and a photograph of the chip.

FPCB and LIG Sensor



ASIC Chip



Open Source Analog Design Flow

We have leveraged an open source analog design flow and EDA tools, where we utilize XSchem for schematic capture, Ngspice for simulation, KLayout and Magic for layout, design rule checks (DRCs)/layout-versus-schematic checks (LVSs), and parasitic extraction [11]. The design of the LIG sensors is also done with open source software, where KiCAD and GDSFactory [12] are used to design FPCBs and sensor patterns, respectively. Figure 5 displays this open source design flow.

Hybrid Folded-Cascode OPAMP Design

The chip contains a class AB folded-cascode OPAMP design with a built-in bias generator [13]. As shown in Figure 6(a), in addition to the high-gain low-noise device sizing design, the OPAMP has a V_{prog} pin that allows the user to trade extra power consumption for even lower noise [14], making this design flexible for different applications. Note that there exists a large difference between the simulated CMRR/PSRR and measured CMRR/PSRR. This is likely due to device mismatch. Monte Carlo simulation is needed to capture this kind of deviation, but the open tools did not support this feature at the time of design. Table 1 lists the results of the OPAMP at a 3.3-V supply, 1-V bias V_{prog} , and 5-mW power consumption for simulation. On the actual chip, the power rails

FIGURE 5: The LIG sensor and ASIC open source analog design flow. The (a) FPCB and LIG sensor and (b) ASIC chip.

are connected together with other blocks, so the power is overestimated in the measured result.

SAR ADC Design

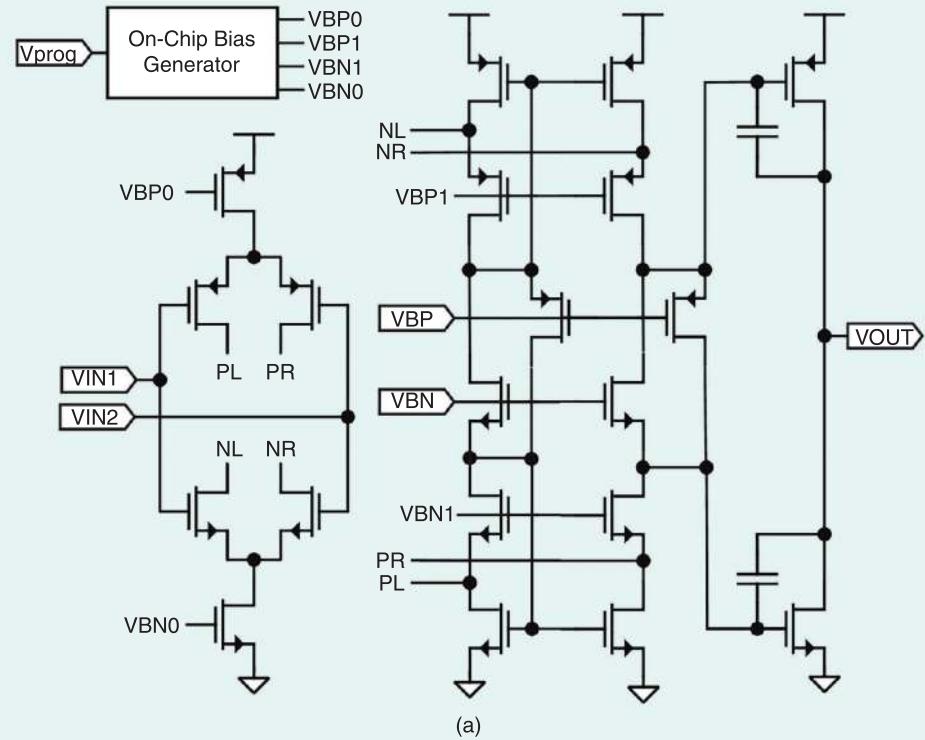
Figure 6(b) is a high-level circuit diagram of the SAR ADC. This 14-b SAR ADC is an asynchronous design using the monotonic switching method [15]. The comparator is based on the Miyahara comparator design that implements automatic offset compensation [16]. A preamp is used to drive the comparator to increase operation speed.

To achieve higher bandwidth, the CDAC array is implemented as metal-oxide–metal (MOM) capacitors, with each individual cell holding less than 20 fF of capacitance. This requires an accurate parasitic extraction of the MOM capacitor to ensure that the fabricated chip matches the simulated results. Unfortunately, postlayout extraction inaccuracies have led to severe dc distortion in the fabricated chip. Unlike the noise-limited ENOB in simulation, the ENOB of the fabricated chip is primarily limited by distortion (see Table 2). Figure 7

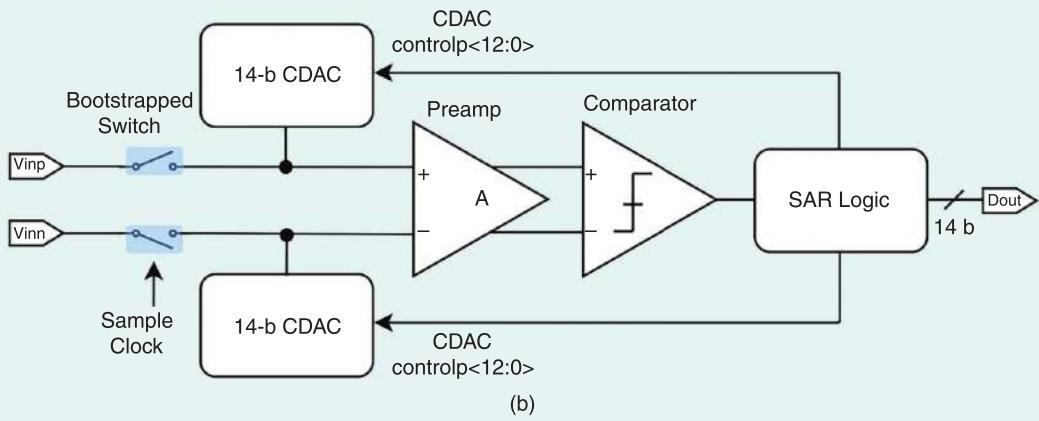
gives the measured spectrum, with a Nyquist-rate signal applied to the input.

Testing Setup and Measurement Results

As a demonstration, we used the penta-direction strain and vibration LIG sensor in Figure 3(a) to behave like a resistor whose value changes with the external input, such as bending, temperature change, and vibrations [17]. The aforementioned AFE chip is then used to convert the resistance into digital readouts. Figure 8(a) shows



(a)



(b)

FIGURE 6: The circuit block designs. The (a) hybrid folded-cascode circuit and (b) SAR ADC.

that the AFE is first connected with external passive components to form a prototype digitizing system for the LIG sensors. The prototype is then consolidated into a compact digitizer board, illustrated in Figure 8(b), with the silicon chip directly wire bonded to the PCB.

Figure 9(a) displays the schematic diagram of the digitizer board. It consists of a Wheatstone bridge, a Sallen-Key second-order antialiasing filter (AAF), and an ADC. The Wheatstone is built using one of the two OPAMPs as a TIA; the AAF is built using another on-chip OPAMP to remove aliasing

and drive the input capacitance of the ADC. The output data stream is further low-pass filtered in a software FIR filter, and eventually, it gives a dynamic response of the flex sensors, as in Figure 9(b) and (c).

Five resistive patterns on the same circular penta-direction LIG sensor patch are put into a temperature chamber to test how they react to temperature change. The sensors are first exposed to a temperature sweep, with one of them used as the reference sensor. As plotted in Figure 10(a), all the sensors follow a quadratic curve after normalization despite the sensors having significant absolute value differences due to fabrication inaccuracies. Curve fitting to the quadratic formula shows an R^2 factor of 0.9989, indicating a good fit. The sensor is then attached to different parts of the human body to see how it performs as a body temperature monitoring device [17]. As evident in Figure 10(b), the sensor can take a couple of minutes to stabilize until it converges to a desirable result.

Conclusion

This article presented a custom readout chip for an AFE designed using an open source design flow. The chip can function as a universal readout platform for resistive sensors. The AFE components are designed to support the operation of an ADC with a 14-b resolution and a 10-MHz sampling rate. The real-time bend detection example demonstrates that the signal chain is capable of detecting different stopping angles of finger bending at a rate of 10 kHz. The temperature sensing demonstration shows that the system can monitor temperature changes from -20 to 40 °C using a quadratic curve fitting with $R^2 = 0.9989$. These results build confidence in the open source chip flow and the designed LIG (low-cost, flexible, and ion-permeable) sensors. In future iterations, we look forward to expanding the design by adding multisensor muxing, a capacitor-to-digital converter for the capacitive LIG sensors, and reducing the external components.

TABLE 1. A COMPARISON OF OPEN SOURCE TOOLS SIMULATION RESULTS AND SILICON RESULTS OF THE HYBRID FOLDED-CASCODE OPAMP.

METRIC (AT $V_{DD} = 3.3V$)	OPEN TOOLS SIMULATION	MEASURED RESULTS
Power (mW)	5	<10
Gain bandwidth product (MHz)	14	12.5
DC gain (dB)	99	92
Offset (mV)	Monte Carlo simulation is not supported in open tools.	5~20
PSRR (dB)	94.2	81.5
CMRR (dB)	118	58
Input range (V)	—	0.8~2.6

TABLE 2. A COMPARISON OF OPEN SOURCE TOOLS SIMULATION RESULTS AND SILICON RESULTS OF THE SAR ADC.

METRIC	OPEN TOOLS SIMULATION	MEASURED RESULTS
Functional sampling rate	31.25 MS/s	>30 MS/s
ENOB at 20 MS/s	7.92 b (noise limited)	4.27 b (distortion limited)
SFDR	>70 dB	33.7 dB
SNR at 20 MS/s	—	41 dB
Input swing	6 V _{pp}	6 V _{pp}

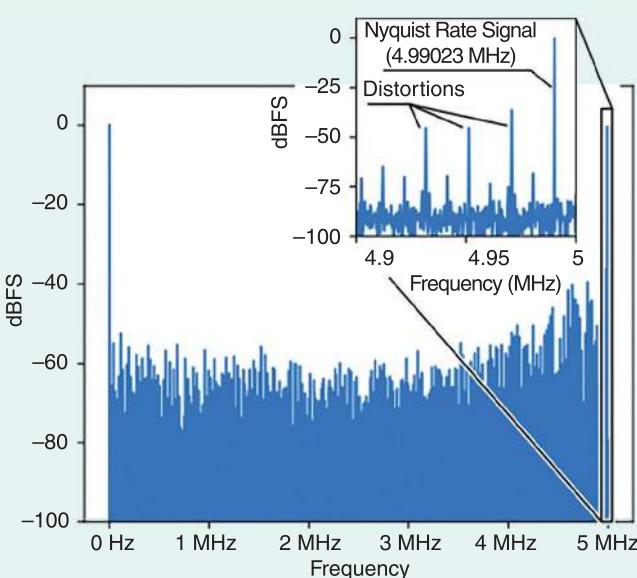


FIGURE 7: The ADC measured spectrum with Nyquist input.

Acknowledgment

The authors would like to thank Google for its support and Global Foundries for chip fabrication. Certain commercial entities, equipment,

or materials may be identified in this article in order to describe an experimental procedure or concept adequately. Such identification is not intended to imply recommendation or

endorsement by the National Institute of Standards and Technology nor is it intended to imply that the entities, materials, or equipment are necessarily the best available for the purpose.

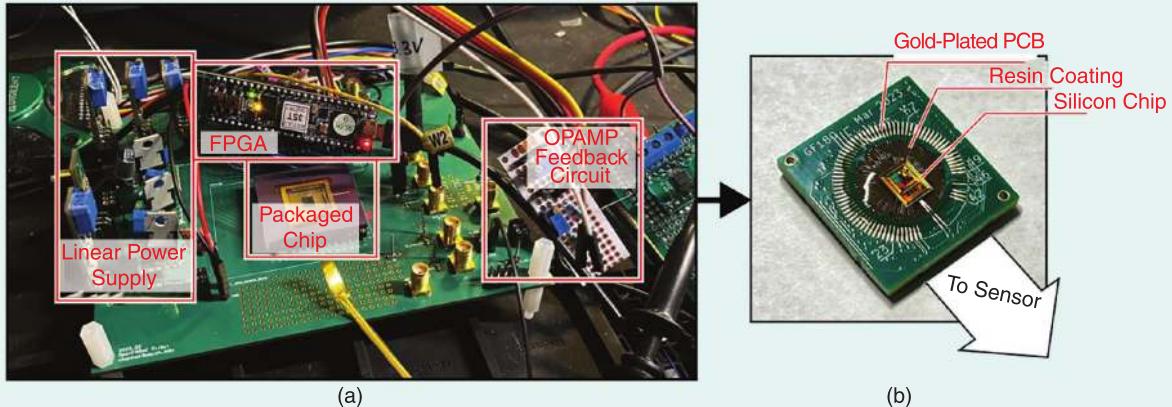


FIGURE 8: The test setup and sensor platform design. The (a) prototype boards for testing and (b) wire-bonded chip.

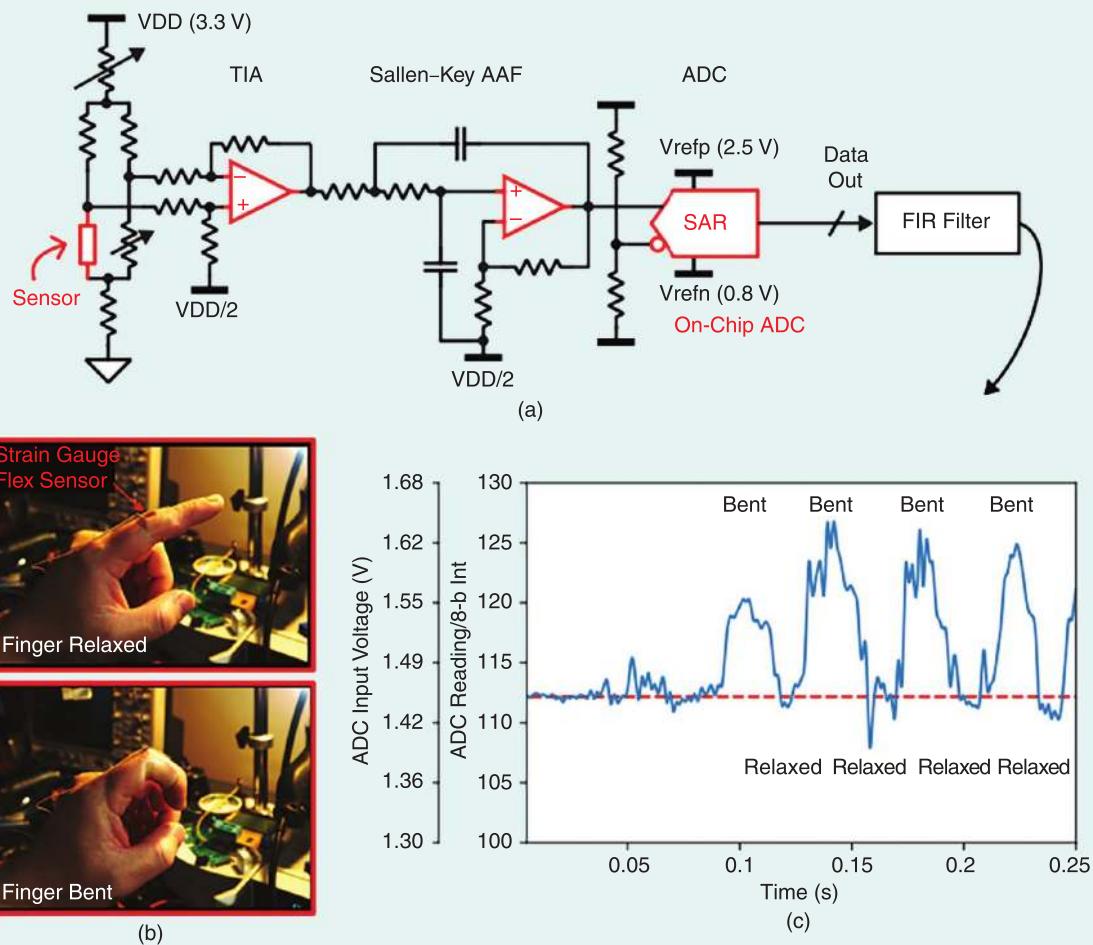


FIGURE 9: The ASIC-based Wheatstone bridge circuit and a flex sensor application. The (a) sensor test setup, (b) user input, and (c) recorded waveform. AAF: antialiasing filter; Int: integer.

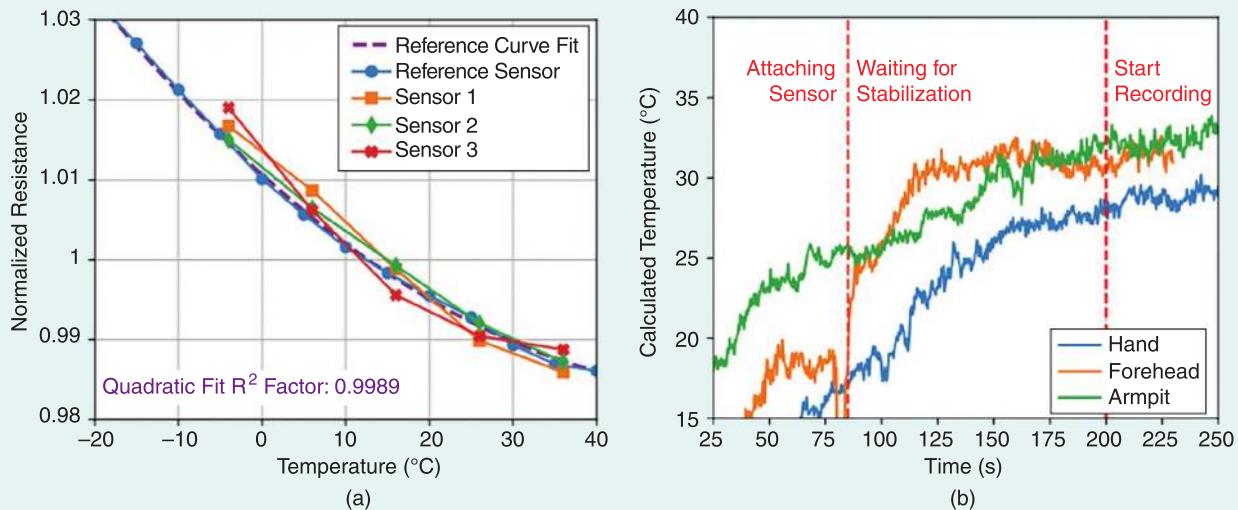


FIGURE 10: The temperature sensor characterization and measurement results. (a) The characterization of temperature sensors. (b) Body temperature measurements in different spots.

References

- [1] "GlobalFoundries GF180MCU open source PDK." Google. Accessed: Apr. 1, 2024. [Online]. Available: <https://github.com/google/gf180mcu-pdk>
- [2] A. K. Geim, "Graphene: Status and prospects," *Science*, vol. 324, no. 5934, pp. 1530–1534, 2009, doi: [10.1126/science.1158877](https://doi.org/10.1126/science.1158877).
- [3] J. Lin et al., "Laser-induced porous graphene films from commercial polymers," *Nature Commun.*, vol. 5, no. 1, 2014, Art. no. 5714, doi: [10.1038/ncomms6714](https://doi.org/10.1038/ncomms6714).
- [4] F. M. Vivaldi et al., "Three-dimensional (3D) laser-induced graphene: Structure, properties, and application to chemical sensing," *ACS Appl. Mater. Interfaces*, vol. 13, no. 26, pp. 30,245–30,260, 2021, doi: [10.1021/acsami.1c05614](https://doi.org/10.1021/acsami.1c05614).
- [5] H. Wang et al., "A soft and stretchable electronics using laser-induced graphene on polyimide/PDMS composite substrate," *NPJ Flexible Electron.*, vol. 6, no. 1, 2022, Art. no. 26, doi: [10.1038/s41528-022-00161-z](https://doi.org/10.1038/s41528-022-00161-z).
- [6] J. Tu et al., "A wireless patch for the monitoring of C-reactive protein in sweat," *Nature Biomed. Eng.*, vol. 7, no. 10, pp. 1293–1306, 2023, doi: [10.1038/s41551-023-01059-5](https://doi.org/10.1038/s41551-023-01059-5).
- [7] G. Li, "Direct laser writing of graphene electrodes," *J. Appl. Phys.*, vol. 127, no. 1, 2020, Art. no. 010901, doi: [10.1063/1.5120056](https://doi.org/10.1063/1.5120056).
- [8] M. G. Stanford et al., "High-resolution laser-induced graphene. Flexible electronics beyond the visible limit," *ACS Appl. Mater. Interfaces*, vol. 12, no. 9, pp. 10902–10907, 2020, doi: [10.1021/acsami.0c01377](https://doi.org/10.1021/acsami.0c01377).
- [9] J. Qu, Q. Wu, T. Clancy, Q. Fan, X. Wang, and X. Liu, "3D-printed strain-gauge micro force sensors," *IEEE Sensors J.*, vol. 20, no. 13, pp. 6971–6978, Jul. 2020, doi: [10.1109/JSEN.2020.2976508](https://doi.org/10.1109/JSEN.2020.2976508).
- [10] "OpenFASoC-Tapeouts." GitHub. Accessed: Jan. 24, 2024. [Online]. Available: <https://github.com/idea-fasoc/openfasoc-tapeouts>
- [11] "EE628 open-source tools." GitHub. Accessed: Apr. 1, 2024. [Online]. Available: https://github.com/bmurmurmann/EE628/tree/main/3_Tools
- [12] "Gdsfactory: An open-source platform for end-to-end chip design and validation." Gdsfactory. Accessed: Apr. 1, 2024. [Online]. Available: <https://gdsfactory.github.io/gdsfactory/index.html>
- [13] K. J. De Langen and J. H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct. 1998, doi: [10.1109/4.720394](https://doi.org/10.1109/4.720394).
- [14] C. Bronkowsky and D. Schroeder, "An ultra low-noise CMOS operational amplifier with programmable noise-power trade-off," in *Proc. 32nd Eur. Solid-State Circuits Conf.*, 2006, pp. 368–371, doi: [10.1109/ESSCIR.2006.307607](https://doi.org/10.1109/ESSCIR.2006.307607).
- [15] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010, doi: [10.1109/JSSC.2010.2042254](https://doi.org/10.1109/JSSC.2010.2042254).
- [16] M. Miyahara, Y. Asada, D. Paik, and A. Matsumura, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Fukuoka, Japan, 2008, pp. 269–272, doi: [10.1109/ASSCC.2008.4708780](https://doi.org/10.1109/ASSCC.2008.4708780).
- [17] A. Kaidarová and J. Kosek, "Physical sensors based on laser-induced graphene: A review," *IEEE Sensors J.*, vol. 21, no. 11, pp. 12,426–12,443, Jun. 2021, doi: [10.1109/JSEN.2020.3034845](https://doi.org/10.1109/JSEN.2020.3034845).

About the Authors

Anhang Li (anhangli@umich.edu) received his B.S. degree in microelectronics at Sun Yat-Sen University, Guangzhou, China, and his M.S. degree in electrical engineering at Columbia University, New York, NY, USA, in 2022. He is currently pursuing his Ph.D. degree in electrical and computer engineering at the University of Michigan, Ann Arbor, MI 48109 USA. His research interests include computer-aided mixed-signal design, SoCs, and RF/MMIC circuit design.

Hongyi Wu (hongyiwu@umich.edu) received his B.S. degree in applied physics from the University of Science and Technology of China, Hefei, China, in 2022. He is currently pursuing his M.S. and Ph.D. degrees in electrical and computer engineering at the University of Michigan, Ann Arbor, MI 48109 USA. His research interests include mixed-signal circuit design and ICs for biomedical and sensor applications.

Madhulika Lingamguntla (lmadhu@umich.edu) received her B.S. degree in electrical engineering from the Indian Institute of Technology Gandhinagar, Palaj, India, and is currently pursuing her M.S. degree in electrical and computer engineering at the University of Michigan, Ann Arbor, MI 48109 USA. Previously, she worked at the Indian Space Research Organization on the design and characterization of electro-optical image sensors. She also has prior experience in designing overprotection and overtemperature detection circuits for buck regulators at Texas Instruments. Her research interests include mixed-signal design for biosensing circuits, the design of low-power low-noise amplifiers, and residue amplifiers for SAR ADCs for various applications.

Ashbir Aviat Fadila (fadila@ssc.pe.titech.ac.jp) received his B.S. degree in electrical engineering from the Bandung Institute of Technology, Bandung, Indonesia, in 2015. After graduating, he worked as a standard cell mask layout engineer at Marvell Technology, Jakarta, Indonesia, for a year. From 2016 to 2017, he served as a research assistant at his alma mater, where his work focused on developing SoCs designed for IoT applications. He completed his M.S. degree in 2020 in electrical and electronic engineering at the Tokyo Institute of Technology, Tokyo 152-8550, Japan, where he is now working toward his Ph.D. degree. His research interests include analog-mixed-signal processing, data converters, and the design of synthesizable analog circuits. He is a Graduate Student Member of IEEE.

Chan-Ho Kye (chanho.kye@suwon.ac.kr) received his B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2016, and his Ph.D. degree in electrical and computer engineering from Seoul National University, Seoul, in 2021. In 2021, he was with the Inter-University Semiconductor Research Center, Seoul National University. In 2022, he was a postdoctoral researcher at the Swiss Federal Institute of Technology Lausanne, Neuchâtel, Switzerland. In 2023, he was a postdoctoral research fellow at the University of Michigan, Ann Arbor, MI, USA. Since October 2023, he has been an assistant professor at the University of Suwon, 445743 Hwaseong, South Korea. His research interests include the design of high-speed I/O circuits and high-speed ADCs.

Arvind Balijepalli (arvind.balijepalli@nist.gov) is a project leader in the Physical Measurement Laboratory, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899 USA. He received his Ph.D. degree at the University of Maryland, College Park, College Park, MD, USA. He joined NIST after completing a joint National Research Council postdoctoral fellowship between NIST and the National Institutes of Health. At NIST,

he develops new chip-scale sensing techniques to enable measurements of fundamental biophysical phenomena, including biomolecular interactions of proteins, nucleic acids, and small molecules.

Tim (Mithro) Ansell (me@mith.ro) is a pioneering figure in open source silicon, known for his crucial role in democratizing chip design. Through initiatives like the SkyWater and GlobalFoundries open source process design kits and the Open MPW program, he has significantly lowered barriers to entry, enabling innovation and access for individuals and smaller entities in semiconductor technology. Tim recently left Google and will soon be joining Arc PBCs to build out their new R&D Lab.

Nigel J. Coburn (nigelcoburn@google.com) is currently a sensor design engineer at Google, San Diego, CA 92108 USA. He received his Ph.D. degree from the University of Cambridge, Cambridge, U.K., where he was part of the Solid State Electronics and Nanoscale Science Group, based out of the Center for Advanced Photonics and Electronics. He received his M.Eng. degree from Queen's University Belfast, Belfast, U.K., after completing research and studies at Chalmers University of Technology, Gothenburg, Sweden, as an Erasmus scholar. He has previously been a visiting scholar at McGill University, Montréal, QC, Canada, and Northeastern University, Boston, MA, USA, as well as an adjunct professor within the Department of Materials Science and Engineering, Boston University, Boston, MA, USA. Prior to his work at Google, he worked on the development of single-molecule sensors, devices, and instrumentation for applications in genomics at Illumina, San Diego. He has also worked for BAE Systems, Analog Devices, and the European Space Agency, where much of his work focused on the research and development of various sensors and devices.

Sachin Nadig (sachinnadig@google.com) received his B.Eng. degree in electrical engineering from the PES Institute of Technology, Ben-

galuru, India, and his Ph.D. degree in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2017. He was a staff MEMS engineer and a researcher involved in the research and development of high-performance automotive MEMS BAW gyroscopes with the Panasonic Device Solutions Laboratory, Panasonic R&D of North America, Boston, MA, USA. He was a staff engineer at Qualcomm, San Diego, CA, USA, and worked toward commercialization of 5G RF front-end modules with MEMS BAW and SAW filter integration. He currently is a sensor architect at Google, San Francisco, CA 92108 USA. His research interests include capacitive and piezoelectric transducers, optical sensing, MEMS + CMOS systems, and their applications in sensors, actuators, metrology, and compute. He is a recipient of the Cornell Jacob's Fellowship. He serves as a reviewer for major MEMS journals and is frequently part of the technical program committee for the IEEE International Symposium on Inertial Sensors and Systems.

Mehdi Saligane (mehdi@umich.edu) is a research scientist and lecturer at the University of Michigan, Ann Arbor, MI 48109 USA. His research interests include low-power and energy-efficient IC design, biosensors, open source electronics design automation, and analog and mixed-signal IC design automation. He was the recipient of the Google Cloud Research Innovators Award and the Google Research Faculty Award in 2023 and 2021, respectively. He currently serves as chair of the Analog Working Group; as a member of the Technical Steering Committee of the Common Hardware for Interfaces, Processors, and Systems Alliance; and as a technical member of the IEEE Solid-State Circuit Society's (SSCS) open source ecosystem. He is also the cofounder and organizer of the SSCS Code-a-Chip Notebook Competition at the IEEE International Solid-State Circuits Conference and the SSCS Chipathon Design Contest.

