

Grain Media, Inc.

GM8136 BGA196 EVB
(2014/06/04) Rev : 1V0

[illegible]

Release Version	Description
Version: 1V0	

Owing to the GM8136 is a high speed IC with high speed DDR3-SDRAM interface, improper PCB layout will cause the function fail.

From our experience, we found that the GM8136 performance and stability is strongly related to the PCB layout.

In order to ensure your system will work when making your own EVB at the first time, please copy the Power/Ground and DDR layout of our sample design into your system.


If your PCB layout of the Power/Ground and DDR part is not identical to our sample design, we may refuse to support your EVB debugging.

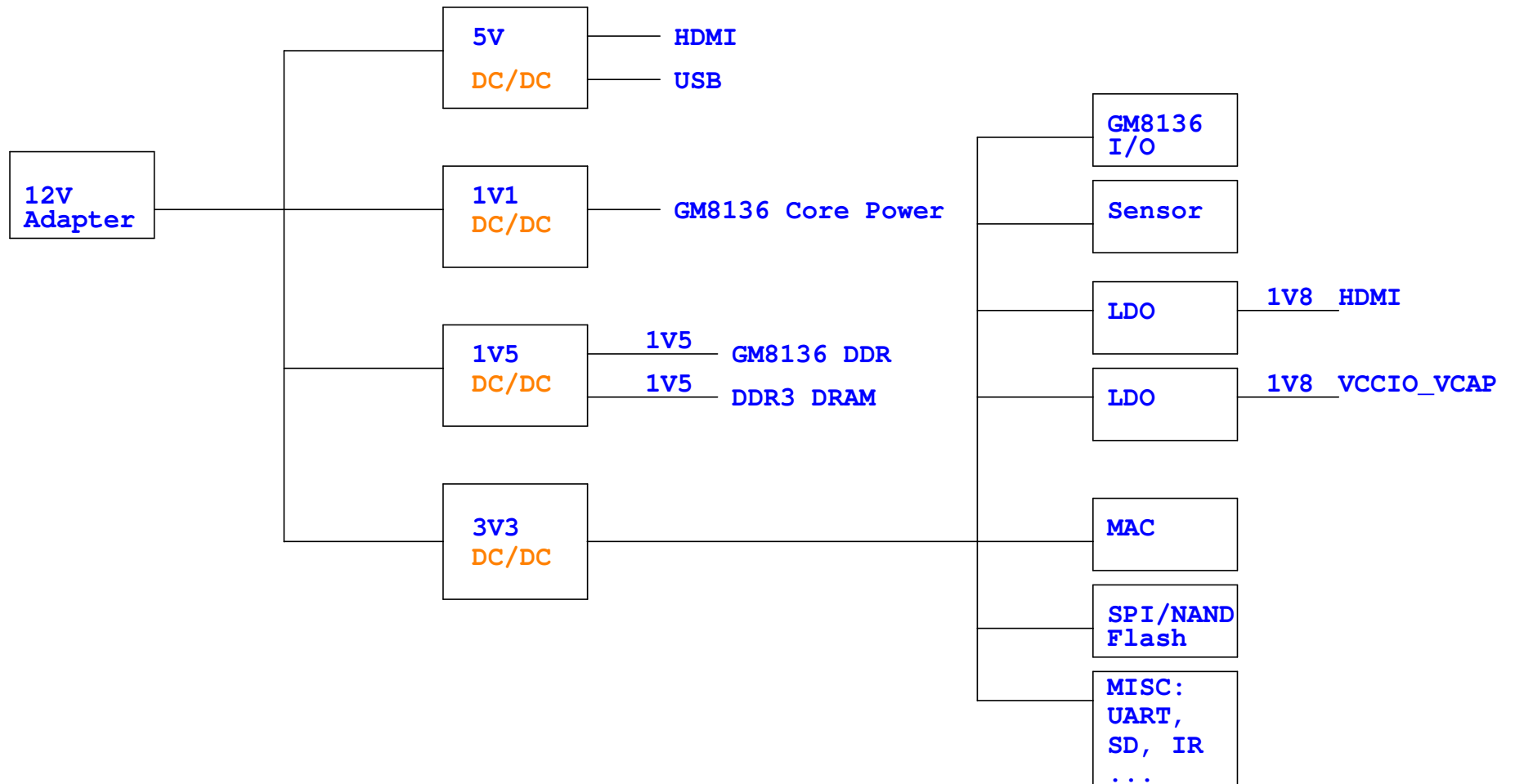


Title: Cover Page				
Size: B	Document Number: GM8136	Department: MTD/SE	Designer: Wayne Ko	Rev: 1/0
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Revision

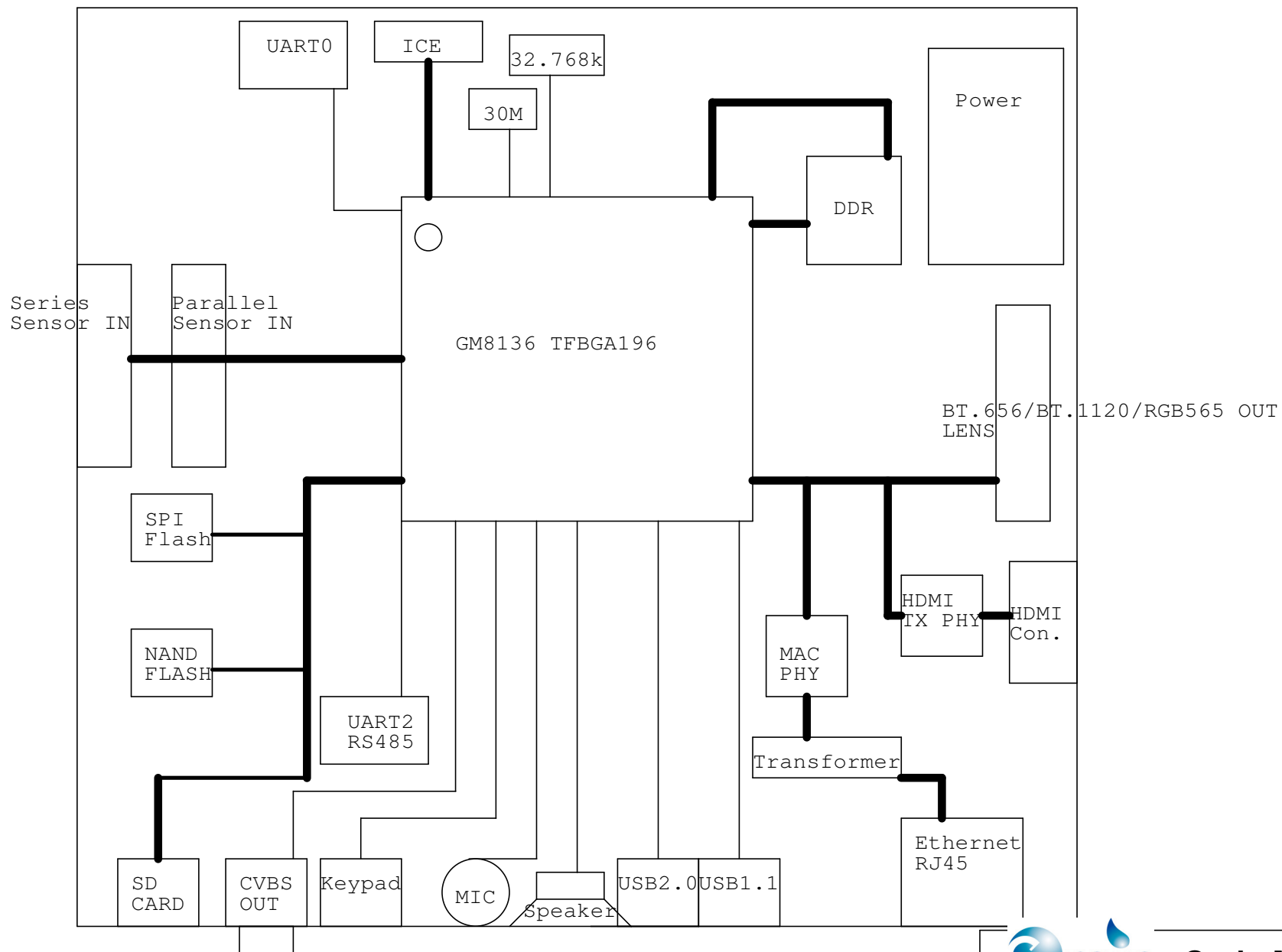
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Title:				
Revision History				
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Grain Media, Inc.

Title: Power Block				
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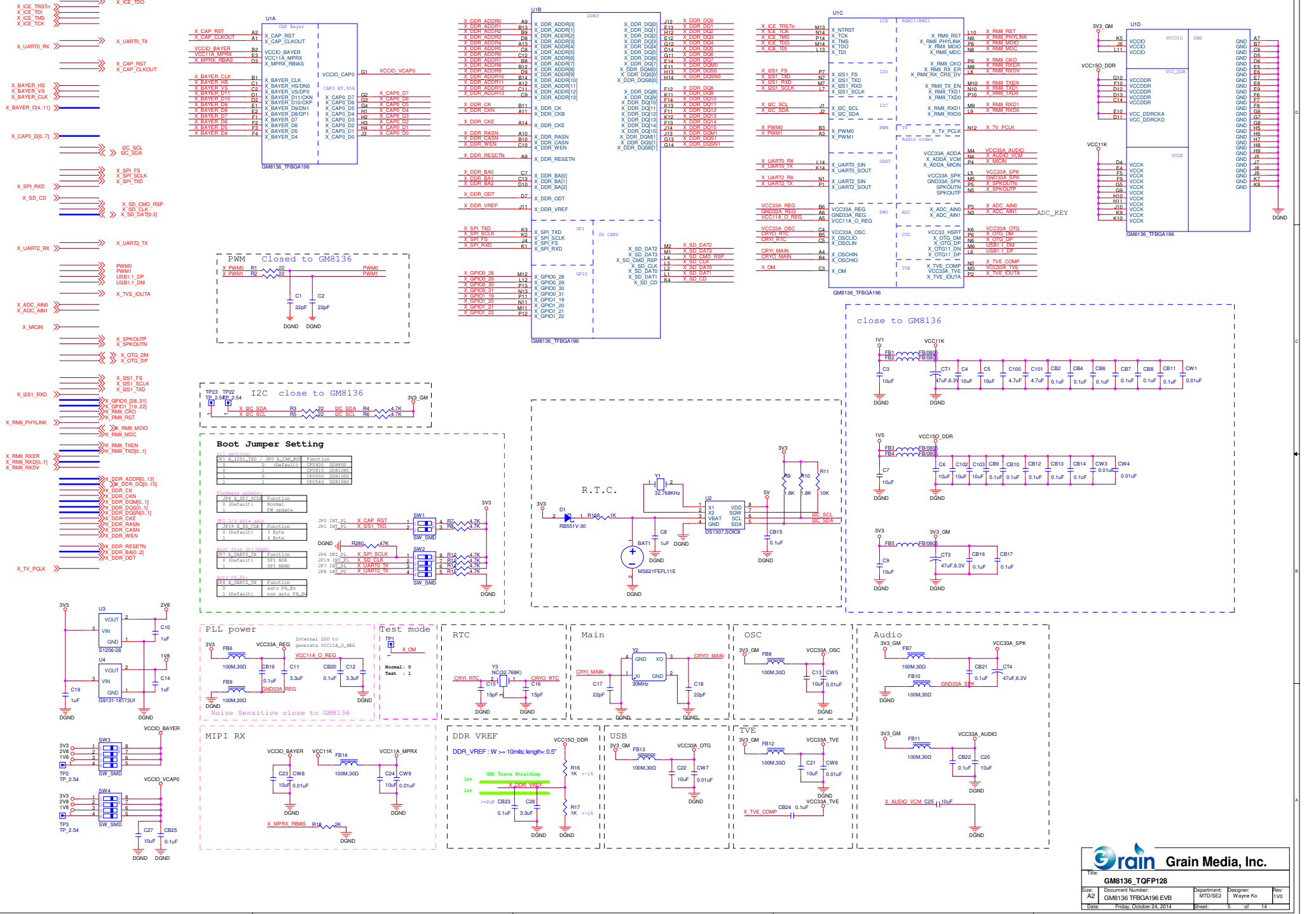


Grain Media, Inc.

Title:

Block Diagram

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X_DDR_ADDR[0..13] >> >>X_DDR_DQ[0..15]

X_DDR_CK
X_DDR_CKIN

X_DDR_DQM[0..1]
X_DDR_DQS[0..1]
X_DDR_DQSIN[0..1]

X_DDR_CKE
X_DDR_RASN
X_DDR_CASN
X_DDR_WEN

X_DDR_RESETN

X_DDR_BA[0..2]

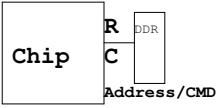
X_DDR_ODT

Place close to the GM8136 chip
or center of signal trace

DDR3
VCC150_DQS: -0.5~1.4V
VCC10A_P15: -0.5~1.4V
VCC150_DDR: -0.5~2.5V
Vref: 0.50*VCC150_DDR
DC Load and
output: 50mA

DDR CLK/DQS Traces
Differential Impedance 90 ohms
Trace Width 4mil
Trace Space 4mil

DDR CLK/DQS Traces
Differential Impedance 90 ohms
Trace Width 4mil
Trace Space 4mil



IVI Remove DQ Rn

X_DDR_DQM1	DDR_DQM1
X_DDR_DQ15	DDR_DQ15
X_DDR_DQ11	DDR_DQ11

X_DDR_DQ7	DDR_DQ7
X_DDR_DQ1	DDR_DQ1
X_DDR_DQ10	DDR_DQ10
X_DDR_DQ14	DDR_DQ14

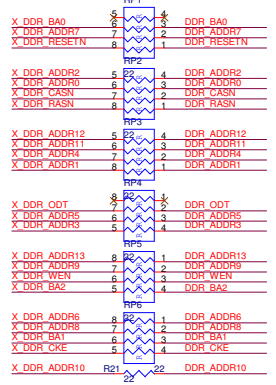
X_DDR_DQ9	DDR_DQ9
X_DDR_DQ13	DDR_DQ13
X_DDR_DQ5	DDR_DQ5

X_DDR_DQ4	DDR_DQ4
X_DDR_DQ6	DDR_DQ6
X_DDR_DQ2	DDR_DQ2
X_DDR_DQ0	DDR_DQ0

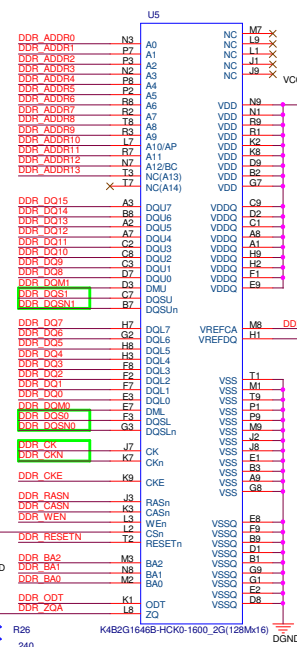
X_DDR_DQSIN1	DDR_DQSIN1
X_DDR_DQS1	DDR_DQS1
X_DDR_DQSIN0	DDR_DQSIN0
X_DDR_DQS0	DDR_DQS0

X_DDR_DQ3	DDR_DQ3
X_DDR_DQM0	DDR_DQM0
X_DDR_DQ8	DDR_DQ8
X_DDR_DQ12	DDR_DQ12

Differential Impedance
85 ohm at Green Line

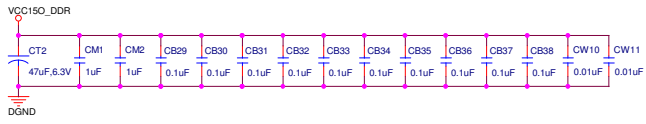


Requirement
Default = 2Gb(x16) * 1
DDR3 Die (256Mbyte)

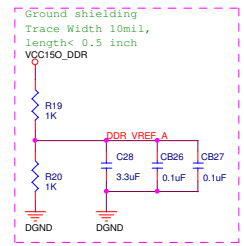


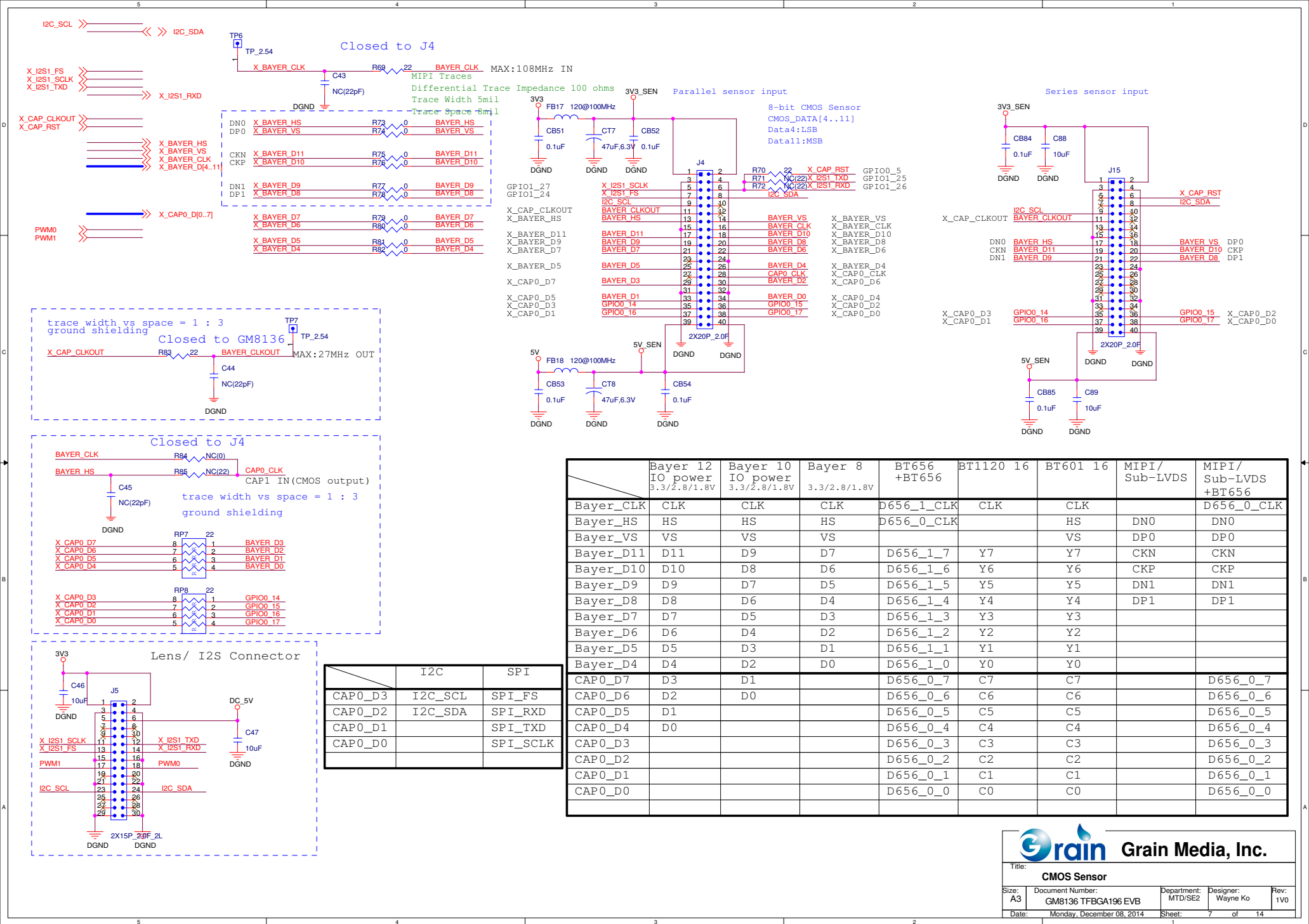
Sametong / K4B2G1646E-BCR0 USD:1.9
Sametong / K4B1G1646G-BCR0 USD:1.1

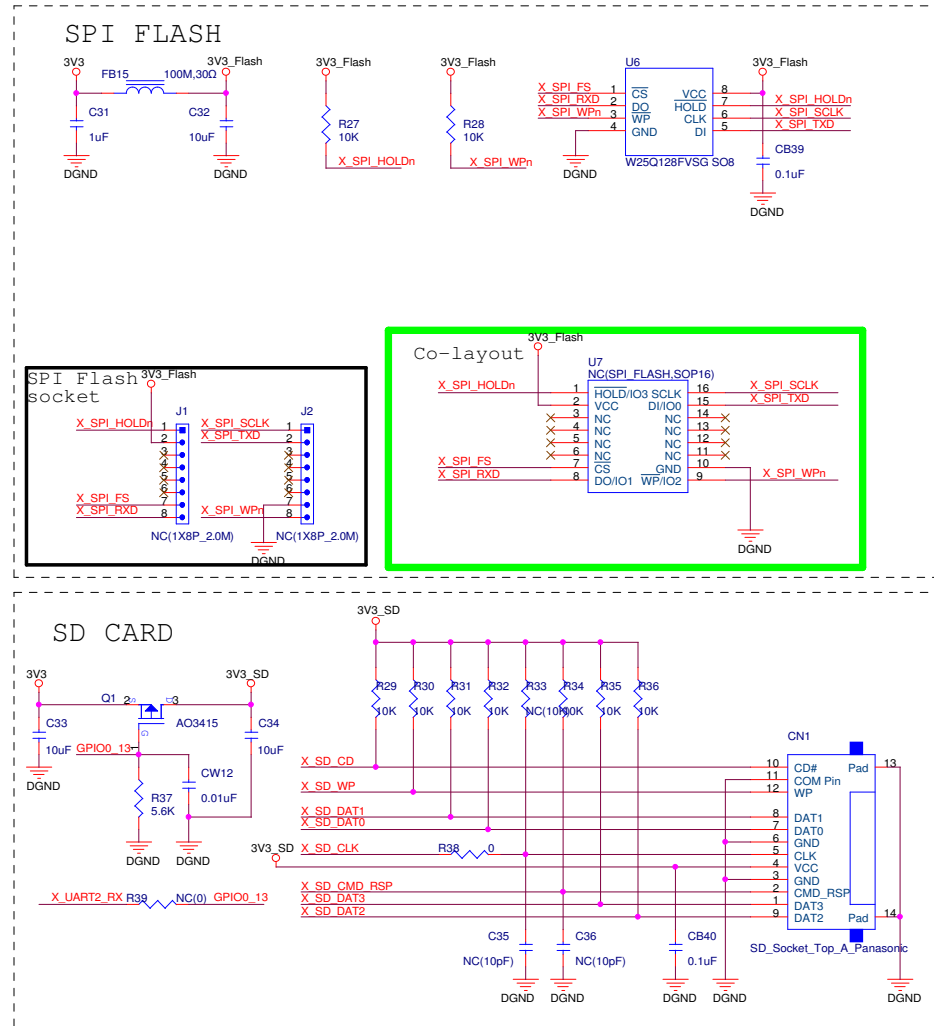
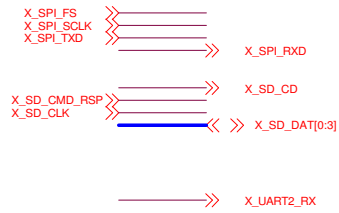
Bypass Cap:Place Near DDRIII Chip



Impedance
DQ: 45- 60 ohm,Target=50ohm
DQ: 45- 60 ohm,Target=50ohm

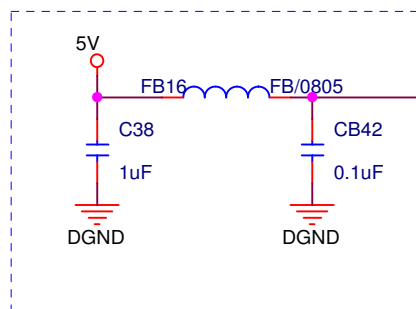






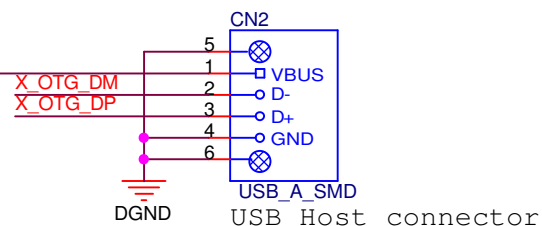
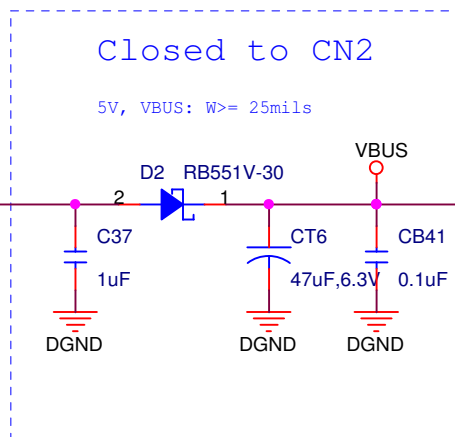
\gg X_OTG_DM
 \gg X_OTG_DP
 USB1.1_DP \gg
 USB1.1_DM \gg

Closed to Source



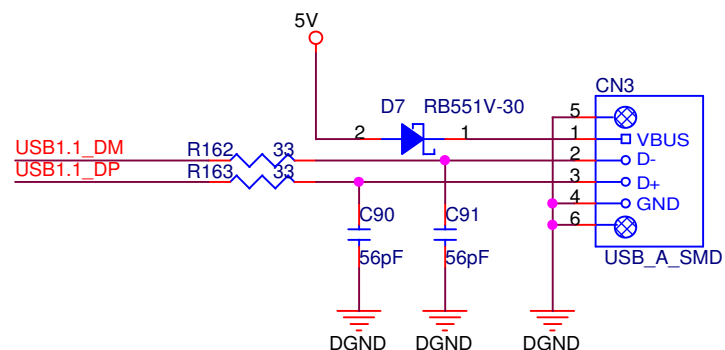
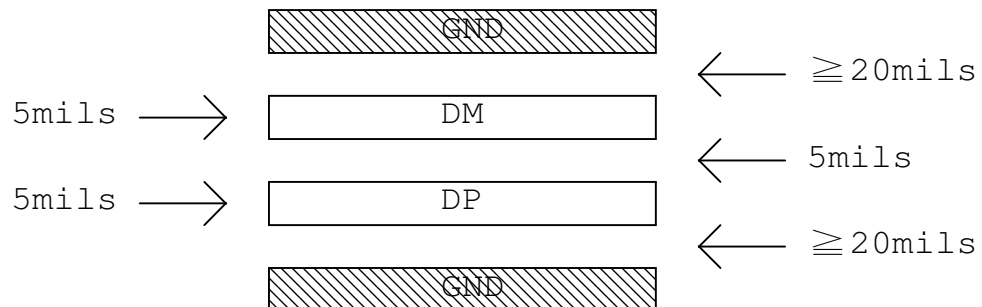
Closed to CN2

5V, VBUS: W>= 25mils



DP, DM

Differential Trace Impedance 90 ohms

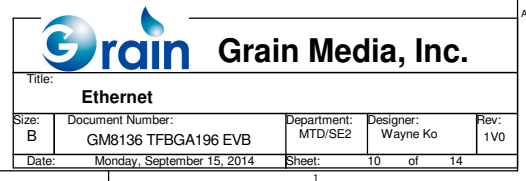


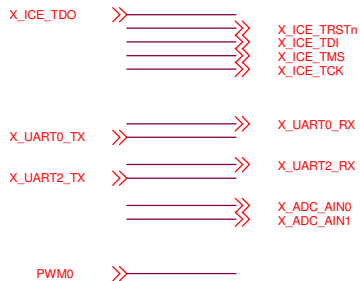
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Title:

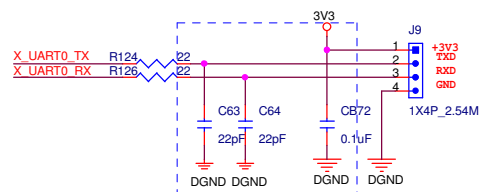
USB HOST

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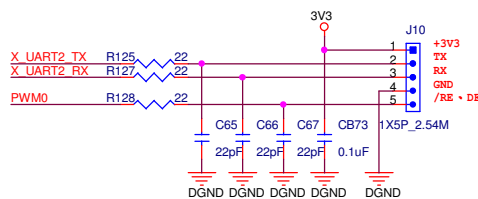


UART 0 (Debug console)



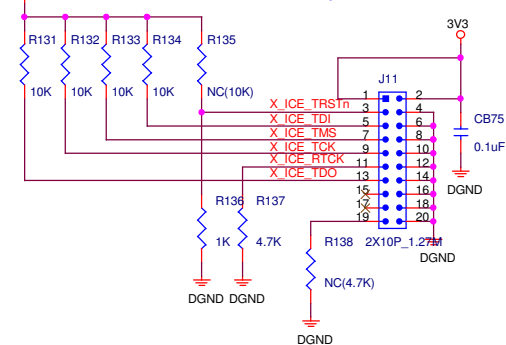
UART 2 or RS485

Closed to J10



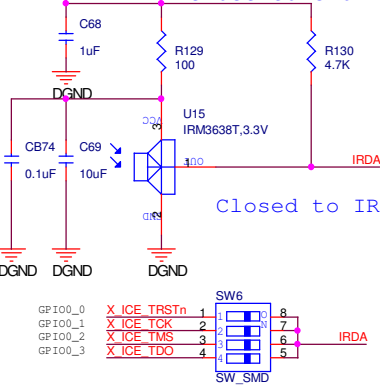
ICE

Closed to J11



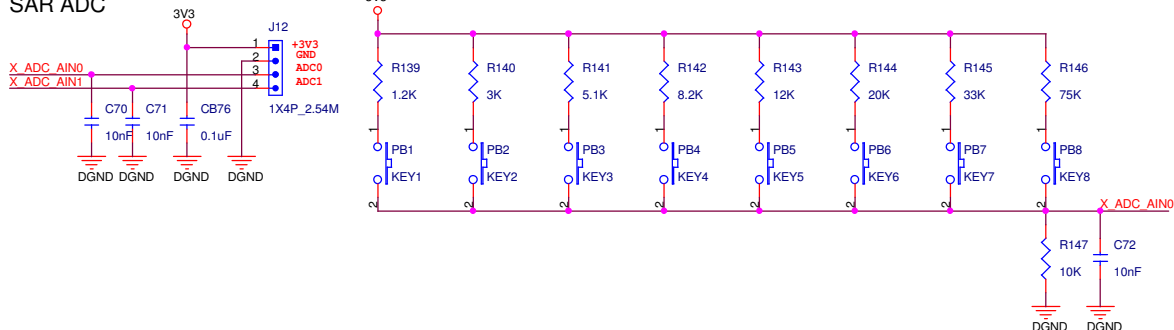
IR

IR Remote control



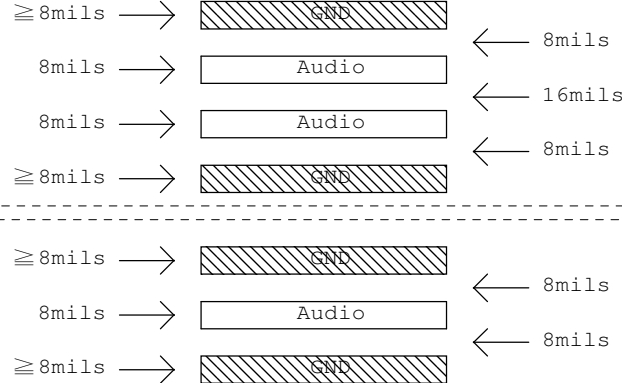
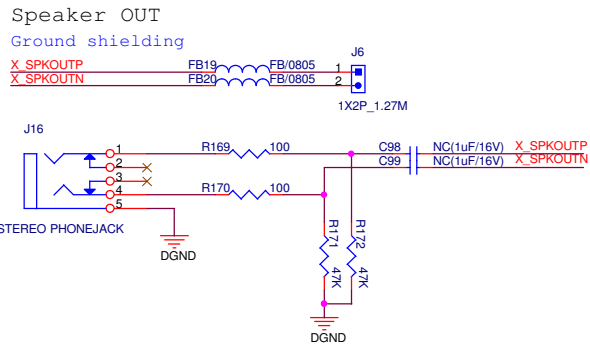
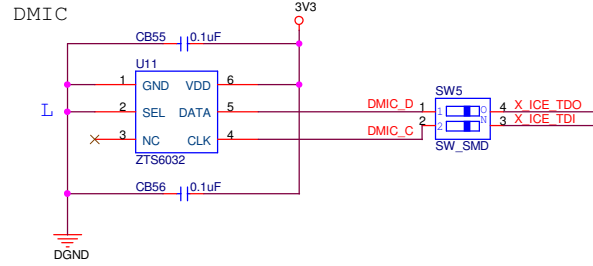
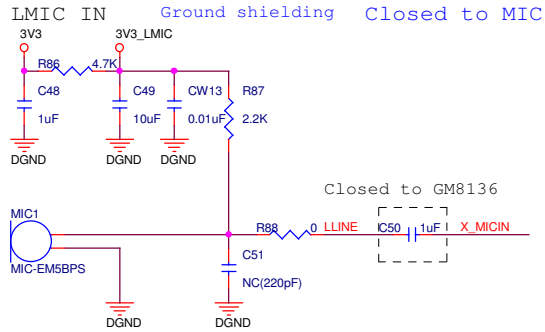
SAR ADC

Closed to J12

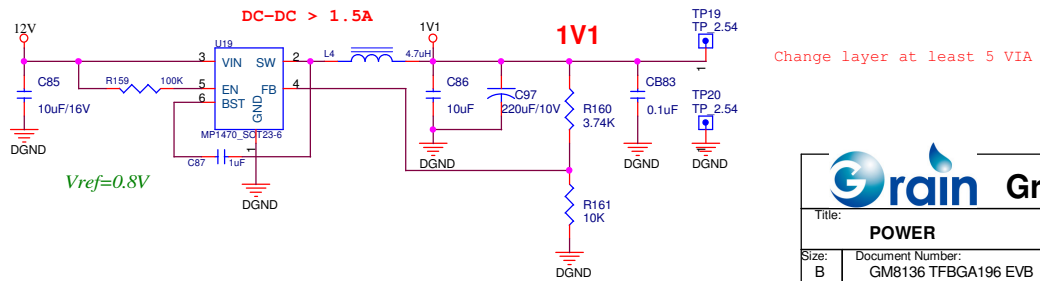
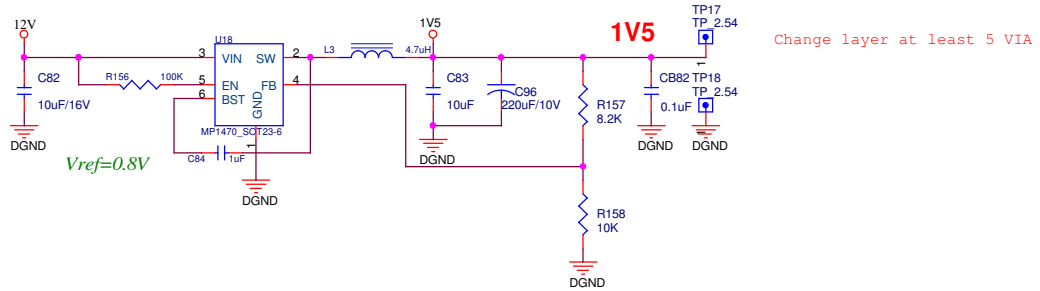
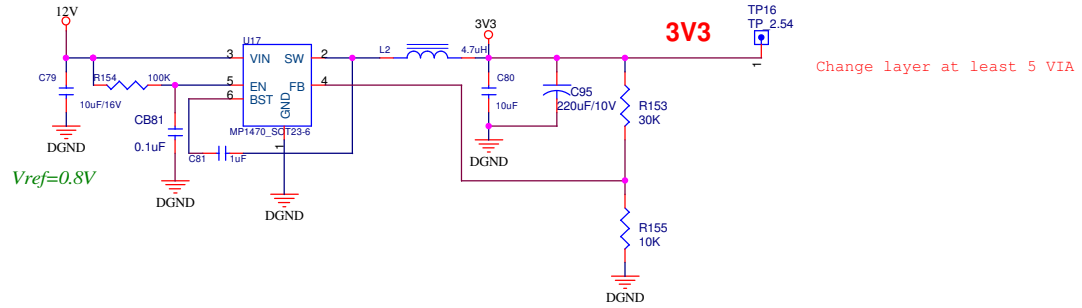
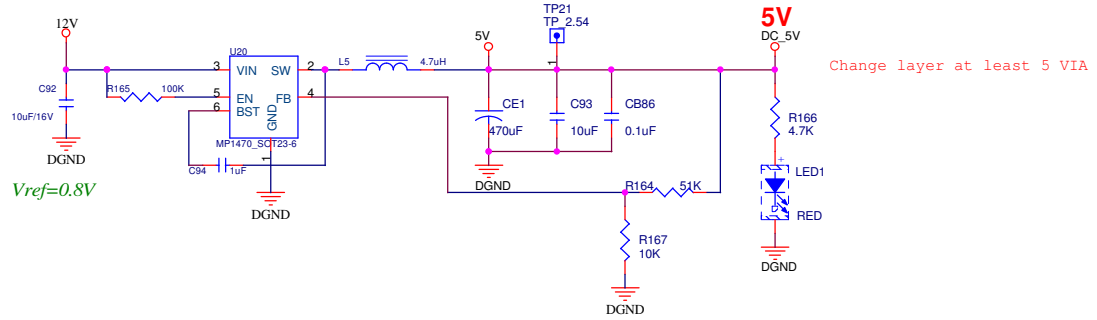
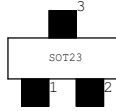
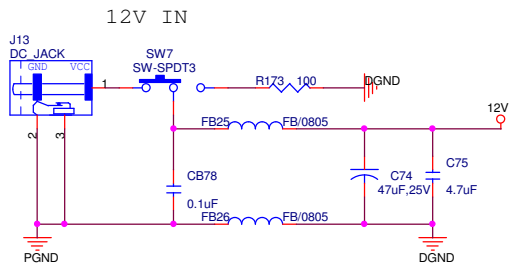


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X_ICE_TDO
X_ICE_TDI
X_MICIN
X_SPKOUTP
X_SPKOUTN



Title: Audio IN/OUT				
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