Pinout Of 8086

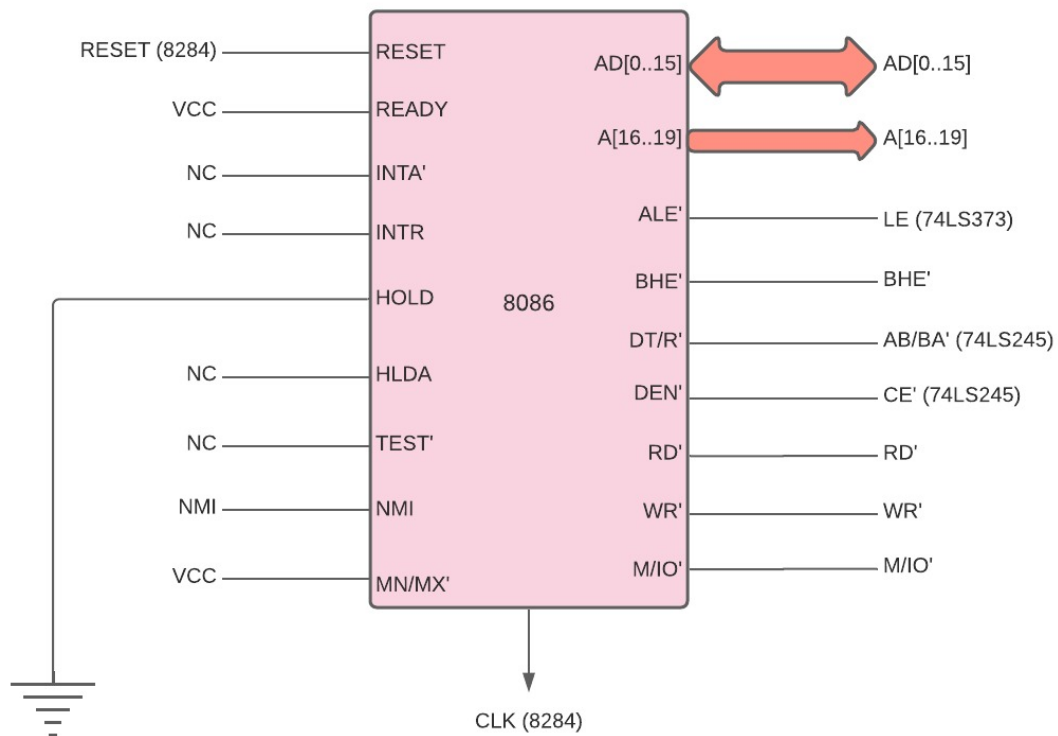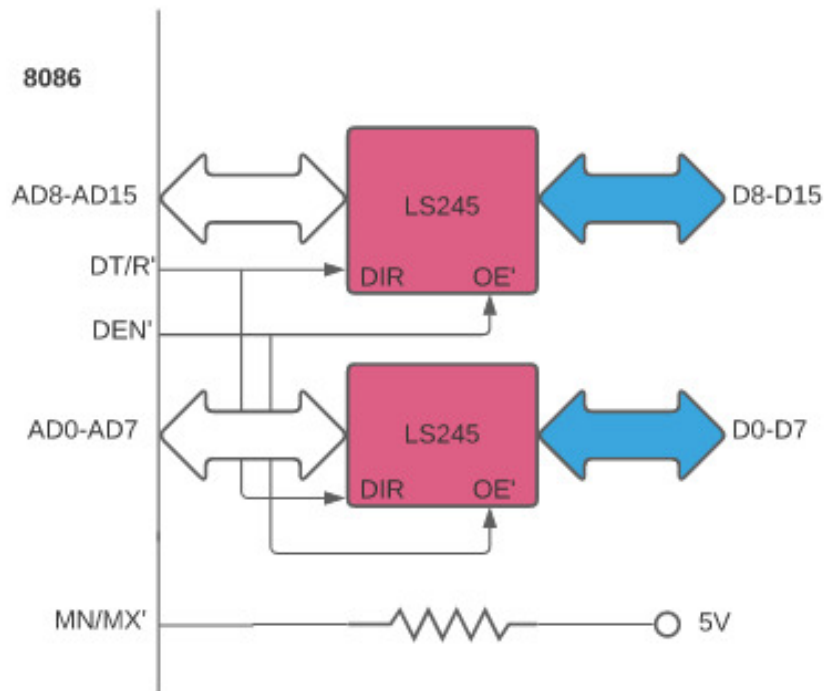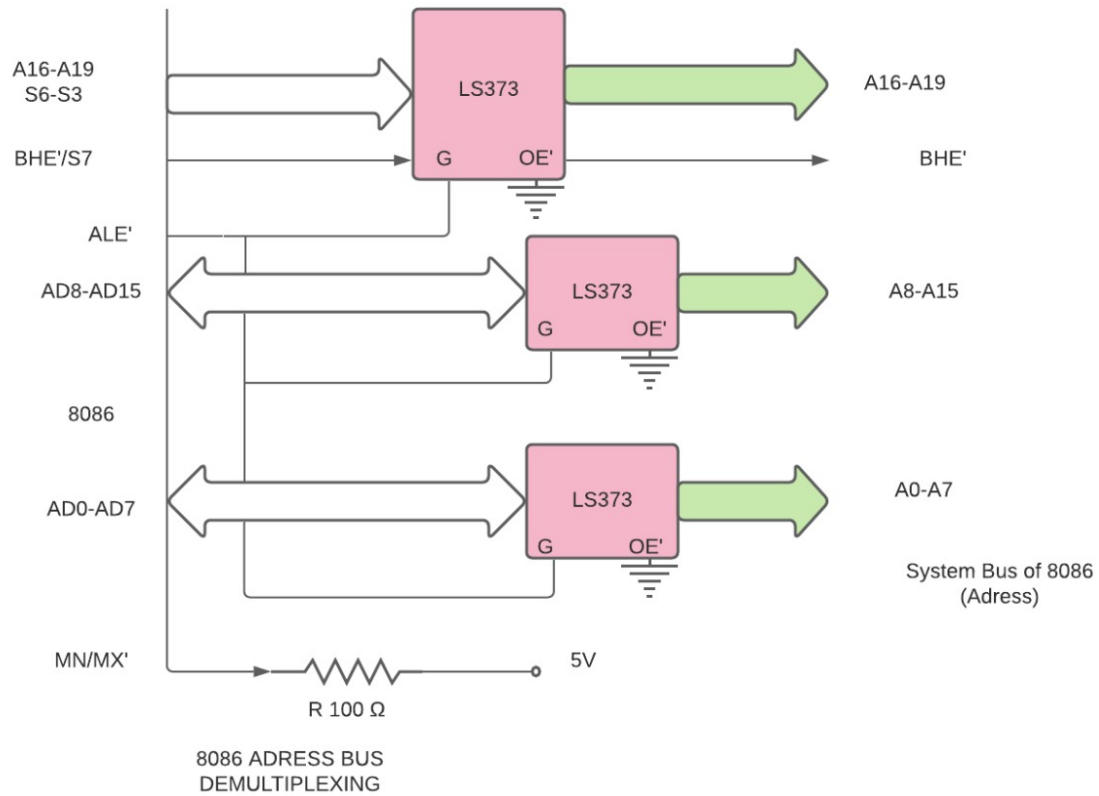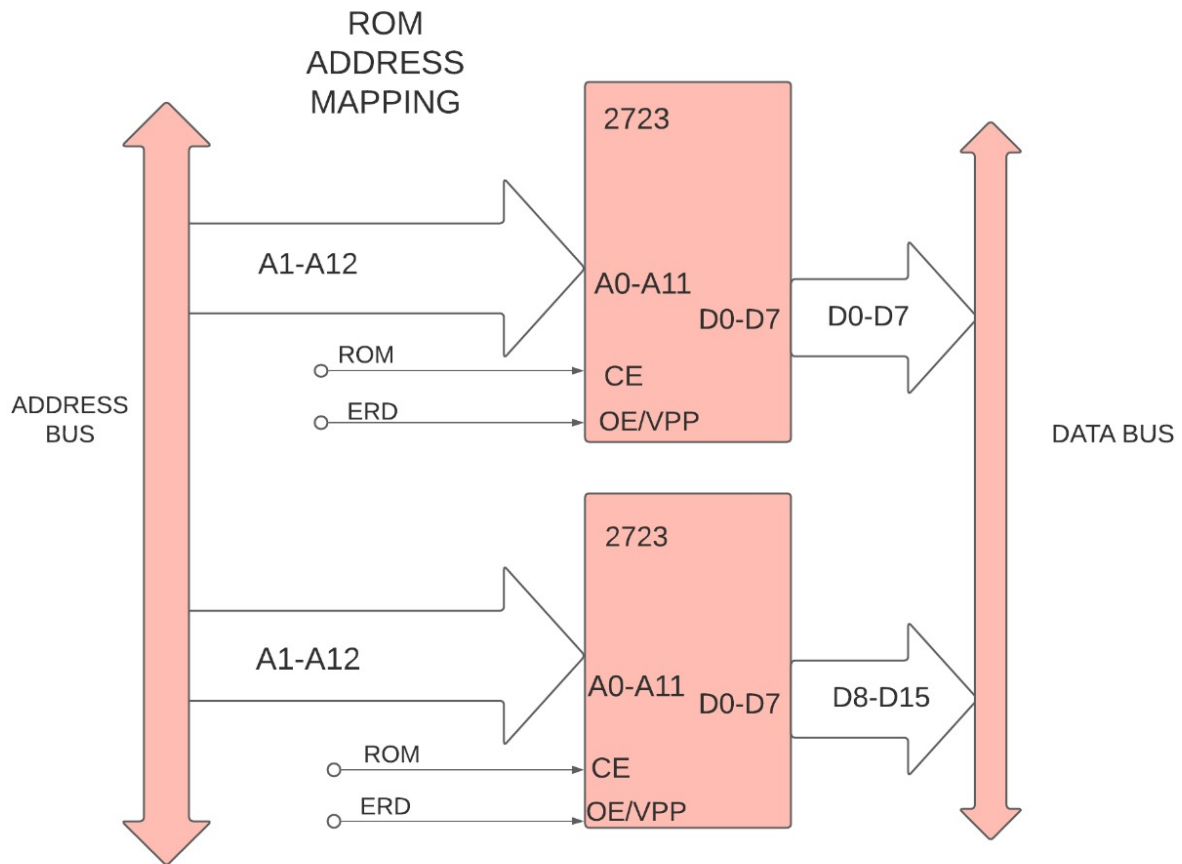|	
RESET (8284) —— RESET	AD[0..15] ⟷ AD[0..15]
VCC —— READY	A[16..19] → A[16..19]
NC —— INTA'	ALE' —— LE (74LS373)
NC —— INTR	BHE' —— BHE'
HOLD	8086 DT/R' —— AB/BA' (74LS245)
NC —— HLDA	DEN' —— CE' (74LS245)
NC —— TEST'	RD' —— RD'
NMI —— NMI	WR' —— WR'
VCC —— MN/MX'	M/IO' —— M/IO'

CLK (8284)

PINOUT OF 8086

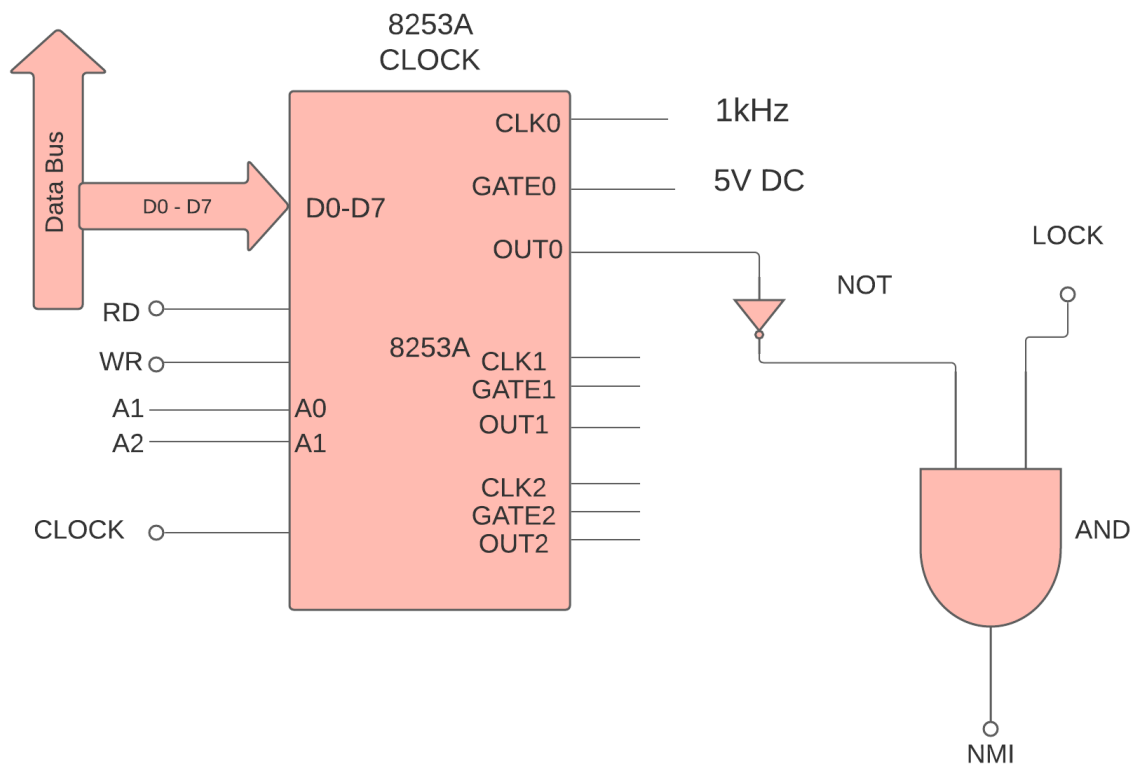# Pinout Of 8086 - Data Bus Latching

8086 Data Bus
Latching

Pinout Of 8086 Address Bus

A16-A19
S6-S3   LS373   A16-A19

BHE'/S7   G   OE'   BHE'

ALE'

AD8-AD15   LS373   A8-A15

                    G   OE'

8086

AD0-AD7   LS373   A0-A7

                    G   OE'

                                    System Bus of 8086
                                    (Adress)

MN/MX'   R 100 Ω   5V

8086 ADRESS BUS
DEMULTIPLEXING

Pinout Of ROM Interfacing

ROM
ADDRESS
MAPPING

2723

A1-A12

A0-A11

D0-D7   D0-D7

ROM

CE

ERD

OE/VPP

ADDRESS
BUS

DATA BUS

2723

A1-A12

A0-A11   D0-D7   D8-D15

ROM

CE

ERD

OE/VPP

Pinout Of 8253A

8253A
CLOCK

Data Bus

D0 - D7 → D0-D7

CLK0 —— 1kHz

GATE0 —— 5V DC

OUT0

RD

WR

A1 —— A0

A2 —— A1

CLOCK

8253A

CLK1
GATE1
OUT1

CLK2
GATE2
OUT2

NOT

LOCK

AND

NMI

Pinout Of 8284

PINOUT OF 8284

X1		
15 MHZ		5V R 100 Ω
		INTR
		NC INTA'
X2	RESET	RESET
	CLK	CLK
RDY1	READY	READY
RDY2		5V
F/C		
	RES	
8284		
		NMI NMI
		HOLD
		GND
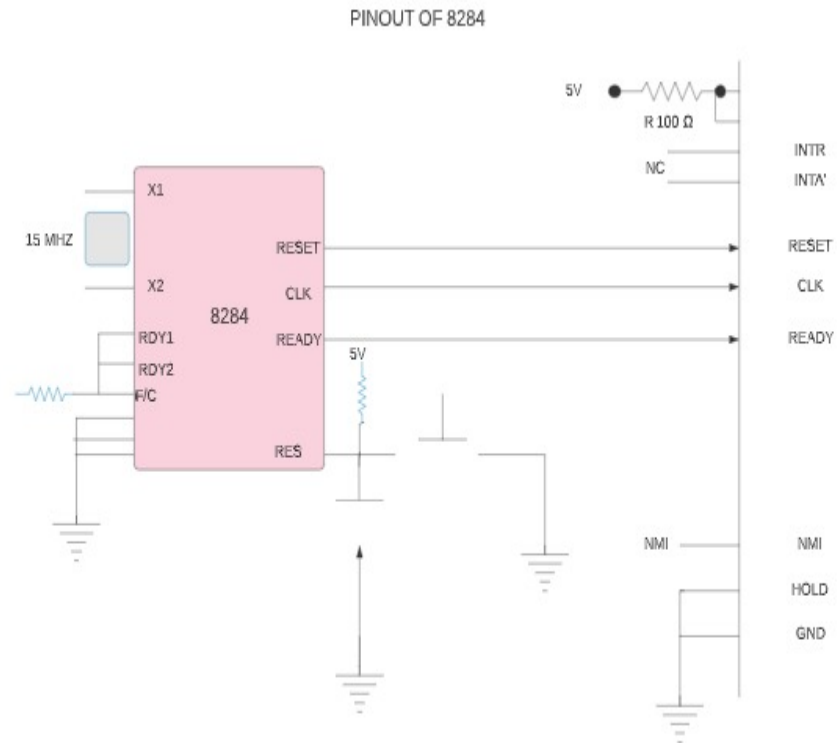
Pinout Of 8255A

PINOUT OF 8255A - 1

D0 - D7(DATA BUS) →	DO-D7	PA0-PA7 ← D0-D7(LCD)

8255A

- RD → RD'
- WR → WR'
- A1 → A0
- A2 → A1
- RESET → RESET
- LCD → CS'

- PB0 — 12/24
- PB1 — ALARM ON/OFF
- PB2-PB7 — (ground)

- PC0 — RS(LCD)
- PC1 — RW(LCD)
- PC2 — E(LCD)

DATA BUS

D0-D7 →	D0-D7	PA0-PA7 ← Q1-Q8

8255A

- RD → RD'
- WR → WR'
- A1 → A0
- A2 → A1
- RESET → RESET
- Y2 → CS'

- PB0 — INC
- PB1 — DEC
- PB2-PB7 — (ground)

- PC0 — BUZZER
- PC1-PC7
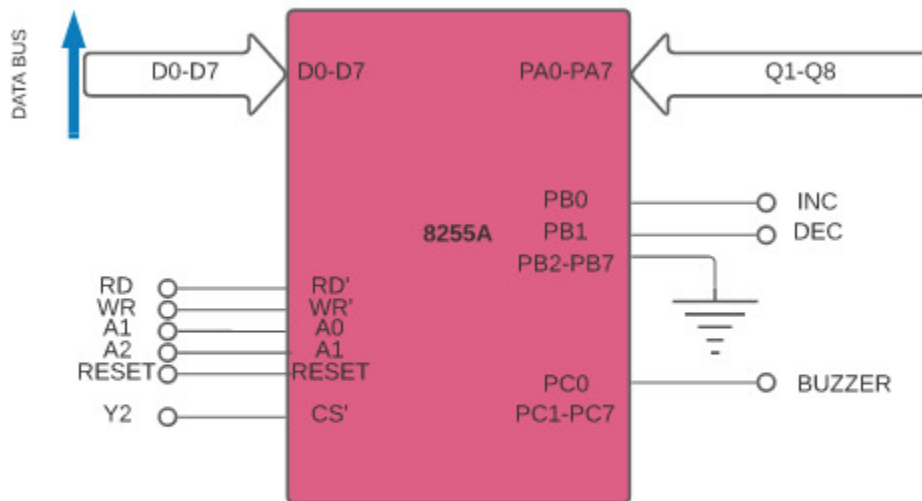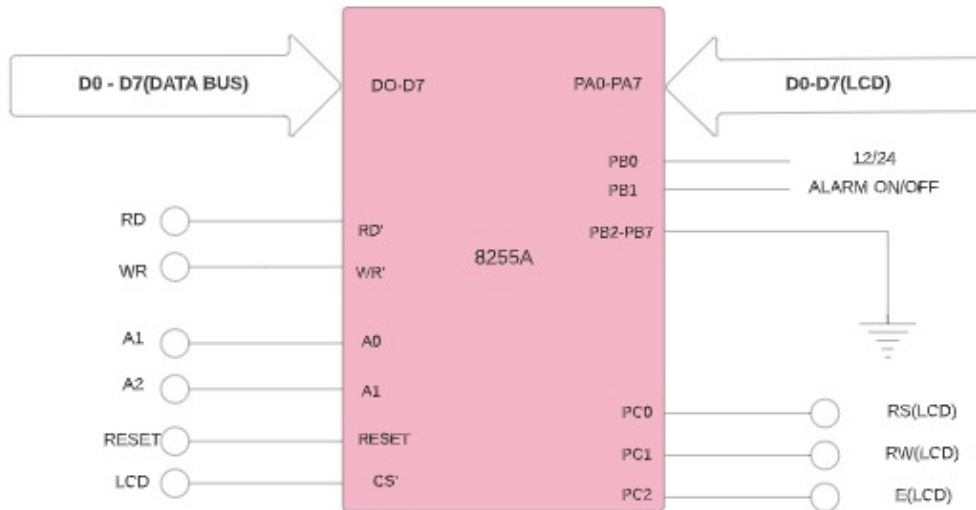
8255A #2

Pinout Of Buzzer Circuit

PC0 (8255A #2) ○———

LED - RED

SOUNDER

○ LOCK

○

ALARM ON/OFF

BUZZER CIRCUIT
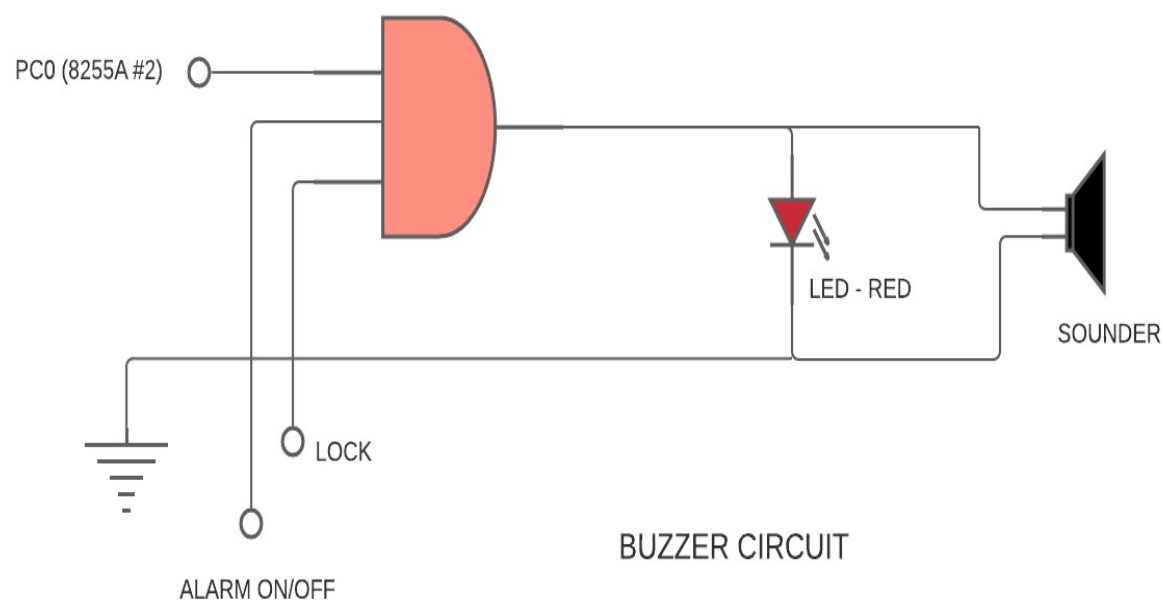
Pinout Of LCD Screen Interfacing

LCD SCREEN
INTERFACING

VCC VDD VEE   RS RW E   D0-D7

R
100
Ω

PC0PC1PC2
(8255A #1)

5V

PA0-PA1 (8255A #1)
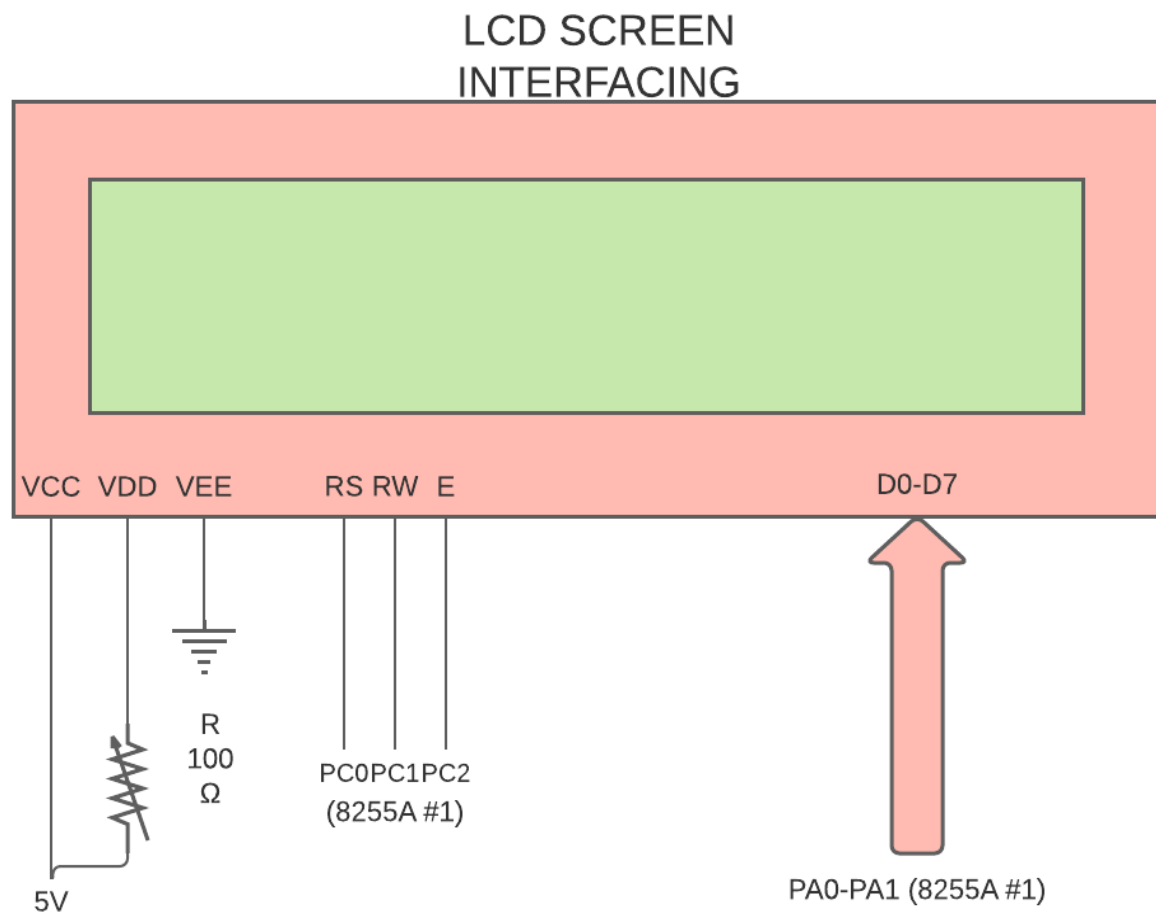
Pinout Of RAM Interfacing

ADDRESS BUS

A1-A11 → 6116

A0	D0
A1	D1
A2	D2
A3	D3
A4	D4
A5	D5
A6	D6
A7	D7
A8	
A9	
A10	

RAM ○— CE'
ERD ○— OE'
EWD ○— WE'

D0-D7 →

A1-A11 → 6116

A0	D0
A1	D1
A2	D2
A3	D3
A4	D4
A5	D5
A6	D6
A7	D7
A8	
A9	
A10	

RAM ○— CE'
ORD ○— OE'
OWD ○— WE'

D8-D15 →

DATA BUS

RAM INTERFACING
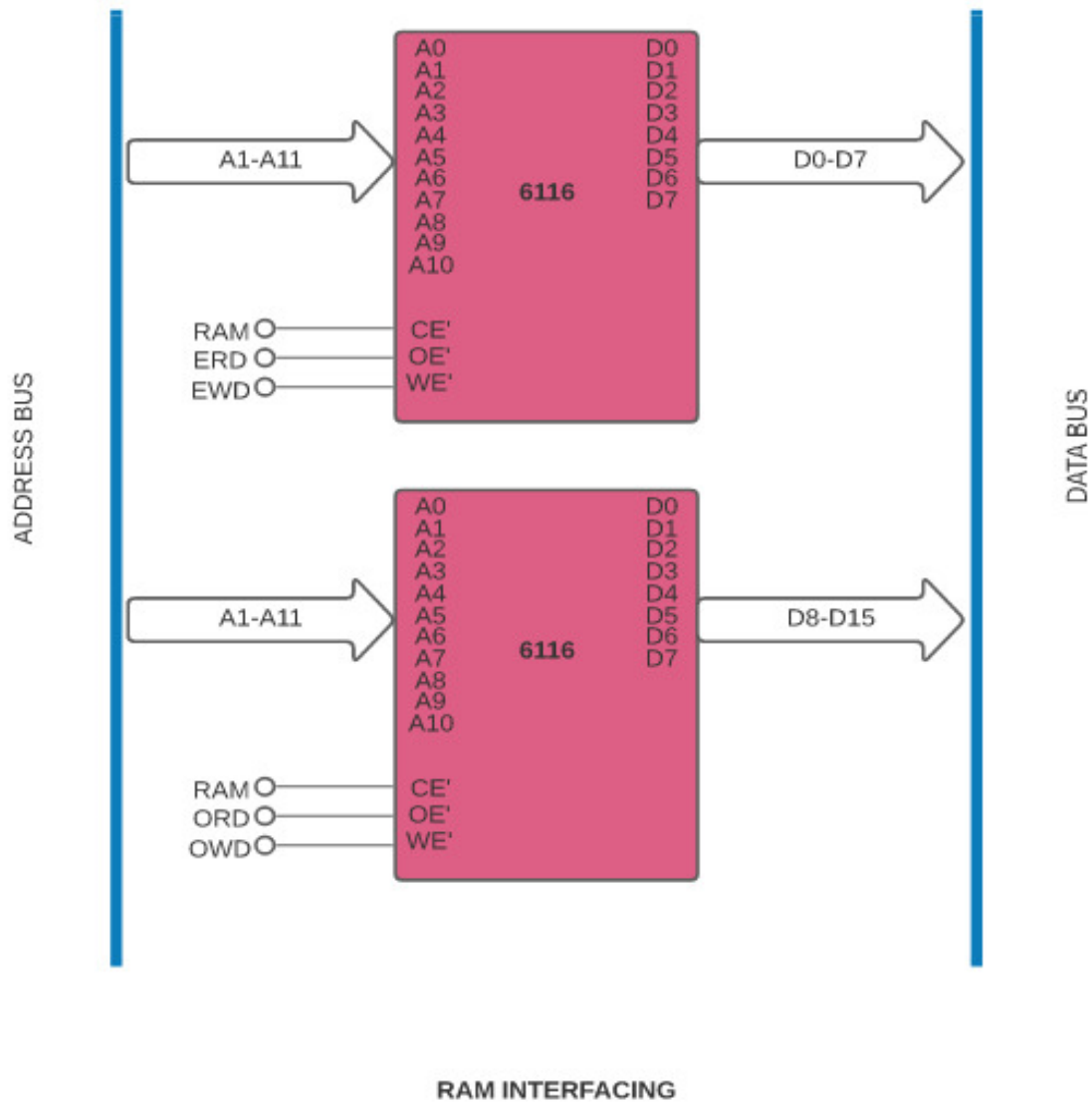
Pinout Of I/O Mapping

IO Mapping
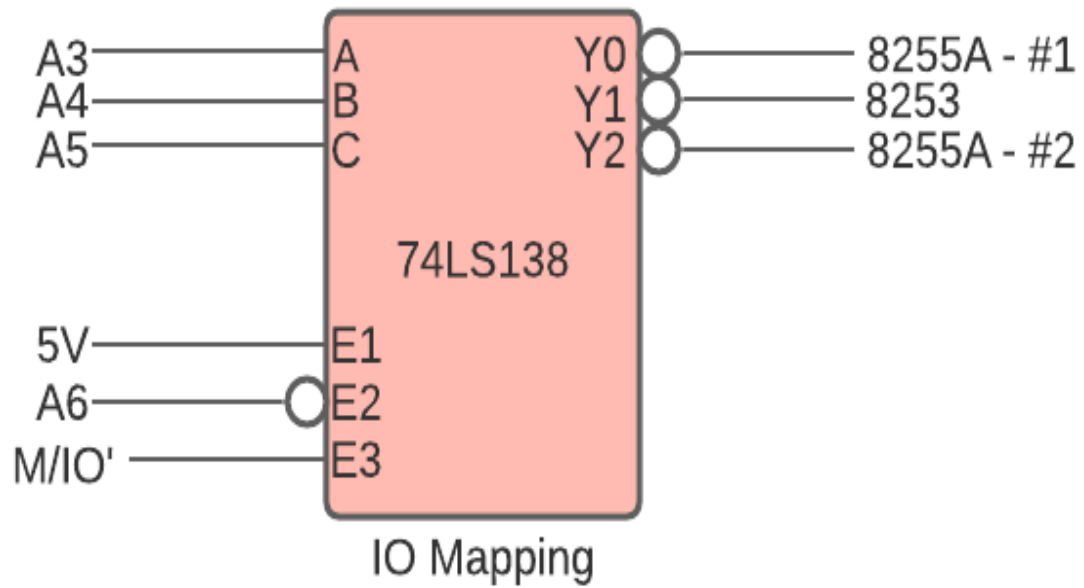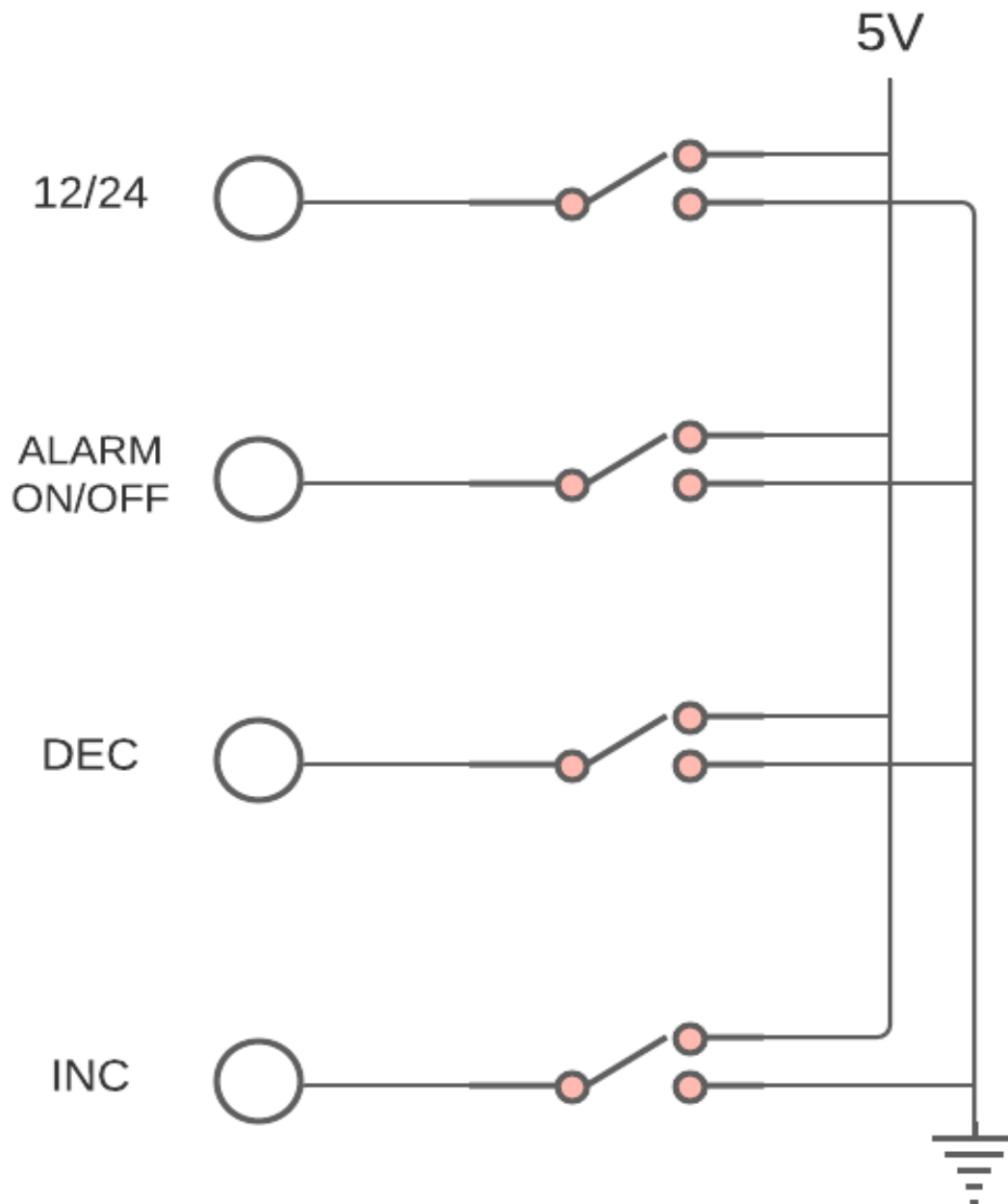
Pinout of RAM / ROM Selection
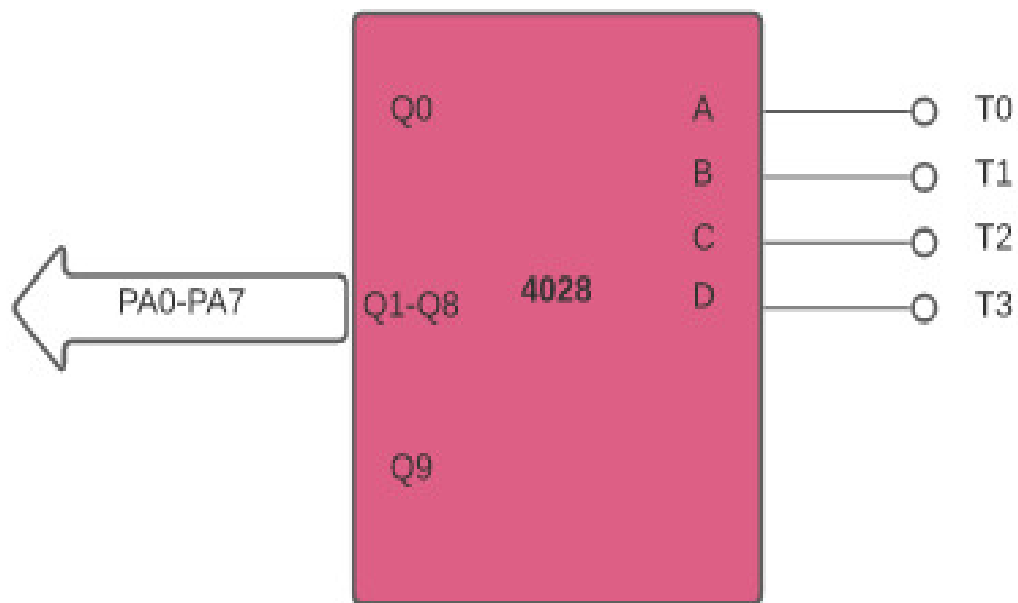

ROM/RAM
SELECTION

RAM/ROM
SELECTION
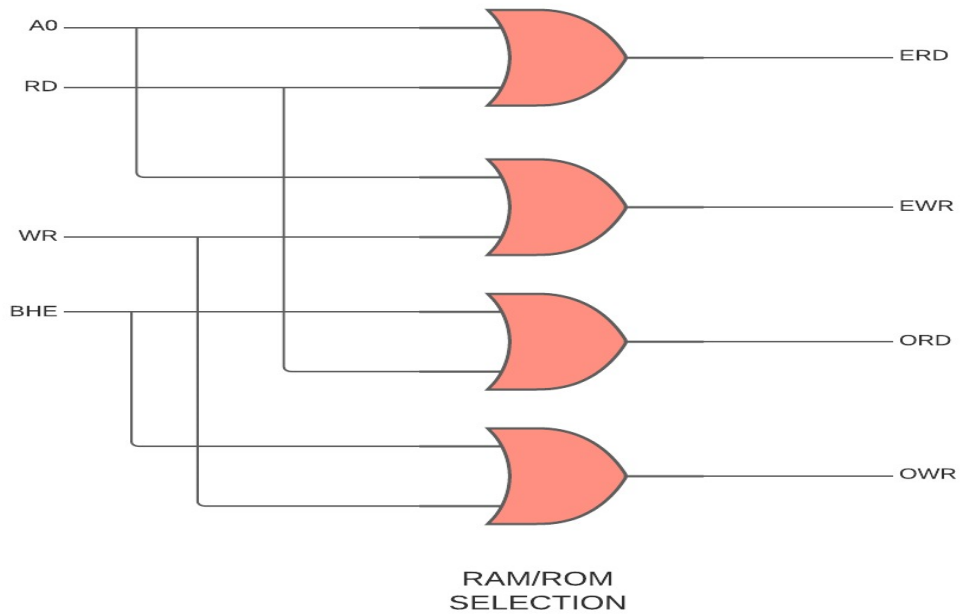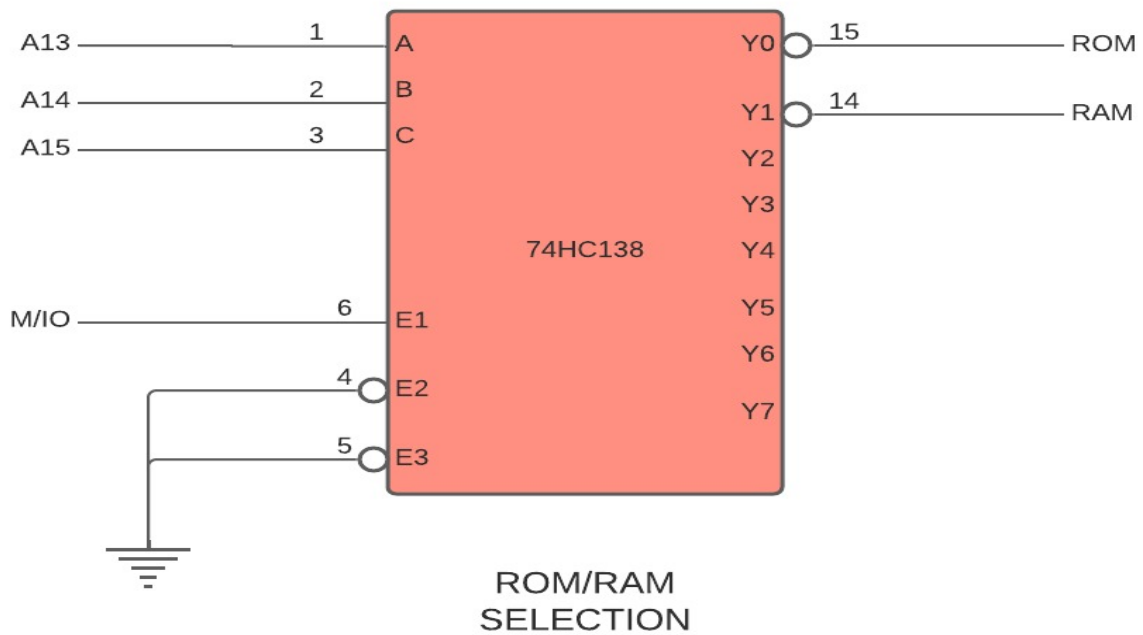
Pinout of Switches

Switches

Pinout of Thumbswitch Decoder

Pinout of Thumbswitch

T0 T1 T2 T3

THUMBSWITCH

LOCK