



8086 16-BIT HMOS MICROPROCESSOR 8086/8086-2/8086-1

- Direct Addressing Capability 1 MByte of Memory
- Architecture Designed for Powerful Assembly Language and Efficient High Level Languages
- 14 Word, by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide
- Range of Clock Rates:
 - 5 MHz for 8086,
 - 8 MHz for 8086-2,
 - 10 MHz for 8086-1
- MULTIBUS System Compatible Interface
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range
- Available in 40-Lead Cerdip and Plastic Package
 - (See Packaging Spec. Order #231369)

The Intel 8086 high performance 16-bit CPU is available in three clock rates: 5, 8 and 10 MHz. The CPU is implemented in N-Channel, depletion load, silicon gate technology (HMOS-III), and packaged in a 40-pin CERDIP or plastic package. The 8086 operates in both single processor and multiple processor configurations to achieve high performance levels.

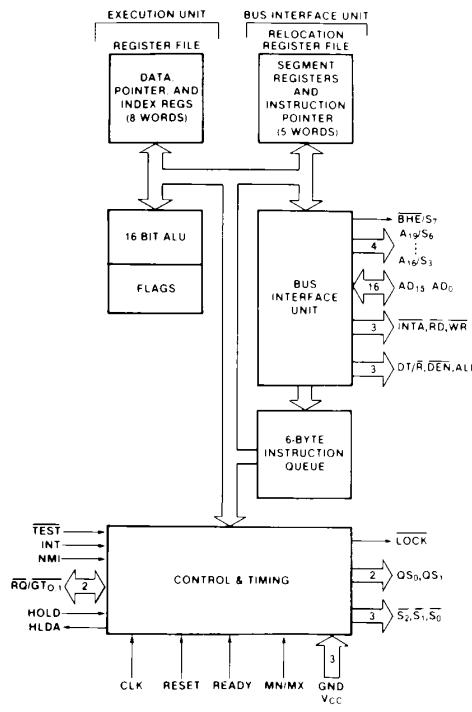
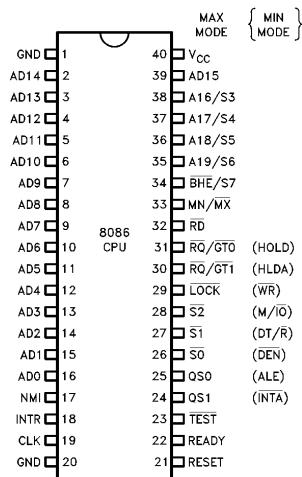


Figure 1. 8086 CPU Block Diagram

231455-1



231455-2

40 Lead
Figure 2. 8086 Pin Configuration

Table 1. Pin Description

The following pin function descriptions are for 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).

| Symbol | Pin No. | Type | Name and Function | | | | | | | | | | | | | | | | | | |
|--|---------------------------------|---------------------------------|---|---------------------------------|---------------------------------|-----------------|---------|---|----------------|---|---|--------------------------------|----------|---|---------------------------------|---|---|------|------------------------------|--|--|
| AD ₁₅ –AD ₀ | 2–16, 39 | I/O | ADDRESS DATA BUS: These lines constitute the time multiplexed memory/I/O address (T ₁), and data (T ₂ , T ₃ , T _W , T ₄) bus. A ₀ is analogous to BHE for the lower byte of the data bus, pins D ₇ –D ₀ . It is LOW during T ₁ when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A ₀ to condition chip select functions. (See BHE.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge". | | | | | | | | | | | | | | | | | | |
| A ₁₉ /S ₆ , A ₁₈ /S ₅ , A ₁₇ /S ₄ , A ₁₆ /S ₃ | 35–38 | O | ADDRESS/STATUS: During T ₁ these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T ₂ , T ₃ , T _W , T ₄ . The status of the interrupt enable FLAG bit (S ₅) is updated at the beginning of each CLK cycle. A ₁₇ /S ₄ and A ₁₆ /S ₃ are encoded as shown. This information indicates which relocation register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge." | | | | | | | | | | | | | | | | | | |
| | | | <table border="1"> <thead> <tr> <th>A₁₇/S₄</th> <th>A₁₆/S₃</th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td>0 (LOW)</td> <td>0</td> <td>Alternate Data</td> </tr> <tr> <td>0</td> <td>1</td> <td>Stack</td> </tr> <tr> <td>1 (HIGH)</td> <td>0</td> <td>Code or None</td> </tr> <tr> <td>1</td> <td>1</td> <td>Data</td> </tr> <tr> <td>S₆ is 0 (LOW)</td> <td></td> <td></td> </tr> </tbody> </table> | A ₁₇ /S ₄ | A ₁₆ /S ₃ | Characteristics | 0 (LOW) | 0 | Alternate Data | 0 | 1 | Stack | 1 (HIGH) | 0 | Code or None | 1 | 1 | Data | S ₆ is 0 (LOW) | | |
| A ₁₇ /S ₄ | A ₁₆ /S ₃ | Characteristics | | | | | | | | | | | | | | | | | | | |
| 0 (LOW) | 0 | Alternate Data | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Stack | | | | | | | | | | | | | | | | | | | |
| 1 (HIGH) | 0 | Code or None | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Data | | | | | | | | | | | | | | | | | | | |
| S ₆ is 0 (LOW) | | | | | | | | | | | | | | | | | | | | | |
| BHE/S ₇ | 34 | O | BUS HIGH ENABLE/STATUS: During T ₁ the bus high enable signal (BHE) should be used to enable data onto the most significant half of the data bus, pins D ₁₅ –D ₈ . Eight-bit oriented devices tied to the upper half of the bus would normally use BHE to condition chip select functions. BHE is LOW during T ₁ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S ₇ status information is available during T ₂ , T ₃ , and T ₄ . The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during T ₁ for the first interrupt acknowledge cycle. | | | | | | | | | | | | | | | | | | |
| | | | <table border="1"> <thead> <tr> <th>BHE</th> <th>A₀</th> <th>Characteristics</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Whole word</td> </tr> <tr> <td>0</td> <td>1</td> <td>Upper byte from/to odd address</td> </tr> <tr> <td>1</td> <td>0</td> <td>Lower byte from/to even address</td> </tr> <tr> <td>1</td> <td>1</td> <td>None</td> </tr> </tbody> </table> | BHE | A ₀ | Characteristics | 0 | 0 | Whole word | 0 | 1 | Upper byte from/to odd address | 1 | 0 | Lower byte from/to even address | 1 | 1 | None | | | |
| BHE | A ₀ | Characteristics | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Whole word | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Upper byte from/to odd address | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Lower byte from/to even address | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | None | | | | | | | | | | | | | | | | | | | |
| RD | 32 | O | READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S ₂ pin. This signal is used to read devices which reside on the 8086 local bus. RD is active LOW during T ₂ , T ₃ and T _W of any read cycle, and is guaranteed to remain HIGH in T ₂ until the 8086 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge". | | | | | | | | | | | | | | | | | | |

Table 1. Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function |
|-----------------|---------|------|---|
| READY | 22 | I | READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/I/O is synchronized by the 8284A Clock Generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met. |
| INTR | 18 | I | INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH. |
| TEST | 23 | I | TEST: input is examined by the "Wait" instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK. |
| NMI | 17 | I | NON-MASKABLE INTERRUPT: an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized. |
| RESET | 21 | I | RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized. |
| CLK | 19 | I | CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. |
| V _{CC} | 40 | | V_{CC}: +5V power supply pin. |
| GND | 1, 20 | | GROUND |
| MN/MX | 33 | I | MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections. |

The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., MN/MX = V_{SS}). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

| | | | |
|--|-------|---|---|
| $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ | 26–28 | O | STATUS: active during T ₄ , T ₁ , and T ₂ and is returned to the passive state (1, 1, 1) during T ₃ or during T _W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T ₄ is used to indicate the beginning of a bus cycle, and the return to the passive state in T ₃ or T _W is used to indicate the end of a bus cycle. |
|--|-------|---|---|

Table 1. Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function | | | |
|---|----------------|-------------|--|------------------------------------|------------------------------------|------------------------|
| $\overline{S_2}, \overline{S_1}, \overline{S_0}$ (Continued) | 26–28 | O | These signals float to 3-state OFF in “hold acknowledge”. These status lines are encoded as shown. | | | |
| | | | $\overline{S_2}$ | $\overline{S_1}$ | $\overline{S_0}$ | Characteristics |
| | | | 0 (LOW) | 0 | 0 | Interrupt Acknowledge |
| | | | 0 | 0 | 1 | Read I/O Port |
| | | | 0 | 1 | 0 | Write I/O Port |
| | | | 0 | 1 | 1 | Halt |
| | | | 1 (HIGH) | 0 | 0 | Code Access |
| | | | 1 | 0 | 1 | Read Memory |
| | | | 1 | 1 | 0 | Write Memory |
| | | | 1 | 1 | 1 | Passive |
| $\overline{RQ}/\overline{GT}_0,$ $\overline{RQ}/\overline{GT}_1$ | 30, 31 | I/O | <p>REQUEST/GANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT}_0$ having higher priority than $\overline{RQ}/\overline{GT}_1$. $\overline{RQ}/\overline{GT}$ pins have internal pull-up resistors and may be left unconnected. The request/grant sequence is as follows (see Page 2-24):</p> <ol style="list-style-type: none"> 1. A pulse 1 CLK wide from another local bus master indicates a local bus request (“hold”) to the 8086 (pulse 1). 2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the “hold acknowledge” state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during “hold acknowledge”. 3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the “hold” request is about to end and that the 8086 can reclaim the local bus at the next CLK. <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. <p>If the local bus is idle when the request is made the two possible events will follow:</p> <ol style="list-style-type: none"> 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied. | | | |
| LOCK | 29 | O | <p>LOCK: output indicates that other system bus masters are not to gain control of the system bus while \overline{LOCK} is active LOW. The \overline{LOCK} signal is activated by the “LOCK” prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in “hold acknowledge”.</p> | | | |

Table 1. Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function | | |
|-----------------------------------|----------------|-------------|---|-----------------------|----------------------------------|
| QS ₁ , QS ₀ | 24, 25 | O | QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS ₁ and QS ₀ provide status to allow external tracking of the internal 8086 instruction queue. | | |
| | | | QS₁ | QS₀ | Characteristics |
| | | | 0 (LOW) | 0 | No Operation |
| | | | 0 | 1 | First Byte of Op Code from Queue |
| | | | 1 (HIGH) | 0 | Empty the Queue |
| | | | 1 | 1 | Subsequent Byte from Queue |

The following pin function descriptions are for the 8086 in minimum mode (i.e., MN/MX = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

| | | | |
|------------------|--------|-----|---|
| M/I ^O | 28 | O | STATUS LINE: logically equivalent to S ₂ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/I ^O becomes valid in the T ₄ preceding a bus cycle and remains valid until the final T ₄ of the cycle (M = HIGH, IO = LOW). M/I ^O floats to 3-state OFF in local bus "hold acknowledge". |
| WR | 29 | O | WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/I ^O signal. WR is active for T ₂ , T ₃ and T _W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge". |
| INTA | 24 | O | INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T ₂ , T ₃ and T _W of each interrupt acknowledge cycle. |
| ALE | 25 | O | ADDRESS LATCH ENABLE: provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T ₁ of any bus cycle. Note that ALE is never floated. |
| DT/R | 27 | O | DATA TRANSMIT/RECEIVE: needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/R is equivalent to S ₁ in the maximum mode, and its timing is the same as for M/I ^O . (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge". |
| DEN | 26 | O | DATA ENABLE: provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. DEN is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T ₂ until the middle of T ₄ , while for a write cycle it is active from the beginning of T ₂ until the middle of T ₄ . DEN floats to 3-state OFF in local bus "hold acknowledge". |
| HOLD, HLDA | 31, 30 | I/O | HOLD: indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T ₄ or T _i clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWER the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold acknowledge (HLDA) and HOLD have internal pull-up resistors. The same rules as for RQ/GT apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. |

FUNCTIONAL DESCRIPTION

General Operation

The internal functions of the 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operands and addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million

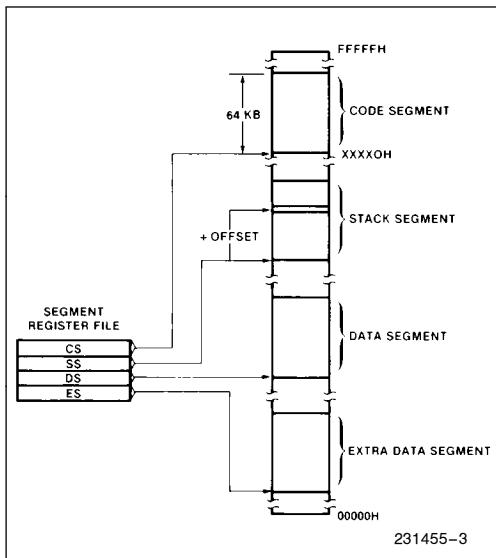
bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank ($D_{15}-D_8$) and a low bank (D_7-D_0) of 512K 8-bit bytes addressed in parallel by the processor's address lines $A_{19}-A_1$. Byte data with even addresses is transferred on the D_7-D_0 bus lines while odd addressed byte data (A_0 HIGH) is transferred on the $D_{15}-D_8$ bus lines. The processor provides two enable signals, \bar{BHE} and A_0 , to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

| Memory Reference Need | Segment Register Used | Segment Selection Rule |
|------------------------|-----------------------|---|
| Instructions | CODE (CS) | Automatic with all instruction prefetch. |
| Stack | STACK (SS) | All stack pushes and pops. Memory references relative to BP base register except data references. |
| Local Data | DATA (DS) | Data references when: relative to stack, destination of string operation, or explicitly overridden. |
| External (Global) Data | EXTRA (ES) | Destination of string operations: explicitly selected using a segment override. |

**Figure 3a. Memory Organization**

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

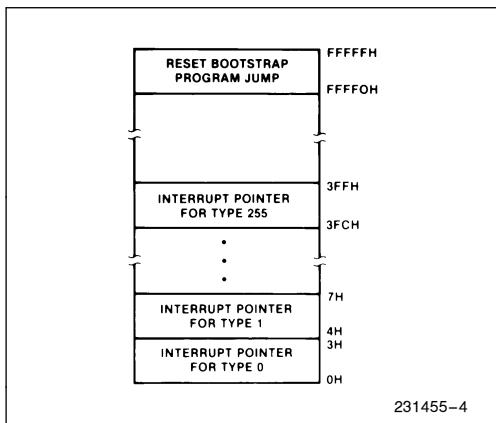
MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a strap pin (MN/MX) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/MX pin is strapped to GND, the 8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into $\overline{S_0}$, $\overline{S_2}$, $\overline{S_2}$ to generate bus timing and control signals compatible with the MULTIBUS architecture. When the MN/MX pin is strapped to V_{CC}, the 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

BUS OPERATION

The 8086 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T₁, T₂, T₃ and T₄ (see Figure 5). The address is emitted from the processor during T₁ and data transfer occurs on the bus during T₃ and T₄. T₂ is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_W) are inserted between T₃ and T₄. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods

**Figure 3b. Reserved Memory Locations**

Certain locations in memory are reserved for specific CPU operations (see Figure 3b). Locations from

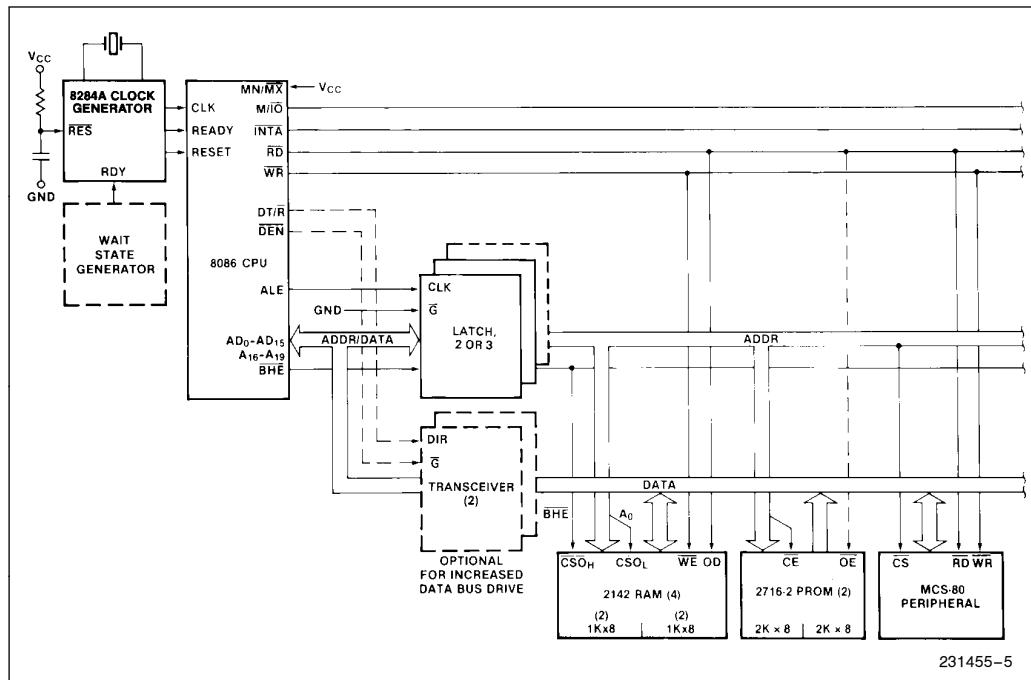


Figure 4a. Minimum Mode 8086 Typical Configuration

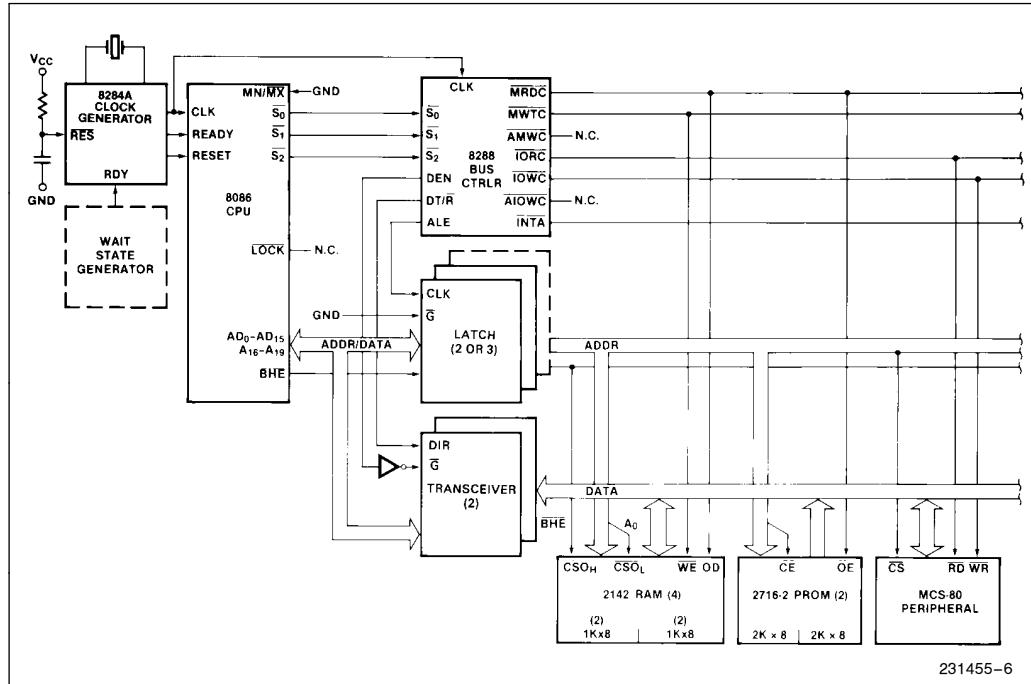


Figure 4b. Maximum Mode 8086 Typical Configuration

can occur between 8086 bus cycles. These are referred to as "Idle" states (T_i) or inactive CLK cycles. The processor uses these cycles for internal house-keeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/MX strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits \overline{S}_0 , \overline{S}_1 , and \overline{S}_2 are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

| \overline{S}_2 | \overline{S}_1 | \overline{S}_0 | Characteristics |
|------------------|------------------|------------------|------------------------|
| 0 (LOW) | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | Read I/O |
| 0 | 1 | 0 | Write I/O |
| 0 | 1 | 1 | Halt |
| 1 (HIGH) | 0 | 0 | Instruction Fetch |
| 1 | 0 | 1 | Read Data from Memory |
| 1 | 1 | 0 | Write Data to Memory |
| 1 | 1 | 1 | Passive (no bus cycle) |

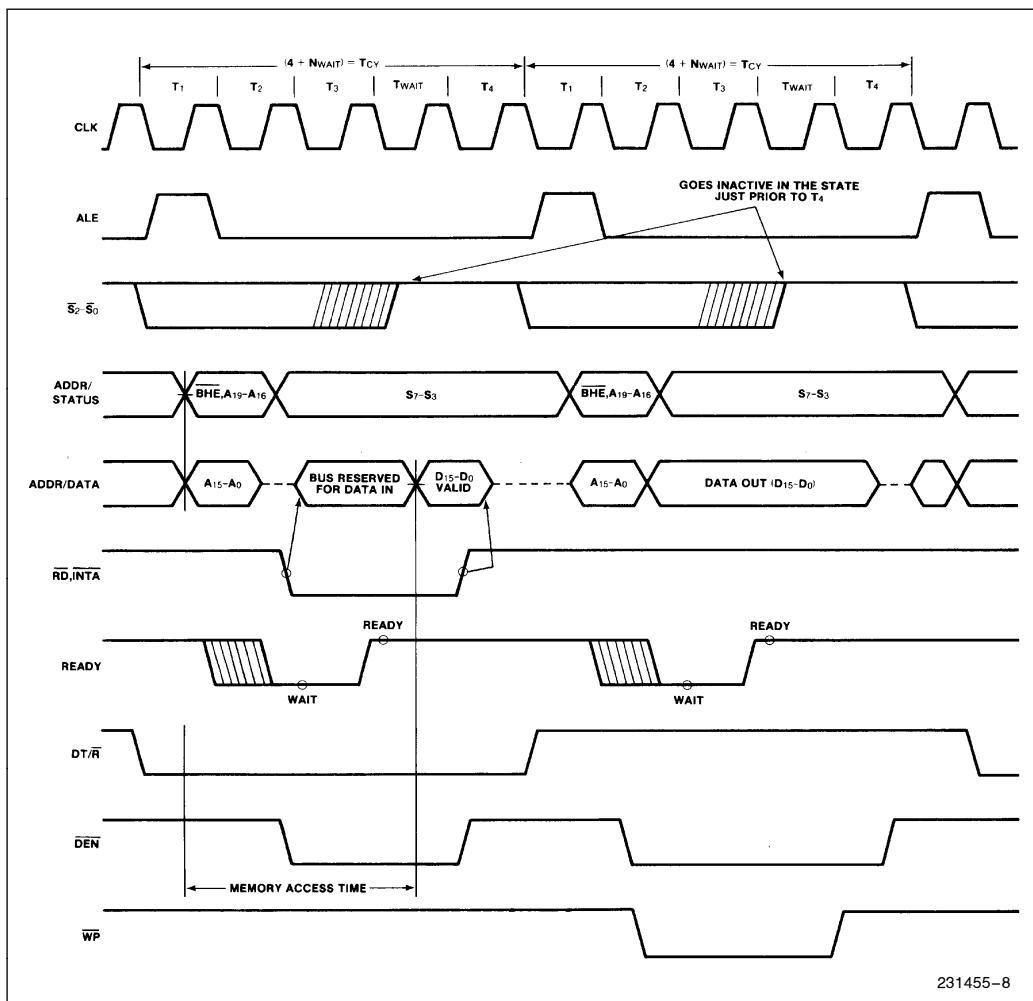


Figure 5. Basic System Timing

Status bits S₃ through S₇ are multiplexed with high-order address bits and the BHE signal, and are therefore valid during T₂ through T₄. S₃ and S₄ indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

| S ₄ | S ₃ | Characteristics |
|----------------|----------------|--------------------------------|
| 0 (LOW) | 0 | Alternate Data (extra segment) |
| 0 | 1 | Stack |
| 1 (HIGH) | 0 | Code or None |
| 1 | 1 | Data |

S₅ is a reflection of the PSW interrupt enable bit. S₆ = 0 and S₇ is a spare status bit.

I/O ADDRESSING

In the 8086, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A₁₅-A₀. The address lines A₁₉-A₁₆ are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D₇-D₀ bus lines and odd addressed bytes on D₁₅-D₈. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

External Interface

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8086 RESET is required to be HIGH for greater than 4 CLK cycles. The 8086 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 10 CLK cycles. After this interval the 8086 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3b). The details of this operation are specified in the Instruction Set description of the MCS-86 Family User's Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 µs after power-up, to allow complete initialization of the 8086.

NMI asserted prior to the 2nd clock after the end of RESET will not be honored. If NMI is asserted after that point and during the internal reset sequence, the processor may execute one instruction before responding to the interrupt. A hold request active immediately after RESET will be honored before the first instruction fetch.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF. ALE and HLDA are driven low.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See Instruction Set description.)

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The 8086 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 6) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 8086 emits the LOCK signal from T₂ of the first bus cycle until T₂ of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode, the processor issues appropriate HALT status on \bar{S}_2 , \bar{S}_1 , and \bar{S}_0 ; and the 8288 bus controller issues one ALE. The 8086 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the 8086 out of the "HALT" state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The LOCK status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multi-processor system configurations to accomplish "test and set lock" operations. The LOCK signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While LOCK is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

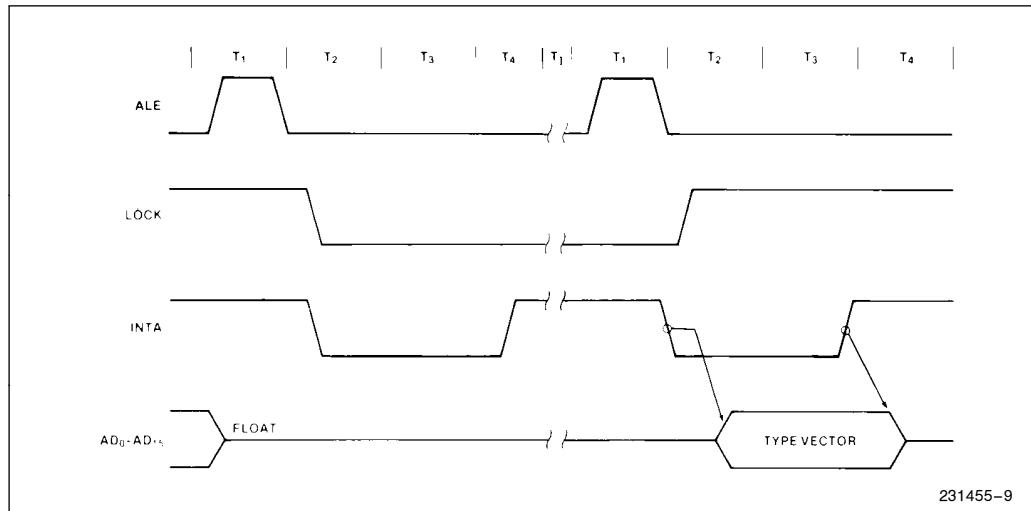


Figure 6. Interrupt Acknowledge Sequence

EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the 8086 provides a single software-testable input known as the TEST signal. At any time the program may execute a WAIT instruction. If at that time the TEST signal is inactive (HIGH), program execution becomes suspended while the processor waits for TEST to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All 8086 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-fetches and re-executes the WAIT instruction upon returning from the interrupt.

Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/MX pin is strapped to V_{CC} and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/MX pin is strapped to V_{SS} and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 5 illustrates the signal timing relationships.

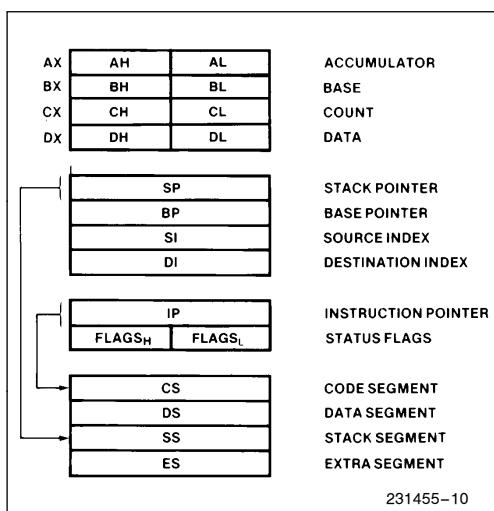


Figure 7. 8086 Register Model

SYSTEM TIMING—MINIMUM SYSTEM

The read cycle begins in T₁ with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the address latch. The BHE and A₀ signals address the low, high, or both bytes. From T₁ to T₄ the M/I/O signal indicates a memory or I/O operation. At T₂ the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T₂. The read (RD) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 8086 local bus, signals DT/R and DEN are provided by the 8086.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/I/O signal is again asserted to indicate a memory or I/O write operation. In the T₂ immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of T₄. During T₂, T₃, and T_W the processor asserts the write control signal. The write (WR) signal becomes active at the beginning of T₂ as opposed to the read which is delayed somewhat into T₂ to provide time for the bus to float.

The BHE and A₀ signals are used to select the proper byte(s) of the memory/IO word to be read or written according to the following table:

| BHE | A ₀ | Characteristics |
|-----|----------------|---------------------------------|
| 0 | 0 | Whole word |
| 0 | 1 | Upper byte from/to odd address |
| 1 | 0 | Lower byte from/to even address |
| 1 | 1 | None |

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D₇-D₀ bus lines and odd addressed bytes on D₁₅-D₈.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal (INTA) is asserted in place of the read (RD) signal and the address bus is floated. (See Figure 6.) In the second of two successive INTA cycles, a byte of information is read from bus

lines D₇-D₀ as supplied by the interrupt system logic (i.e., 8259A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

BUS TIMING—MEDIUM SIZE SYSTEMS

For medium size systems the MN/MX pin is connected to V_{SS} and the 8288 Bus Controller is added to the system as well as a latch for latching the system address, and a transceiver to allow for bus loading greater than the 8086 is capable of handling. Signals ALE, DEN, and DT/R are generated by the 8288 instead of the processor in this configuration although their timing remains relatively the same. The 8086 status outputs ($\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$) provide type-of-cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt

acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The transceiver receives the usual DIR and \overline{G} inputs from the 8288's DT/R and DEN.

The pointer into the interrupt vector table, which is passed during the second INTA cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8259A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|-----------------|
| Ambient Temperature Under Bias | 0°C to 70°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground..... | -1.0V to +7V |
| Power Dissipation..... | 2.5W |

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS (8086: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$)

(8086-1: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

(8086-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|----------|---|------|-------------------|---------------|--|
| V_{IL} | Input Low Voltage | -0.5 | +0.8 | V | (Note 1) |
| V_{IH} | Input High Voltage | 2.0 | $V_{CC} + 0.5$ | V | (Notes 1, 2) |
| V_{OL} | Output Low Voltage | | 0.45 | V | $I_{OL} = 2.5\text{ mA}$ |
| V_{OH} | Output High Voltage | 2.4 | | V | $I_{OH} = -400\text{ }\mu\text{A}$ |
| I_{CC} | Power Supply Current: 8086 8086-1 8086-2 | | 340 360 350 | mA | $T_A = 25^\circ\text{C}$ |
| I_{LI} | Input Leakage Current | | ± 10 | μA | $0\text{V} \leq V_{IN} \leq V_{CC}$ (Note 3) |
| I_{LO} | Output Leakage Current | | ± 10 | μA | $0.45\text{V} \leq V_{OUT} \leq V_{CC}$ |
| V_{CL} | Clock Input Low Voltage | -0.5 | +0.6 | V | |
| V_{CH} | Clock Input High Voltage | 3.9 | $V_{CC} + 1.0$ | V | |
| C_{IN} | Capacitance of Input Buffer (All input except $AD_0-AD_{15}, \overline{RQ}/\overline{GT}$) | | 15 | pF | $f_c = 1\text{ MHz}$ |
| C_{IO} | Capacitance of I/O Buffer ($AD_0-AD_{15}, \overline{RQ}/\overline{GT}$) | | 15 | pF | $f_c = 1\text{ MHz}$ |

NOTES:

1. V_{IL} tested with MN/\overline{MX} Pin = 0V, V_{IH} tested with MN/\overline{MX} Pin = 5V. MN/\overline{MX} Pin is a Strap Pin.

2. Not applicable to $\overline{RQ}/\overline{GT}_0$ and $\overline{RQ}/\overline{GT}_1$ (Pins 30 and 31).

3. HOLD and HLDA I_{LI} min = 30 μA , max = 500 μA .



8086

A.C. CHARACTERISTICS (8086: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$)
(8086-1: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$)
(8086-2: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

| Symbol | Parameter | 8086 | | 8086-1 | | 8086-2 | | Units | Test Conditions |
|---------|--|------|-----|--------|-----|--------|-----|-------|-------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| TCLCL | CLK Cycle Period | 200 | 500 | 100 | 500 | 125 | 500 | ns | |
| TCLCH | CLK Low Time | 118 | | 53 | | 68 | | ns | |
| TCHCL | CLK High Time | 69 | | 39 | | 44 | | ns | |
| TCH1CH2 | CLK Rise Time | | 10 | | 10 | | 10 | ns | From 1.0V to 3.5V |
| TCL2CL1 | CLK Fall Time | | 10 | | 10 | | 10 | ns | From 3.5V to 1.0V |
| TDVCL | Data in Setup Time | 30 | | 5 | | 20 | | ns | |
| TCLDX | Data in Hold Time | 10 | | 10 | | 10 | | ns | |
| TR1VCL | RDY Setup Time into 8284A (See Notes 1, 2) | 35 | | 35 | | 35 | | ns | |
| TCLR1X | RDY Hold Time into 8284A (See Notes 1, 2) | 0 | | 0 | | 0 | | ns | |
| TRYHCH | READY Setup Time into 8086 | 118 | | 53 | | 68 | | ns | |
| TCHRYX | READY Hold Time into 8086 | 30 | | 20 | | 20 | | ns | |
| TRYLCL | READY Inactive to CLK (See Note 3) | -8 | | -10 | | -8 | | ns | |
| THVCH | HOLD Setup Time | 35 | | 20 | | 20 | | ns | |
| TINVCH | INTR, NMI, TEST Setup Time (See Note 2) | 30 | | 15 | | 15 | | ns | |
| TILIH | Input Rise Time (Except CLK) | | 20 | | 20 | | 20 | ns | From 0.8V to 2.0V |
| TIHIL | Input Fall Time (Except CLK) | | 12 | | 12 | | 12 | ns | From 2.0V to 0.8V |

A.C. CHARACTERISTICS (Continued)

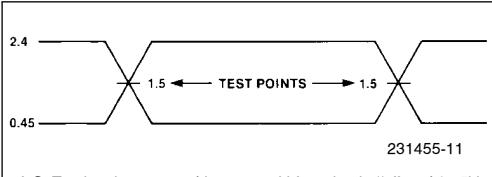
TIMING RESPONSES

| Symbol | Parameter | 8086 | | 8086-1 | | 8086-2 | | Units | Test Conditions |
|--------|--|-----------|-----|-----------|-----|-----------|-----|-------|---|
| | | Min | Max | Min | Max | Min | Max | | |
| TCLAV | Address Valid Delay | 10 | 110 | 10 | 50 | 10 | 60 | ns | $*C_L = 20-100 \text{ pF}$ for all 8086 Outputs (In addition to 8086 selfload) |
| TCLAX | Address Hold Time | 10 | | 10 | | 10 | | ns | |
| TCLAZ | Address Float Delay | TCLAX | 80 | 10 | 40 | TCLAX | 50 | ns | |
| TLHLL | ALE Width | TCLCH-20 | | TCLCH-10 | | TCLCH-10 | | ns | |
| TCLLH | ALE Active Delay | | 80 | | 40 | | 50 | ns | |
| TCHLL | ALE Inactive Delay | | 85 | | 45 | | 55 | ns | |
| TLLAX | Address Hold Time | TCHCL-10 | | TCHCL-10 | | TCHCL-10 | | ns | |
| TCLDV | Data Valid Delay | 10 | 110 | 10 | 50 | 10 | 60 | ns | |
| TCHDX | Data Hold Time | 10 | | 10 | | 10 | | ns | |
| TWHDX | Data Hold Time After WR | TCLCH-30 | | TCLCH-25 | | TCLCH-30 | | ns | |
| TCVCTV | Control Active Delay 1 | 10 | 110 | 10 | 50 | 10 | 70 | ns | |
| TCHCTV | Control Active Delay 2 | 10 | 110 | 10 | 45 | 10 | 60 | ns | |
| TCVCTX | Control Inactive Delay | 10 | 110 | 10 | 50 | 10 | 70 | ns | |
| TAZRL | Address Float to READ Active | 0 | | 0 | | 0 | | ns | |
| TCLRL | \bar{RD} Active Delay | 10 | 165 | 10 | 70 | 10 | 100 | ns | |
| TCLRH | \bar{RD} Inactive Delay | 10 | 150 | 10 | 60 | 10 | 80 | ns | |
| TRHAV | \bar{RD} Inactive to Next Address Active | TCLCL-45 | | TCLCL-35 | | TCLCL-40 | | ns | |
| TCLHAV | HLDA Valid Delay | 10 | 160 | 10 | 60 | 10 | 100 | ns | |
| TRLRH | \bar{RD} Width | 2TCLCL-75 | | 2TCLCL-40 | | 2TCLCL-50 | | ns | |
| TWLWH | \bar{WR} Width | 2TCLCL-60 | | 2TCLCL-35 | | 2TCLCL-40 | | ns | |
| TAVAL | Address Valid to ALE Low | TCLCH-60 | | TCLCH-35 | | TCLCH-40 | | ns | |
| TOLOH | Output Rise Time | | 20 | | 20 | | 20 | ns | From 0.8V to 2.0V |
| TOHOL | Output Fall Time | | 12 | | 12 | | 12 | ns | From 2.0V to 0.8V |

NOTES:

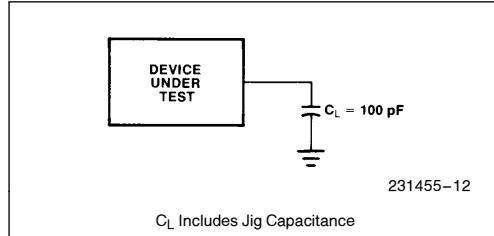
1. Signal at 8284A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3).

A.C. TESTING INPUT, OUTPUT WAVEFORM



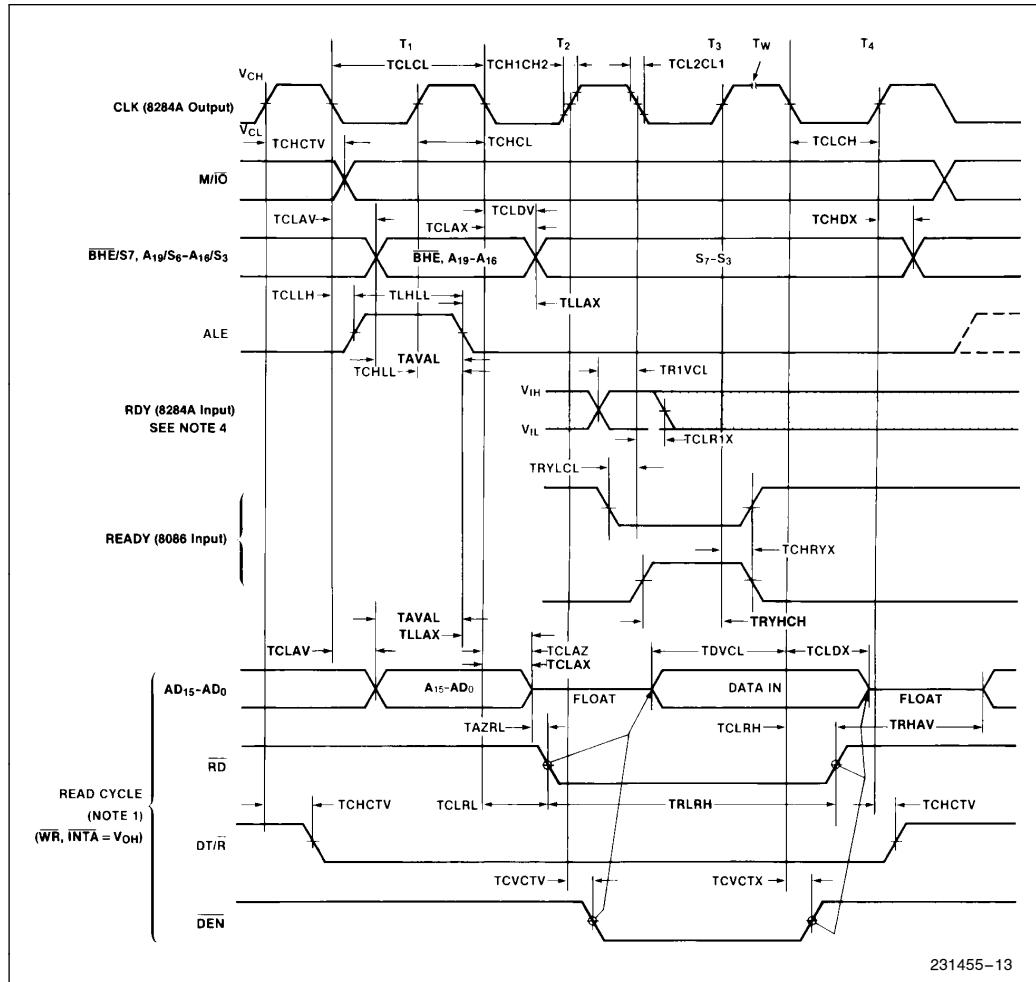
A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 1.5V for both a Logic "1" and "0".

A.C. TESTING LOAD CIRCUIT



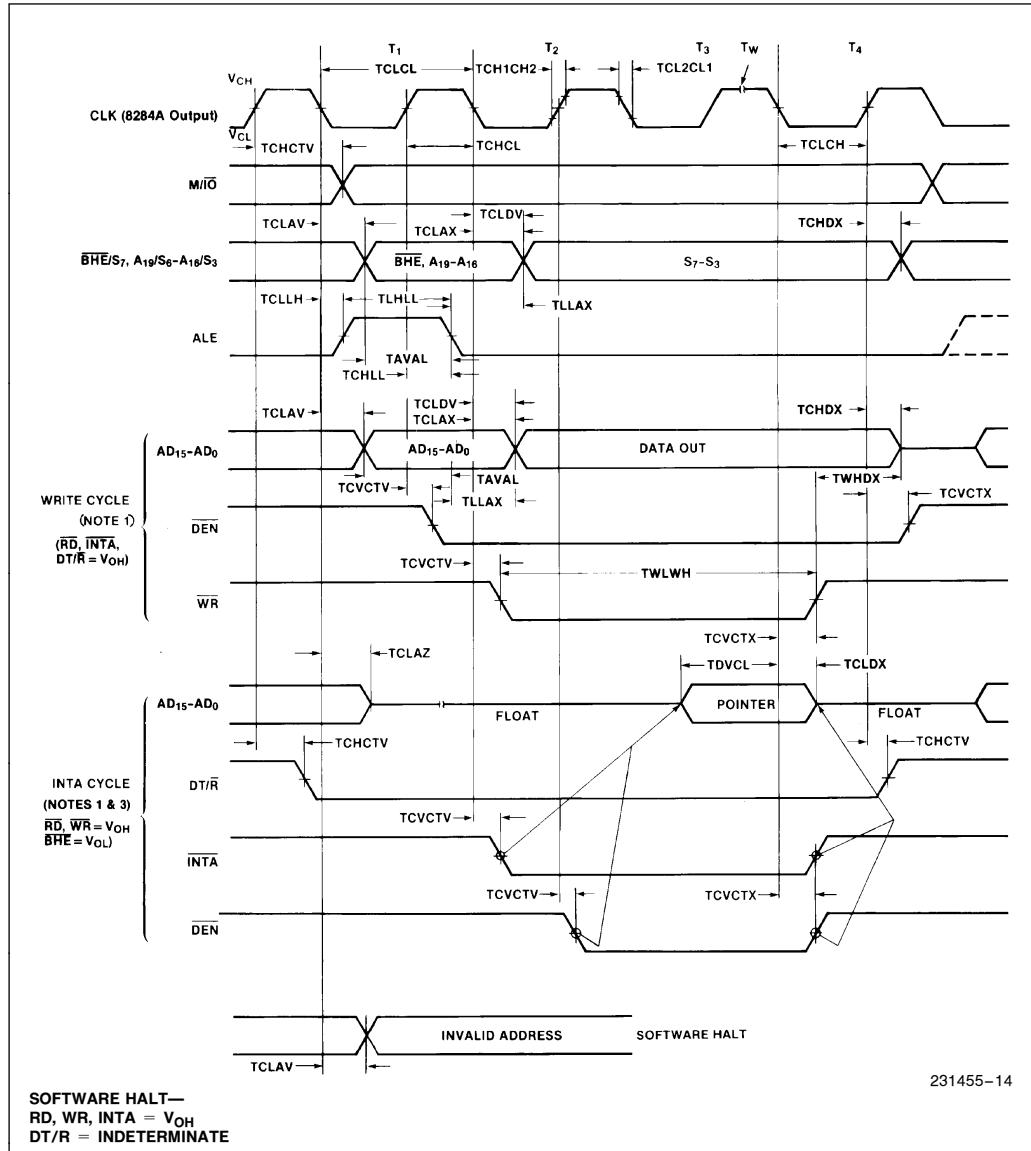
WAVEFORMS

MINIMUM MODE



WAVEFORMS (Continued)

MINIMUM MODE (Continued)



NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2 , T_3 , T_W to determine if T_W machine states are to be inserted.
3. Two INTA cycles run back-to-back. The 8086 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at 8284A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

A.C. CHARACTERISTICS
**MAX MODE SYSTEM (USING 8288 BUS CONTROLLER)
TIMING REQUIREMENTS**

| Symbol | Parameter | 8086 | | 8086-1 | | 8086-2 | | Units | Test Conditions |
|---------|--|------|-----|--------|-----|--------|-----|-------|--|
| | | Min | Max | Min | Max | Min | Max | | |
| TCLCL | CLK Cycle Period | 200 | 500 | 100 | 500 | 125 | 500 | ns | From 1.0V to 3.5V From 3.5V to 1.0V |
| TCLCH | CLK Low Time | 118 | | 53 | | 68 | | ns | |
| TCHCL | CLK High Time | 69 | | 39 | | 44 | | ns | |
| TCH1CH2 | CLK Rise Time | | 10 | | 10 | | 10 | ns | |
| TCL2CL1 | CLK Fall Time | | 10 | | 10 | | 10 | ns | |
| TDVCL | Data in Setup Time | 30 | | 5 | | 20 | | ns | |
| TCLDX | Data in Hold Time | 10 | | 10 | | 10 | | ns | |
| TR1VCL | RDY Setup Time into 8284A (Notes 1, 2) | 35 | | 35 | | 35 | | ns | |
| TCLR1X | RDY Hold Time into 8284A (Notes 1, 2) | 0 | | 0 | | 0 | | ns | |
| TRYHCH | READY Setup Time into 8086 | 118 | | 53 | | 68 | | ns | |
| TCHRYX | READY Hold Time into 8086 | 30 | | 20 | | 20 | | ns | |
| TRYLCL | READY Inactive to CLK (Note 4) | -8 | | -10 | | -8 | | ns | |
| TINVCH | Setup Time for Recognition (INTR, NMI, TEST) (Note 2) | 30 | | 15 | | 15 | | ns | |
| TGVCH | RQ/GT Setup Time (Note 5) | 30 | | 15 | | 15 | | ns | |
| TCHGX | RQ Hold Time into 8086 | 40 | | 20 | | 30 | | ns | |
| TILIH | Input Rise Time (Except CLK) | | 20 | | 20 | | 20 | ns | From 0.8V to 2.0V |
| TIHIL | Input Fall Time (Except CLK) | | 12 | | 12 | | 12 | ns | From 2.0V to 0.8V |

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

| Symbol | Parameter | 8086 | | 8086-1 | | 8086-2 | | Units | Test Conditions |
|---------------|---|-------------|------------|---------------|------------|---------------|------------|--------------|---|
| | | Min | Max | Min | Max | Min | Max | | |
| TCLML | Command Active Delay (See Note 1) | 10 | 35 | 10 | 35 | 10 | 35 | ns | $C_L = 20-100 \text{ pF}$ for all 8086 Outputs (in addition to 8086 self-load) |
| TCLMH | Command Inactive Delay (See Note 1) | 10 | 35 | 10 | 35 | 10 | 35 | ns | |
| TRYHSH | READY Active to Status Passive (See Note 3) | | 110 | | 45 | | 65 | ns | |
| TCHSV | Status Active Delay | 10 | 110 | 10 | 45 | 10 | 60 | ns | |
| TCLSH | Status Inactive Delay | 10 | 130 | 10 | 55 | 10 | 70 | ns | |
| TCLAV | Address Valid Delay | 10 | 110 | 10 | 50 | 10 | 60 | ns | |
| TCLAX | Address Hold Time | 10 | | 10 | | 10 | | ns | |
| TCLAZ | Address Float Delay | TCLAX | 80 | 10 | 40 | TCLAX | 50 | ns | |
| TSVLH | Status Valid to ALE High (See Note 1) | | 15 | | 15 | | 15 | ns | |
| TSVMCH | Status Valid to MCE High (See Note 1) | | 15 | | 15 | | 15 | ns | |
| TCLLH | CLK Low to ALE Valid (See Note 1) | | 15 | | 15 | | 15 | ns | |
| TCLMCH | CLK Low to MCE High (See Note 1) | | 15 | | 15 | | 15 | ns | |
| TCHLL | ALE Inactive Delay (See Note 1) | | 15 | | 15 | | 15 | ns | |
| TCLMCL | MCE Inactive Delay (See Note 1) | | 15 | | 15 | | 15 | ns | |
| TCLDV | Data Valid Delay | 10 | 110 | 10 | 50 | 10 | 60 | ns | |
| TCHDX | Data Hold Time | 10 | | 10 | | 10 | | ns | |
| TCVN | Control Active Delay (See Note 1) | 5 | 45 | 5 | 45 | 5 | 45 | ns | |
| TCVNX | Control Inactive Delay (See Note 1) | 10 | 45 | 10 | 45 | 10 | 45 | ns | |
| TAZRL | Address Float to READ Active | 0 | | 0 | | 0 | | ns | |
| TCLR | RD Active Delay | 10 | 165 | 10 | 70 | 10 | 100 | ns | |
| TCLR | RD Inactive Delay | 10 | 150 | 10 | 60 | 10 | 80 | ns | |

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES (Continued)

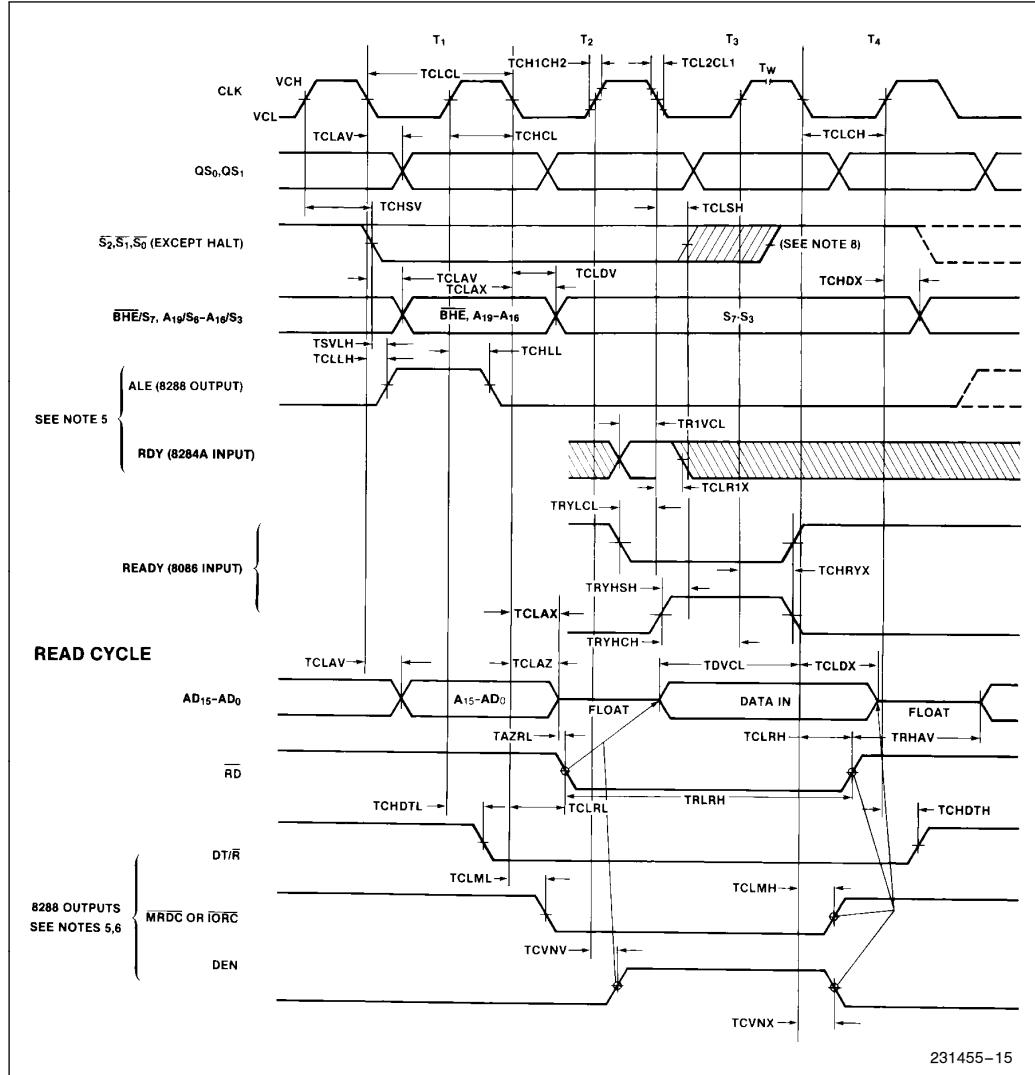
| Symbol | Parameter | 8086 | | 8086-1 | | 8086-2 | | Units | Test Conditions |
|---------------|---|-------------|------------|---------------|------------|---------------|------------|--------------|---|
| | | Min | Max | Min | Max | Min | Max | | |
| TRHAV | RD Inactive to Next Address Active | TCLCL-45 | | TCLCL-35 | | TCLCL-40 | | ns | $C_L = 20-100 \text{ pF}$ for all 8086 Outputs (In addition to 8086 self-load) |
| TCHDTL | Direction Control Active Delay (Note 1) | | 50 | | 50 | | 50 | ns | |
| TCHDTH | Direction Control Inactive Delay (Note 1) | | 30 | | 30 | | 30 | ns | |
| TCLGL | GT Active Delay | 0 | 85 | 0 | 38 | 0 | 50 | ns | |
| TCLGH | GT Inactive Delay | 0 | 85 | 0 | 45 | 0 | 50 | ns | |
| TRLRH | RD Width | 2TCLCL-75 | | 2TCLCL-40 | | 2TCLCL-50 | | ns | |
| TOLOH | Output Rise Time | | 20 | | 20 | | 20 | ns | From 0.8V to 2.0V |
| TOHOL | Output Fall Time | | 12 | | 12 | | 12 | ns | From 2.0V to 0.8V |

NOTES:

1. Signal at 8284A or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).

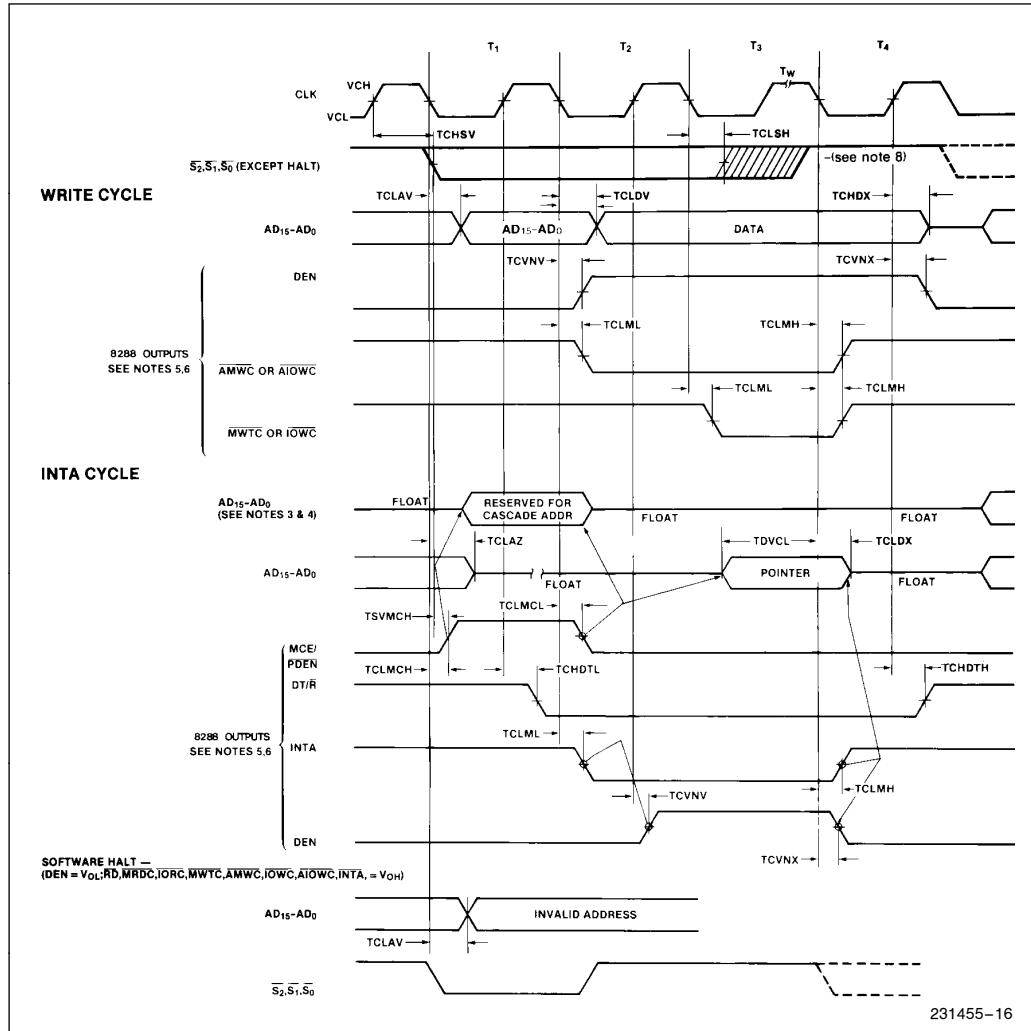
WAVEFORMS

MAXIMUM MODE



WAVEFORMS (Continued)

MAXIMUM MODE (Continued)

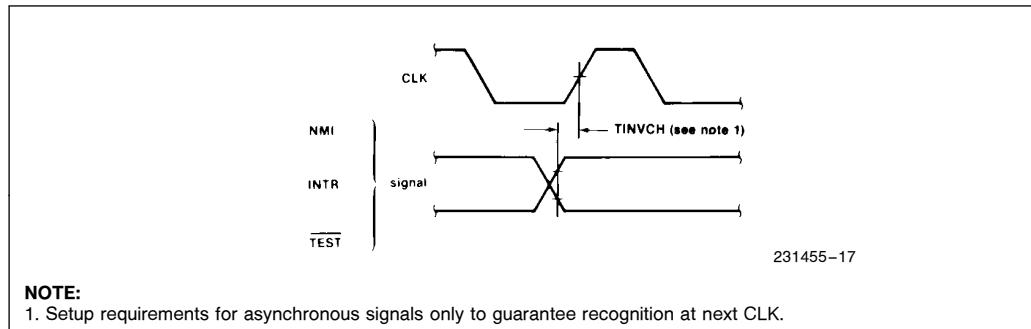


NOTES:

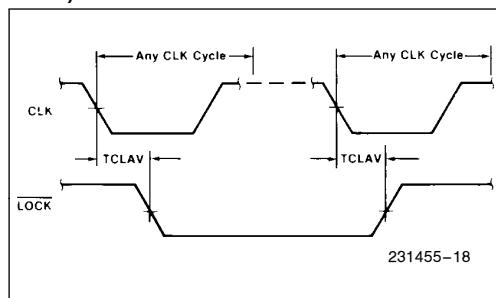
- All signals switch between V_{OH} and V_{OL} unless otherwise specified.
- RDY is sampled near the end of T₂, T₃, T_W to determine if T_W machine states are to be inserted.
- Cascade address is valid between first and second INTA cycle.
- Two INTA cycles run back-to-back. The 8086 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
- Signals at 8284A or 8288 are shown for reference only.
- The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
- All timing measurements are made at 1.5V unless otherwise noted.
- Status inactive in state just prior to T₄.

WAVEFORMS (Continued)

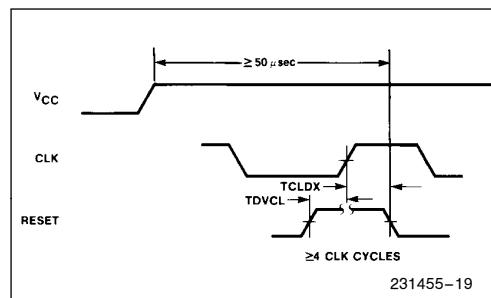
ASYNCHRONOUS SIGNAL RECOGNITION



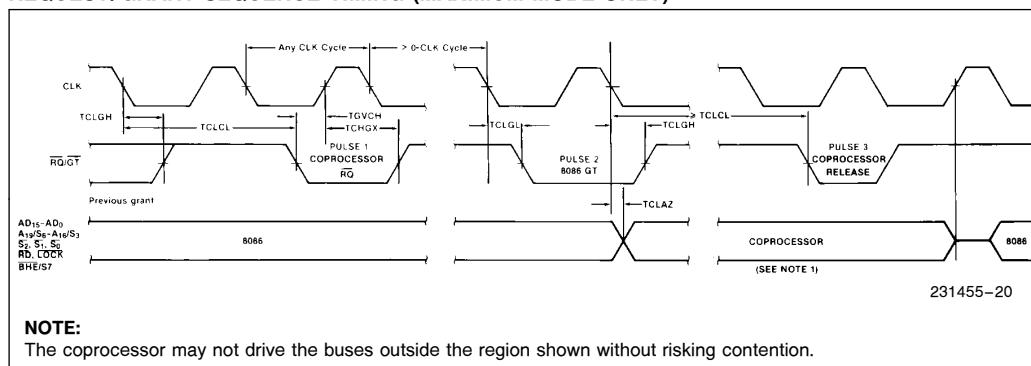
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



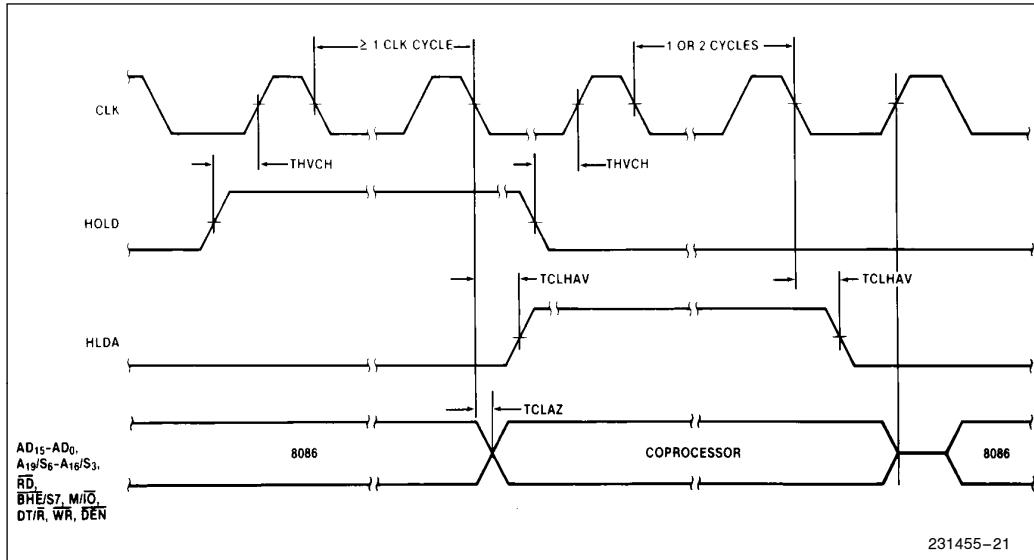
RESET TIMING



REQUEST/GANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



WAVEFORMS (Continued)

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)


231455-21

Table 2. Instruction Set Summary

| Mnemonic and Description | Instruction Code | | | |
|-------------------------------------|------------------|-----------------|-----------------|-----------------|
| DATA TRANSFER | | | | |
| MOV = Move: | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| Register/Memory to/from Register | 1 0 0 0 1 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 1 0 0 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1 |
| Immediate to Register | 1 0 1 1 w reg | data | data if w = 1 | |
| Memory to Accumulator | 1 0 1 0 0 0 w | addr-low | addr-high | |
| Accumulator to Memory | 1 0 1 0 0 1 w | addr-low | addr-high | |
| Register/Memory to Segment Register | 1 0 0 0 1 1 0 | mod 0 reg r/m | | |
| Segment Register to Register/Memory | 1 0 0 0 1 1 0 0 | mod 0 reg r/m | | |
| PUSH = Push: | | | | |
| Register/Memory | 1 1 1 1 1 1 1 1 | mod 1 1 0 r/m | | |
| Register | 0 1 0 1 0 reg | | | |
| Segment Register | 0 0 0 reg 1 1 0 | | | |
| POP = Pop: | | | | |
| Register/Memory | 1 0 0 0 1 1 1 1 | mod 0 0 0 r/m | | |
| Register | 0 1 0 1 1 reg | | | |
| Segment Register | 0 0 0 reg 1 1 1 | | | |
| XCHG = Exchange: | | | | |
| Register/Memory with Register | 1 0 0 0 0 1 1 w | mod reg r/m | | |
| Register with Accumulator | 1 0 0 1 0 reg | | | |
| IN = Input from: | | | | |
| Fixed Port | 1 1 1 0 0 1 0 w | port | | |
| Variable Port | 1 1 1 0 1 1 0 w | | | |
| OUT = Output to: | | | | |
| Fixed Port | 1 1 1 0 0 1 1 w | port | | |
| Variable Port | 1 1 1 0 1 1 1 w | | | |
| XLAT = Translate Byte to AL | 1 1 0 1 0 1 1 1 | | | |
| LEA = Load EA to Register | 1 0 0 0 1 1 0 1 | mod reg r/m | | |
| LDS = Load Pointer to DS | 1 1 0 0 0 1 0 1 | mod reg r/m | | |
| LES = Load Pointer to ES | 1 1 0 0 0 1 0 0 | mod reg r/m | | |
| LAHF = Load AH with Flags | 1 0 0 1 1 1 1 1 | | | |
| SAHF = Store AH into Flags | 1 0 0 1 1 1 1 0 | | | |
| PUSHF = Push Flags | 1 0 0 1 1 1 0 0 | | | |
| POPF = Pop Flags | 1 0 0 1 1 1 0 1 | | | |

Mnemonics © Intel, 1978

Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | | | |
|--|------------------|-----------------|-----------------|-------------------|
| ARITHMETIC | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| ADD = Add: | | | | |
| Reg./Memory with Register to Either | 0 0 0 0 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 s w | mod 0 0 0 r/m | data | data if s: w = 01 |
| Immediate to Accumulator | 0 0 0 0 1 0 w | data | data if w = 1 | |
| ADC = Add with Carry: | | | | |
| Reg./Memory with Register to Either | 0 0 0 1 0 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 s w | mod 0 1 0 r/m | data | data if s: w = 01 |
| Immediate to Accumulator | 0 0 0 1 0 1 0 w | data | data if w = 1 | |
| INC = Increment: | | | | |
| Register/Memory | 1 1 1 1 1 1 1 w | mod 0 0 0 r/m | | |
| Register | 0 1 0 0 0 reg | | | |
| AAA = ASCII Adjust for Add | 0 0 1 1 0 1 1 1 | | | |
| BAA = Decimal Adjust for Add | 0 0 1 0 0 1 1 1 | | | |
| SUB = Subtract: | | | | |
| Reg./Memory and Register to Either | 0 0 1 0 1 0 d w | mod reg r/m | | |
| Immediate from Register/Memory | 1 0 0 0 0 0 s w | mod 1 0 1 r/m | data | data if s w = 01 |
| Immediate from Accumulator | 0 0 1 0 1 1 0 w | data | data if w = 1 | |
| SSB = Subtract with Borrow | | | | |
| Reg./Memory and Register to Either | 0 0 0 1 1 0 d w | mod reg r/m | | |
| Immediate from Register/Memory | 1 0 0 0 0 0 s w | mod 0 1 1 r/m | data | data if s w = 01 |
| Immediate from Accumulator | 0 0 0 1 1 1 w | data | data if w = 1 | |
| DEC = Decrement: | | | | |
| Register/memory | 1 1 1 1 1 1 1 w | mod 0 0 1 r/m | | |
| Register | 0 1 0 0 1 reg | | | |
| NEG = Change sign | 1 1 1 1 0 1 1 w | mod 0 1 1 r/m | | |
| CMP = Compare: | | | | |
| Register/Memory and Register | 0 0 1 1 1 0 d w | mod reg r/m | | |
| Immediate with Register/Memory | 1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w = 01 |
| Immediate with Accumulator | 0 0 1 1 1 1 0 w | data | data if w = 1 | |
| AAS = ASCII Adjust for Subtract | 0 0 1 1 1 1 1 1 | | | |
| DAS = Decimal Adjust for Subtract | 0 0 1 0 1 1 1 1 | | | |
| MUL = Multiply (Unsigned) | 1 1 1 1 0 1 1 w | mod 1 0 0 r/m | | |
| IMUL = Integer Multiply (Signed) | 1 1 1 1 0 1 1 w | mod 1 0 1 r/m | | |
| AAM = ASCII Adjust for Multiply | 1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 | | |
| DIV = Divide (Unsigned) | 1 1 1 1 0 1 1 w | mod 1 1 0 r/m | | |
| IDIV = Integer Divide (Signed) | 1 1 1 1 0 1 1 w | mod 1 1 1 r/m | | |
| AAD = ASCII Adjust for Divide | 1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0 | | |
| CBW = Convert Byte to Word | 1 0 0 1 1 0 0 0 | | | |
| CWD = Convert Word to Double Word | 1 0 0 1 1 0 0 1 | | | |

Mnemonics © Intel, 1978

Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | | | |
|---|------------------|-----------------|-----------------|-----------------|
| LOGIC | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| NOT = Invert | 1 1 1 1 0 1 1 w | mod 0 1 0 r/m | | |
| SHL/SAL = Shift Logical/Arithmetic Left | 1 1 0 1 0 0 v w | mod 1 0 0 r/m | | |
| SHR = Shift Logical Right | 1 1 0 1 0 0 v w | mod 1 0 1 r/m | | |
| SAR = Shift Arithmetic Right | 1 1 0 1 0 0 v w | mod 1 1 1 r/m | | |
| ROL = Rotate Left | 1 1 0 1 0 0 v w | mod 0 0 0 r/m | | |
| ROR = Rotate Right | 1 1 0 1 0 0 v w | mod 0 0 1 r/m | | |
| RCL = Rotate Through Carry Flag Left | 1 1 0 1 0 0 v w | mod 0 1 0 r/m | | |
| RCR = Rotate Through Carry Right | 1 1 0 1 0 0 v w | mod 0 1 1 r/m | | |
| AND = And: | | | | |
| Reg./Memory and Register to Either | 0 0 1 0 0 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1 |
| Immediate to Accumulator | 0 0 1 0 0 1 0 w | data | data if w = 1 | |
| TEST = And Function to Flags, No Result: | | | | |
| Register/Memory and Register | 1 0 0 0 0 1 0 w | mod reg r/m | | |
| Immediate Data and Register/Memory | 1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1 |
| Immediate Data and Accumulator | 1 0 1 0 1 0 0 w | data | data if w = 1 | |
| OR = Or: | | | | |
| Reg./Memory and Register to Either | 0 0 0 0 1 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1 |
| Immediate to Accumulator | 0 0 0 0 1 1 0 w | data | data if w = 1 | |
| XOR = Exclusive or: | | | | |
| Reg./Memory and Register to Either | 0 0 1 1 0 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1 |
| Immediate to Accumulator | 0 0 1 1 0 1 0 w | data | data if w = 1 | |
| STRING MANIPULATION | | | | |
| REP = Repeat | 1 1 1 1 0 0 1 z | | | |
| MOVS = Move Byte/Word | 1 0 1 0 0 1 0 w | | | |
| CMPS = Compare Byte/Word | 1 0 1 0 0 1 1 w | | | |
| SCAS = Scan Byte/Word | 1 0 1 0 1 1 1 w | | | |
| LODS = Load Byte/Wd to AL/AX | 1 0 1 0 1 1 0 w | | | |
| STOS = Stor Byte/Wd from AL/A | 1 0 1 0 1 0 1 w | | | |
| CONTROL TRANSFER | | | | |
| CALL = Call: | | | | |
| Direct within Segment | 1 1 1 0 1 0 0 0 | disp-low | disp-high | |
| Indirect within Segment | 1 1 1 1 1 1 1 1 | mod 0 1 0 r/m | | |
| Direct Intersegment | 1 0 0 1 1 0 1 0 | offset-low | offset-high | |
| | | seg-low | seg-high | |
| Indirect Intersegment | 1 1 1 1 1 1 1 1 | mod 0 1 1 r/m | | |

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Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | | |
|--|------------------------|------------------------|------------------------|
| JMP = Unconditional Jump: | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| Direct within Segment | 1 1 1 0 1 0 0 1 | disp-low | disp-high |
| Direct within Segment-Short | 1 1 1 0 1 0 1 1 | disp | |
| Indirect within Segment | 1 1 1 1 1 1 1 1 | mod 1 0 0 r/m | |
| Direct Intersegment | 1 1 1 0 1 0 1 0 | offset-low | offset-high |
| | | seg-low | seg-high |
| Indirect Intersegment | 1 1 1 1 1 1 1 1 | mod 1 0 1 r/m | |
| RET = Return from CALL: | | | |
| Within Segment | 1 1 0 0 0 0 1 1 | | |
| Within Seg Adding Immed to SP | 1 1 0 0 0 0 1 0 | data-low | data-high |
| Intersegment | 1 1 0 0 1 0 1 1 | | |
| Intersegment Adding Immediate to SP | 1 1 0 0 1 0 1 0 | data-low | data-high |
| JE/JZ = Jump on Equal/Zero | 0 1 1 1 0 1 0 0 | disp | |
| JL/JNG = Jump on Less/Not Greater or Equal | 0 1 1 1 1 1 0 0 | disp | |
| JLE/JNG = Jump on Less or Equal/Not Greater | 0 1 1 1 1 1 1 0 | disp | |
| JB/JNAE = Jump on Below/Not Above or Equal | 0 1 1 1 0 0 1 0 | disp | |
| JBE/JNA = Jump on Below or Equal/Not Above | 0 1 1 1 0 1 1 0 | disp | |
| JP/JPE = Jump on Parity/Parity Even | 0 1 1 1 1 0 1 0 | disp | |
| JO = Jump on Overflow | 0 1 1 1 0 0 0 0 | disp | |
| JS = Jump on Sign | 0 1 1 1 1 0 0 0 | disp | |
| JNE/JNZ = Jump on Not Equal/Not Zero | 0 1 1 1 0 1 0 1 | disp | |
| JNL/JGE = Jump on Not Less/Greater or Equal | 0 1 1 1 1 1 0 1 | disp | |
| JNLE/JG = Jump on Not Less or Equal/Greater | 0 1 1 1 1 1 1 1 | disp | |
| JNB/JAE = Jump on Not Below/Above or Equal | 0 1 1 1 0 0 1 1 | disp | |
| JNBE/JA = Jump on Not Below or Equal/Above | 0 1 1 1 0 1 1 1 | disp | |
| JNP/JPO = Jump on Not Par/Par Odd | 0 1 1 1 1 0 1 1 | disp | |
| JNO = Jump on Not Overflow | 0 1 1 1 0 0 0 1 | disp | |
| JNS = Jump on Not Sign | 0 1 1 1 1 0 0 1 | disp | |
| LOOP = Loop CX Times | 1 1 1 0 0 0 1 0 | disp | |
| LOOPZ/LOOPE = Loop While Zero/Equal | 1 1 1 0 0 0 0 1 | disp | |
| LOOPNZ/LOOPNE = Loop While Not Zero/Equal | 1 1 1 0 0 0 0 0 | disp | |
| JCXZ = Jump on CX Zero | 1 1 1 0 0 0 1 1 | disp | |
| INT = Interrupt | | | |
| Type Specified | 1 1 0 0 1 1 0 1 | type | |
| Type 3 | 1 1 0 0 1 1 0 0 | | |
| INTO = Interrupt on Overflow | 1 1 0 0 1 1 1 0 | | |
| IRET = Interrupt Return | 1 1 0 0 1 1 1 1 | | |

Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | |
|--|------------------|-----------------|
| | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| PROCESSOR CONTROL | | |
| CLC = Clear Carry | 1 1 1 1 1 0 0 0 | |
| CMC = Complement Carry | 1 1 1 1 0 1 0 1 | |
| STC = Set Carry | 1 1 1 1 1 0 0 1 | |
| CLD = Clear Direction | 1 1 1 1 1 1 0 0 | |
| STD = Set Direction | 1 1 1 1 1 1 0 1 | |
| CLI = Clear Interrupt | 1 1 1 1 1 0 1 0 | |
| STI = Set Interrupt | 1 1 1 1 1 0 1 1 | |
| HLT = Halt | 1 1 1 1 0 1 0 0 | |
| WAIT = Wait | 1 0 0 1 1 0 1 1 | |
| ESC = Escape (to External Device) | 1 1 0 1 1 x x x | mod x x x r/m |
| LOCK = Bus Lock Prefix | 1 1 1 1 0 0 0 0 | |

NOTES:

AL = 8-bit accumulator

AX = 16-bit accumulator

CX = Count register

DS = Data segment

ES = Extra segment

Above/below refers to unsigned value

Greater = more positive;

Less = less positive (more negative) signed values

if d = 1 then "to" reg; if d = 0 then "from" reg

if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field

if mod = 00 then DISP = 0*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent

if mod = 10 then DISP = disp-high; disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP*

if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high; disp-low.

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if s w = 01 then 16 bits of immediate data form the operand

if s w = 11 then an immediate data byte is sign extended to form the 16-bit operand

if v = 0 then "count" = 1; if v = 1 then "count" in (CL)

x = don't care

z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

| 16-Bit (w = 1) | 8-Bit (w = 0) | Segment |
|----------------|---------------|---------|
| 000 AX | 000 AL | 00 ES |
| 001 CX | 001 CL | 01 CS |
| 010 DX | 010 DL | 10 SS |
| 011 BX | 011 BL | 11 DS |
| 100 SP | 100 AH | |
| 101 BP | 101 CH | |
| 110 SI | 110 DH | |
| 111 DI | 111 BH | |

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

DATA SHEET REVISION REVIEW

The following list represents key differences between this and the -004 data sheet. Please review this summary carefully.

1. The Intel 8086 implementation technology (HMOS) has been changed to (HMOS-III).

2. Delete all "changes from 1985 Handbook Specification" sentences.

SNx4LS245 Octal Bus Transceivers With 3-State Outputs

1 Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

2 Applications

- Building Automation
- Electronic Point of Sale
- Factory Automation and Control
- Test and Measurement

3 Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

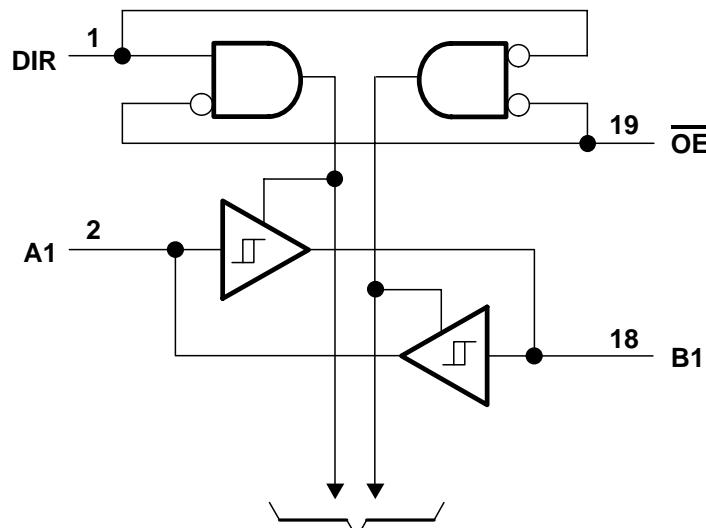
The SNx4LS245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the device so that the buses are effectively isolated.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------|
| SN54LS245J | CDIP (20) | 24.20 mm × 6.92 mm |
| SN54LS245W | CFP (20) | 7.02 mm × 13.72 mm |
| SN54LS245FK | LCCC (20) | 8.89 mm × 8.89 mm |
| SN74LS245DB | SSOP (20) | 7.20 mm × 5.30 mm |
| SN74LS245DW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74LS245N | PDIP (20) | 24.33 mm × 6.35 mm |
| SN74LS245NS | SO (20) | 12.60 mm × 5.30 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



To Seven Other Channels

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

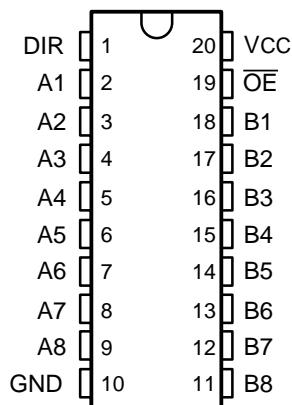
| Changes from Revision A (February 2002) to Revision B | Page |
|--|------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet | 1 |
| • Changed $R_{\theta JA}$ values in <i>Thermal Information</i> table: 70 to 91.7 for DB package, 58 to 79 for DW package, 69 to 46.1 for N package, and 60 to 74.2 for NS package | 4 |

5 Device Comparison Table

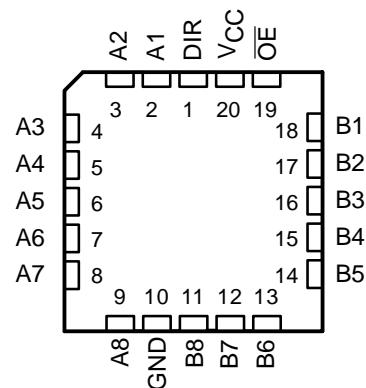
| TYPE | I_{OL} (SINK CURRENT) | I_{OH} (SOURCE CURRENT) |
|-----------|----------------------------|------------------------------|
| SN54LS245 | 12 mA | -12 mA |
| SN74LS245 | 24 mA | -15 mA |

6 Pin Configuration and Functions

J, W, DB, DW, N, or NS Package
20-Pin CDIP, CFP, SSOP, SOIC, PDIP, or SO
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|--|
| NO. | NAME | | |
| 1 | DIR | I | Controls signal direction; Low = Bx to Ax, High = Ax to Bx |
| 2 | A1 | I/O | Channel 1, A side |
| 3 | A2 | I/O | Channel 2, A side |
| 4 | A3 | I/O | Channel 3, A side |
| 5 | A4 | I/O | Channel 4, A side |
| 6 | A5 | I/O | Channel 5, A side |
| 7 | A6 | I/O | Channel 6, A side |
| 8 | A7 | I/O | Channel 7, A side |
| 9 | A8 | I/O | Channel 8, A side |
| 10 | GND | — | Ground |
| 11 | B8 | O/I | Channel 8, B side |
| 12 | B7 | O/I | Channel 7, B side |
| 13 | B6 | O/I | Channel 6, B side |
| 14 | B5 | O/I | Channel 5, B side |
| 15 | B4 | O/I | Channel 4, B side |
| 16 | B3 | O/I | Channel 3, B side |
| 17 | B2 | O/I | Channel 2, B side |
| 18 | B1 | O/I | Channel 1, B side |
| 19 | \overline{OE} | I | Active low output enable; Low = all channels active, High = all channels disabled (high impedance) |
| 20 | V _{CC} | — | Power supply |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------|--|-----|-----|------|
| V_{CC} | Supply voltage | 7 | | V |
| V_I | Input voltage ⁽¹⁾ | 7 | | V |
| T_J | Operating virtual junction temperature | 150 | | °C |
| T_{stg} | Storage temperature | -65 | 150 | °C |

(1) All voltage values are with respect to GND.

7.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|--|-------|------|
| $V_{(ESD)}$ | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|----------|-----------|-----|------|------|
| V_{CC} | Supply voltage | V_{CC} | 4.5 | 5 | 5.5 | V |
| | | V_{CC} | 4.75 | 5 | 5.25 | |
| I_{OH} | High-level output current | I_{OH} | SN54LS245 | | -12 | mA |
| | | I_{OH} | SN74LS245 | | -15 | |
| I_{OL} | Low-level output current | I_{OL} | SN54LS245 | | 12 | mA |
| | | I_{OL} | SN74LS245 | | 24 | |
| T_A | Operating free-air temperature | T_A | SN54LS245 | -55 | 125 | °C |
| | | T_A | SN74LS245 | 0 | 70 | |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SNx4LS245 | | | | | | | UNIT |
|-------------------------------|--|---------------------|----------------------|---------------------|--------------|-------------|------------|-----------|
| | J (CDIP) | W (CFP) | FK (LCCC) | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SO) | |
| | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | N/A | N/A | N/A | 91.7 | 79.0 | 46.1 | 74.2 °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42.3 ⁽²⁾ | 70.1 ⁽²⁾ | 46.7 ⁽²⁾ | 53.1 | 44.4 | 32.1 | 40.4 °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.9 ⁽²⁾ | 109.5 ⁽²⁾ | 45.6 ⁽²⁾ | 46.8 | 46.9 | 27.0 | 41.7 °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | N/A | N/A | N/A | 18.9 | 18.0 | 17.6 | 16.9 °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | N/A | N/A | N/A | 46.4 | 46.3 | 26.9 | 41.3 °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 15.9 ⁽²⁾ | 13.0 ⁽²⁾ | 6.7 ⁽²⁾ | N/A | N/A | N/A | N/A °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) MIL-STD-883 for Rth-JCx JEDEC JESD51 for Rth-JB (body not contact PCB)

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|--|---|--|---------------------------------------|-----------|--------------------|------|------|----|
| V _{IH} | High-level input voltage | | | 2 | | | V | |
| V _{IL} | Low-level input voltage | | SN54LS245 | 0.7 | | 0.8 | V | |
| | | | SN74LS245 | | | | | |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, | I _I = -18 mA | | | -1.5 | V | |
| Hysteresis (V _{T+} - V _{T-}) | A or B | V _{CC} = MIN | | 0.2 | 0.4 | | V | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IL} = V _{IL(max)} V _{IH} = 2 V, | I _{OH} = -3 mA | 2.4 | 3.4 | 2 | V | |
| | | | I _{OH} = MAX | | | | | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL(max)} | I _{OL} = 12 mA | 0.4 | | 0.5 | V | |
| | | | I _{OL} = 24 mA | SN74LS245 | | | | |
| I _{OZH} | Off-state output current, high-level voltage applied | V _{CC} = MAX, OE at 2 V | V _O = 2.7 V | | | 20 | μA | |
| I _{OZL} | Off-state output current, low-level voltage applied | V _{CC} = MAX, OE at 2 V | V _O = 0.4 V | | | -200 | μA | |
| I _I | Input current at maximum input voltage | A or B DIR or \overline{OE} | V _I = 5.5 V | 0.1 | | 0.1 | mA | |
| | | | V _I = 7 V | | | | | |
| I _{IH} | High-level input current | V _{CC} = MAX, | V _{IH} = 2.7 V | | | 20 | μA | |
| I _{IL} | Low-level input current | V _{CC} = MAX, | V _{IL} = 0.4 V | | | -0.2 | mA | |
| I _{OS} | Short-circuit output current ⁽²⁾ | V _{CC} = MAX | | -40 | -225 | | mA | |
| I _{CC} | Supply current | Total, outputs high | V _{CC} = MAX Outputs open | | | 48 | 70 | mA |
| | | Total, outputs low | | | | 62 | 90 | |
| | | Outputs at high Z | | | | 64 | 95 | |

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

7.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see Figure 2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|--|-----|-----|-----|------|
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 45 pF, R _L = 667 Ω | 8 | 12 | ns | |
| t _{PHL} | Propagation delay time, high- to low-level output | | 8 | 12 | | |
| t _{PZL} | Output enable time to low level | C _L = 45 pF, R _L = 667 Ω | 27 | 40 | ns | |
| t _{PZH} | Output enable time to high level | | 25 | 40 | | |
| t _{PLZ} | Output disable time from low level | C _L = 5 pF, R _L = 667 Ω | 15 | 25 | ns | |
| t _{PHZ} | Output disable time from high level | | 15 | 28 | | |

7.7 Typical Characteristics

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45 \text{ pF}$, $R_L = 667 \Omega$

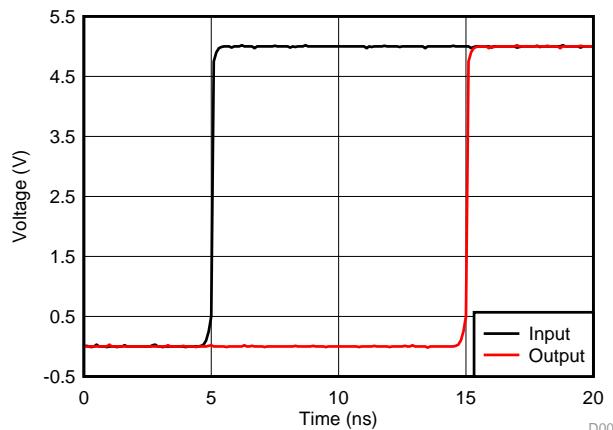
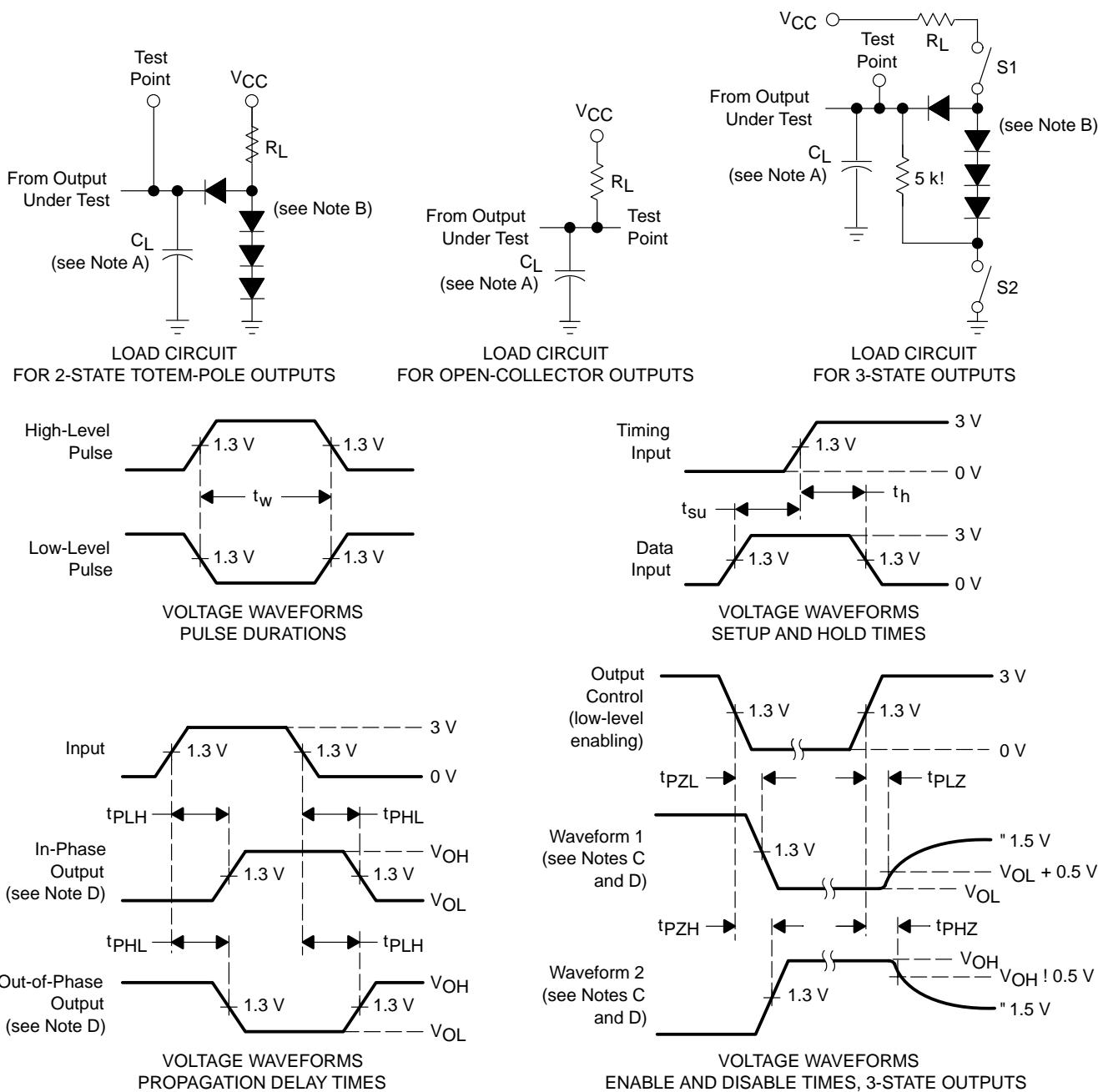


Figure 1. Simulated Propagation Delay From Input to Output

8 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 - F. All input pulses are supplied by generators having the following characteristics: PRR ! 1 MHz, Z_O " 50!, t_r ! 1.5 ns, t_f ! 2.6 ns.
 - G. The outputs are measured one at a time with one input transition per measurement.

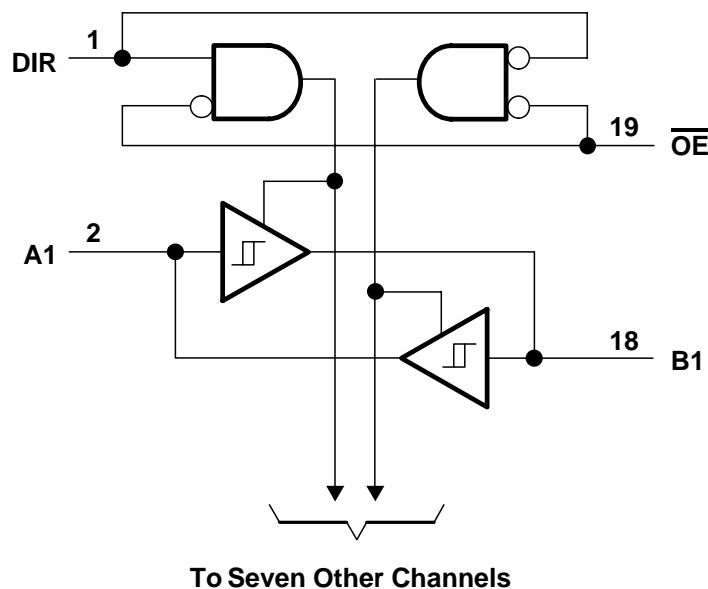
Figure 2. Load Circuits and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4LS245 uses Schottky transistor logic to perform the standard '245 transceiver function. This standard logic function has a common pinout, direction select pin, and active-low output enable. When the outputs are disabled, the A and B sides of the device are effectively isolated.

9.2 Functional Block Diagram



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Figure 3. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 3-State outputs

The 3-state outputs can drive bus lines directly. All outputs can be put into high impedance mode through the \overline{OE} pin.

9.3.2 PNP Inputs

This device has PNP inputs which reduce dc loading on bus lines.

9.3.3 Hysteresis on Bus Inputs

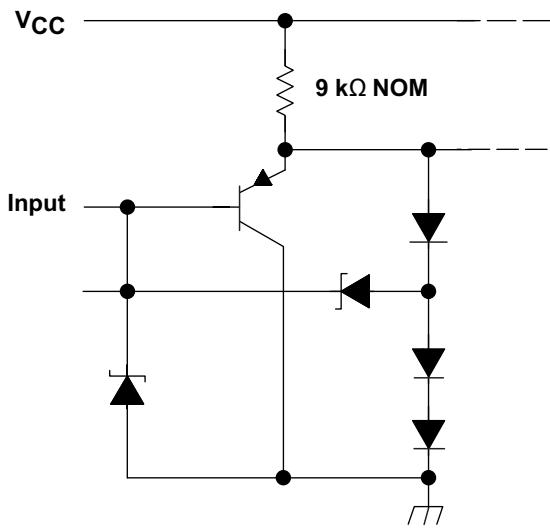
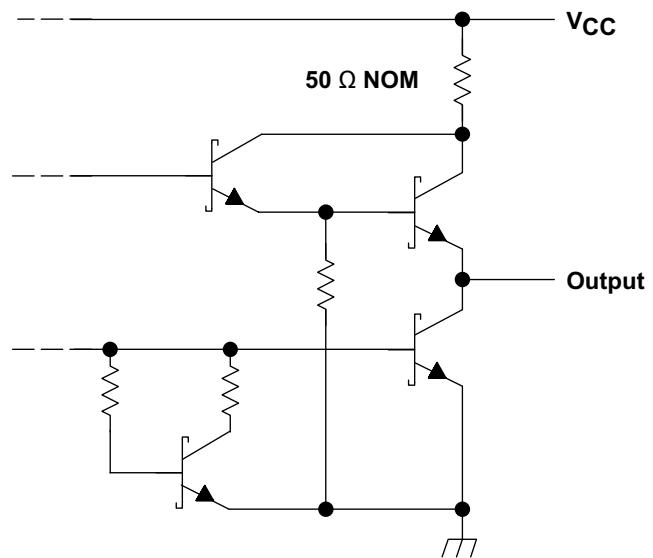
The bus inputs have built-in hysteresis that improves noise margins.

9.4 Device Functional Modes

The SNx4LS245 performs the standard '245 logic function. Data can be transmitted from A to B or from B to A depending on the DIR pin value, or the A and B sides can be isolated from one another by setting the \overline{OE} pin HIGH.

Table 1. Function Table

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

EQUIVALENT OF EACH INPUT

TYPICAL OF ALL OUTPUTS

Figure 4. Schematics of Inputs and Outputs

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SNx4LS245 is commonly used to drive ribbon cables or back plane busses. It allows isolation from the bus when necessary, and increases drive strength on the bus.

10.2 Typical Application

Figure 5 shows the SNx4LS245 wired up as a permanently enabled data bus transceiver for both a master and slave device communicating over a ribbon cable or back plane.

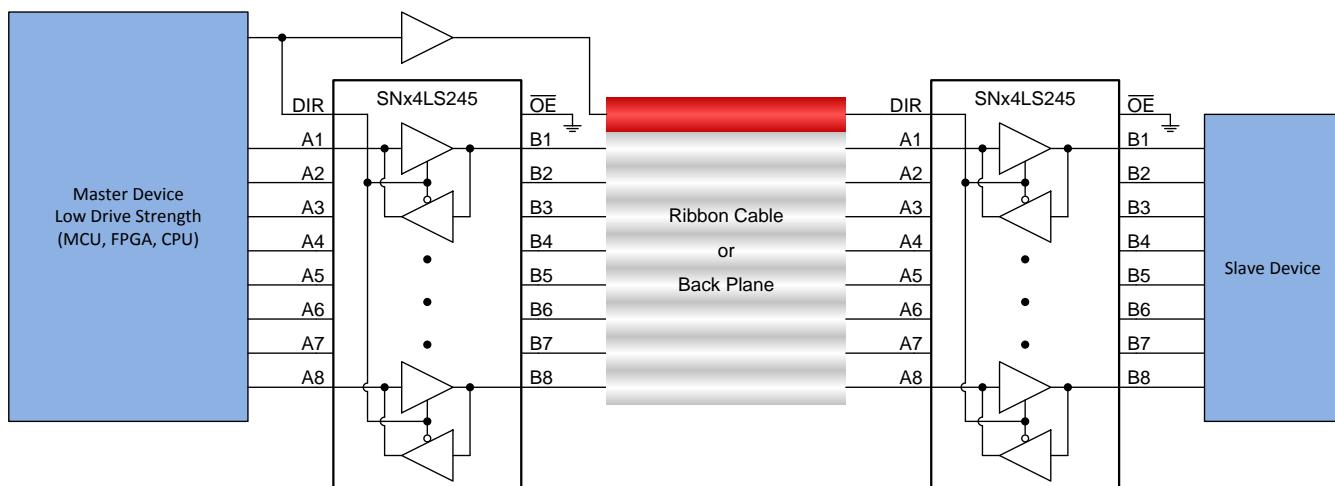


Figure 5. SNx4LS245 Being Used to Communicate Over a Ribbon Cable or Back Plane

10.2.1 Design Requirements

This device uses Schottky transistor logic technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

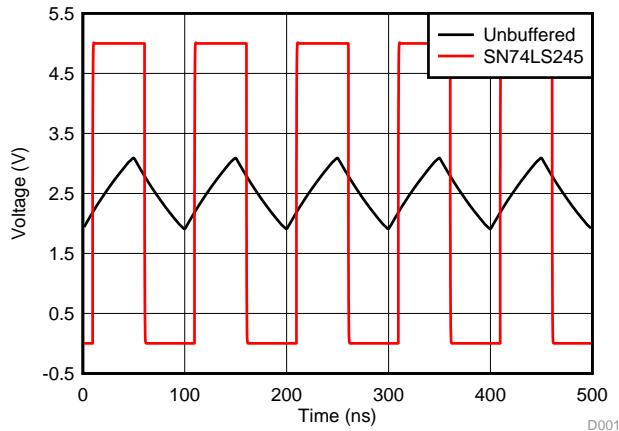
10.2.2 Detailed Design Procedure

- Power Supply
 - Each device must maintain a supply voltage between 4.5 V and 5.5 V
- Inputs
 - Input signals must meet the V_{IH} and V_{IL} specifications in [Electrical Characteristics](#)
 - Inputs leakage values (I_I , I_{IH} , I_{IL}) from [Electrical Characteristics](#) must be considered
- Outputs
 - Output signals are specified to meet the V_{OH} and V_{OL} specifications in [Electrical Characteristics](#) as a minimum (the values could be closer to V_{CC} for high signals or GND for low signals)
 - TI recommends maintaining output currents as specified in [Recommended Operating Conditions](#)
 - The part can be damaged by sourcing or sinking too much current. See [Electrical Characteristics](#) for details.

Typical Application (continued)

10.2.3 Application Curve

It is common to see significant losses in ribbon cables and back planes. Figure 6 shows a simplified simulation of a ribbon cable from a 5-V, 10-MHz low-drive strength source. It shows the difference between an input signal from a weak driver like an MCU or FPGA compared to a strong driver like the SN74LS245 when measured at the distant end of the cable. By adding a high-current drive transceiver before the cable, the signal strength can be significantly improved, and subsequently the cable can be longer.



Unbuffered line is directly connected to low current source, SN74LS245 line is buffered through the transceiver. Both signals are measured at the distant end of the ribbon cable. **Input signal is not shown.**

Figure 6. Simulated Outputs From Ribbon Cable With a 5-V, 10-MHz Source

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F bypass capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01- μ F or 0.022- μ F bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1 μ F and 1 μ F are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs must not be left floating. In many applications, some channels of the SNx4LS245 are unused, and thus must be terminated properly. Because each transceiver channel pin can be either an input or an output, they must be treated as both when being terminated. Ground or V_{CC} (whichever is more convenient) can be used to terminate unused inputs; however, each unused channel should be terminated to the same logic level on both the A and B side. For example, in Figure 7 unused channels 4, 5, 6, and 7 are terminated correctly with both sides connected to the same voltage, while channel 8 is terminated incorrectly with each side being tied to a different voltage. The OE input is also unused in this example, and is terminated directly to ground to permanently enable all outputs.

12.2 Layout Example

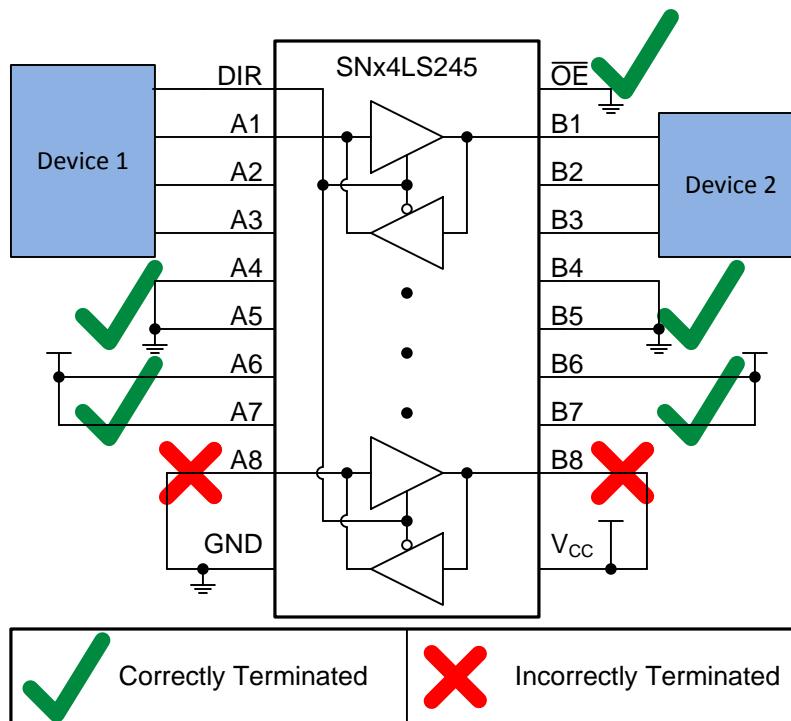


Figure 7. Example Demonstrating How to Terminate Unused Inputs and Channels of a Transceiver

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LS245 | Click here |
| SN74LS245 | Click here |

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|------------------------------------|---|
| 5962-8002101VSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8002101VS A SNV54LS245W | Samples |
| 80021012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 80021012A SNJ54LS 245FK | Samples |
| 8002101SA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8002101SA SNJ54LS245W | Samples |
| JM38510/32803B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32803B2A | Samples |
| JM38510/32803BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BRA | Samples |
| JM38510/32803BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BSA | Samples |
| M38510/32803B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32803B2A | Samples |
| M38510/32803BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BRA | Samples |
| M38510/32803BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BSA | Samples |
| SN54LS245J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS245J | Samples |
| SN74LS245DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS245N | Samples |
| SN74LS245NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS245N | Samples |
| SN74LS245NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS245 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------|---|
| SNJ54LS245FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 80021012A SNJ54LS 245FK | Samples |
| SNJ54LS245J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS245J | Samples |
| SNJ54LS245W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8002101SA SNJ54LS245W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



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PACKAGE OPTION ADDENDUM

9-Mar-2021

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS245, SN54LS245-SP, SN74LS245 :

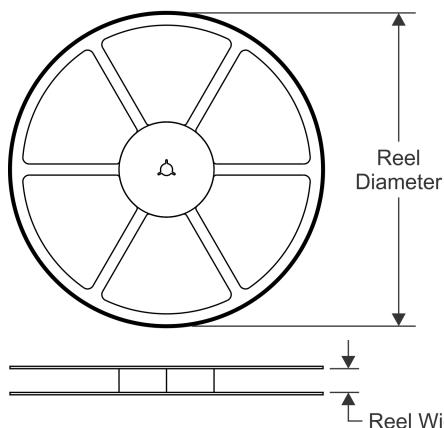
- Catalog: [SN74LS245](#), [SN54LS245](#)
- Military: [SN54LS245](#)
- Space: [SN54LS245-SP](#)

NOTE: Qualified Version Definitions:

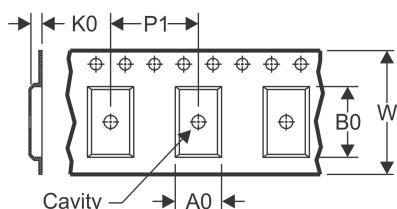
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

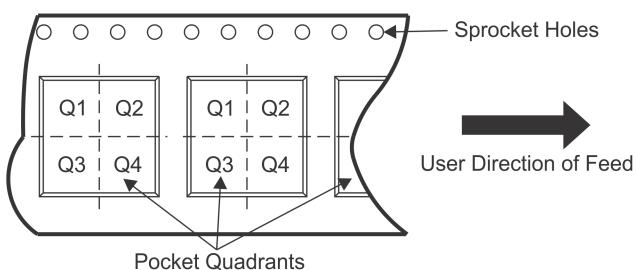


TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

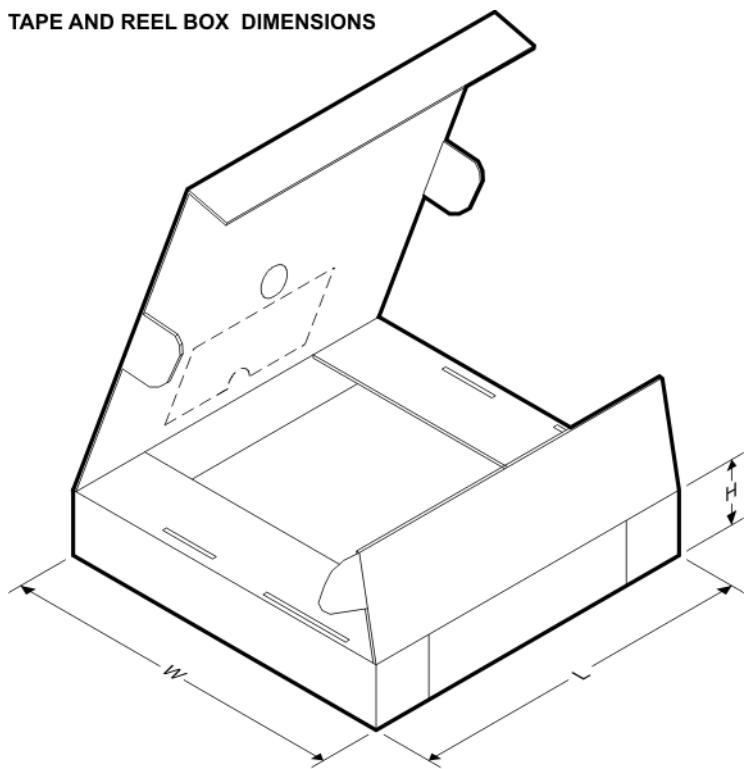
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS245NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



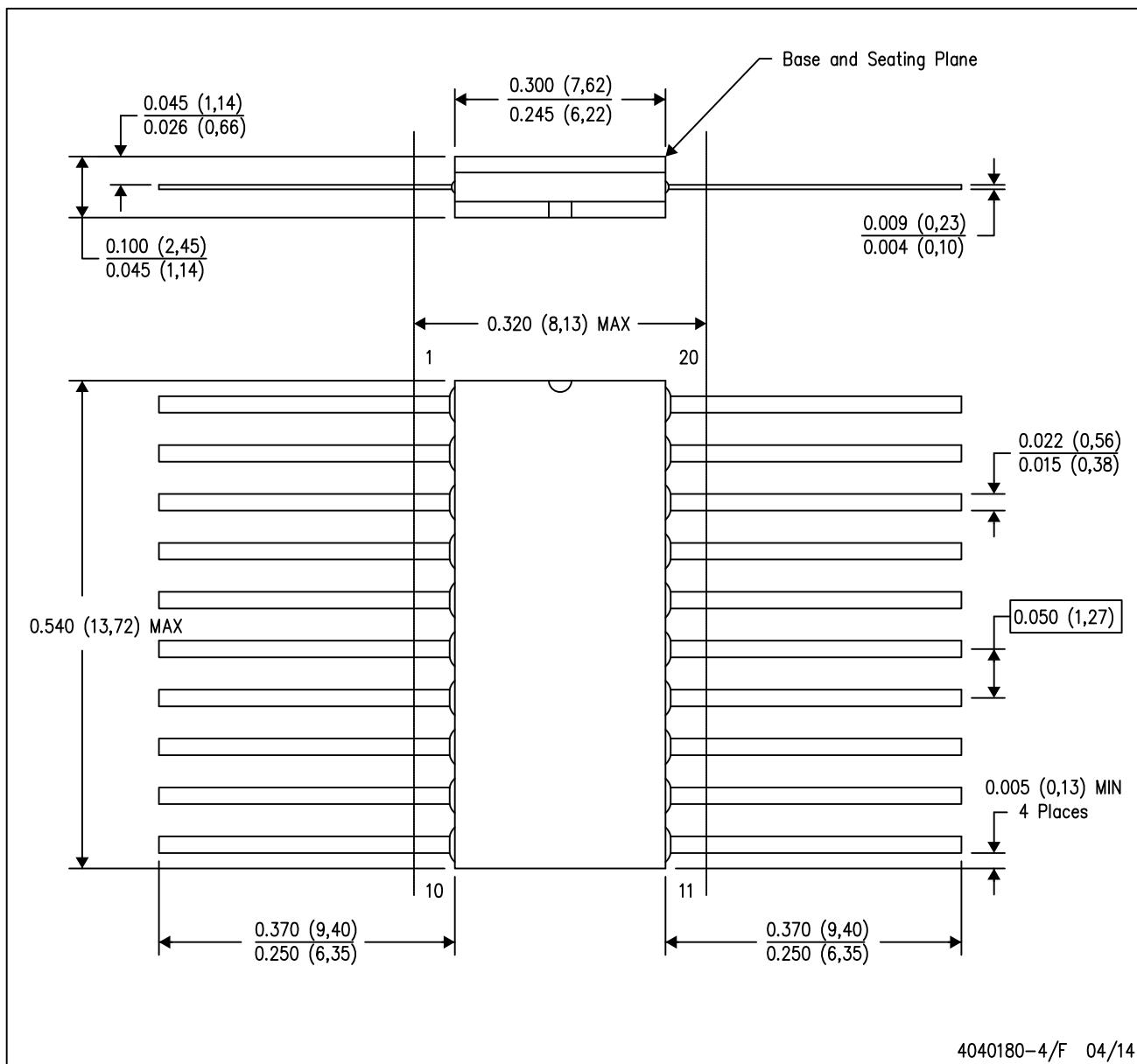
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS245DBR | SSOP | DB | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LS245DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS245NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

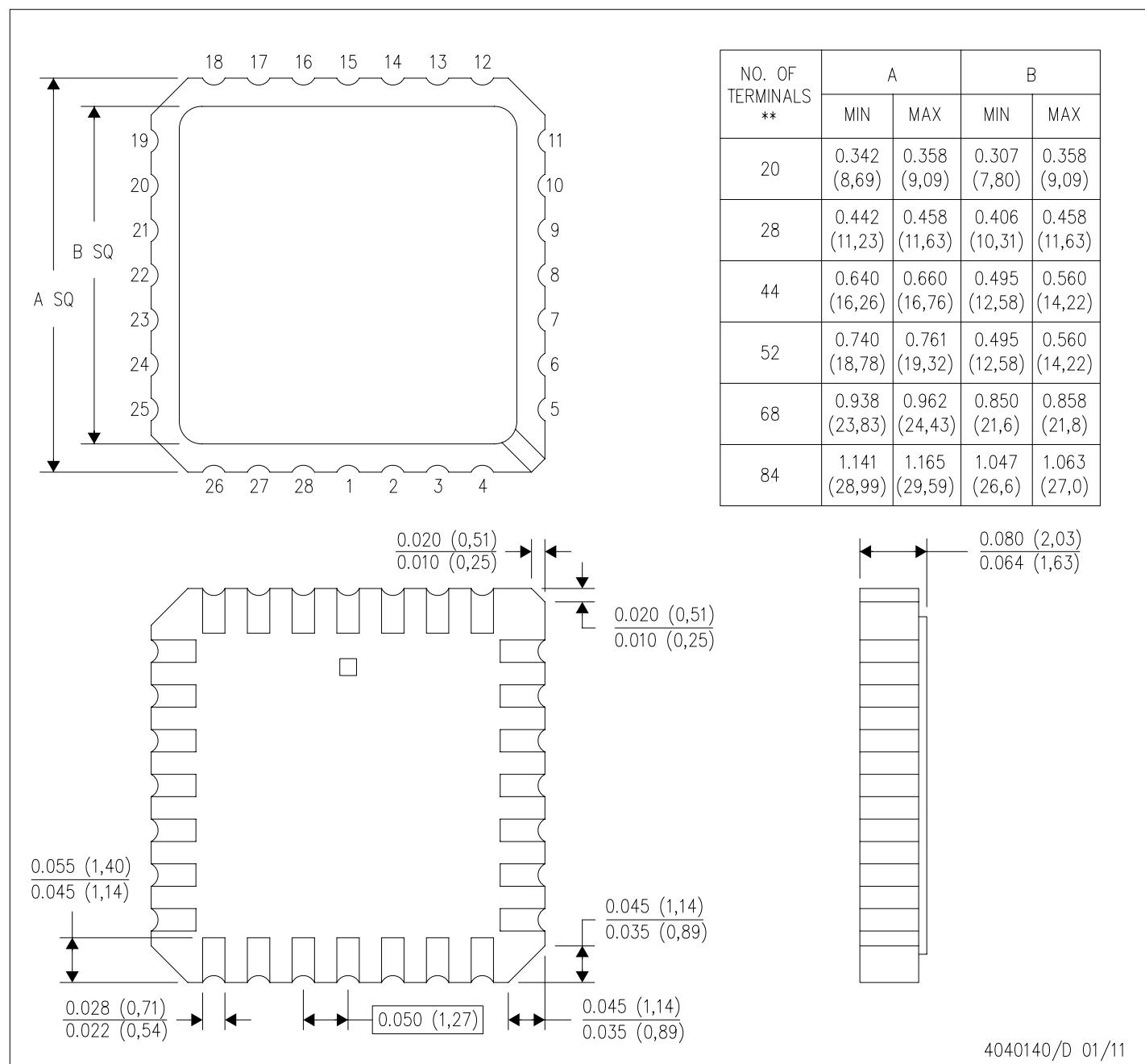


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

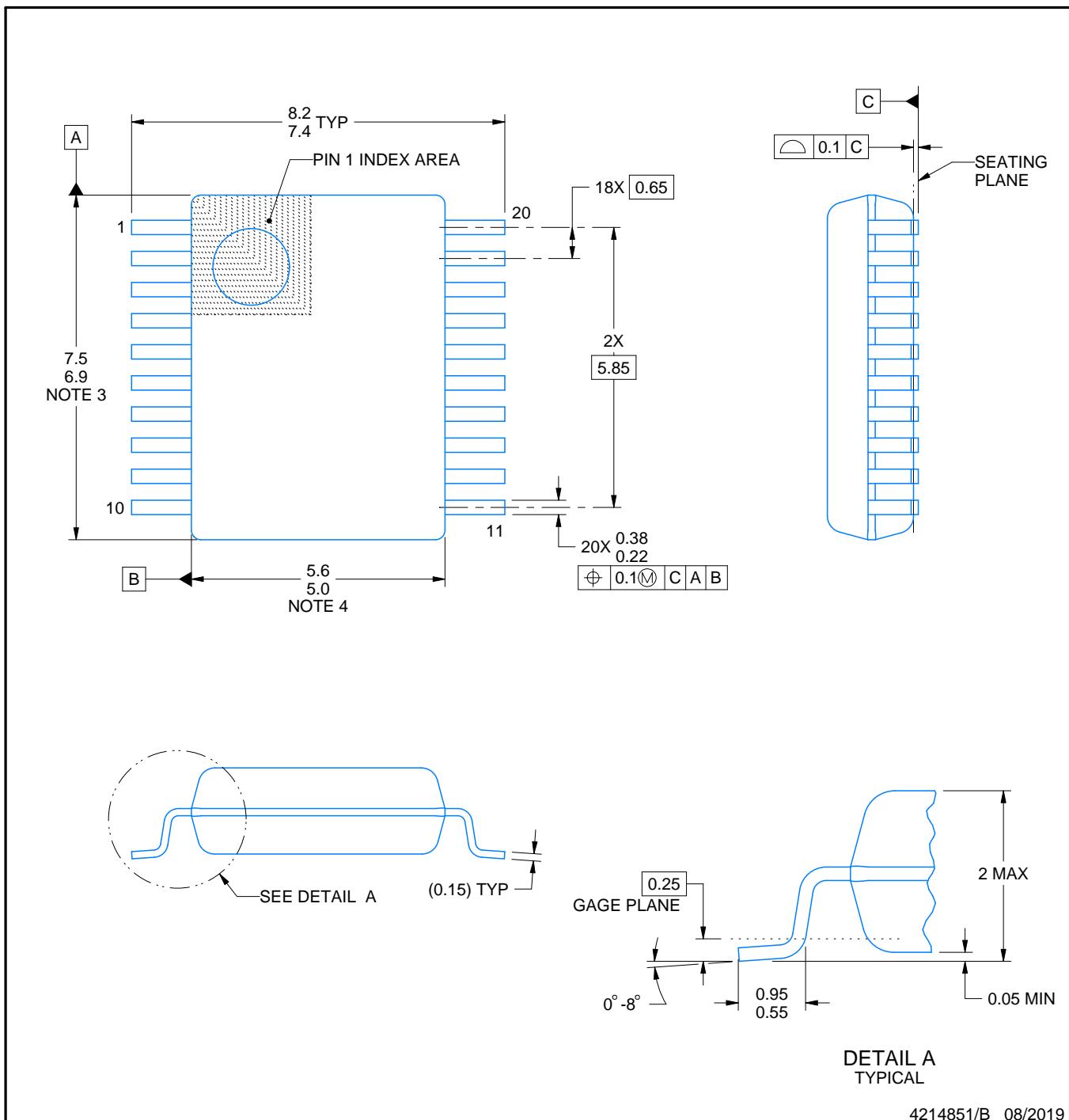
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

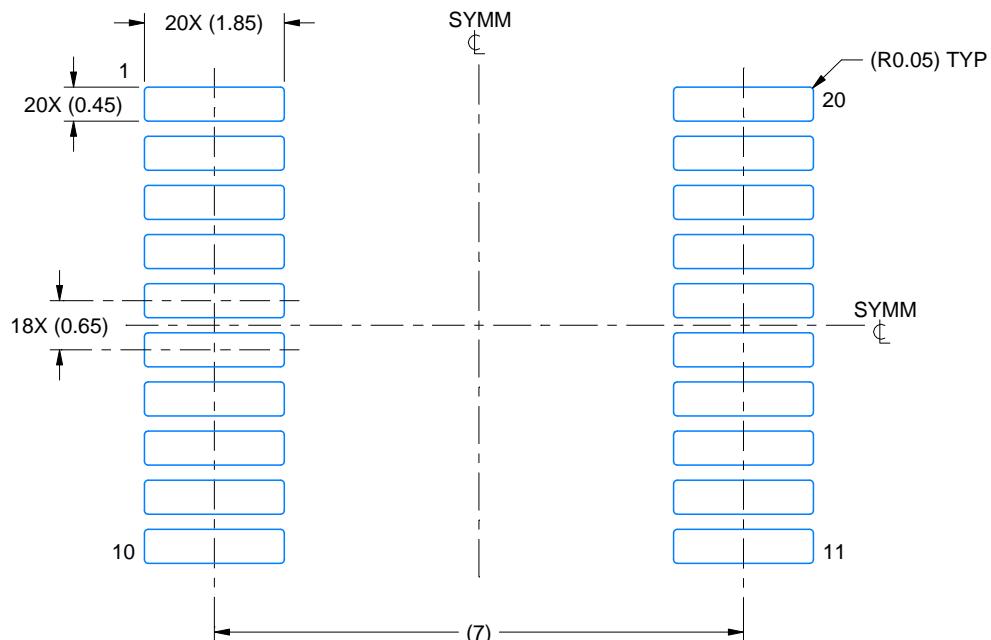
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

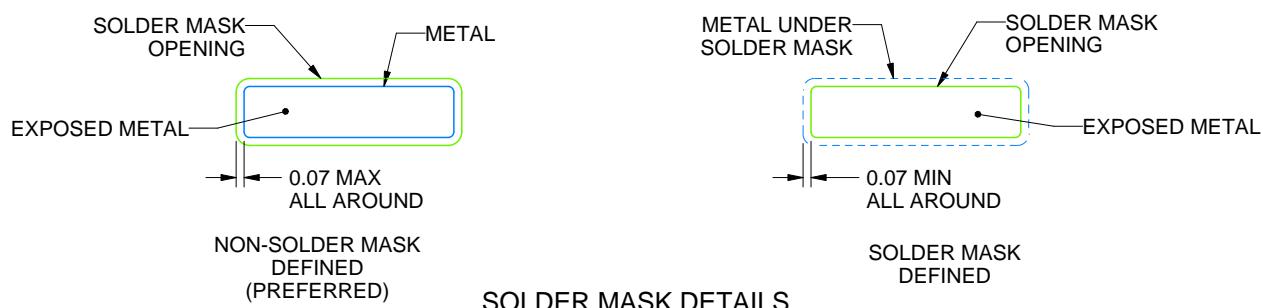
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

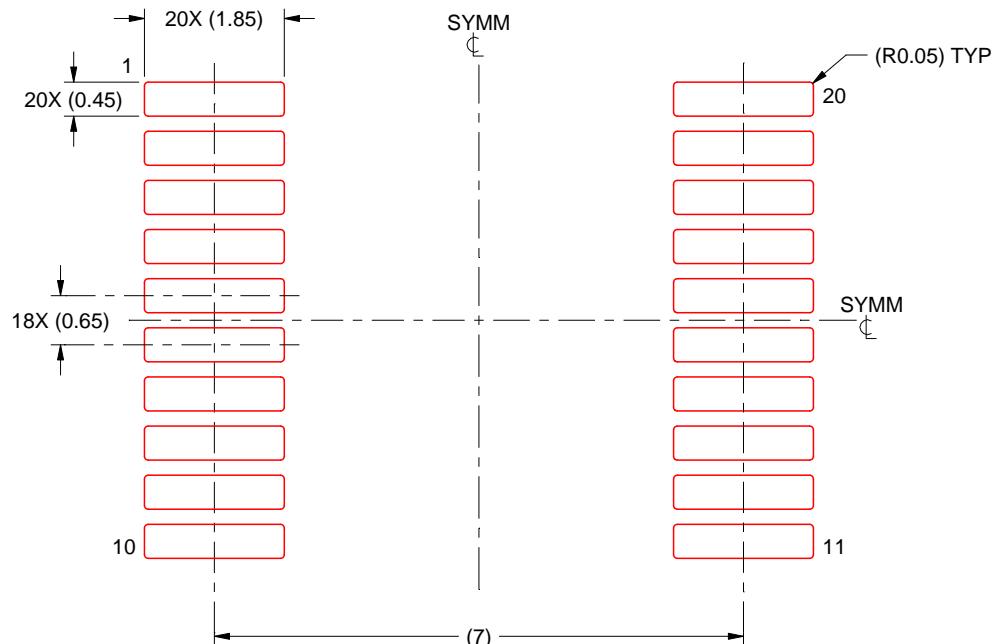
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

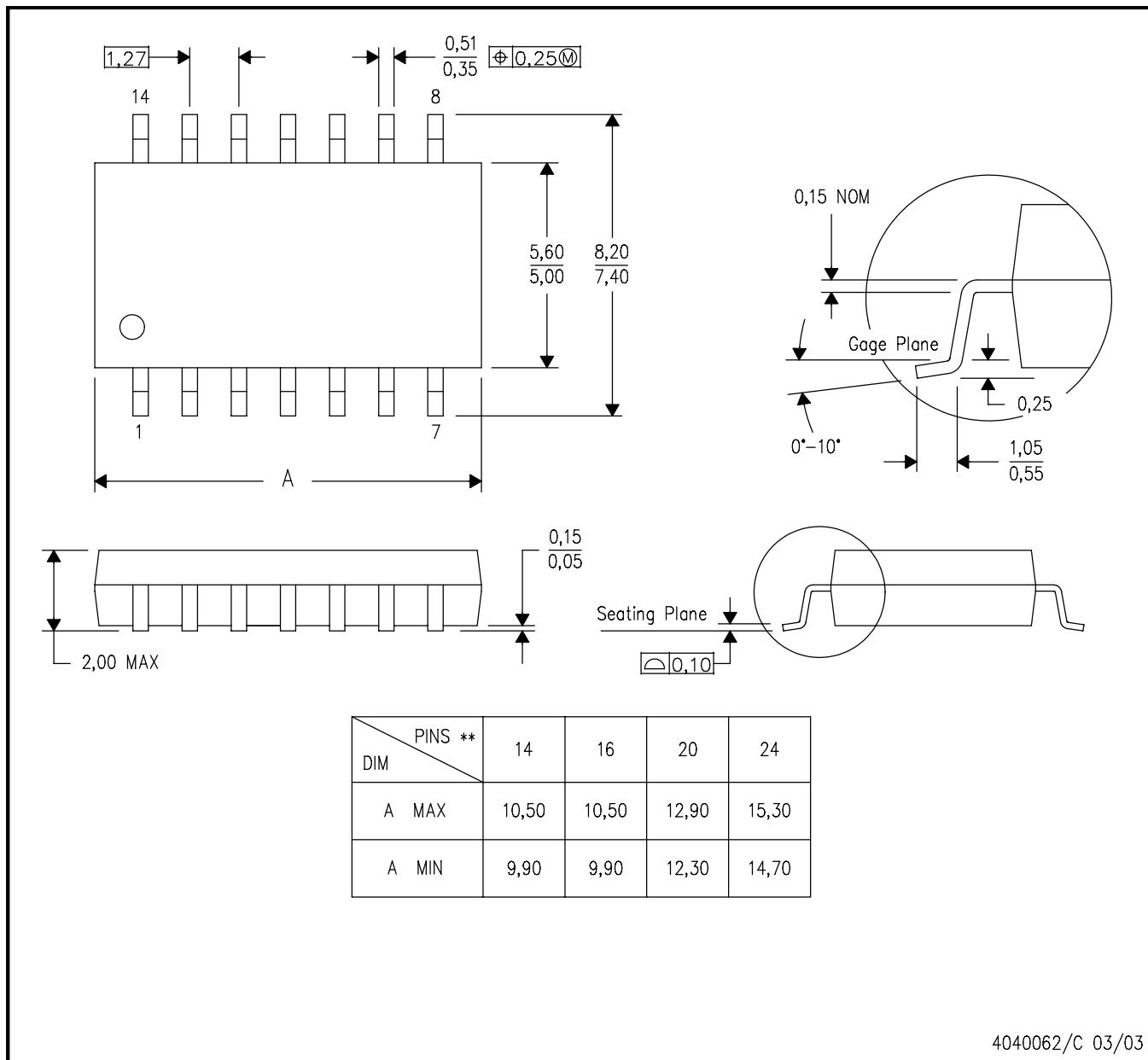
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

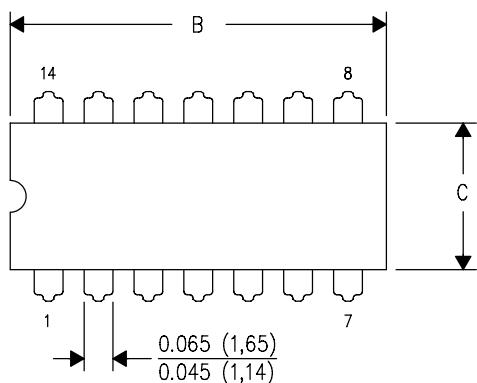


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

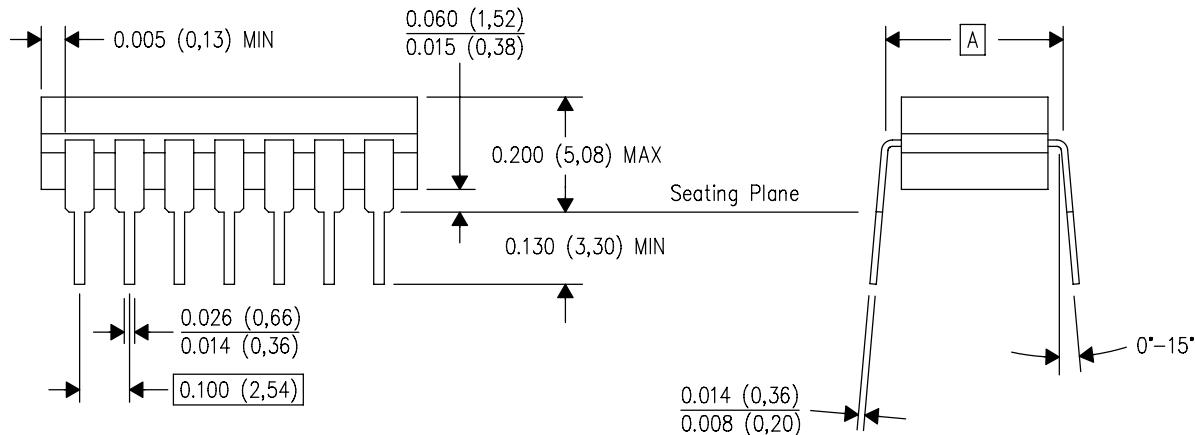
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **\nDIM | 14 | 16 | 18 | 20 |
|--------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



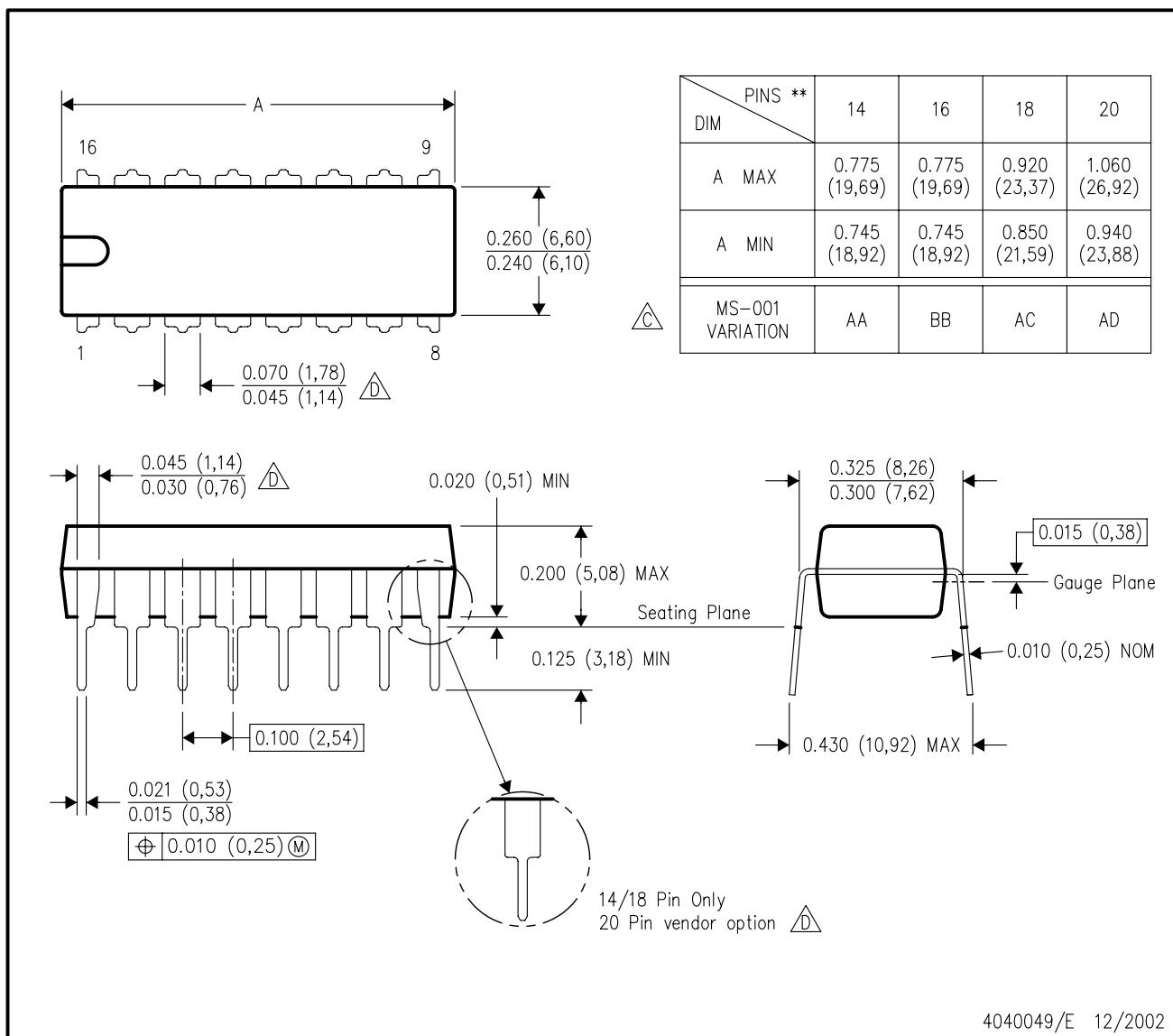
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



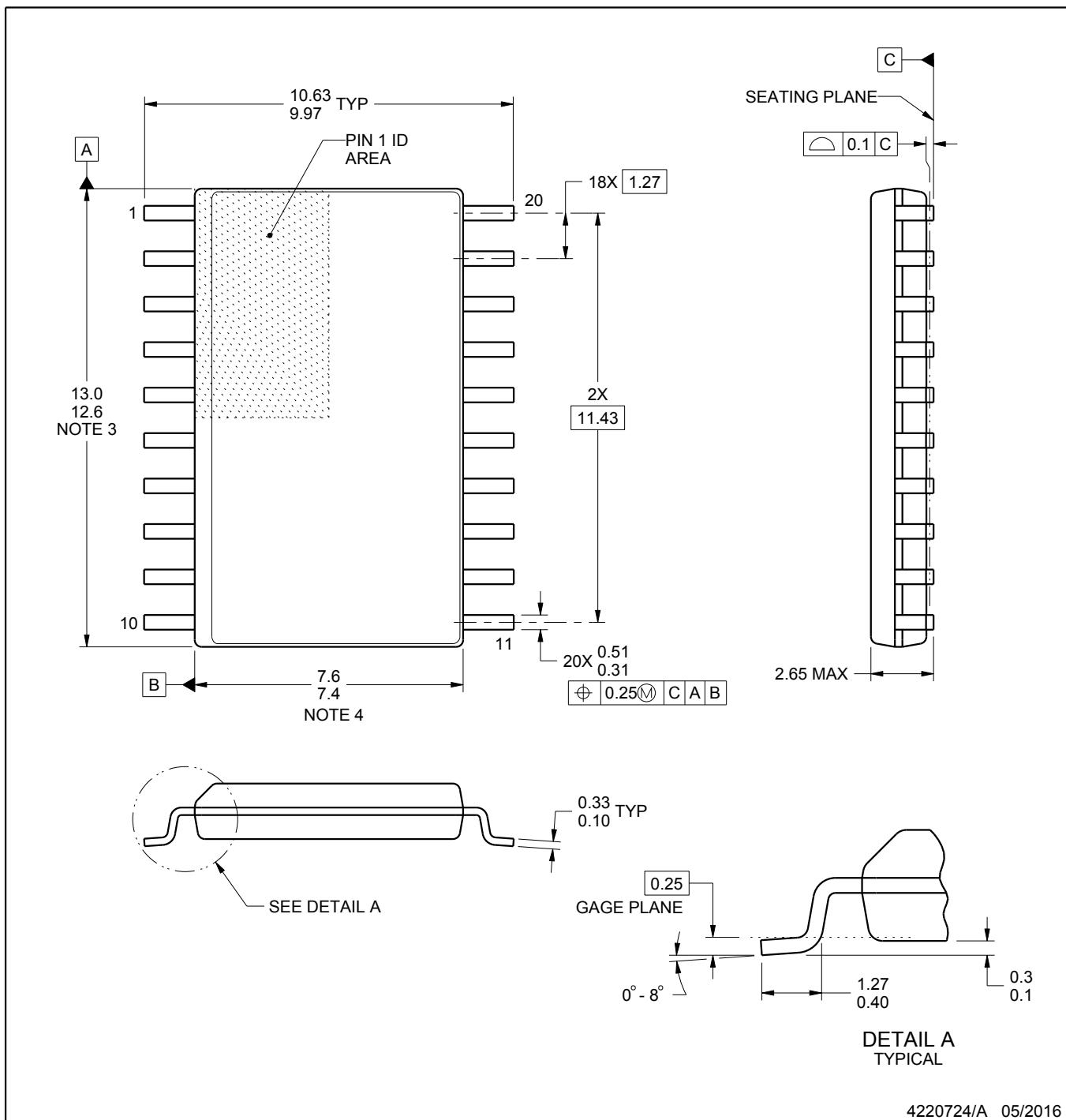
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

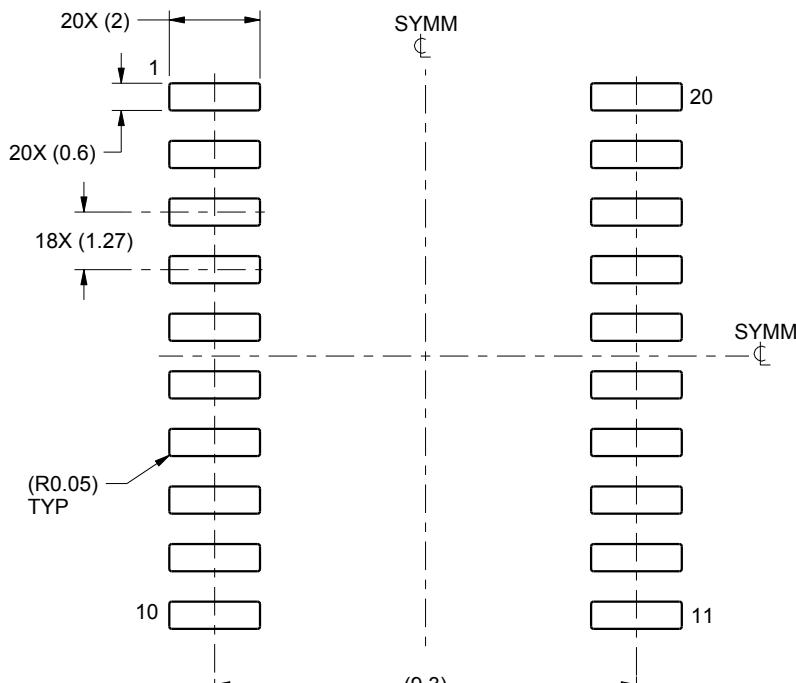
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

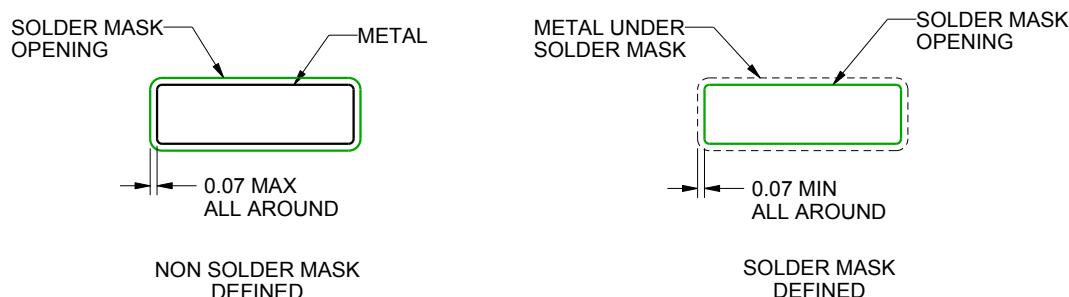
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

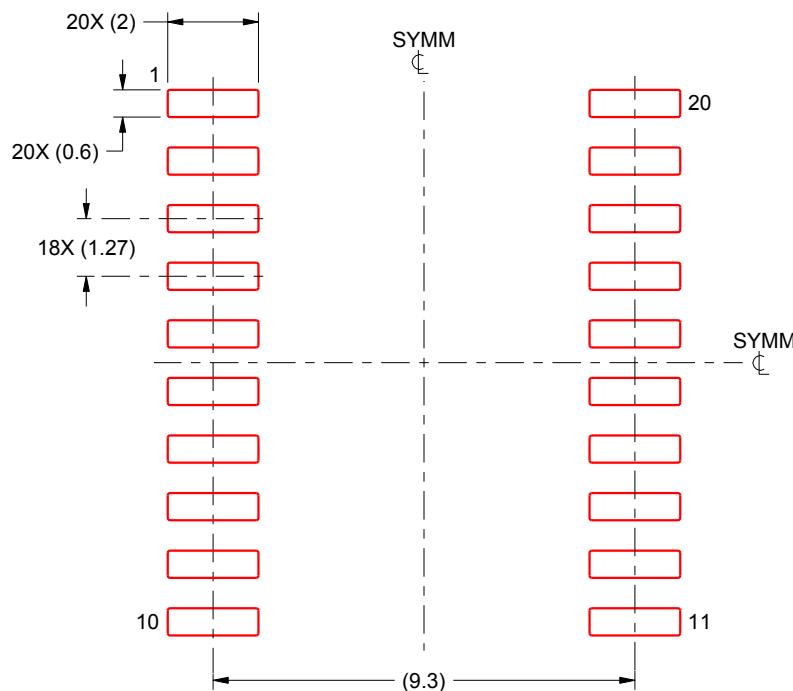
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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August 1986
Revised March 2000

DM74LS138 • DM74LS139 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
 - Memory decoders
 - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
 - DM74LS138 21 ns
 - DM74LS139 21 ns
- Typical power dissipation
 - DM74LS138 32 mW
 - DM74LS139 34 mW

Ordering Code:

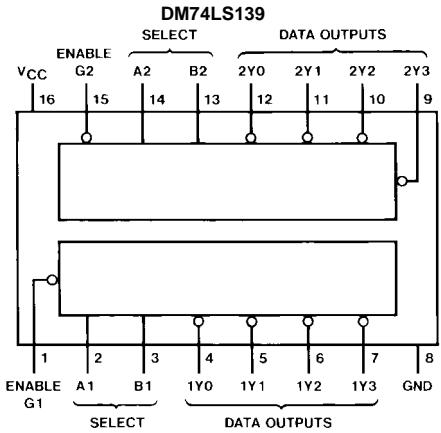
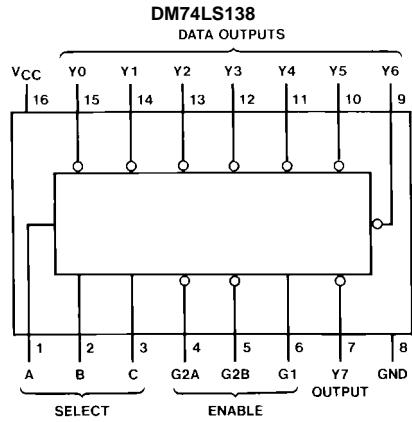
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| DM74LS138M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS138SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS138N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |
| DM74LS139M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS139SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS139N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

DM74LS138 • DM74LS139 Decoder/Demultiplexer

DM74LS138 • DM74LS139

Connection Diagrams



Function Tables

DM74LS138

| Inputs | | | Outputs | | | | | | | | | | |
|----------------|-------------------------|--------|---------|---|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Enable | | Select | C | B | A | Y ₀ | Y ₁ | Y ₂ | Y ₃ | Y ₄ | Y ₅ | Y ₆ | Y ₇ |
| G ₁ | G ₂ (Note 1) | | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | H | H | H | H | H | H | H | H | H | L |

DM74LS139

| Inputs | | | Outputs | | | |
|--------|---|--------|----------------|----------------|----------------|----------------|
| Enable | | Select | Y ₀ | Y ₁ | Y ₂ | Y ₃ |
| G | B | A | H | H | H | H |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = HIGH Level

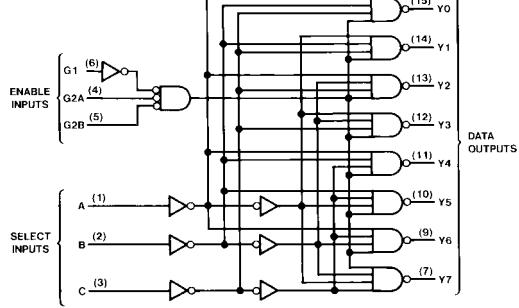
L = LOW Level

X = Don't Care

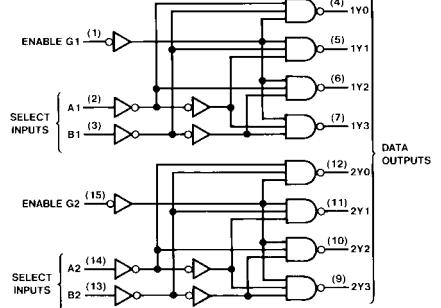
Note 1: G₂ = G_{2A} + G_{2B}

Logic Diagrams

DM74LS138



DM74LS139



Absolute Maximum Ratings (Note 2)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS138 Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-----------------|--------------------------------|------|-----|------|-------|
| V _{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} | HIGH Level Input Voltage | 2 | | | V |
| V _{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I _{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I _{OL} | LOW Level Output Current | | | 8 | mA |
| T _A | Free Air Operating Temperature | 0 | | 70 | °C |

DM74LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 3) | Max | Units |
|-----------------|-----------------------------------|--|-----|-----------------|-------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -18 mA | | | -1.5 | V |
| V _{OH} | HIGH Level Output Voltage | V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min | 2.7 | 3.4 | | V |
| V _{OL} | LOW Level Output Voltage | V _{CC} = Min, I _{OL} = Max, V _{IL} = Max, V _{IH} = Min | | 0.35 | 0.5 | V |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 7V | | | 0.1 | mA |
| I _{IH} | HIGH Level Input Current | V _{CC} = Max, V _I = 2.7V | | | 20 | µA |
| I _{IL} | LOW Level Input Current | V _{CC} = Max, V _I = 0.4V | | | -0.36 | mA |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 4) | -20 | | -100 | mA |
| I _{CC} | Supply Current | V _{CC} = Max (Note 5) | | 6.3 | 10 | mA |

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

| Symbol | Parameter | From (Input) To (Output) | Levels of Delay | R _L = 2 kΩ | | Units | |
|------------------|--|-----------------------------|--------------------|------------------------|-----|-------|--|
| | | | | C _L = 15 pF | | | |
| | | | | Min | Max | | |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Select to Output | 2 | | 18 | | |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Select to Output | 2 | | 27 | | |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Select to Output | 3 | | 18 | | |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Select to Output | 3 | | 27 | | |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Enable to Output | 2 | | 18 | | |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Enable to Output | 2 | | 24 | | |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Enable to Output | 3 | | 18 | | |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Enable to Output | 3 | | 28 | | |

DM74LS139 Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|----------|--------------------------------|------|-----|------|-------|
| V_{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I_{OL} | LOW Level Output Current | | | 8 | mA |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |

DM74LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 6) | Max | Units |
|----------|-----------------------------------|--|-----|-----------------|-------|-------|
| V_I | Input Clamp Voltage | $V_{CC} = \text{Min}$, $I_h = -18 \text{ mA}$ | | | -1.5 | V |
| V_{OH} | HIGH Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$, $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | 2.7 | 3.4 | | V |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ | | 0.35 | 0.5 | V |
| | | $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | | 0.25 | 0.4 | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}$, $V_I = 7V$ | | | 0.1 | mA |
| I_{IH} | HIGH Level Input Current | $V_{CC} = \text{Max}$, $V_I = 2.7V$ | | | 20 | μA |
| I_{IL} | LOW Level Input Current | $V_{CC} = \text{Max}$, $V_I = 0.4V$ | | | -0.36 | mA |
| I_{OS} | Short Circuit Output Current | $V_{CC} = \text{Max}$ (Note 7) | -20 | | -100 | mA |
| I_{CC} | Supply Current | $V_{CC} = \text{Max}$ (Note 8) | | 6.8 | 11 | mA |

Note 6: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

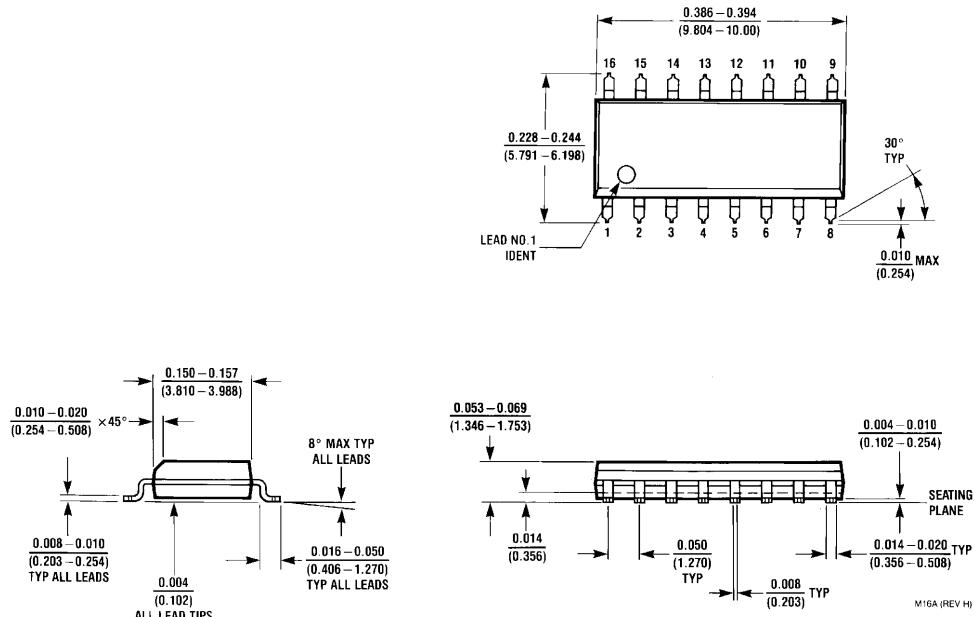
Note 8: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS139 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2 \text{ k}\Omega$ | | | | Units | |
|-----------|--|-----------------------------|---------------------------|-----|-----------------------|-----|-------|--|
| | | | $C_L = 15 \text{ pF}$ | | $C_L = 50 \text{ pF}$ | | | |
| | | | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Select to Output | | 18 | | 27 | ns | |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Select to Output | | 27 | | 40 | ns | |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Enable to Output | | 18 | | 27 | ns | |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Enable to Output | | 24 | | 40 | ns | |

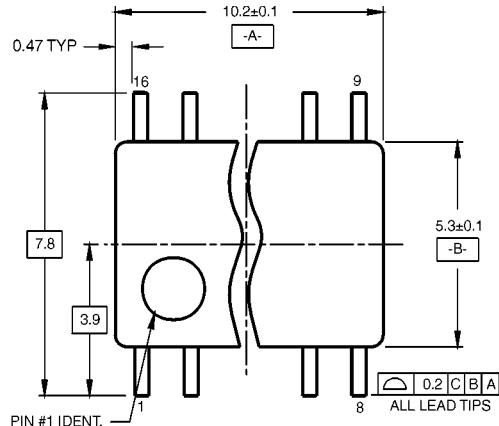
Physical Dimensions inches (millimeters) unless otherwise noted



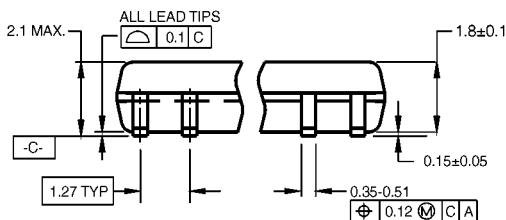
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

DM74LS138 • DM74LS139

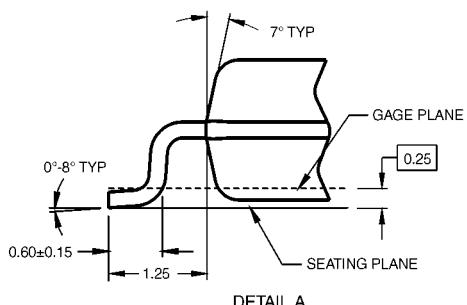
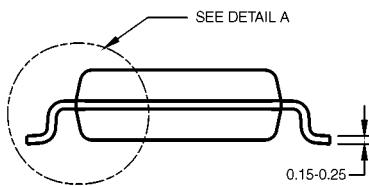
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



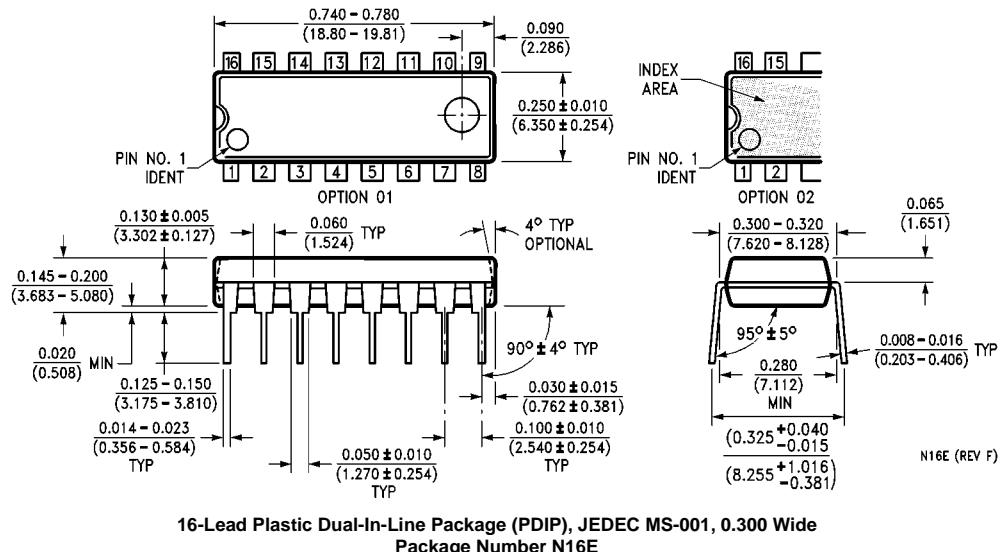
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K x 8 BIT)

IDT6116SA
IDT6116LA

FEATURES:

- High-speed access and chip select times
 - Military: 20/25/35/45/55/70/90/120/150ns (max.)
 - Commercial: 15/20/25/35/45ns (max.)
- Low-power consumption
- Battery backup operation
 - 2V data retention voltage (LA version only)
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip and 24-pin SOIC and 24-pin SOJ
- Military product compliant to MIL-STD-833, Class B

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

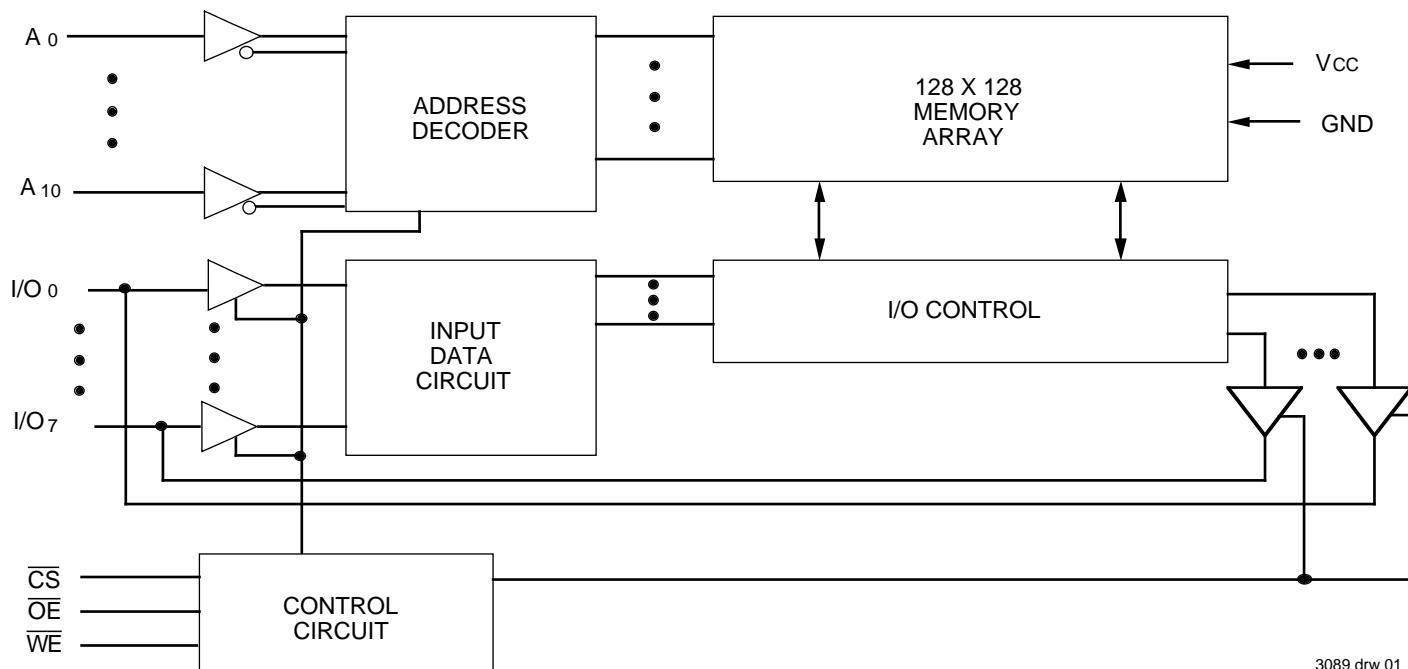
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When CS goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as CS remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1 μ W to 4 μ W operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP and a 24-lead gull-wing SOIC, and a 24-lead J-bend SOJ providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

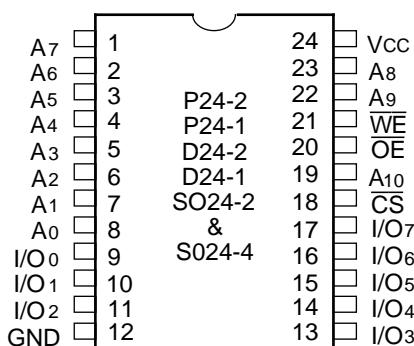


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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MARCH 1996

PIN CONFIGURATIONS



3089 drw 02

DIP/SOIC/SOJ
TOP VIEW

PIN DESCRIPTIONS

| | |
|------------------------------------|-------------------|
| A ₀ -A ₁₃ | Address Inputs |
| I/O ₀ -I/O ₇ | Data Input/Output |
| CS | Chip Select |
| WE | Write Enable |
| OE | Output Enable |
| VCC | Power |
| GND | Ground |

3089 tbl 01

TRUTH TABLE⁽¹⁾

| Mode | CS | OE | WE | I/O |
|---------|----|----|----|---------|
| Standby | H | X | X | High-Z |
| Read | L | L | H | DATAOUT |
| Read | L | H | H | High-Z |
| Write | L | X | L | DATAIN |

NOTE:

3089 tbl 02

1. H = VIH, L = Vil, X = Don't Care.

CAPACITANCE (TA = +25°C, F = 1.0 MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 8 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 0V | 8 | pF |

NOTE:

3089 tbl 03

- This parameter is determined by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Commercial | Military | Unit |
|----------------------|--------------------------------------|---------------|--------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to + 7.0 | -0.5 to +7.0 | V |
| T _A | Operating Temperature | 0 to + 70 | -55 to +125 | °C |
| T _{BIAZ} | Temperature Under Bias | -55 to + 125 | -65 to +135 | °C |
| T _{TSG} | Storage Temperature | -55 to + 125 | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | 50 | mA |

NOTES:

3089 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. VTERM must not exceed Vcc +0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | VCC |
|------------|---------------------|-----|------------|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

3089 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|--------------------|---------------------|------|--------------------|------|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 ⁽²⁾ | V |
| GND | Supply Ground | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | 3.5 | Vcc +0.5 | V |
| VIL | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

NOTES:

3089 tbl 06

1. VIL (min.) = -3.0V for pulse width less than 20ns, once per cycle.
2. VIN must not exceed Vcc +0.5V.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

| Symbol | Parameter | Test Conditions | IDT6116SA | | IDT6116LA | | Unit | |
|--------|------------------------|---|----------------|--------|-----------|--------|--------|----|
| | | | Min. | Max. | Min. | Max. | | |
| ILI | Input Leakage Current | Vcc = Max., VIN = GND to Vcc | MIL. COM'L. | — — | 10 5 | — — | 5 2 | µA |
| ILO | Output Leakage Current | Vcc = Max. CS = VIH, VOUT = GND to Vcc | MIL. COM'L. | — — | 10 5 | — — | 5 2 | µA |
| VOL | Output Low Voltage | IOL = 8mA, Vcc = Min. | — | 0.4 | — | 0.4 | V | |
| VOH | Output High Voltage | IOH = -4mA, Vcc = Min. | 2.4 | — | 2.4 | — | V | |

3089 tbl 07

DC ELECTRICAL CHARACTERISTICS ⁽¹⁾

VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V

| Symbol | Parameter | Power | 6116SA15 ⁽²⁾ | | 6116SA20 | | 6116SA25 | | 6116SA35 | | Unit |
|--------|--|-------|-------------------------|------|----------|------|----------|------|----------|------|------|
| | | | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | |
| Icc1 | Operating Power Supply Current, CS ≤ VIL, Outputs Open, Vcc = Max., f = 0 | SA | 105 | — | 105 | 130 | 80 | 90 | 80 | 90 | mA |
| | | LA | 95 | — | 95 | 120 | 75 | 85 | 75 | 85 | |
| Icc2 | Dynamic Operating Current, CS ≤ VIL, Vcc = Max., Outputs Open, f = fMAX ⁽⁴⁾ | SA | 150 | — | 130 | 150 | 120 | 135 | 100 | 115 | mA |
| | | LA | 140 | — | 120 | 140 | 110 | 125 | 95 | 105 | |
| Isb | Standby Power Supply Current (TTL Level) CS ≥ VIH, Vcc = Max., Outputs Open, f = fMAX ⁽⁴⁾ | SA | 40 | — | 40 | 50 | 40 | 45 | 25 | 35 | mA |
| | | LA | 35 | — | 35 | 45 | 35 | 40 | 25 | 30 | |
| Isb1 | Full Standby Power Supply Current (CMOS Level), CS ≥ VHC, Vcc = Max., VIN ≥ VHC or VIN ≤ VLC, f = 0 | SA | 2 | — | 2 | 10 | 2 | 10 | 2 | 10 | mA |
| | | LA | 0.1 | — | 0.1 | 0.9 | 0.1 | 0.9 | 0.1 | 0.9 | |

NOTES:

3089 tbl 08

1. All values are maximum guaranteed values.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. fMAX = 1/tRC, only address inputs are cycling at fMAX, f = 0 means address inputs are not changing.

DC ELECTRICAL CHARACTERISTICS ⁽¹⁾ (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

| Symbol | Parameter | Power | 6116SA45 6116LA45 | | 6116SA55 ⁽³⁾ 6116LA55 ⁽³⁾ | | 6116SA70 ⁽³⁾ 6116LA70 ⁽³⁾ | | 6116SA90 ⁽³⁾ 6116LA90 ⁽³⁾ | | 6116SA120 ⁽³⁾ 6116LA120 ⁽³⁾ | | 6116SA150 ⁽³⁾ 6116LA150 ⁽³⁾ | | Unit |
|------------------|--|-------|----------------------|------|--|------|--|------|--|------|--|------|--|------|------|
| | | | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | |
| I _{CC1} | Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V _{CC} = Max., f = 0 | SA | 80 | 90 | — | 90 | — | 90 | — | 90 | — | 90 | — | 90 | mA |
| | | LA | 75 | 85 | — | 85 | — | 85 | — | 85 | — | 85 | — | 85 | mA |
| I _{CC2} | Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽⁴⁾ | SA | 100 | 100 | — | 100 | — | 100 | — | 100 | — | 100 | — | 90 | mA |
| | | LA | 90 | 95 | — | 90 | — | 90 | — | 85 | — | 85 | — | 85 | mA |
| I _{SB} | Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽⁴⁾ | SA | 25 | 25 | — | 25 | — | 25 | — | 25 | — | 25 | — | 25 | mA |
| | | LA | 20 | 20 | — | 20 | — | 20 | — | 25 | — | 15 | — | 15 | mA |
| I _{SB1} | Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 | SA | 2 | 10 | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | mA |
| | | LA | 0.1 | 0.9 | — | 0.9 | — | 0.9 | — | 0.9 | — | 0.9 | — | 0.9 | mA |

NOTES:

1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}, only address inout are toggling at f_{MAX}, f = 0 means address inputs are not changing.

3089 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

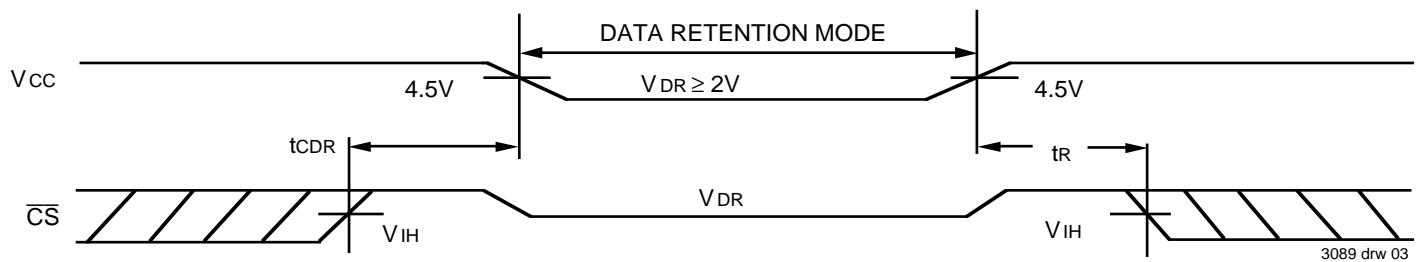
| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | | Max. | | Unit |
|---------------------------------|--------------------------------------|---------------------------------------|--------|--------------------------------|---------------------|------|-----------------|------|------|
| | | | | | V _{CC} | 2.0V | V _{CC} | 2.0V | |
| V _{DR} | V _{CC} for Data Retention | — | | 2.0 | — | — | — | — | V |
| I _{CCDR} | Data Retention Current | $\overline{CS} \geq V_{HC}$ | MIL. | — | 0.5 | 1.5 | 200 | 300 | μA |
| | | | COM'L. | — | 0.5 | 1.5 | 20 | 30 | |
| t _{CDR} ⁽³⁾ | Data Deselect to Data Retention Time | $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | | — | 0 | — | — | — | ns |
| t _R ⁽³⁾ | Operation Recovery Time | | | t _{RC} ⁽²⁾ | — | — | — | — | ns |
| I _{LI} | Input Leakage Current | | | — | — | — | 2 | 2 | μA |

NOTES:

1. TA = + 25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

3089 tbl 10

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

3089 tbl 11

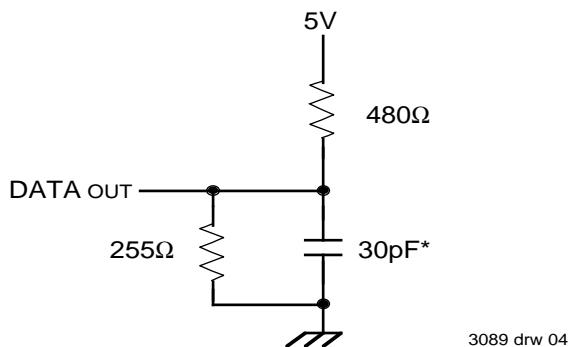


Figure 1. AC Test Load

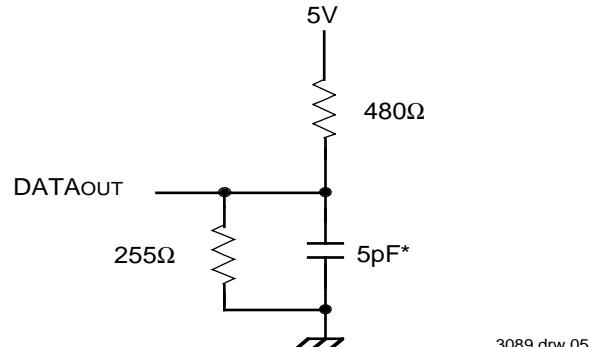


Figure 2. AC Test Load
(for t_{OLZ} , t_{CLZ} , t_{OHZ} ,
 t_{WHZ} , t_{CHZ} & t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 6116SA15 ⁽¹⁾ 6116LA15 ⁽¹⁾ | | 6116SA20 6116LA20 | | 6116SA25 6116LA25 | | 6116SA35 6116LA35 | | Unit |
|----------------------------------|------------------------------------|--|------|----------------------|------|----------------------|------|----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t _{AA} | Address Access Time | — | 15 | — | 19 | — | 25 | — | 35 | ns |
| t _{TCS} | Chip Select Access Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| t _{TCLZ} ⁽³⁾ | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OE} | Output Enable to Output Valid | — | 10 | — | 10 | — | 13 | — | 20 | ns |
| t _{TOLZ} ⁽³⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 5 | — | 5 | — | ns |
| t _{TCHZ} ⁽³⁾ | Chip Deselect to Output in High-Z | — | 10 | — | 11 | — | 12 | — | 15 | ns |
| t _{TOHZ} ⁽³⁾ | Output Disable to Output in High-Z | — | 8 | — | 8 | — | 10 | — | 13 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{TPU} ⁽³⁾ | Chip Select to Power-Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{TPD} ⁽³⁾ | Chip Deselect to Power-Down Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |

3089 tbl 12

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges) (Continued)

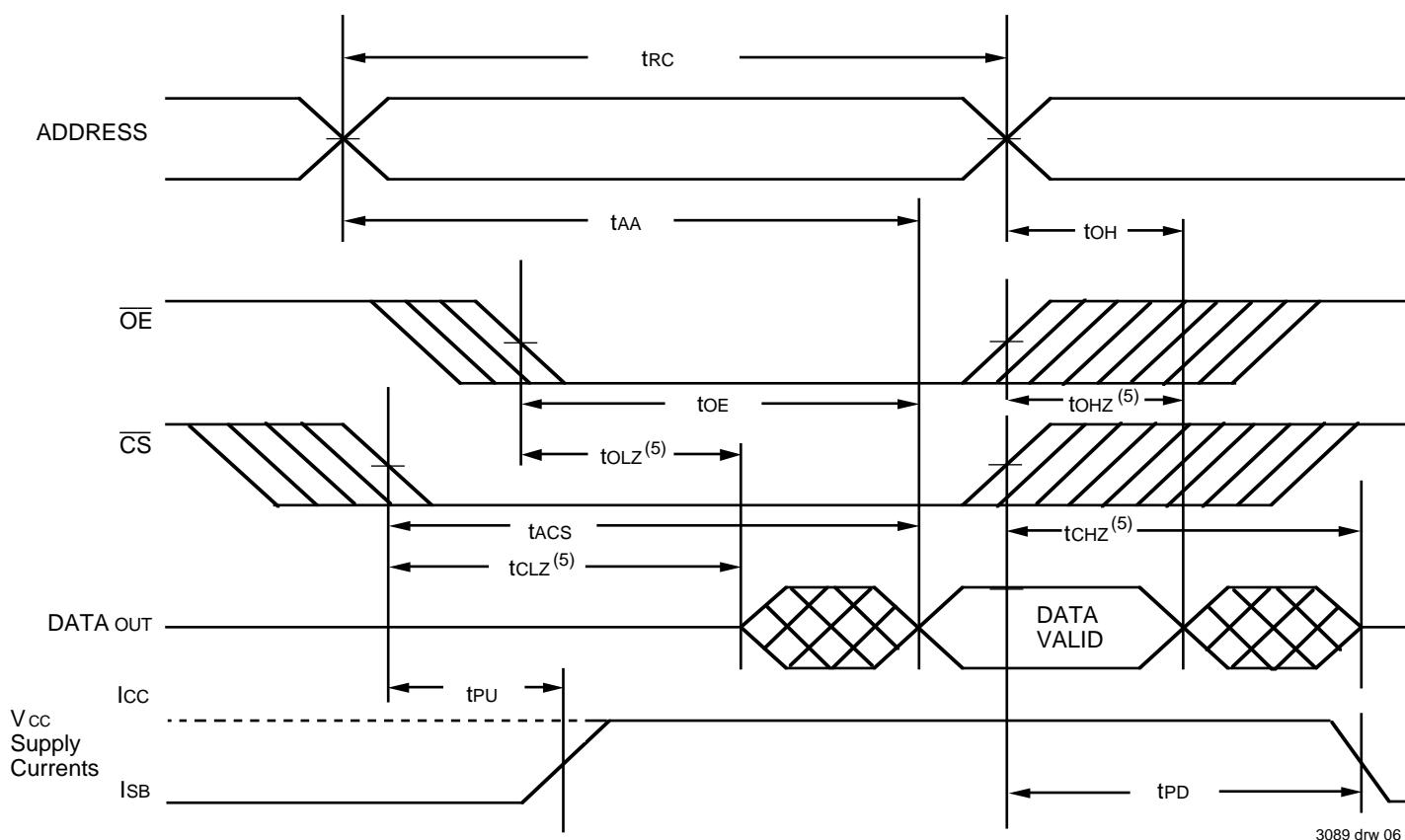
| Symbol | Parameter | 6116SA45 6116LA45 | | 6116SA55 ⁽²⁾ 6116LA55 ⁽²⁾ | | 6116SA70 ⁽²⁾ 6116LA70 ⁽²⁾ | | 6116SA90 ⁽²⁾ 6116LA90 ⁽²⁾ | | 6116SA120 ⁽²⁾ 6116LA120 ⁽²⁾ | | 6116SA150 ⁽²⁾ 6116LA150 ⁽²⁾ | | Unit |
|----------------------------------|------------------------------------|----------------------|------|--|------|--|------|--|------|--|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 45 | — | 55 | — | 70 | — | 90 | — | 120 | — | 150 | — | ns |
| t _{AA} | Address Access Time | — | 45 | — | 55 | — | 70 | — | 90 | — | 120 | — | 150 | ns |
| t _{TCS} | Chip Select Access Time | — | 45 | — | 50 | — | 65 | — | 90 | — | 120 | — | 150 | ns |
| t _{TCLZ} ⁽³⁾ | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OE} | Output Enable to Output Valid | — | 25 | — | 40 | — | 50 | — | 60 | — | 80 | — | 100 | ns |
| t _{TOLZ} ⁽³⁾ | Output Enable to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{TCHZ} ⁽³⁾ | Chip Deselect to Output in High-Z | — | 20 | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | ns |
| t _{TOHZ} ⁽³⁾ | Output Disable to Output in High-Z | — | 15 | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |

NOTES:

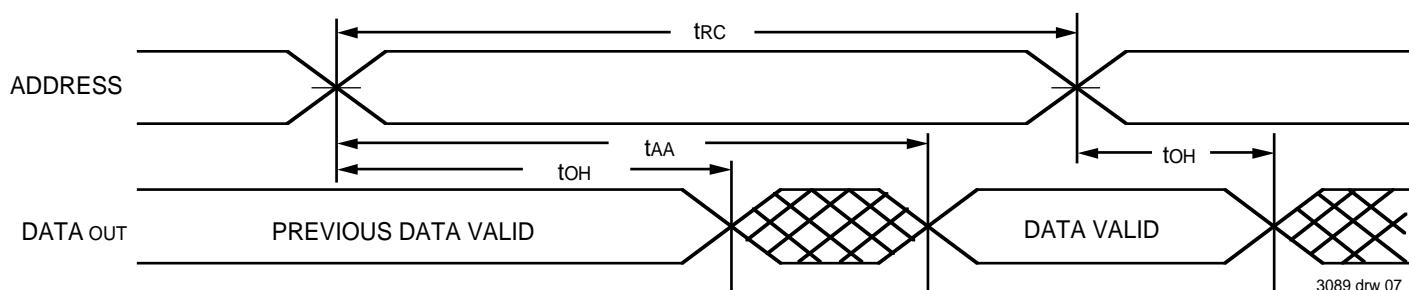
1. 0°C to + 70°C temperature range only.
2. -55°C to + 125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3089 tbl 13

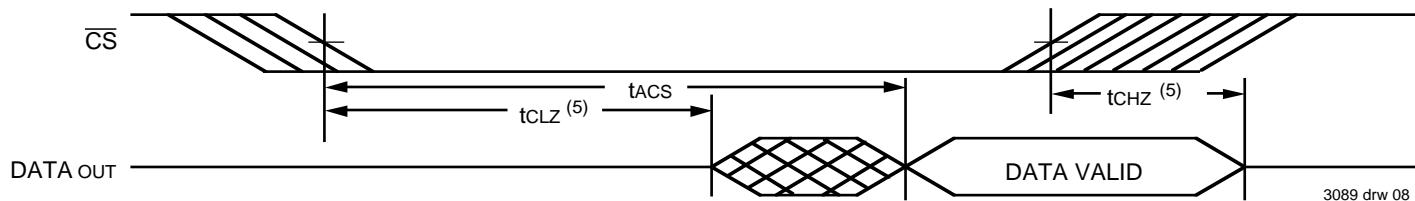
TIMING WAVEFORM OF READ CYCLE NO. 1^(1, 3)



TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)



NOTES:

1. $\overline{\text{WE}}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{\text{CS}}$ is LOW.
3. Address valid prior to or coincident with $\overline{\text{CS}}$ transition LOW.
4. $\overline{\text{OE}}$ is LOW.
5. Transition is measured $\pm 500\text{mV}$ from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 6116SA15 ⁽¹⁾ 6116LA15 ⁽¹⁾ | | 6116SA20 6116LA20 | | 6116SA25 6116LA25 | | 6116SA35 6116LA35 | | Unit |
|----------------------------------|---------------------------------|--|------|----------------------|------|----------------------|------|----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t _{CW} | Chip Select to End-of-Write | 13 | — | 15 | — | 17 | — | 25 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 14 | — | 15 | — | 17 | — | 25 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 12 | — | 12 | — | 15 | — | 20 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WHZ} ⁽³⁾ | Write to Output in High-Z | — | 7 | — | 8 | — | 16 | — | 20 | ns |
| t _{DW} | Data to Write Time Overlap | 12 | — | 12 | — | 13 | — | 15 | — | ns |
| t _{DH} ⁽⁴⁾ | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ^(3,4) | Output Active from End-of-Write | 0 | — | 0 | — | 0 | — | 0 | — | ns |

3089 tbl 14

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

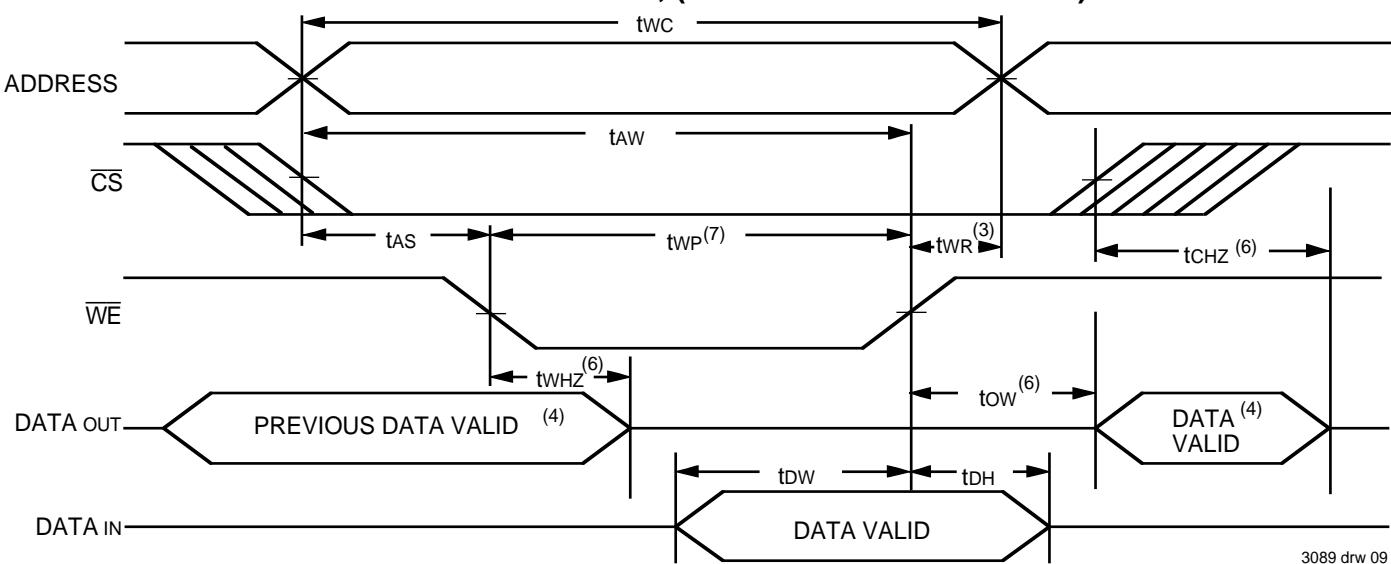
| Symbol | Parameter | 6116SA45 6116LA45 | | 6116SA55 ⁽²⁾ 6116LA55 ⁽²⁾ | | 6116SA70 ⁽²⁾ 6116LA70 ⁽²⁾ | | 6116SA90 ⁽²⁾ 6116LA90 ⁽²⁾ | | 6116SA120 ⁽²⁾ 6116LA120 ⁽²⁾ | | 6116SA150 ⁽²⁾ 6116LA150 ⁽²⁾ | | Unit |
|----------------------------------|---------------------------------|----------------------|------|--|------|--|------|--|------|--|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 45 | — | 55 | — | 70 | — | 90 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Select to End of Write | 30 | — | 40 | — | 40 | — | 55 | — | 70 | — | 90 | — | ns |
| t _{AW} | Address Valid to End of Write | 30 | — | 45 | — | 65 | — | 80 | — | 105 | — | 120 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 5 | — | 15 | — | 15 | — | 20 | — | 20 | — | ns |
| t _{WP} | Write Pulse Width | 25 | — | 40 | — | 40 | — | 55 | — | 70 | — | 90 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 5 | — | 5 | — | 5 | — | 5 | — | 10 | — | ns |
| t _{WHZ} ⁽³⁾ | Write to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | ns |
| t _{DW} | Data to Write Time Overlap | 20 | — | 25 | — | 30 | — | 30 | — | 35 | — | 40 | — | ns |
| t _{DH} ⁽⁴⁾ | Data Hold from Write Time | 0 | — | 5 | — | 5 | — | 5 | — | 5 | — | 10 | — | ns |
| t _{OW} ^(3,4) | Output Active from End of Write | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |

NOTES:

3089 tbl 15

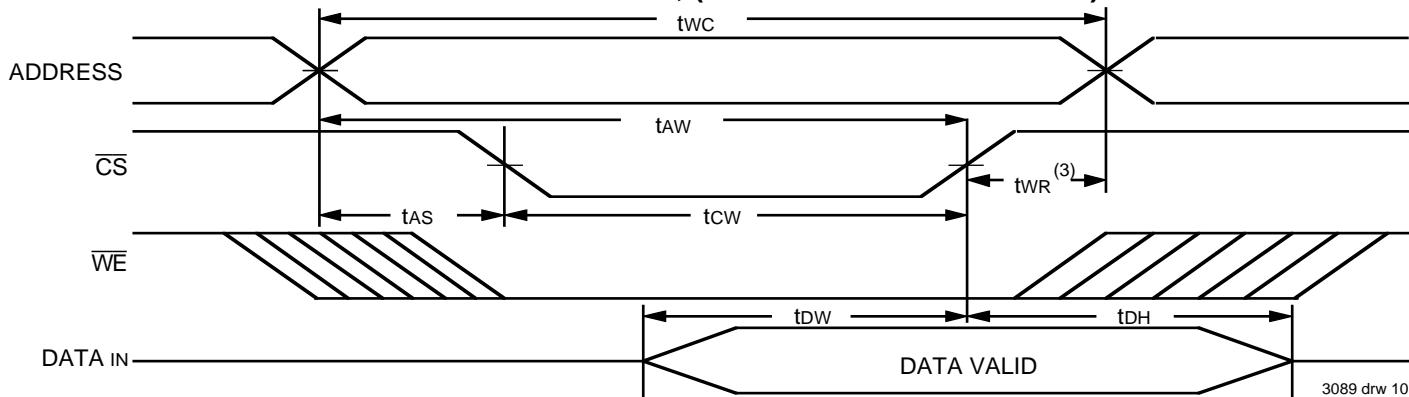
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and tow values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual tow.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (\overline{WE} CONTROLLED TIMING) (1, 2, 5, 7)



3089 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, (\overline{CS} CONTROLLED TIMING) (1, 2, 3, 5, 7)

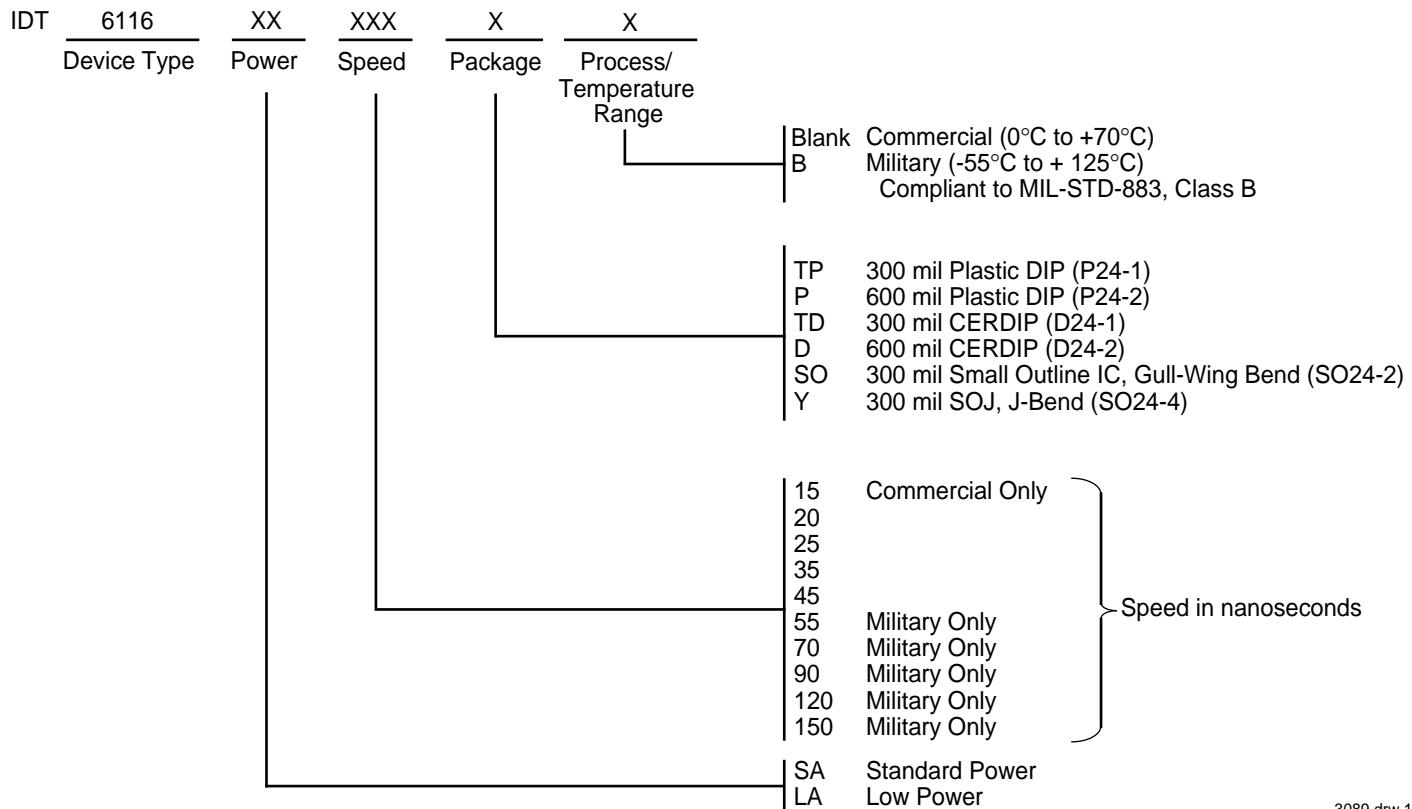


3089 drw 10

NOTES:

1. \overline{WE} or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
3. tWR is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state.
7. \overline{OE} is continuously HIGH. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse is the specified tWP. For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to tCW.

ORDERING INFORMATION



3089 drw 11

NMOS 32K (4K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- INPUTS and OUTPUTS TTL COMPATIBLE DURING READ and PROGRAM
- COMPLETELY STATIC

DESCRIPTION

The M2732A is a 32,768 bit UV erasable and electrically programmable memory EPROM. It is organized as 4,096 words by 8 bits. The M2732A with its single 5V power supply and with an access time of 200 ns, is ideal suited for applications where fast turn around and pattern experimentation one important requirements.

The M2732A is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be then written to the device by following the programming procedure.

Table 1. Signal Names

| | |
|----------------|--------------------------------|
| A0 - A11 | Address Inputs |
| Q0 - Q7 | Data Outputs |
| \bar{E} | Chip Enable |
| \bar{G}_{VP} | Output Enable / Program Supply |
| Vcc | Supply Voltage |
| Vss | Ground |

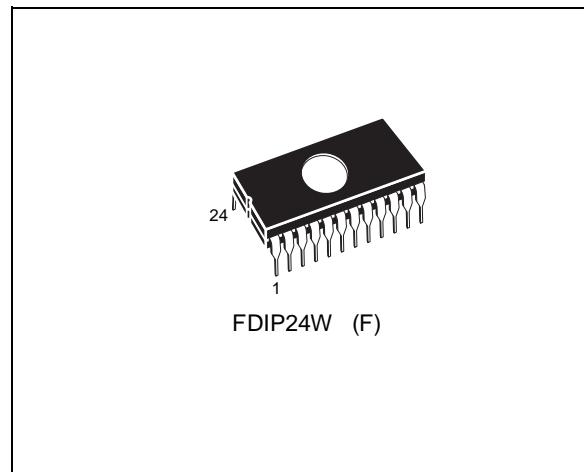


Figure 1. Logic Diagram

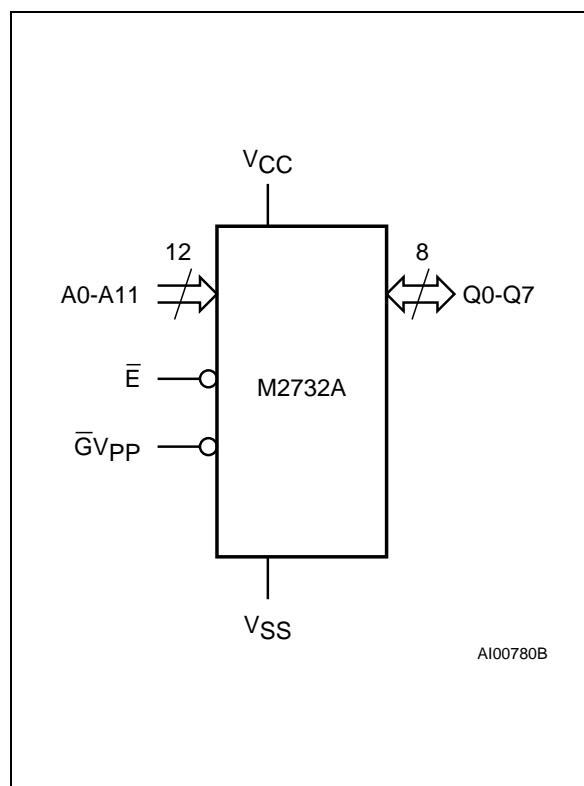
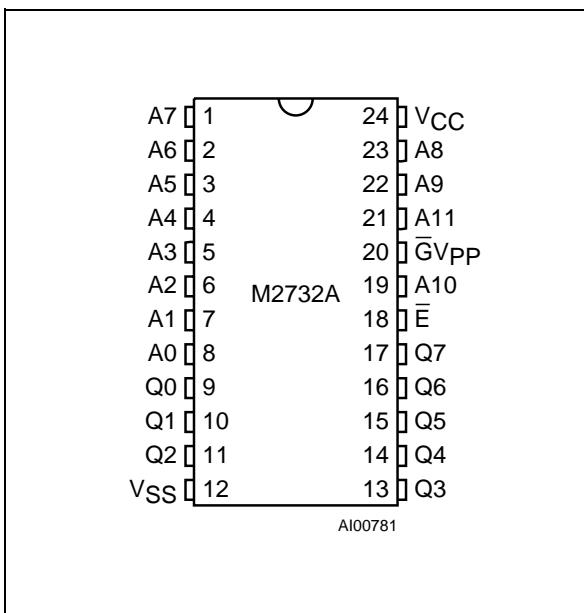


Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-------------------|-------------------------------|--------------------|---------------------------|
| T _A | Ambient Operating Temperature | grade 1 grade 6 | 0 to 70 -40 to 85 °C |
| T _{BIAS} | Temperature Under Bias | grade 1 grade 6 | -10 to 80 -50 to 95 °C |
| T _{STG} | Storage Temperature | | -65 to 125 °C |
| V _{IO} | Input or Output Voltages | | -0.6 to 6 V |
| V _{CC} | Supply Voltage | | -0.6 to 6 V |
| V _{PP} | Program Supply Voltage | | -0.6 to 22 V |

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections

DEVICE OPERATION

The six modes of operation for the M2732A are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL level except for V_{PP}.

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (\bar{E}) is the power control and should be used for device selection. Output Enable (\bar{G}) is the output control and should

be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVAQ}) is equal to the delay from \bar{E} to output (t_{ELQV}). Data is available at the outputs after the falling edge of \bar{G} , assuming that \bar{E} has been low and the addresses have been stable for at least $t_{AVQV}-t_{GLQV}$.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to \bar{E} input. When in standby mode, the outputs are in a high impedance state, independent of the \bar{GVPP} input.

Two Line Output Control

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that \bar{E} be decoded and used as the primary device selecting function, while \bar{G} should be made a common connection to all devices in the array and connected to the \bar{READ} line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Programming

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the \overline{GV}_{PP} input is at 21V. A $0.1\mu F$ capacitor must be placed across \overline{GV}_{PP} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50ms, active low, TTL program pulse is applied to the \overline{E} input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55ms. The M2732A must not be programmed with a DC signal applied to the \overline{E} input.

Programming of multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the \overline{E} input programs the paralleled 2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for \overline{E} , all like inputs (including \overline{GV}_{PP}) of the parallel M2732As may be common. A TTL level program

pulse applied to a M2732A's \overline{E} input with \overline{GV}_{PP} at 21V will program that M2732A. A high level \overline{E} input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is carried out with \overline{GV}_{PP} and E at V_{IL} .

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 $\mu W/cm^2$ power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 3. Operating Modes

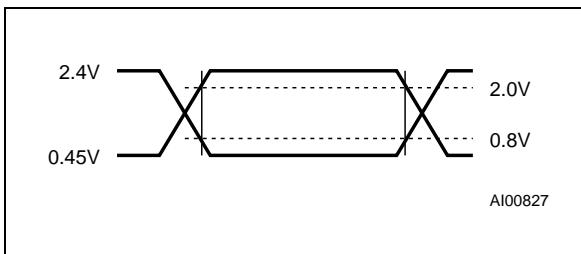
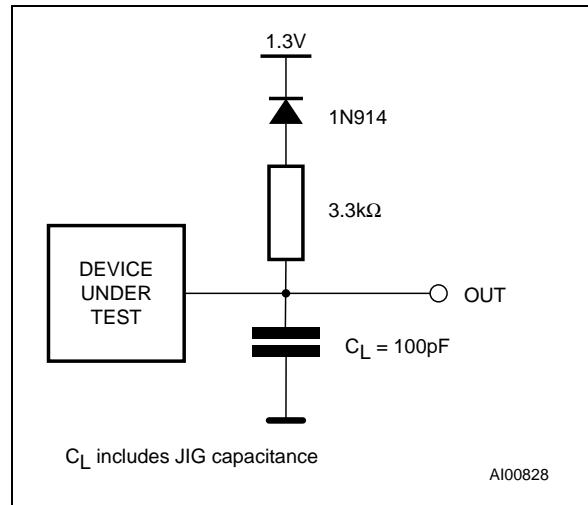
| Mode | \overline{E} | \overline{GV}_{PP} | V_{CC} | $Q_0 - Q_7$ |
|-----------------|----------------|----------------------|----------|-------------|
| Read | V_{IL} | V_{IL} | V_{CC} | Data Out |
| Program | V_{IL} Pulse | V_{PP} | V_{CC} | Data In |
| Verify | V_{IL} | V_{IL} | V_{CC} | Data Out |
| Program Inhibit | V_{IH} | V_{PP} | V_{CC} | Hi-Z |
| Standby | V_{IH} | X | V_{CC} | Hi-Z |

Note: X = V_{IH} or V_{IL} .

AC MEASUREMENT CONDITIONS

| | |
|---------------------------------------|--------------------|
| Input Rise and Fall Times | $\leq 20\text{ns}$ |
| Input Pulse Voltages | 0.45V to 2.4V |
| Input and Output Timing Ref. Voltages | 0.8V to 2.0V |

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms**Figure 4. AC Testing Load Circuit****Table 4. Capacitance ⁽¹⁾ ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|-----------|---|-----------------------|-----|-----|------|
| C_{IN} | Input Capacitance (except $\bar{G}V_{PP}$) | $V_{IN} = 0\text{V}$ | | 6 | pF |
| C_{IN1} | Input Capacitance ($\bar{G}V_{PP}$) | $V_{IN} = 0\text{V}$ | | 20 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0\text{V}$ | | 12 | pF |

Note: 1. Sampled only, not 100% tested.

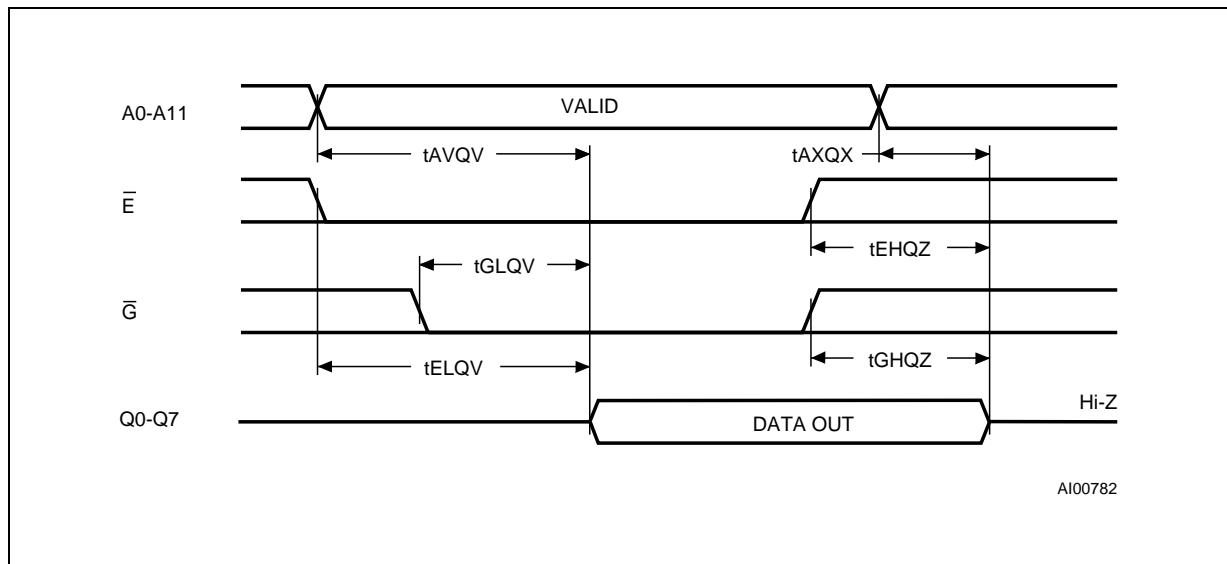
Figure 5. Read Mode AC Waveforms

Table 5. Read Mode DC Characteristics⁽¹⁾

(TA = 0 to 70 °C or -40 to 85 °C; VCC = 5V ± 5% or 5V ± 10%; VPP = VCC)

| Symbol | Parameter | Test Condition | Value | | Unit |
|------------------|--------------------------|---|-------|---------------------|------|
| | | | Min | Max | |
| I _{LI} | Input Leakage Current | 0 ≤ V _{IN} ≤ V _{CC} | | ±10 | µA |
| I _{LO} | Output Leakage Current | V _{OUT} = V _{CC} | | ±10 | µA |
| I _{CC} | Supply Current | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | | 125 | mA |
| I _{CC1} | Supply Current (Standby) | $\bar{E} = V_{IH}$, $\bar{G} = V_{IL}$ | | 35 | mA |
| V _{IL} | Input Low Voltage | | -0.1 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2 | V _{CC} + 1 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1mA | | 0.45 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400µA | 2.4 | | V |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics⁽¹⁾

(TA = 0 to 70 °C or -40 to 85 °C; VCC = 5V ± 5% or 5V ± 10%; VPP = VCC)

| Symbol | Alt | Parameter | Test Condition | M2732A | | | | | | | | Unit | |
|----------------------------------|------------------|---|---|---------|-----|------------|-----|-----|-----|-----|-----|------|--|
| | | | | -2, -20 | | blank, -25 | | -3 | | -4 | | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| t _{AVQV} | t _{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | | 200 | | 250 | | 300 | | 450 | ns | |
| t _{ELQV} | t _{CCE} | Chip Enable Low to Output Valid | $\bar{G} = V_{IL}$ | | 200 | | 250 | | 300 | | 450 | ns | |
| t _{GLQV} | t _{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 100 | | 100 | | 150 | | 150 | ns | |
| t _{EHQZ} ⁽²⁾ | t _{DF} | Chip Enable High to Output Hi-Z | $\bar{G} = V_{IL}$ | 0 | 60 | 0 | 60 | 0 | 130 | 0 | 130 | ns | |
| t _{GHQZ} ⁽²⁾ | t _{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 60 | 0 | 60 | 0 | 130 | 0 | 130 | ns | |
| t _{AQXQ} | t _{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | 0 | | 0 | | 0 | | 0 | | ns | |

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

2. Sampled only, not 100% tested.

Table 7. Programming Mode DC Characteristics⁽¹⁾
 $(T_A = 25^\circ C; V_{CC} = 5V \pm 5\%; V_{PP} = 21V \pm 0.5V)$

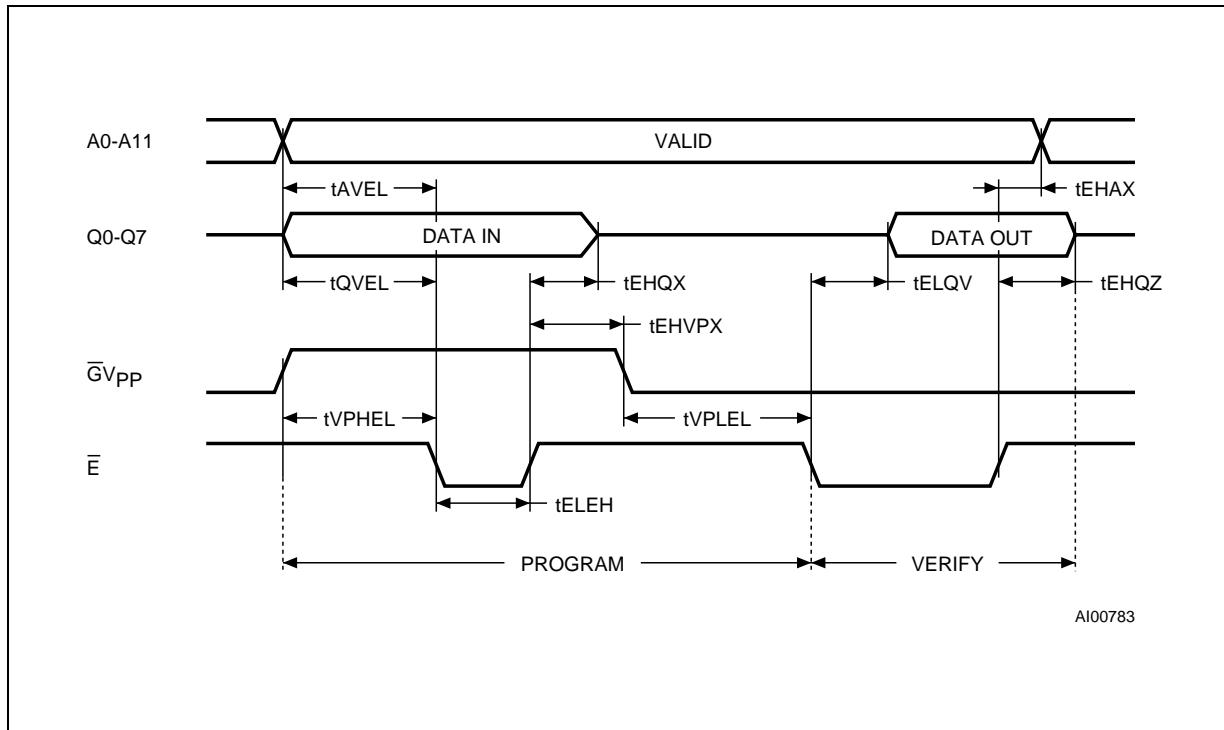
| Symbol | Parameter | Test Condition | Min | Max | Units |
|----------|-----------------------|--------------------------------------|------|--------------|---------|
| I_{LI} | Input Leakage Current | $V_{IL} \leq V_{IN} \leq V_{IH}$ | | ± 10 | μA |
| I_{CC} | Supply Current | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | | 125 | mA |
| I_{PP} | Program Current | $\bar{E} = V_{IL}, \bar{G} = V_{PP}$ | | 30 | mA |
| V_{IL} | Input Low Voltage | | -0.1 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2 | $V_{CC} + 1$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1mA$ | | 0.45 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -400\mu A$ | 2.4 | | V |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Table 8. Programming Mode AC Characteristics⁽¹⁾
 $(T_A = 25^\circ C; V_{CC} = 5V \pm 5\%; V_{PP} = 21V \pm 0.5V)$

| Symbol | Alt | Parameter | Test Condition | Min | Max | Units |
|----------------|-----------|---|--------------------------------------|-----|-----|---------|
| t_{AVEL} | t_{AS} | Address Valid to Chip Enable Low | | 2 | | μs |
| t_{QVEL} | t_{DS} | Input Valid to Chip Enable Low | | 2 | | μs |
| t_{VPHEL} | t_{OES} | V_{PP} High to Chip Enable Low | | 2 | | μs |
| $t_{VPL1VPL2}$ | t_{PRT} | V_{PP} Rise Time | | 50 | | ns |
| t_{ELEH} | t_{PW} | Chip Enable Program Pulse Width | | 45 | 55 | ms |
| t_{EHQX} | t_{DH} | Chip Enable High to Input Transition | | 2 | | μs |
| t_{EHVPX} | t_{OEH} | Chip Enable High to V_{PP} Transition | | 2 | | μs |
| t_{VPLEL} | t_{VR} | V_{PP} Low to Chip Enable Low | | 2 | | μs |
| t_{ELQV} | t_{DV} | Chip Enable Low to Output Valid | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | | 1 | μs |
| t_{EHQZ} | t_{DF} | Chip Enable High to Output Hi-Z | | 0 | 130 | ns |
| t_{EHAX} | t_{AH} | Chip Enable High to Address Transition | | 0 | | ns |

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Figure 6. Programming and Verify Modes AC Waveforms**ORDERING INFORMATION SCHEME**

Example:

M2732A -2 F 1

| Speed and V_{CC} Tolerance | | Package | Temperature Range |
|------------------------------|-----------------------|---------|-------------------|
| -2 | 200 ns, 5V $\pm 5\%$ | F | 1 0 to 70 °C |
| blank | 250 ns, 5V $\pm 5\%$ | FDIP24W | 6 -40 to 85 °C |
| -3 | 300 ns, 5V $\pm 5\%$ | | |
| -4 | 450 ns, 5V $\pm 5\%$ | | |
| -20 | 200 ns, 5V $\pm 10\%$ | | |
| -25 | 250 ns, 5V $\pm 10\%$ | | |

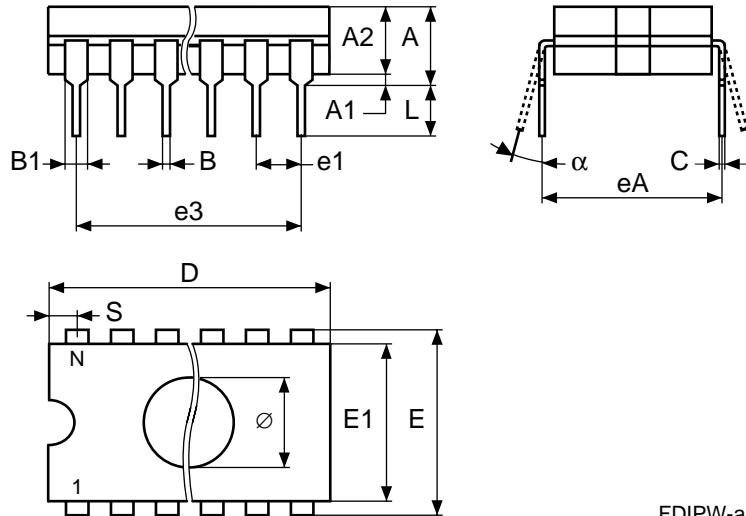
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP24W - 24 pin Ceramic Frit-seal DIP, with window

| Symb | mm | | | inches | | |
|------|-------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 5.71 | | | 0.225 |
| A1 | | 0.50 | 1.78 | | 0.020 | 0.070 |
| A2 | | 3.90 | 5.08 | | 0.154 | 0.200 |
| B | | 0.40 | 0.55 | | 0.016 | 0.022 |
| B1 | | 1.17 | 1.42 | | 0.046 | 0.056 |
| C | | 0.22 | 0.31 | | 0.009 | 0.012 |
| D | | | 32.30 | | | 1.272 |
| E | | 15.40 | 15.80 | | 0.606 | 0.622 |
| E1 | | 13.05 | 13.36 | | 0.514 | 0.526 |
| e1 | 2.54 | — | — | 0.100 | — | — |
| e3 | 27.94 | — | — | 1.100 | — | — |
| eA | | 16.17 | 18.32 | | 0.637 | 0.721 |
| L | | 3.18 | 4.10 | | 0.125 | 0.161 |
| S | | 1.52 | 2.49 | | 0.060 | 0.098 |
| Ø | 7.11 | — | — | 0.280 | — | — |
| α | | 4° | 15° | | 4° | 15° |
| N | | 24 | | | 24 | |

FDIP24W



FDIPW-a

Drawing is not to scale

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CD4028BC BCD-to-Decimal Decoder

General Description

The CD4028BC is a BCD-to-decimal or binary-to-octal decoder consisting of 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the 4 inputs, A, B, C, and D, results in a high level at the selected 1-of-10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B, and C is decoded in octal at outputs 0–7. A high level signal at the D input inhibits octal decoding and causes outputs 0–7 to go LOW.

All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS} .

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- Low power
- Glitch free outputs
- "Positive logic" on inputs and outputs

Applications

- Code conversion
- Address decoding
- Indicator-tube decoder

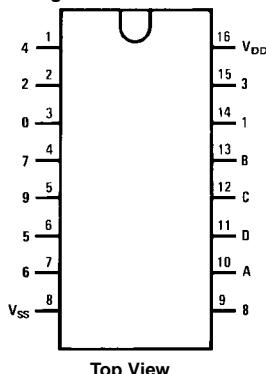
Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| CD4028BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| CD4028BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC

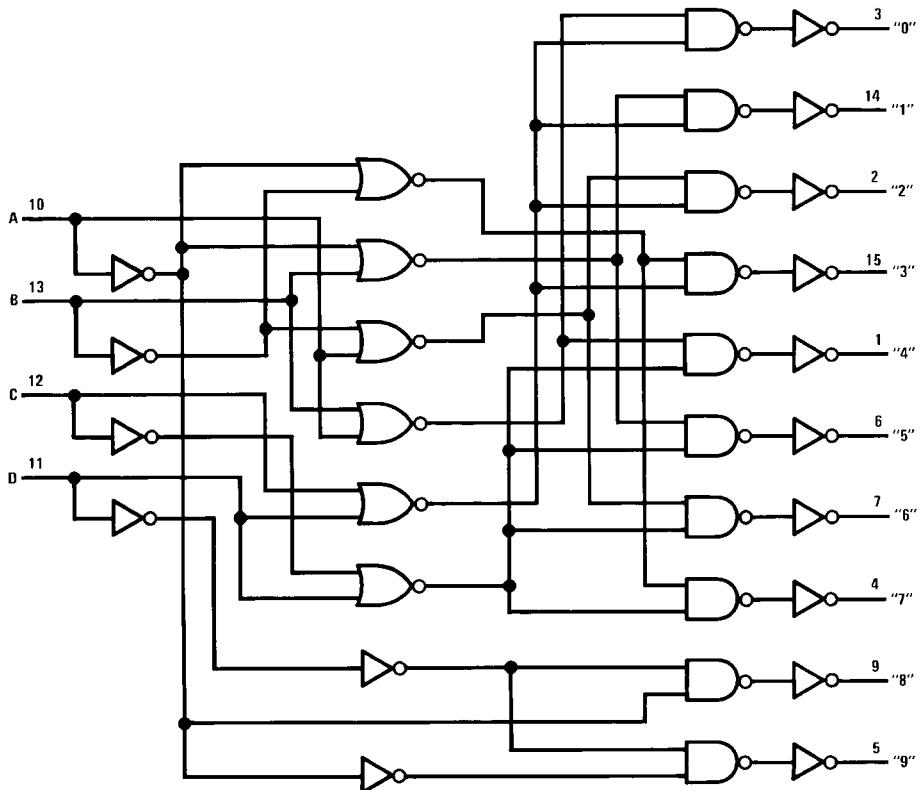


Truth Table

| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 = HIGH Level | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 = LOW Level | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

BCD States

Extraordinary States

Logic Diagram

Absolute Maximum Ratings(Note 1)

(Note 2)

| | |
|-------------------------------------|------------------------|
| Supply Voltage (V_{DD}) | -0.5 to +18V |
| Input Voltage (V_{IN}) | -0.5 to V_{DD} +0.5V |
| Storage Temperature Range (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|---------------------------------------|-----------------|
| Supply Voltage (V_{DD}) | 3 to 15V |
| Input Voltage (V_{IN}) | 0 to V_{DD} V |
| Operating Temperature Range (T_A) | -40°C to +85°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

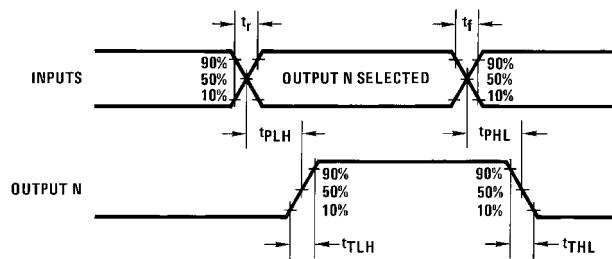
| Symbol | Parameter | Conditions | -40°C | | +25°C | | | +85°C | | Units |
|----------|---------------------------------------|---|-------|-------|-------|-------|------|-------|-------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS} | | 20 | | 0.01 | 20 | | 150 | μA |
| | | $V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS} | | 40 | | 0.01 | 40 | | 300 | μA |
| | | $V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS} | | 80 | | 0.02 | 80 | | 600 | μA |
| V_{OL} | LOW Level Output Voltage | $ I_O < 1 \mu A, V_{IL} = 0V, V_{IH} = V_{DD}$ | | | 0.05 | | 0 | 0.05 | | V |
| | | $V_{DD} = 5V$ | | | 0.05 | | 0 | 0.05 | | V |
| | | $V_{DD} = 10V$ | | | 0.05 | | 0 | 0.05 | | V |
| V_{OH} | HIGH Level Output Voltage | $ I_O < 1 \mu A, V_{IL} = 0V, V_{IH} = V_{DD}$ | | 4.95 | | 4.95 | 5 | | 4.95 | V |
| | | $V_{DD} = 5V$ | | 9.95 | | 9.95 | 10 | | 9.95 | V |
| | | $V_{DD} = 10V$ | | 14.95 | | 14.95 | 15 | | 14.95 | V |
| V_{IL} | LOW Level Input Voltage | $ I_O < 1 \mu A$ | | | 1.5 | | 2.25 | 1.5 | | V |
| | | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | | 3.0 | | 4.5 | 3.0 | | V |
| | | $V_{DD} = 10V, V_O = 1V$ or $9V$ | | | 4.0 | | 6.75 | 4.0 | | V |
| V_{IH} | HIGH Level Input Voltage | $ I_O < 1 \mu A$ | | 3.5 | | 3.5 | | | 3.5 | V |
| | | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | 7.0 | | 7.0 | | | 7.0 | V |
| | | $V_{DD} = 10V, V_O = 1V$ or $9V$ | | 11.0 | | 11.0 | | | 11.0 | V |
| I_{OL} | LOW Level Output Current (Note 3) | $V_{IH} = V_{DD}, V_{IL} = 0V$ | | 0.52 | | 0.44 | 0.88 | | 0.36 | mA |
| | | $V_{DD} = 5V, V_O = 0.4V$ | | 1.3 | | 1.1 | 2.2 | | 0.9 | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | | 3.6 | | 3.0 | 6.0 | | 2.4 | mA |
| I_{OH} | HIGH Level Output Current (Note 3) | $V_{IH} = V_{DD}, V_{IL} = 0V$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 4.6V$ | -0.2 | | -0.16 | -0.32 | | -0.12 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -0.5 | | -0.4 | -0.8 | | -0.3 | | mA |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.3 | | | -0.3 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.3 | | | 0.3 | | 1.0 | μA |

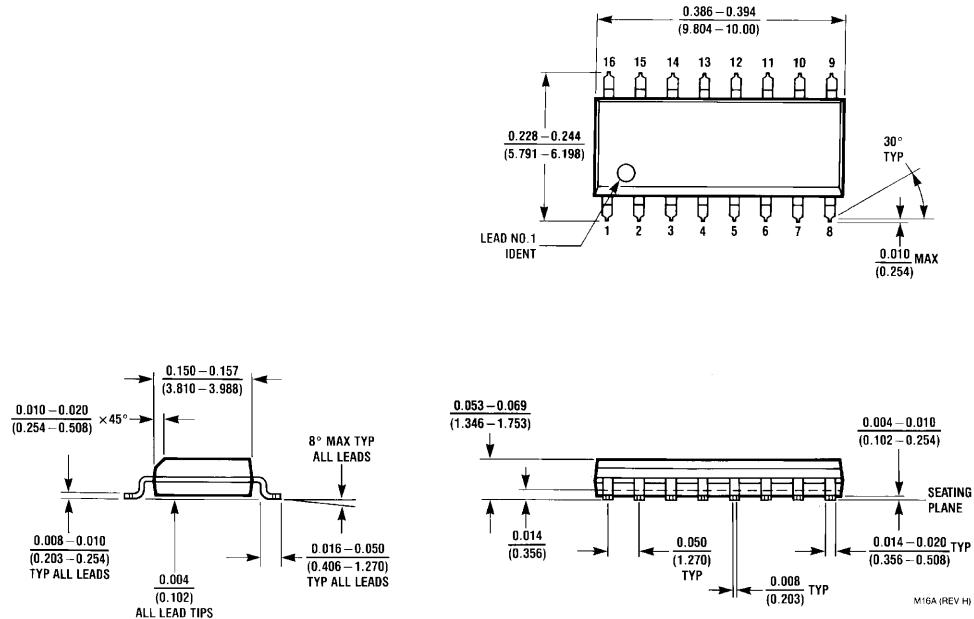
Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 4) $T_A = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200\text{k}$, Input $t_r = t_f = 20 \text{ ns}$, unless otherwise specified

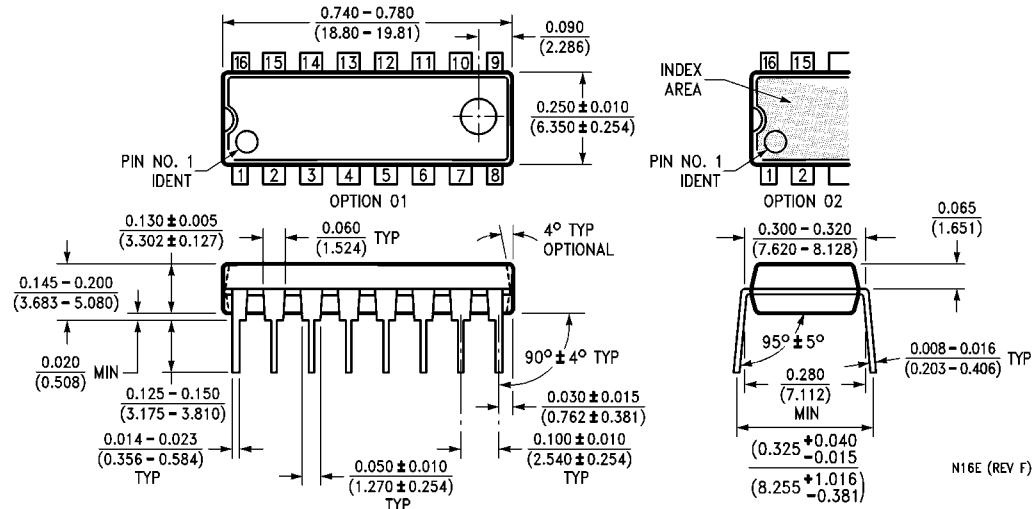
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|------------------------|--|-----|------------------|-------------------|----------------|
| t_{PHL} or t_{PLH} | Propagation Delay Time | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$ | | 240 100 70 | 480 200 140 | ns ns ns |
| t_{THL} or t_{TLH} | Transition Time | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$ | | 175 75 60 | 350 150 110 | ns ns ns |
| C_{IN} | Input Capacitance | Any Input | | 5 | 7.5 | pF |

Note 4: AC Parameters are guaranteed by DC correlated testing.

Switching Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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8253/8253-5 PROGRAMMABLE INTERVAL TIMER

- MCS-85™ Compatible 8253-5
- 3 Independent 16-Bit Counters
- DC to 2.6 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

The Intel® 8253 is a programmable counter/timer device designed for use as an Intel microcomputer peripheral. It uses NMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.

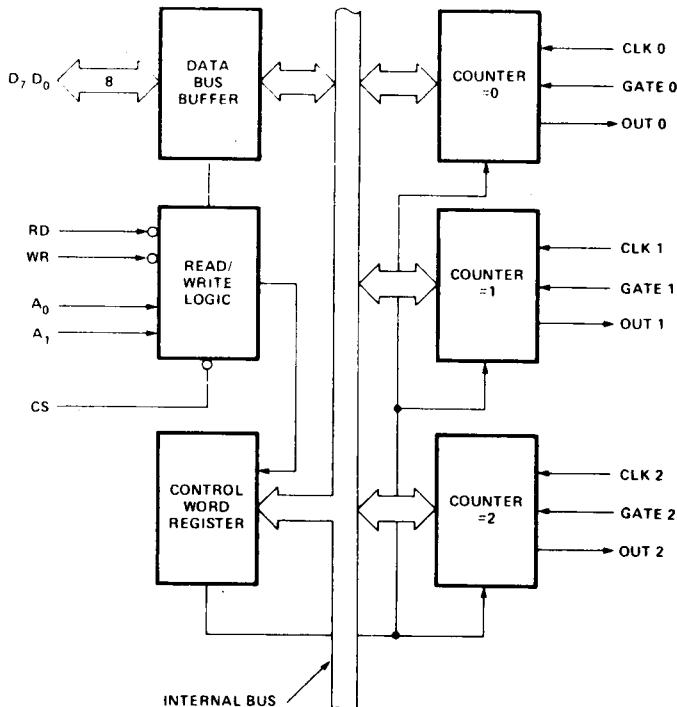


Figure 1. Block Diagram

231306-1

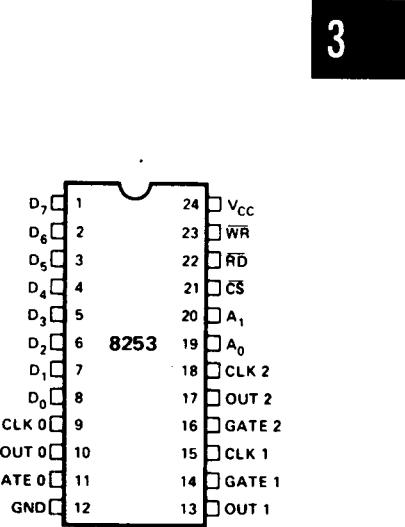


Figure 2. Pin Configuration

231306-2

FUNCTIONAL DESCRIPTION

General

The 8253 is programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

The 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

RD (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

WR (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

CS (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The CS input has no effect upon the actual operation of the counters.

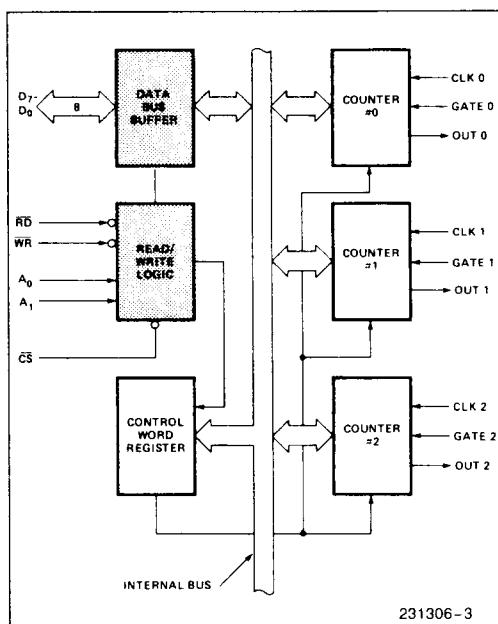


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

231306-3

| CS | RD | WR | A ₁ | A ₀ | |
|----|----|----|----------------|----------------|----------------------|
| 0 | 1 | 0 | 0 | 0 | Load Counter No. 0 |
| 0 | 1 | 0 | 0 | 1 | Load Counter No. 1 |
| 0 | 1 | 0 | 1 | 0 | Load Counter No. 2 |
| 0 | 1 | 0 | 1 | 1 | Write Mode Word |
| 0 | 0 | 1 | 0 | 0 | Read Counter No. 0 |
| 0 | 0 | 1 | 0 | 1 | Read Counter No. 1 |
| 0 | 0 | 1 | 1 | 0 | Read Counter No. 2 |
| 0 | 0 | 1 | 1 | 1 | No-Operation 3-State |
| 1 | X | X | X | X | Disable 3-State |
| 0 | 1 | 1 | X | X | No-Operation 3-State |

Control Word Register

The Control Word Register is selected when A₀, A₁ are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operation MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate MODE configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer systems and interfaces in the same manner as all other peripherals of the family. It is treated by the

systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A₀, A₁ connect to the A₀, A₁ address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

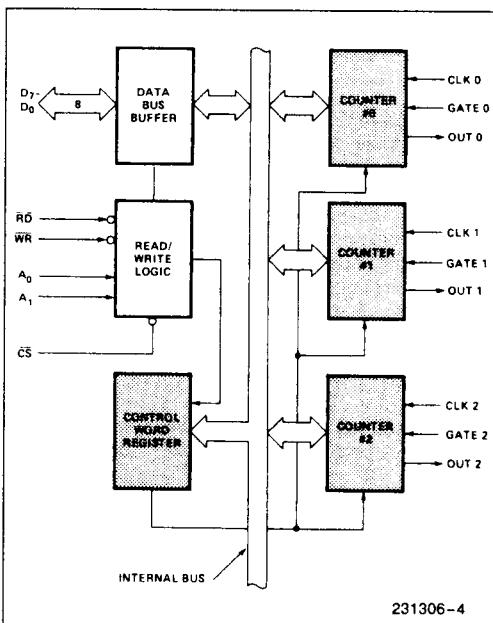


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

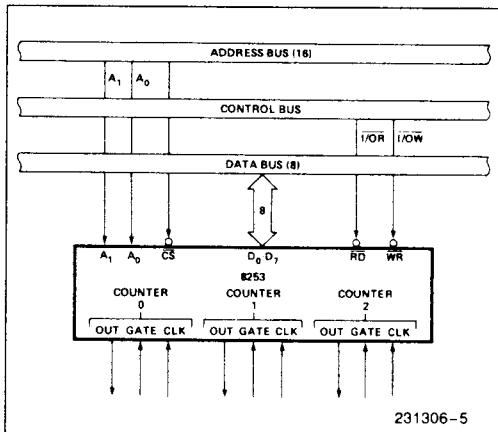


Figure 5. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words *must* be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

| D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |

Definition Of Control

SC—SELECT COUNTER:

| SC1 | SC0 | |
|-----|-----|------------------|
| 0 | 0 | Select Counter 0 |
| 0 | 1 | Select Counter 1 |
| 1 | 0 | Select Counter 2 |
| 1 | 1 | Illegal |

RL—READ/LOAD:

RL1 RL0

| | | |
|---|---|---|
| 0 | 0 | Counter Latching operation (see READ/WRITE Procedure Section). |
| 1 | 0 | Read/Load most significant byte only. |
| 0 | 1 | Read/Load least significant byte only. |
| 1 | 1 | Read/Load least significant byte first, then most significant byte. |

M—MODE:

| M2 | M1 | M0 | |
|----|----|----|--------|
| 0 | 0 | 0 | Mode 0 |
| 0 | 0 | 1 | Mode 1 |
| X | 1 | 0 | Mode 2 |
| X | 1 | 1 | Mode 3 |
| 1 | 0 | 0 | Mode 4 |
| 1 | 0 | 1 | Mode 5 |

BCD:

| | |
|---|---|
| 0 | Binary Counter 16-Bits |
| 1 | Binary Coded Decimal (BCD) Counter (4 Decades) |

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE DEFINITION

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

- (1) Write 1st byte stops the current counting.
- (2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (or even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following WR of a new count value.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

| Signal Status Modes | Low Or Going Low | Rising | High |
|---------------------|---|--|------------------|
| 0 | Disables counting | — | Enables counting |
| 1 | — | 1) Initiates counting 2) Resets output after next clock | — |
| 2 | 1) Disables counting 2) Sets output immediately high | 1) Reloads counter 2) Initiates counting | Enables counting |
| 3 | 1) Disables counting 2) Sets output immediately high | 1) Reloads counter 2) Initiates counting | Enables counting |
| 4 | Disables counting | — | Enables counting |
| 5 | — | Initiates counting | — |

3

Figure 6. Gate Pin Operations Summary

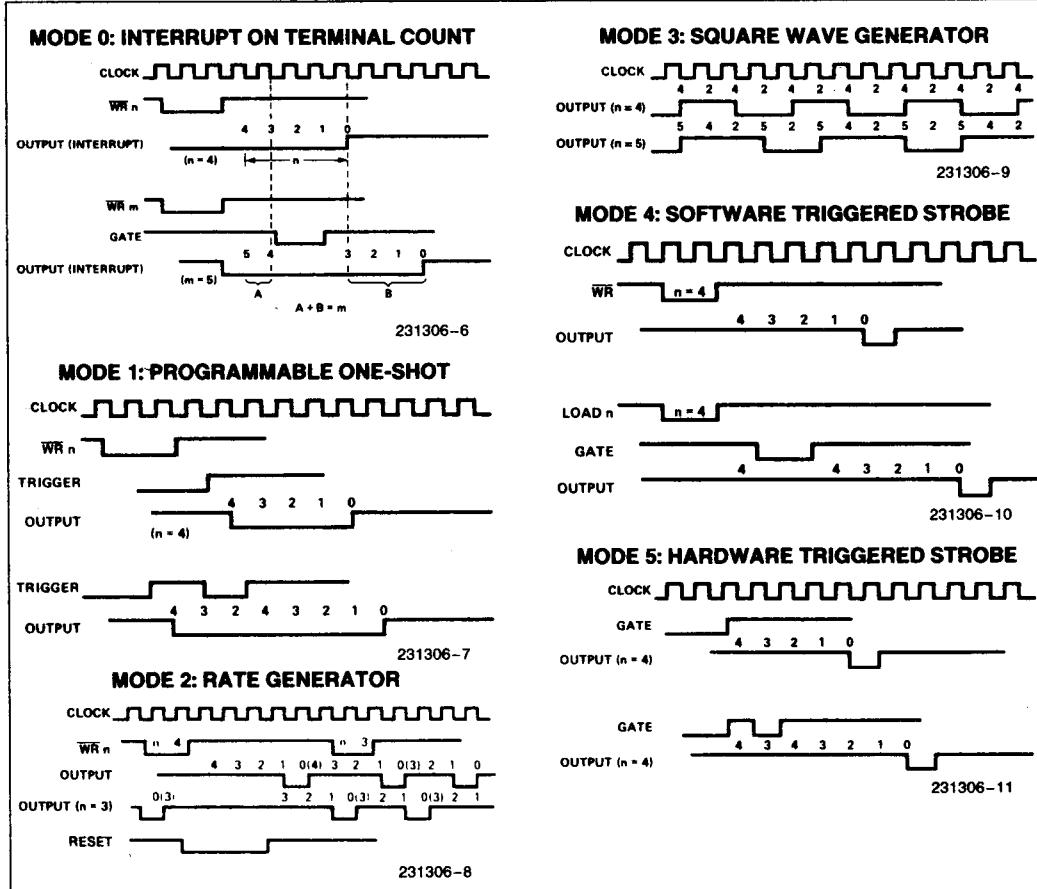


Figure 7. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1).

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it *must* be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeros into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

| MODE Control Word | |
|-------------------|------------------------------------|
| Counter n | |
| LSB | Counter Register byte Counter n |
| MSB | Counter Register byte Counter n |

NOTE:

Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 8. Programming Format

| | A1 | A0 |
|-------|---|--------|
| No. 1 | MODE Control Word Counter 0 | 1 1 |
| No. 2 | MODE Control Word Counter 1 | 1 1 |
| No. 3 | MODE Control Word Counter 2 | 1 1 |
| No. 4 | LSB Count Register Byte Counter 1 | 0 1 |
| No. 5 | MSB Count Register Byte Counter 1 | 0 1 |
| No. 6 | LSB Count Register Byte Counter 2 | 1 0 |
| No. 7 | MSB Count Register Byte Counter 2 | 1 0 |
| No. 8 | LSB Count Register Byte Counter 0 | 0 0 |
| No. 9 | MSB Count Register Byte Counter 0 | 0 0 |

NOTE:

The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully initialized.

Figure 9. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter *must be inhibited* either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

First I/O Read contains the least significant byte (LSB).

Second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read, then two bytes *must* be read before any loading WR command can be sent to the same counter.

Read Operation Chart

| A1 | A0 | RD | |
|----|----|----|--------------------|
| 0 | 0 | 0 | Read Counter No. 0 |
| 0 | 1 | 0 | Read Counter No. 1 |
| 1 | 0 | 0 | Read Counter No. 2 |
| 1 | 1 | 0 | Illegal |

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

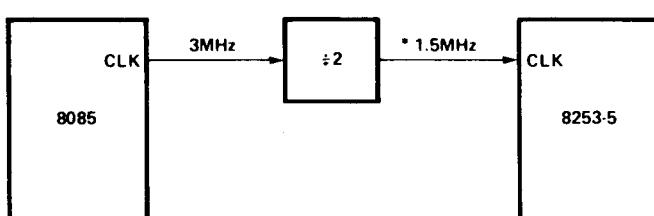
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|----|----|----|----|----|----|
| SC1 | SC0 | 0 | 0 | X | X | X | X |

SC1, SC0— specify counter to be latched.

D5, D4 — 00 designates counter latching operation.

X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.



*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2 MHz or less.

231306-12

Figure 10. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|-----------------|
| Ambient Temperature Under Bias | 0°C to 70°C |
| Storage Temperature | -65°C to +150°C |
| Voltage On Any Pin with Respect to Ground..... | -0.5V to 7V |
| Power Dissipation | 1 Watt |

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$ *

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|-----------|-------------------------|------|-----------------------|---------------|-----------------------------|
| V_{IL} | Input Low Voltage | -0.5 | 0.8 | V | |
| V_{IH} | Input High Voltage | 2.2 | $V_{CC} + .5\text{V}$ | V | |
| V_{OL} | Output Low Voltage | | 0.45 | V | (Note 1) |
| V_{OH} | Output High Voltage | 2.4 | | V | (Note 2) |
| I_{IL} | Input Load Current | | ± 10 | μA | $V_{IN} = V_{CC}$ to 0V |
| I_{OFL} | Output Float Leakage | | ± 10 | μA | $V_{OUT} = V_{CC}$ to 0.45V |
| I_{CC} | V_{CC} Supply Current | | 140 | mA | |

3

CAPACITANCE $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|-----------|-------------------|-----|-----|-----|------|--------------------------------------|
| C_{IN} | Input Capacitance | | | 10 | pF | $f_C = 1\text{ MHz}$ |
| $C_{I/O}$ | I/O Capacitance | | | 20 | pF | Unmeasured pins returned to V_{SS} |

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 10\%$, $\text{GND} = 0\text{V}^*$ **Bus Parameters(3)****READ CYCLE**

| Symbol | Parameter | 8253 | | 8253-5 | | Unit |
|----------|--|------|-----|--------|-----|---------------|
| | | Min | Max | Min | Max | |
| t_{AR} | Address Stable before $\overline{\text{READ}}$ | 50 | | 30 | | ns |
| t_{RA} | Address Hold Time for $\overline{\text{READ}}$ | 5 | | 5 | | ns |
| t_{RR} | $\overline{\text{READ}}$ Pulse Width | 400 | | 300 | | ns |
| t_{RD} | Data Delay from $\overline{\text{READ}}$ ⁽⁴⁾ | | 300 | | 200 | ns |
| t_{DF} | $\overline{\text{READ}}$ to Data Floating | 25 | 125 | 25 | 100 | ns |
| t_{RV} | Recovery Time between $\overline{\text{READ}}$ and Any Other Control Signal | 1 | | 1 | | μs |

A.C. CHARACTERISTICS (Continued)**WRITE CYCLE**

| Symbol | Parameter | 8253 | | 8253-5 | | Unit |
|-----------------|--|------|-----|--------|-----|------|
| | | Min | Max | Min | Max | |
| t _{AW} | Address Stable before WRITE | 50 | | 30 | | ns |
| t _{WA} | Address Hold Time for WRITE | 30 | | 30 | | ns |
| t _{WW} | WRITE Pulse Width | 400 | | 300 | | ns |
| t _{DW} | Data Set Up Time for WRITE | 300 | | 250 | | ns |
| t _{WD} | Data Hold Time for WRITE | 40 | | 30 | | ns |
| t _{RV} | Recovery Time between WRITE and Any Other Control Signal | 1 | | 1 | | μs |

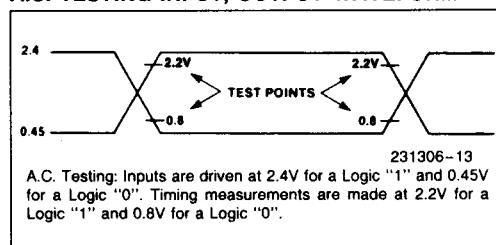
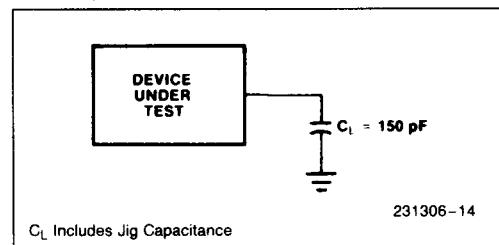
CLOCK AND GATE TIMING

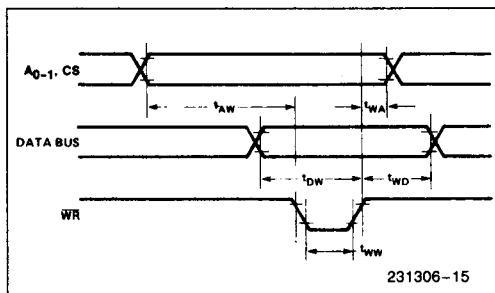
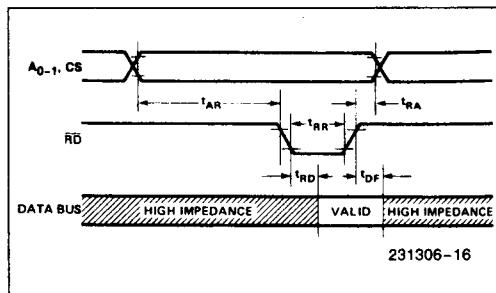
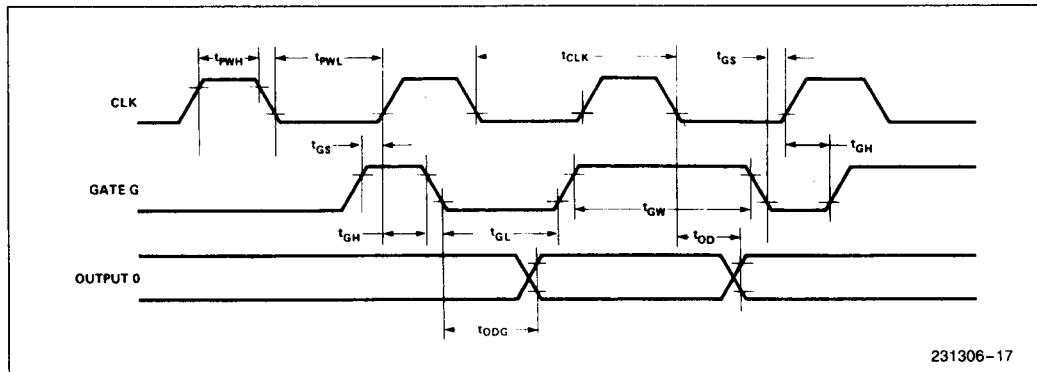
| Symbol | Parameter | 8253 | | 8253-5 | | Unit |
|------------------|---|------|-----|--------|-----|------|
| | | Min | Max | Min | Max | |
| t _{CLK} | Clock Period | 380 | dc | 380 | dc | ns |
| t _{PWH} | High Pulse Width | 230 | | 230 | | ns |
| t _{PWL} | Low Pulse Width | 150 | | 150 | | ns |
| t _{GW} | Gate Width High | 150 | | 150 | | ns |
| t _{GL} | Gate Width Low | 100 | | 100 | | ns |
| t _{GS} | Gate Set Up Time to CLK ↑ | 100 | | 100 | | ns |
| t _{GH} | Gate Hold Time after CLK ↑ | 50 | | 50 | | ns |
| t _{OD} | Output Delay from CLK ↓ ⁽⁴⁾ | | 400 | | 400 | ns |
| t _{ODG} | Output Delay from Gate ↓ ⁽⁴⁾ | | 300 | | 300 | ns |

NOTES:

1. I_{OL} = 2.2 mA.
2. I_{OH} = -400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150 pF.

*For Extended Temperature EXPRESS, use M8253 electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM**A.C. TESTING LOAD CIRCUIT**

WAVEFORMS**WRITE TIMING****READ TIMING****CLOCK AND GATE TIMING**

82C55A

CMOS Programmable Peripheral Interface

FN2969
Rev 11.00
Dec 8, 2015

The Intersil 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJ1 IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Intersil advanced SAJ1 process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Features

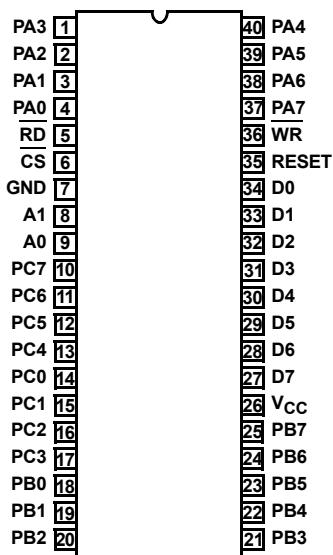
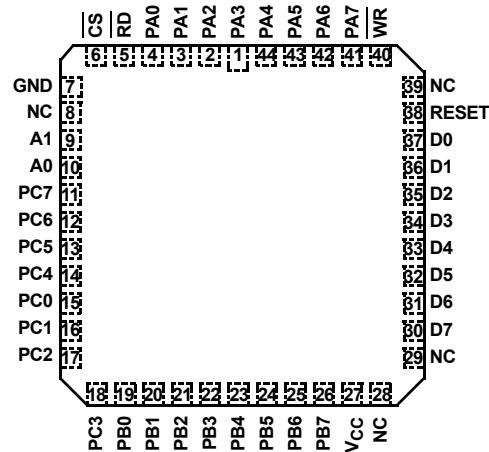
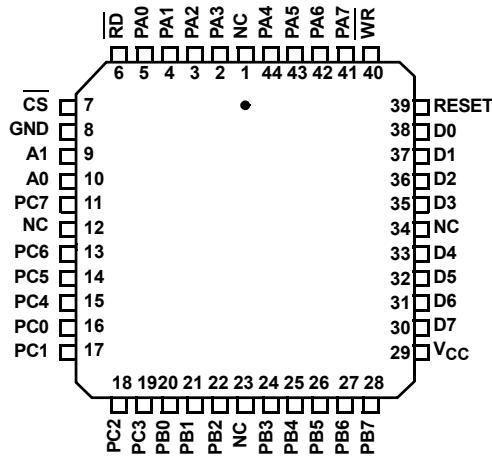
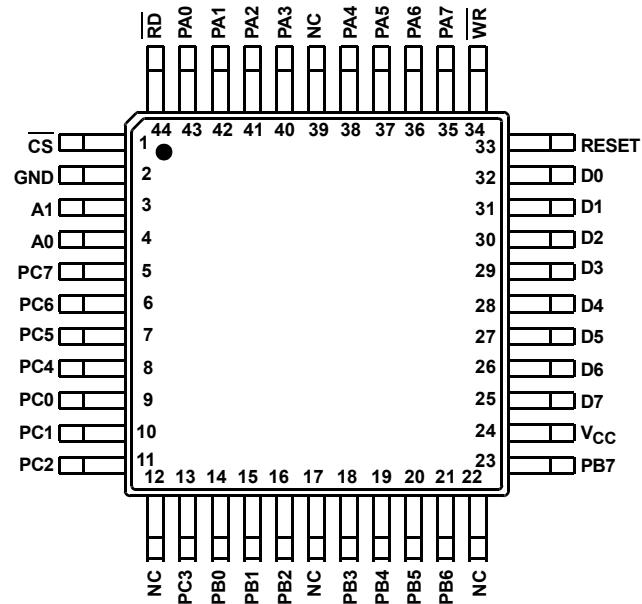
- Pb-Free Plus Anneal Available (RoHS Compliant) (See Ordering Info)
- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- L7 Process
- 2.5mA Drive Capability on All I/O Ports
- Low Standby Power (ICCSB) 10µA

Ordering Information

| PART NUMBERS | | | | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|-----------------|-------------------|-----------------|---------------------|----------------------|-------------|
| 5MHz | PART MARKING | 8MHz | PART MARKING | | | |
| CP82C55A-5 (No longer available, recommended replacement: CP82C55A-5Z) | CP82C55A-5 | CP82C55A | CP82C55A | 0 to +70 | 40 Ld PDIP | E40.6 |
| CP82C55A-5Z (Note) | CP82C55A-5Z | CP82C55AZ (Note) | CP82C55AZ | 0 to +70 | 40 Ld PDIP (Pb-free) | |
| | | IP82C55A | IP82C55A | -40 to +85 | 40 Ld PDIP | |
| | | IP82C55AZ (Note) | IP82C55AZ | -40 to +85 | 40 Ld PDIP (Pb-free) | |
| CS82C55A-5* (No longer available, recommended replacement: CS82C55A-5Z) | CS82C55A-5 | CS82C55A* | CS82C55A* | 0 to +70 | 44 Ld PLCC | N44.65 |
| CS82C55A-5Z* (Note) | CS82C55A-5Z | CS82C55AZ* (Note) | CS82C55AZ | 0 to +70 | 44 Ld PLCC (Pb-free) | |
| IS82C55A-5* | IS82C55A-5 | IS82C55A* | IS82C55A* | -40 to +85 | 44 Ld PLCC | |
| IS82C55A-5Z* (Note) | IS82C55A-5Z | IS82C55AZ* (Note) | IS82C55AZ | -40 to +85 | 44 Ld PLCC (Pb-free) | Q44.10x10 |
| | | CQ82C55AZ (Note) | CQ82C55AZ | 0 to +70 | 44 Ld MQFP (Pb-free) | |
| | | IQ82C55AZ* (Note) | IQ82C55AZ | -40 to +85 | 44 Ld MQFP (Pb-free) | |
| | | ID82C55A | ID82C55A | -40 to +85 | 40 Ld CERDIP | F40.6 |
| | | MD82C55A/B | MD82C55A/B | -55 to +125 | | |
| | | 8406602QA | 8406602QA | SMD# | | |
| | | 8406602XA | 8406602XA | SMD# | 44 Ld CLCC | J44.A |

*Add "96" suffix to part number for tape and reel packaging.

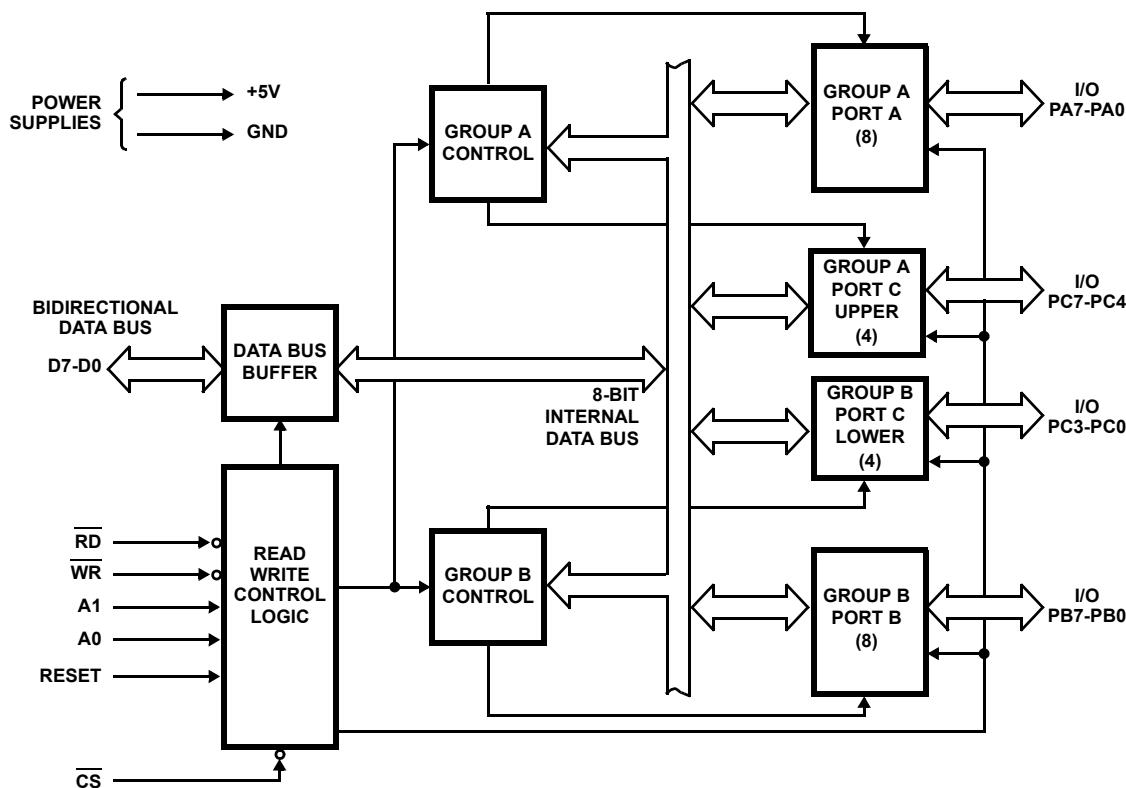
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts**82C55A (PDIP, CERDIP)**
TOP VIEW**82C55A (CLCC)**
TOP VIEW**82C55A (PLCC)**
TOP VIEW**82C55A (MQFP)**
TOP VIEW

Pin Description

| SYMBOL | TYPE | DESCRIPTION |
|-----------------|------|---|
| V_{CC} | | V_{CC} : The +5V power supply pin. A $0.1\mu F$ capacitor between V_{CC} and GND is recommended for decoupling. |
| GND | | GROUND |
| D0-D7 | I/O | DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus. |
| RESET | I | RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on. |
| \overline{CS} | I | CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications. |
| \overline{RD} | I | READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus. |
| \overline{WR} | I | WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A. |
| A0-A1 | I | ADDRESS: These input signals, in conjunction with the \overline{RD} and \overline{WR} inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1. |
| PA0-PA7 | I/O | PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port. |
| PB0-PB7 | I/O | PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port. |
| PC0-PC7 | I/O | PORT C: 8-bit input and output port. Bus hold circuitry is present on this port. |

Functional Diagram



Functional Description

Data Bus Buffer

This three-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A “low” on this input pin enables the communication between the 82C55A and the CPU.

(RD) Read. A “low” on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to “read from” the 82C55A.

(WR) Write. A “low” on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

| | | | | | INPUT OPERATION (READ) |
|----|----|----|----|----|-----------------------------|
| A1 | A0 | RD | WR | CS | |
| 0 | 0 | 0 | 1 | 0 | Port A → Data Bus |
| 0 | 1 | 0 | 1 | 0 | Port B → Data Bus |
| 1 | 0 | 0 | 1 | 0 | Port C → Data Bus |
| 1 | 1 | 0 | 1 | 0 | Control Word → Data Bus |
| | | | | | OUTPUT OPERATION (WRITE) |
| 0 | 0 | 1 | 0 | 0 | Data Bus → Port A |
| 0 | 1 | 1 | 0 | 0 | Data Bus → Port B |
| 1 | 0 | 1 | 0 | 0 | Data Bus → Port C |
| 1 | 1 | 1 | 0 | 0 | Data Bus → Control |
| | | | | | DISABLE FUNCTION |
| X | X | X | X | 1 | Data Bus → Three-State |
| X | X | 1 | 1 | 0 | Data Bus → Three-State |

(RESET) Reset. A “high” on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. “Bus hold” devices internal to the 82C55A will hold the I/O port inputs to a logic “1” state with a maximum hold current of 400µA.

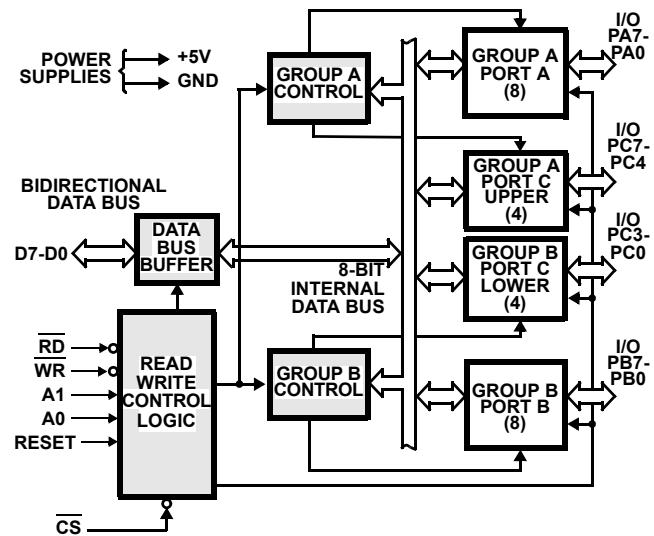


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the 82C55A. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the “Basic Operation” table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or “personality” to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both “pull-up” and “pull-down” bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into

two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

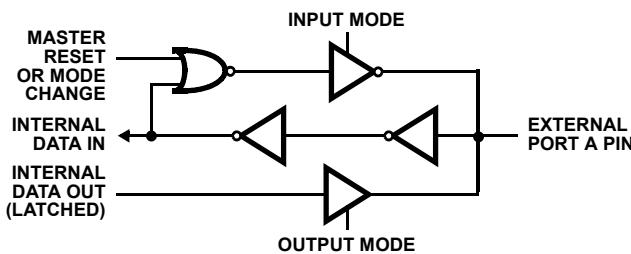


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

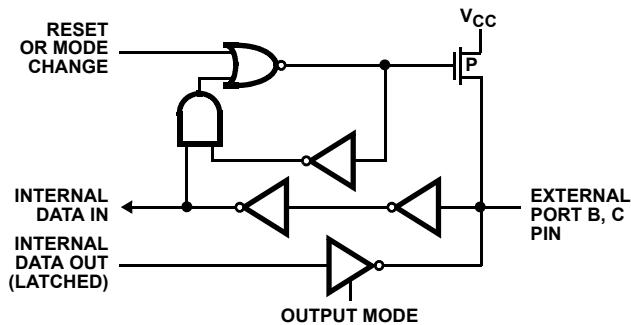


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bidirectional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pull-up or pull-down resistors in all-CMOS designs. The control word register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

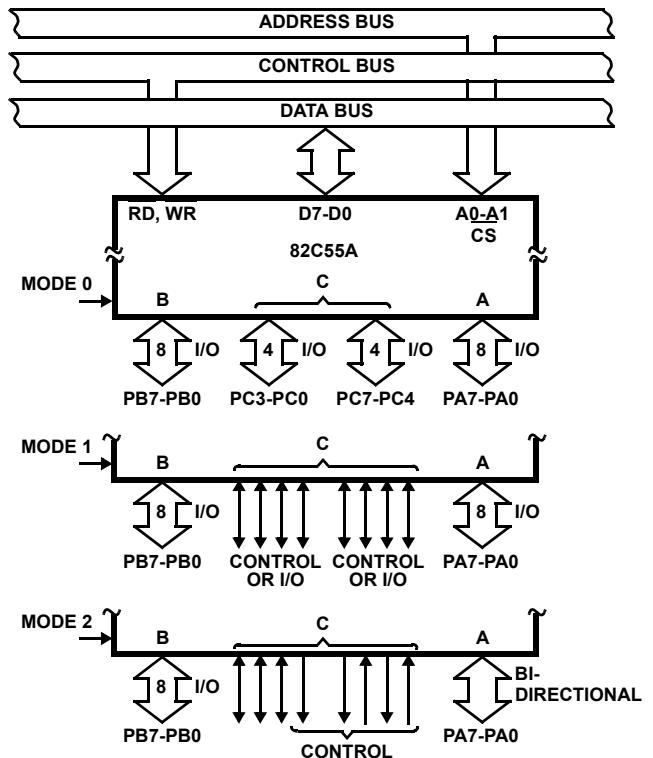


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

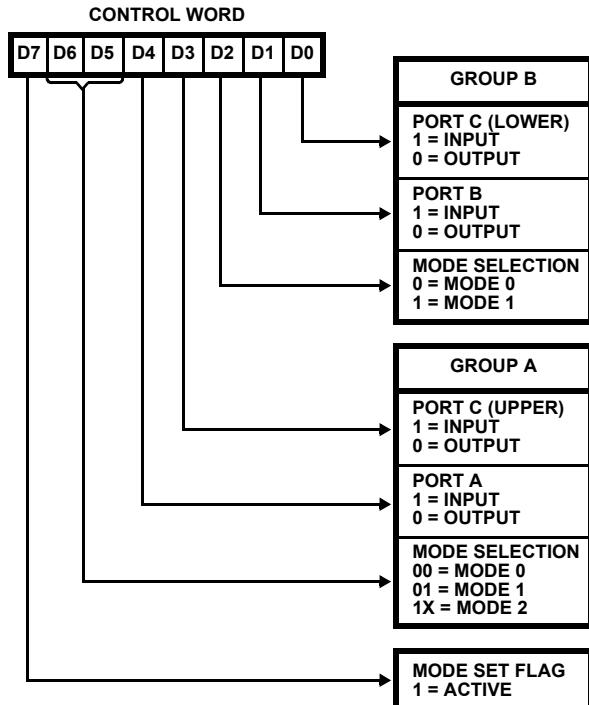


FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

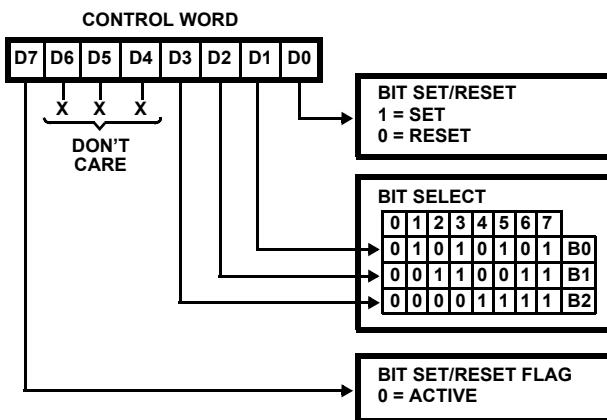


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

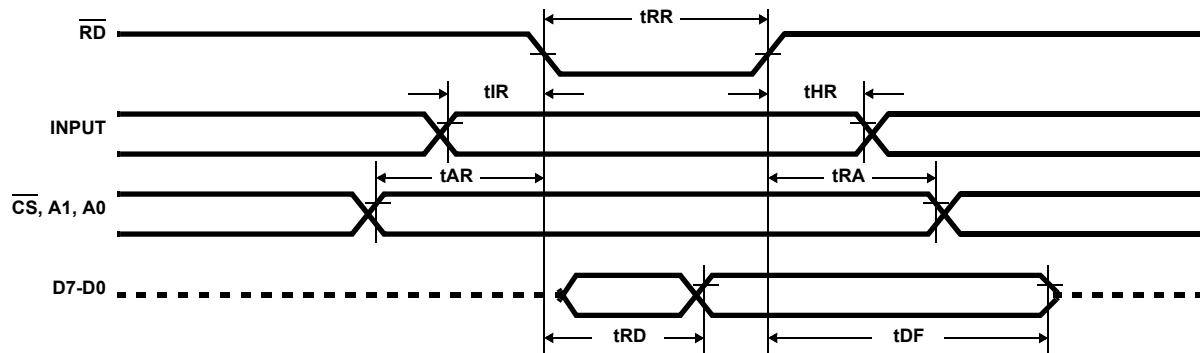
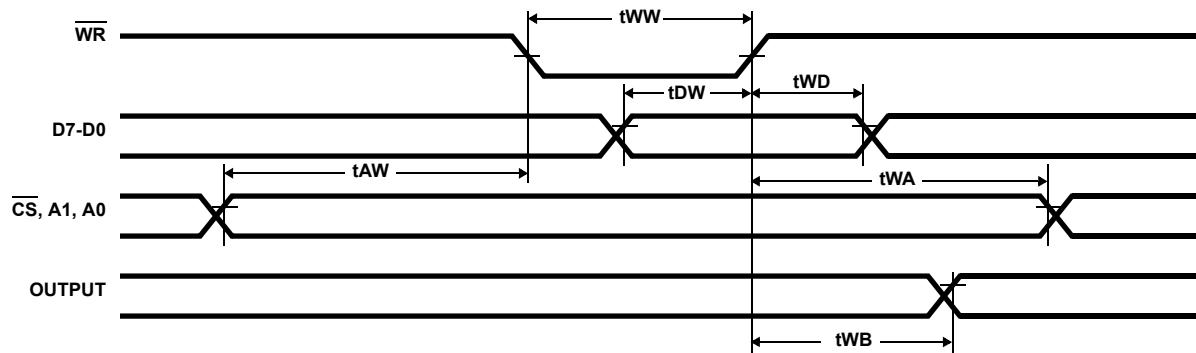
Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible

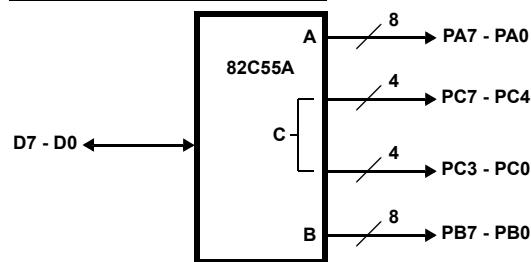
MODE 0 PORT DEFINITION

| A | | B | | GROUP A | | # | GROUP B | |
|----|----|----|----|------------------|------------------|----|---------|------------------|
| D4 | D3 | D1 | D0 | PORTC (Upper) | PORTC (Lower) | | PORT B | PORTC (Lower) |
| 0 | 0 | 0 | 0 | Output | Output | 0 | Output | Output |
| 0 | 0 | 0 | 1 | Output | Output | 1 | Output | Input |
| 0 | 0 | 1 | 0 | Output | Output | 2 | Input | Output |
| 0 | 0 | 1 | 1 | Output | Output | 3 | Input | Input |
| 0 | 1 | 0 | 0 | Output | Input | 4 | Output | Output |
| 0 | 1 | 0 | 1 | Output | Input | 5 | Output | Input |
| 0 | 1 | 1 | 0 | Output | Input | 6 | Input | Output |
| 0 | 1 | 1 | 1 | Output | Input | 7 | Input | Input |
| 1 | 0 | 0 | 0 | Input | Output | 8 | Output | Output |
| 1 | 0 | 0 | 1 | Input | Output | 9 | Output | Input |
| 1 | 0 | 1 | 0 | Input | Output | 10 | Input | Output |
| 1 | 0 | 1 | 1 | Input | Output | 11 | Input | Input |
| 1 | 1 | 0 | 0 | Input | Input | 12 | Output | Output |
| 1 | 1 | 0 | 1 | Input | Input | 13 | Output | Input |
| 1 | 1 | 1 | 0 | Input | Input | 14 | Input | Output |
| 1 | 1 | 1 | 1 | Input | Input | 15 | Input | Input |

Mode 0 (Basic Input)**Mode 0 (Basic Output)****Mode 0 Configurations**

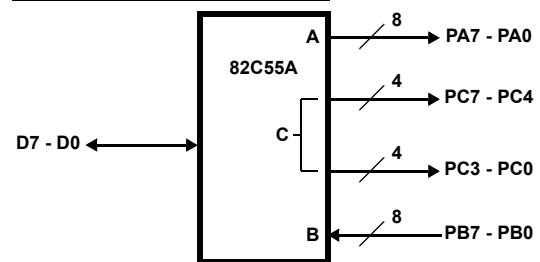
CONTROL WORD #0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |



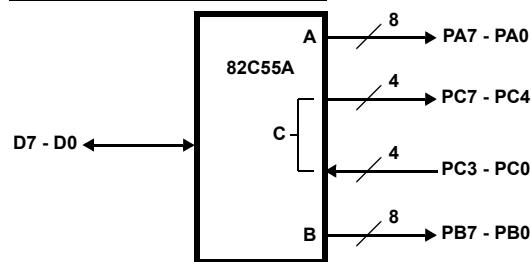
CONTROL WORD #2

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |



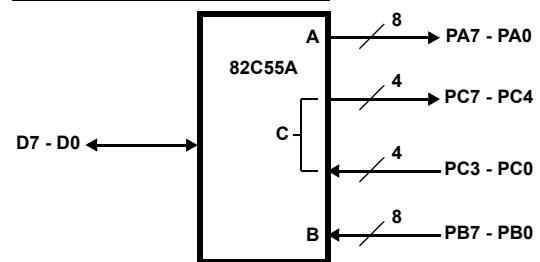
CONTROL WORD #1

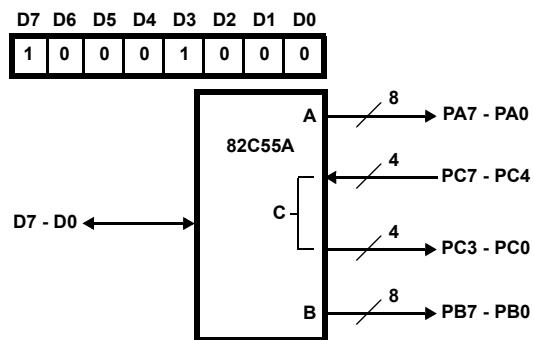
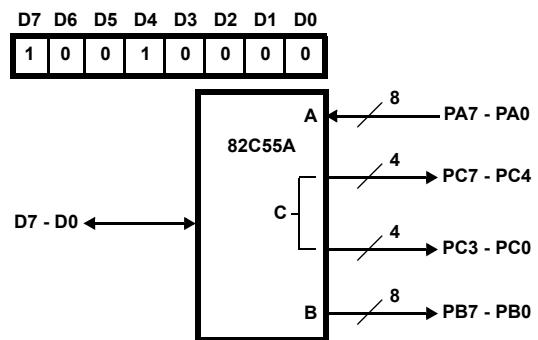
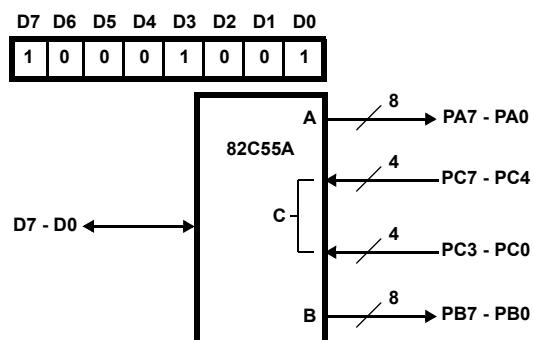
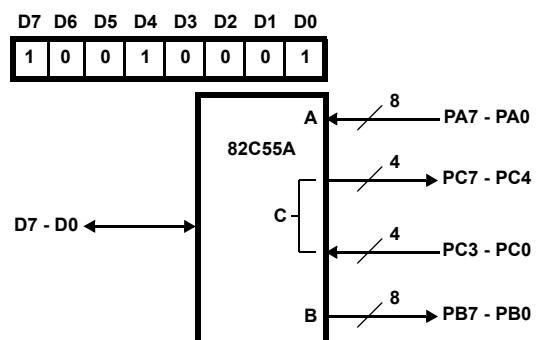
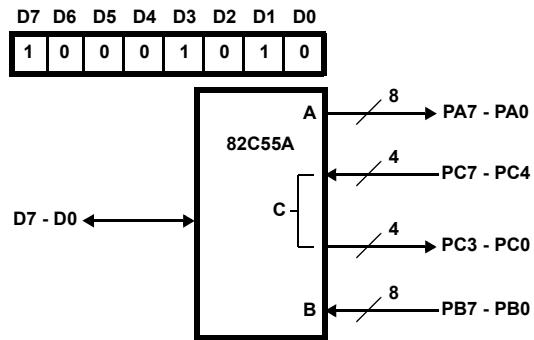
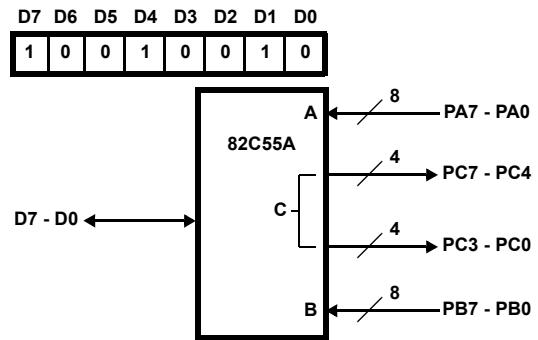
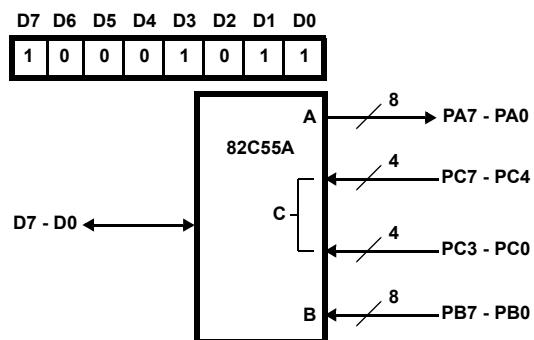
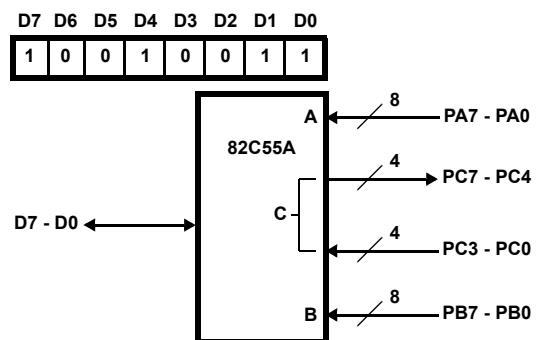
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |



CONTROL WORD #3

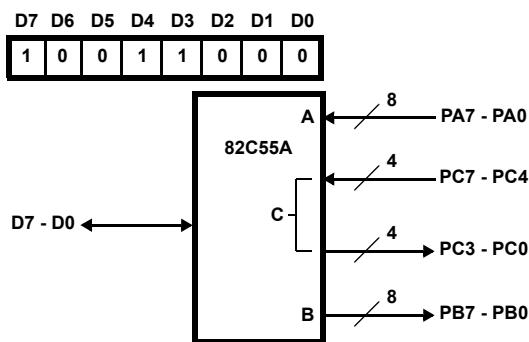
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |



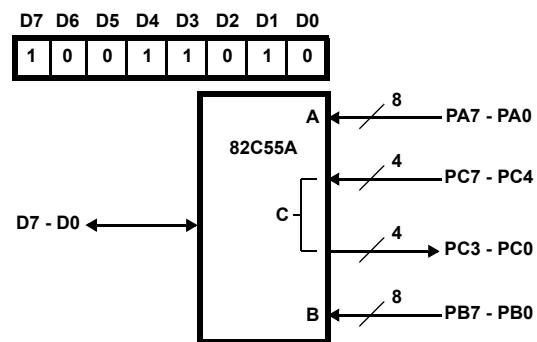
Mode 0 Configurations (Continued)**CONTROL WORD #4****CONTROL WORD #8****CONTROL WORD #5****CONTROL WORD #9****CONTROL WORD #6****CONTROL WORD #10****CONTROL WORD #7****CONTROL WORD #11**

Mode 0 Configurations (Continued)

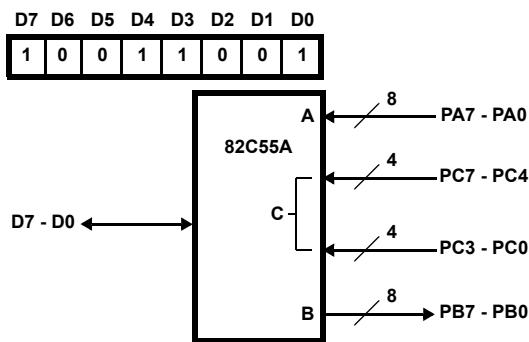
CONTROL WORD #12



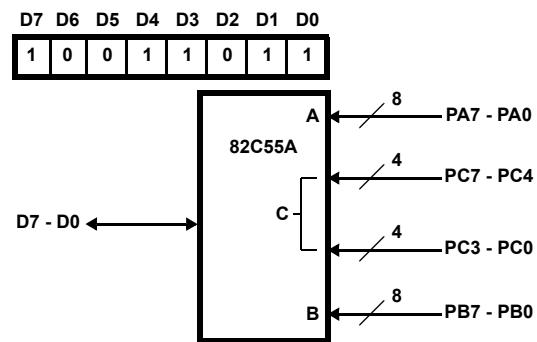
CONTROL WORD #14



CONTROL WORD #13



CONTROL WORD #15

**Operating Modes**

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "hand shaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand shaking" signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch: in essence, an acknowledgment. IBF is set by STB input being low and is reset by the rising edge of the RD input.

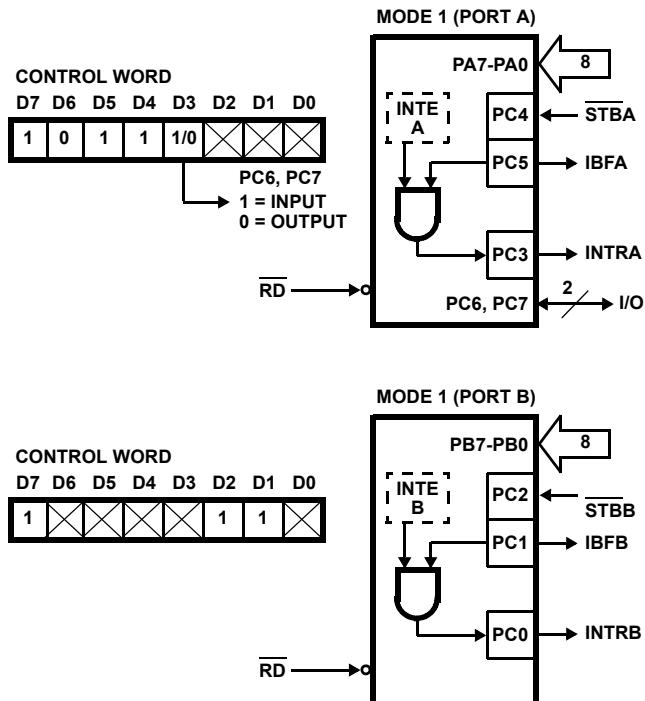


FIGURE 6. MODE 1 INPUT

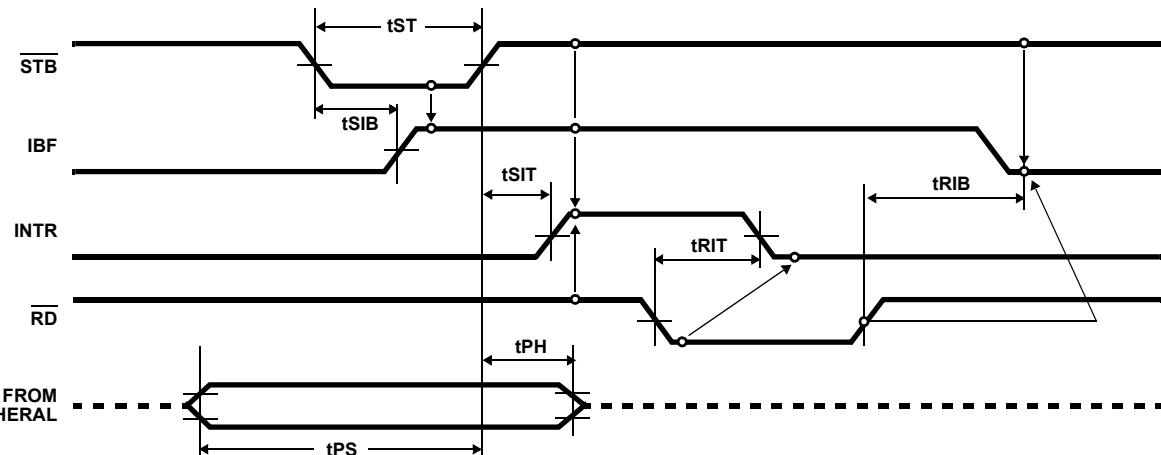


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A “high” on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition: STB is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

OBF - (Output Buffer Full F/F). The OBF output will go “low” to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the port at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF, (See Note 1). The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

ACK - (Acknowledge Input). A “low” on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a “one”, OBF is a “one” and INTE is a “one”. It is reset by the falling edge of WR.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send OBF to the peripheral device, generates an ACK from the peripheral device and then latch data into the peripheral device on the rising edge of OBF.

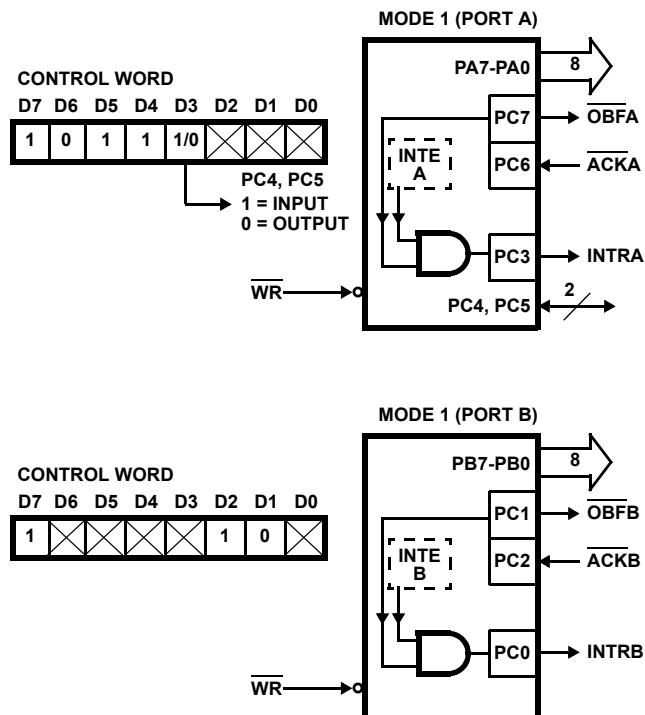


FIGURE 8. MODE 1 OUTPUT

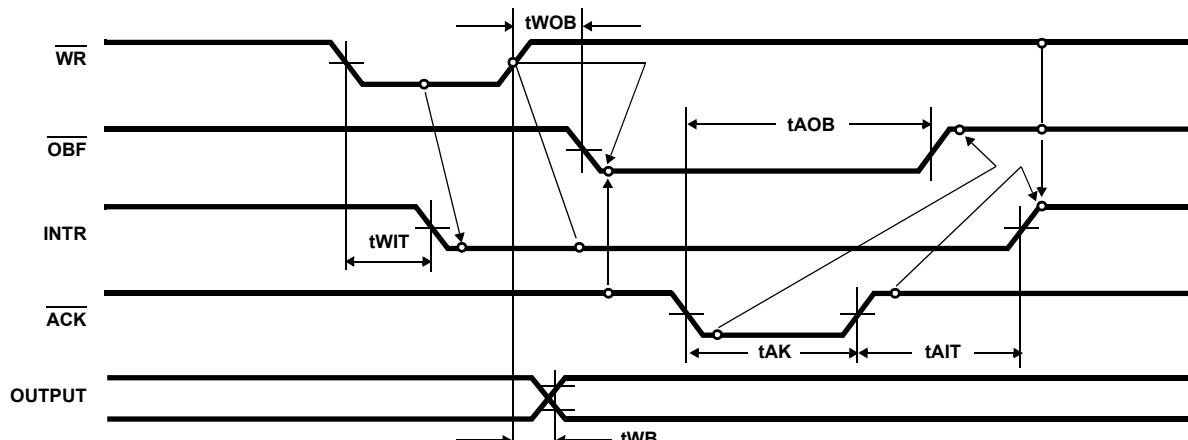
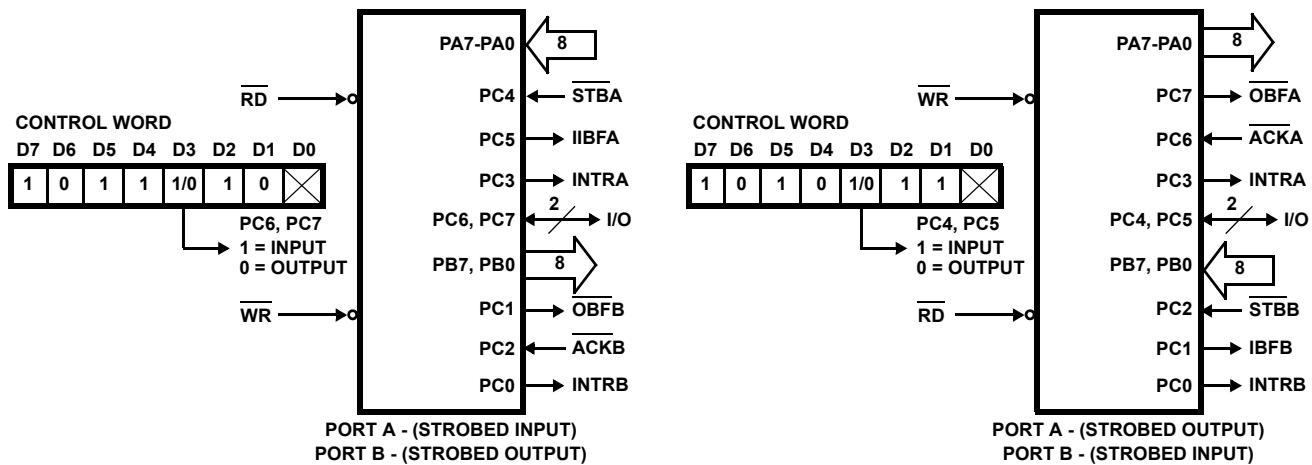


FIGURE 9. MODE 1 (STROBED OUTPUT)



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bidirectional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Hand shaking" signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bidirectional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bidirectional bus port (Port A)

Bidirectional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

OBF - (Output Buffer Full). The **OBF** output will go "low" to indicate that the CPU has written data out to port A.

ACK - (Acknowledge). A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with **OBF**). Controlled by bit set/reset of PC4.

Input Operations

STB - (Strobe Input). A "low" on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with **IBF**). Controlled by bit set/reset of PC4.

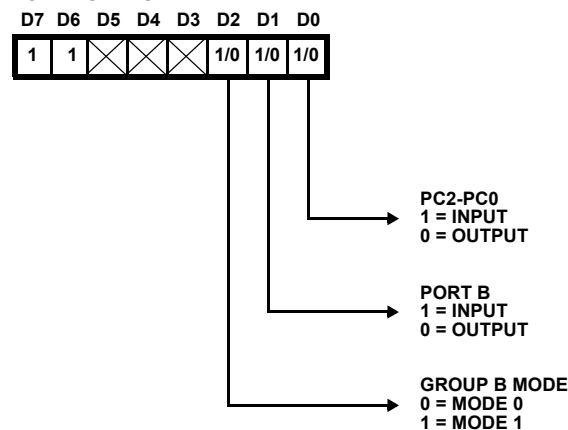
CONTROL WORD

FIGURE 11. MODE CONTROL WORD

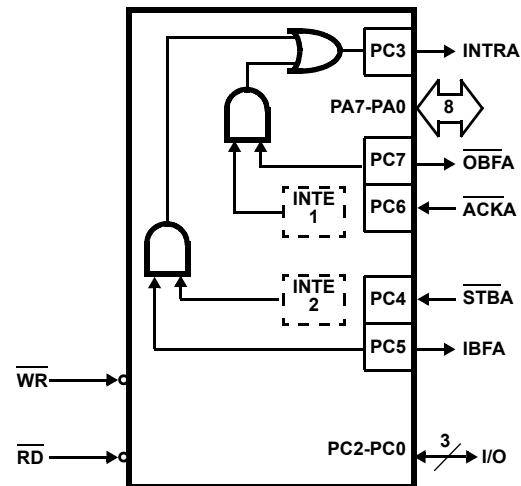


FIGURE 12. MODE 2

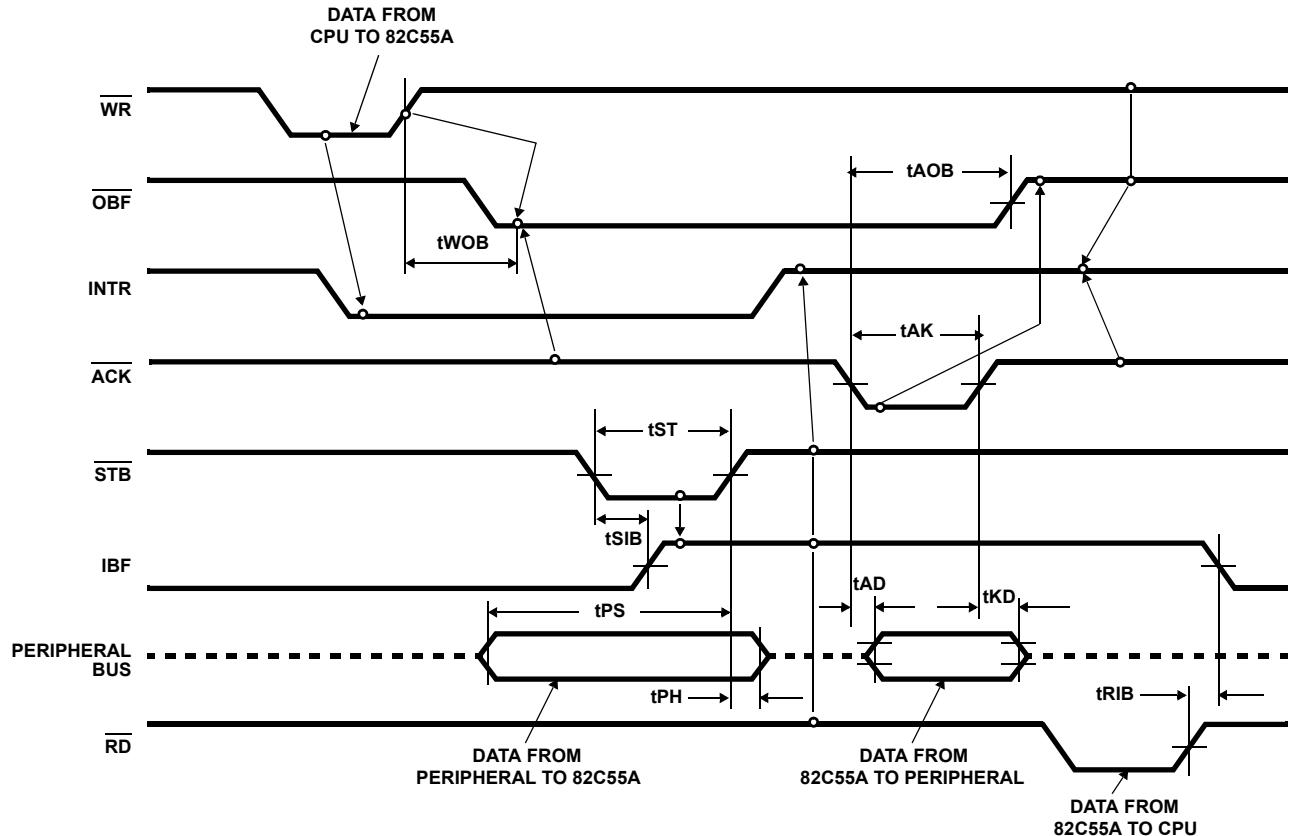
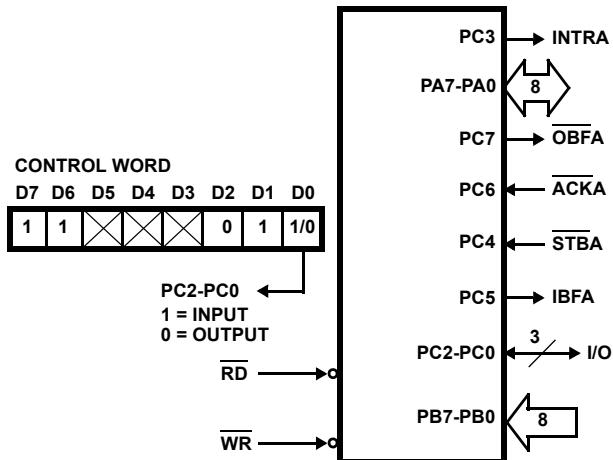
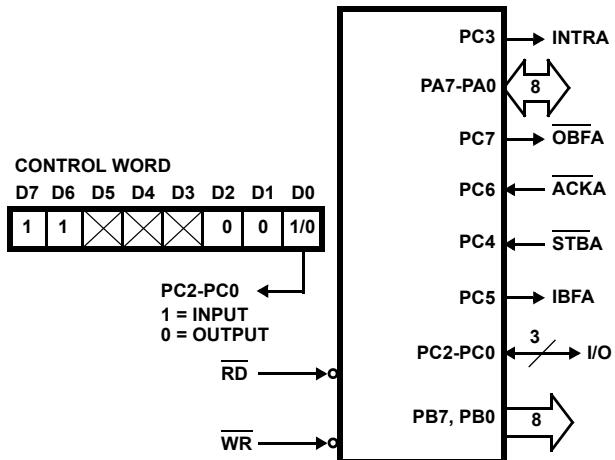


FIGURE 13. MODE 2 (BIDIRECTIONAL)

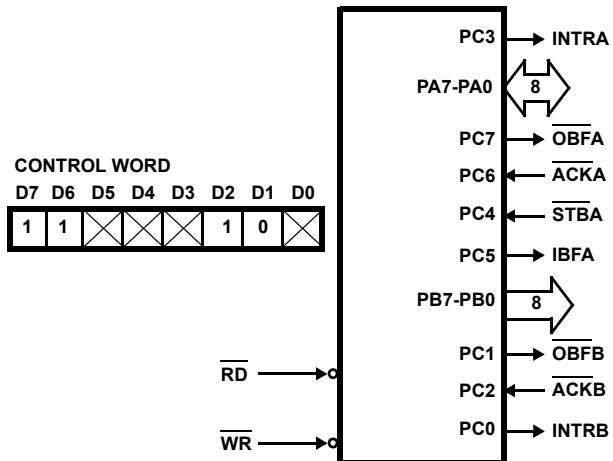
MODE 2 AND MODE 0 (INPUT)



MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)

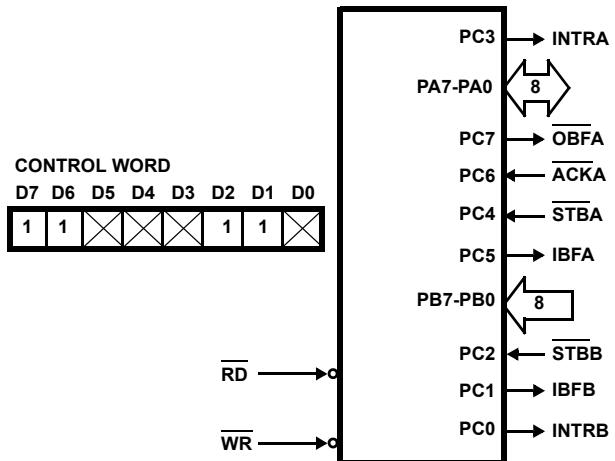
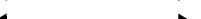
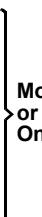


FIGURE 14. MODE 2 COMBINATIONS

MODE DEFINITION SUMMARY

| | MODE 0 | | MODE 1 | | MODE 2 |
|-----|--------|-----|--------|-------|---|
| | IN | OUT | IN | OUT | GROUP A ONLY |
| PA0 | In | Out | In | Out |  |
| PA1 | In | Out | In | Out |  |
| PA2 | In | Out | In | Out |  |
| PA3 | In | Out | In | Out |  |
| PA4 | In | Out | In | Out |  |
| PA5 | In | Out | In | Out |  |
| PA6 | In | Out | In | Out |  |
| PA7 | In | Out | In | Out |  |
| PB0 | In | Out | In | Out |  Mode 0 or Mode 1 Only |
| PB1 | In | Out | In | Out | |
| PB2 | In | Out | In | Out | |
| PB3 | In | Out | In | Out | |
| PB4 | In | Out | In | Out | |
| PB5 | In | Out | In | Out | |
| PB6 | In | Out | In | Out | |
| PB7 | In | Out | In | Out | |
| PC0 | In | Out | INTRB | INTRB | I/O |
| PC1 | In | Out | IBFB | OBFB | I/O |
| PC2 | In | Out | STBB | ACKB | I/O |
| PC3 | In | Out | INTRA | INTRA | INTRA |
| PC4 | In | Out | STBA | I/O | STBA |
| PC5 | In | Out | IBFA | I/O | IBFA |
| PC6 | In | Out | I/O | ACKA | ACKA |
| PC7 | In | Out | I/O | OBFA | OBFA |

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a “Set Mode” command.

During a read of Port C, the state of all the Port C lines, except the ACK and STB lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a “Write Port C” command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a “Write Port C” command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the “Set/Reset Port C Bit” command must be used.

With a “Set/Reset Port C Bit” command, any Port C line programmed as an output (including IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including ACK and STB lines, associated with Port C are not affected by a “Set/Reset Port C Bit” command. Writing to the corresponding Port C bit positions of the ACK and STB lines with the “Set Reset Port C Bit” command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

| INPUT CONFIGURATION | | | | | | | |
|---------------------|-----|------|-------|---------|-------|------|-------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| I/O | I/O | IBFA | INTEA | INTRA | INTEB | IBFB | INTRB |
| GROUP A | | | | GROUP B | | | |

| OUTPUT CONFIGURATION | | | | | | | | |
|----------------------|-------|-----|-----|-------|---------|------|-------|--|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| OBFA | INTEA | I/O | I/O | INTRA | INTEB | OBFB | INTRB | |
| GROUP A | | | | | GROUP B | | | |

FIGURE 15. MODE 1 STATUS WORD FORMAT

FIGURE 16 MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes

1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is not a special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

| INTERRUPT ENABLE FLAG | POSITION | ALTERNATE PORT C PIN SIGNAL (MODE) |
|--------------------------|----------|--|
| INTE B | PC2 | ACKB (Output Mode 1) or STBB (Input Mode 1) |
| INTE A2 | PC4 | STBA (Input Mode 1 or Mode 2) |
| INTE A1 | PC6 | ACKA (Output Mode 1 or Mode 2) |

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

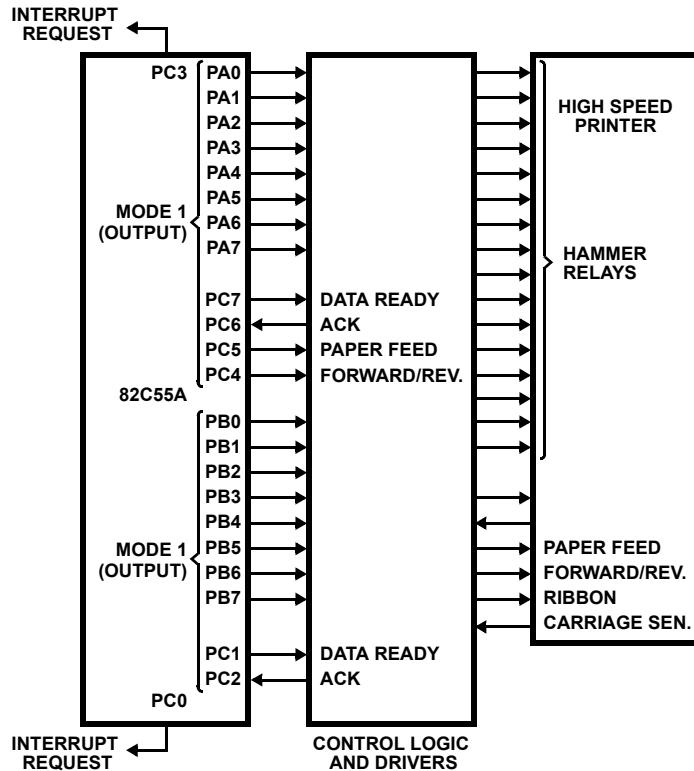
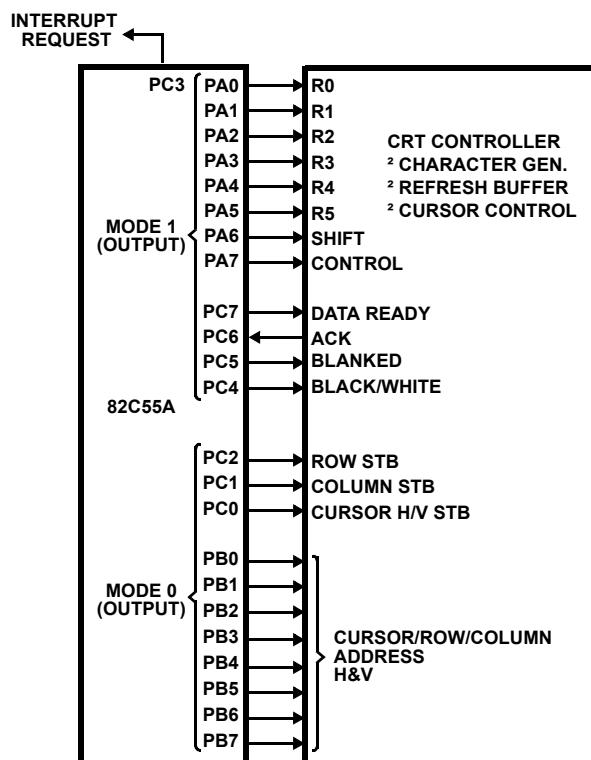
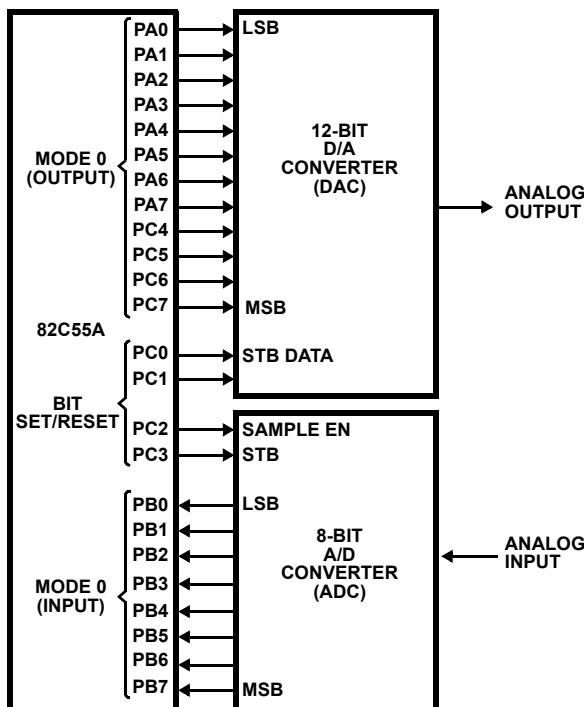
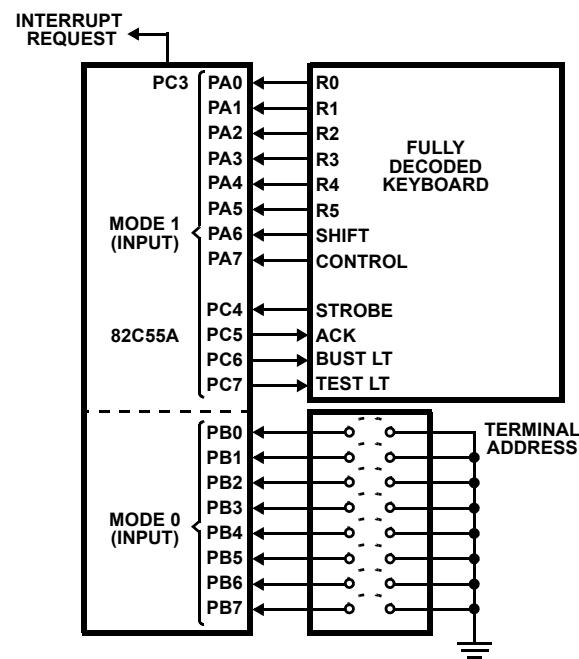
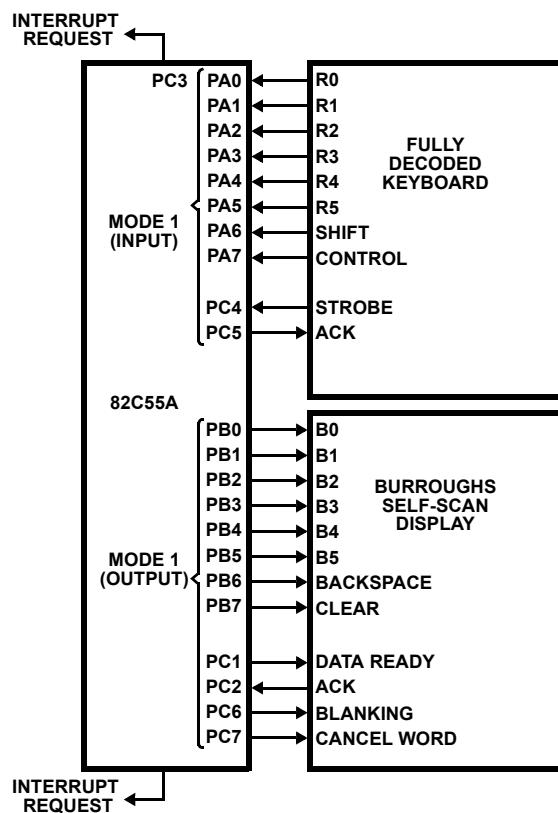


FIGURE 18. PRINTER INTERFACE



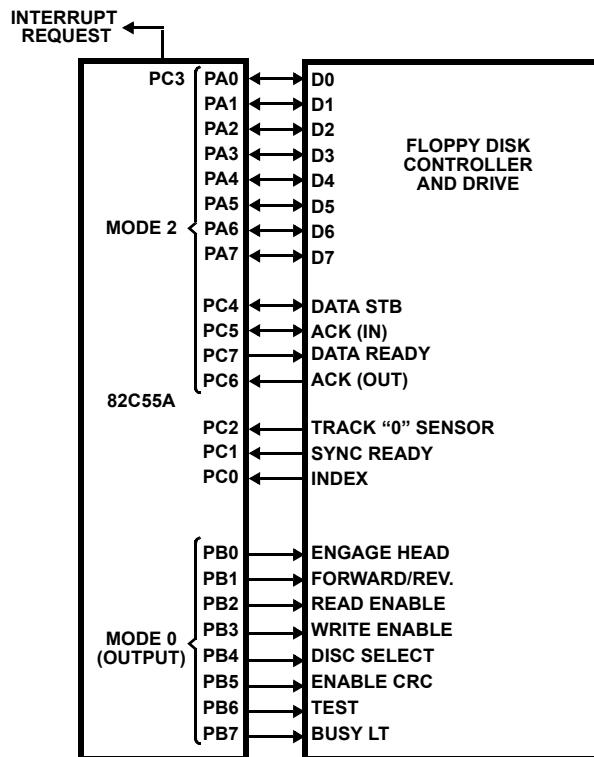


FIGURE 23. BASIC FLOPPY DISC INTERFACE

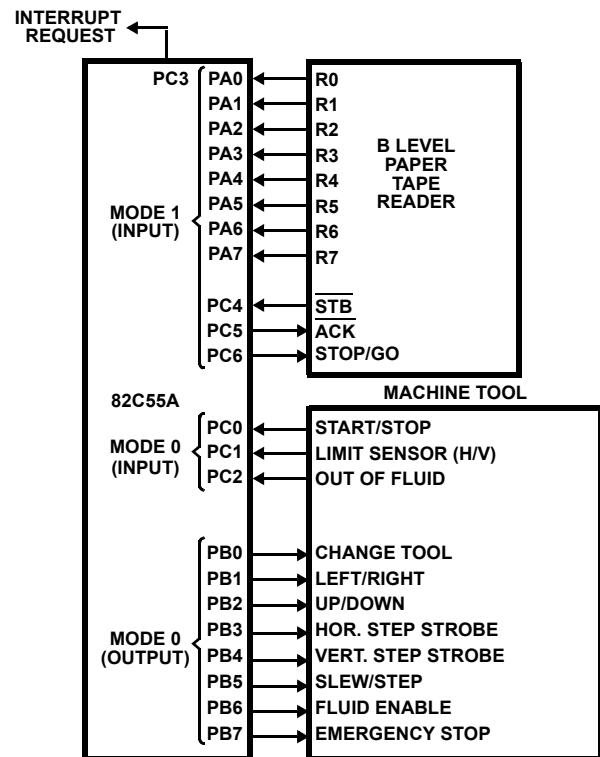


FIGURE 24. MACHINE TOOL CONTROLLER INTERFACE

Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

| | |
|-----------------------------------|----------------------------------|
| Supply Voltage..... | +8.0V |
| Input, Output or I/O Voltage..... | GND-0.5V to $V_{CC}+0.5\text{V}$ |
| ESD Classification..... | Class 1 |

Operating Conditions

| | |
|-----------------------------|----------------|
| Voltage Range..... | +4.5V to 5.5V |
| Operating Temperature Range | |
| CX82C55A..... | 0°C to 70°C |
| IX82C55A..... | -40°C to 85°C |
| MX82C55A..... | -55°C to 125°C |

Die Characteristics

| | |
|-----------------|------------|
| Gate Count..... | 1000 Gates |
|-----------------|------------|

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{CC} = 5.0\text{V} \pm 10\%$; T_A = Operating Temperature Range

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | MAX | UNITS |
|----------|--------------------------------|---|-----------------------|-----------|---------------|
| V_{IH} | Logical One Input Voltage | | 2.0 2.2 | - | V |
| V_{IL} | Logical Zero Input Voltage | | - | 0.8 | V |
| V_{OH} | Logical One Output Voltage | $I_{OH} = -2.5\text{mA}$, $I_{OH} = -100\mu\text{A}$ | 3.0 $V_{CC} - 0.4$ | - | V |
| V_{OL} | Logical Zero Output Voltage | $I_{OL} +2.5\text{mA}$ | - | 0.4 | V |
| I_I | Input Leakage Current | $V_{IN} = V_{CC}$ or GND, \overline{RD} , \overline{CS} , A1, A0, RESET, WR | -1.0 | +1.0 | μA |
| IO | I/O Pin Leakage Current | $VO = V_{CC}$ or GND, D0 - D7 | -10 | +10 | μA |
| IBHH | Bus Hold High Current | $VO = 3.0\text{V}$. Ports A, B, C | | | |
| | | $T_A = -55^\circ\text{C}$ | -50 | -450 | μA |
| IBHL | Bus Hold Low Current | $VO = 1.0\text{V}$. Port A ONLY | | | |
| | | $T_A = -55^\circ\text{C}$ | 50 | 450 | μA |
| | | $T_A = +128^\circ\text{C}$ | 50 | 400 | μA |
| IDAR | Darlington Drive Current | Ports A, B, C. Test Condition 3 | -2.5 | Note 2, 4 | mA |
| ICCSB | Standby Power Supply Current | $V_{CC} = 5.5\text{V}$, $V_{IN} = V_{CC}$ or GND. Output Open | - | 10 | μA |
| ICCOP | Operating Power Supply Current | $T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, Typical (See Note 3) | - | 1 | mA/MHz |

NOTES:

2. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
3. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: $1.0\mu\text{s}$ I/O Read/Write cycle time = 1mA).
4. Tested as V_{OH} at -2.5mA.

Capacitance $T_A = +25^\circ\text{C}$

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|--------|-------------------|---------|-------|--|
| CIN | Input Capacitance | 10 | pF | FREQ = 1MHz, All Measurements are referenced to device GND |
| CI/O | I/O Capacitance | 20 | pF | |

AC Electrical Specifications V_{CC} = +5V± 10%, GND = 0V; T_A = Operating Temperature Range

| SYMBOL | PARAMETER | 82C55A-5 | | 82C55A | | UNITS | TEST CONDITIONS |
|---------------------|---|----------|-----|--------|-----|-------|-----------------|
| | | MIN | MAX | MIN | MAX | | |
| READ TIMING | | | | | | | |
| (1) tAR | Address Stable Before \overline{RD} | 0 | - | 0 | - | ns | |
| (2) tRA | Address Stable After \overline{RD} | 0 | - | 0 | - | ns | |
| (3) tRR | \overline{RD} Pulse Width | 250 | - | 150 | - | ns | |
| (4) tRD | Data Valid From \overline{RD} | - | 200 | - | 120 | ns | 1 |
| (5) tDF | Data Float After \overline{RD} | 10 | 75 | 10 | 75 | ns | 2 |
| (6) tRV | Time Between \overline{RD} s and/or \overline{WR} s | 300 | - | 300 | - | ns | |
| WRITE TIMING | | | | | | | |
| (7) tAW | Address Stable Before \overline{WR} | 0 | - | 0 | - | ns | |
| (8) tWA | Address Stable After \overline{WR} | 20 | - | 20 | - | ns | |
| (9) tWW | \overline{WR} Pulse Width | 100 | - | 100 | - | ns | |
| (10) tDW | Data Valid to \overline{WR} High | 100 | - | 100 | - | ns | |
| (11) tWD | Data Valid After \overline{WR} High | 30 | - | 30 | - | ns | |
| OTHER TIMING | | | | | | | |
| (12) tWB | \overline{WR} = 1 to Output | - | 350 | - | 350 | ns | 1 |
| (13) tIR | Peripheral Data Before \overline{RD} | 0 | - | 0 | - | ns | |
| (14) tHR | Peripheral Data After \overline{RD} | 0 | - | 0 | - | ns | |
| (15) tAK | ACK Pulse Width | 200 | - | 200 | - | ns | |
| (16) tST | STB Pulse Width | 100 | - | 100 | - | ns | |
| (17) tPS | Peripheral Data Before STB High | 20 | - | 20 | - | ns | |
| (18) tPH | Peripheral Data After STB High | 50 | - | 50 | - | ns | |
| (19) tAD | ACK = 0 to Output | - | 175 | - | 175 | ns | 1 |
| (20) tKD | ACK = 1 to Output Float | 20 | 250 | 20 | 250 | ns | 2 |
| (21) tWOB | \overline{WR} = 1 to OBF = 0 | - | 150 | - | 150 | ns | 1 |
| (22) tAOB | ACK = 0 to OBF = 1 | - | 150 | - | 150 | ns | 1 |
| (23) tSIB | STB = 0 to IBF = 1 | - | 150 | - | 150 | ns | 1 |
| (24) tRIB | \overline{RD} = 1 to IBF = 0 | - | 150 | - | 150 | ns | 1 |
| (25) tRIT | \overline{RD} = 0 to INTR = 0 | - | 200 | - | 200 | ns | 1 |
| (26) tSIT | STB = 1 to INTR = 1 | - | 150 | - | 150 | ns | 1 |
| (27) tAIT | ACK = 1 to INTR = 1 | - | 150 | - | 150 | ns | 1 |
| (28) tWIT | \overline{WR} = 0 to INTR = 0 | - | 200 | - | 200 | ns | 1 |
| (29) tRES | Reset Pulse Width | 500 | - | 500 | - | ns | 1, (Note) |

NOTE: Period of initial Reset pulse after power-on must be at least 50 μ sec. Subsequent Reset pulses may be 500ns minimum.

Timing Waveforms

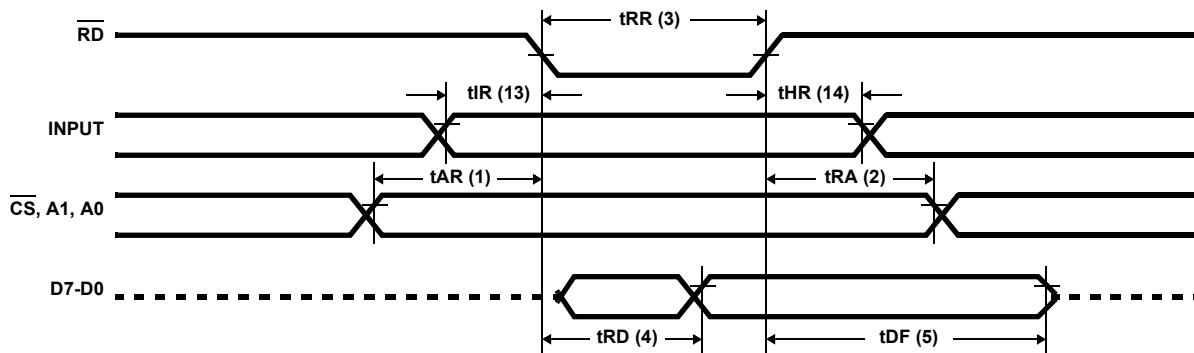


FIGURE 25. MODE 0 (BASIC INPUT)

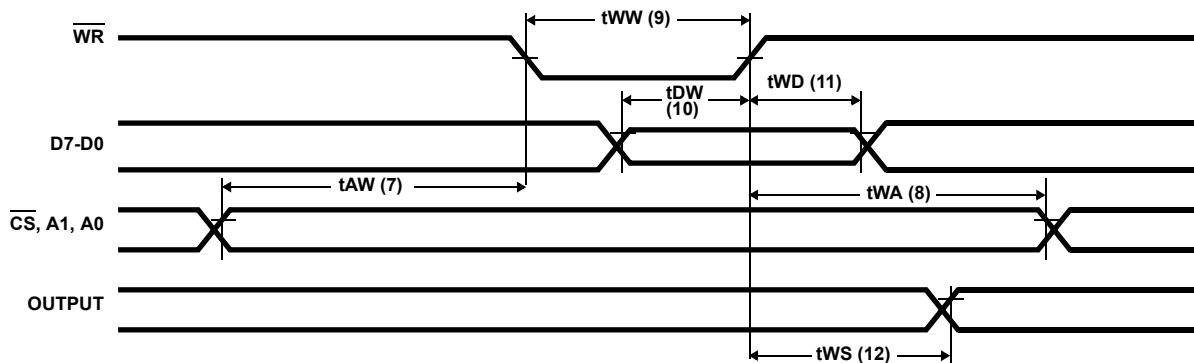


FIGURE 26. MODE 0 (BASIC OUTPUT)

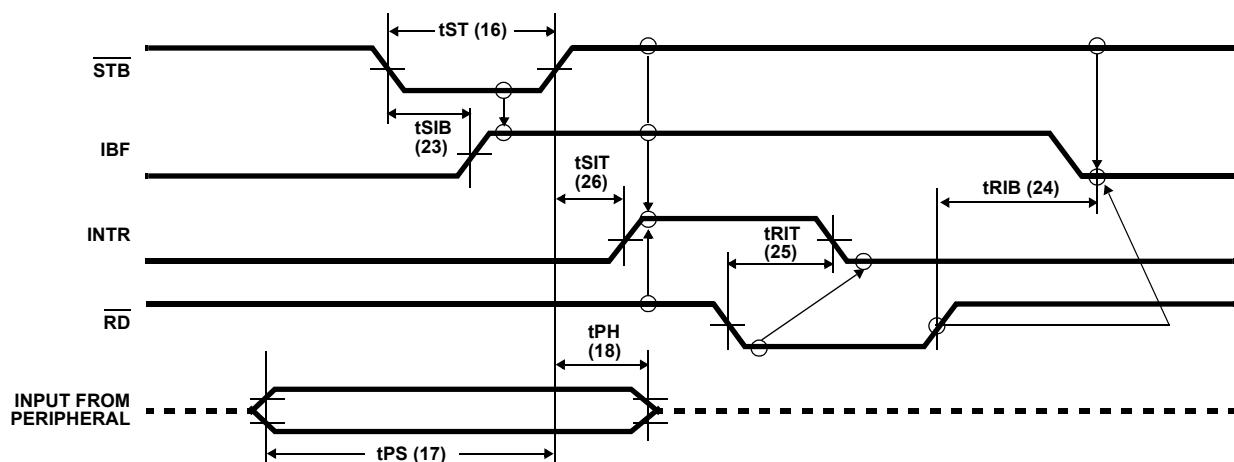


FIGURE 27. MODE 1 (STROBED INPUT)

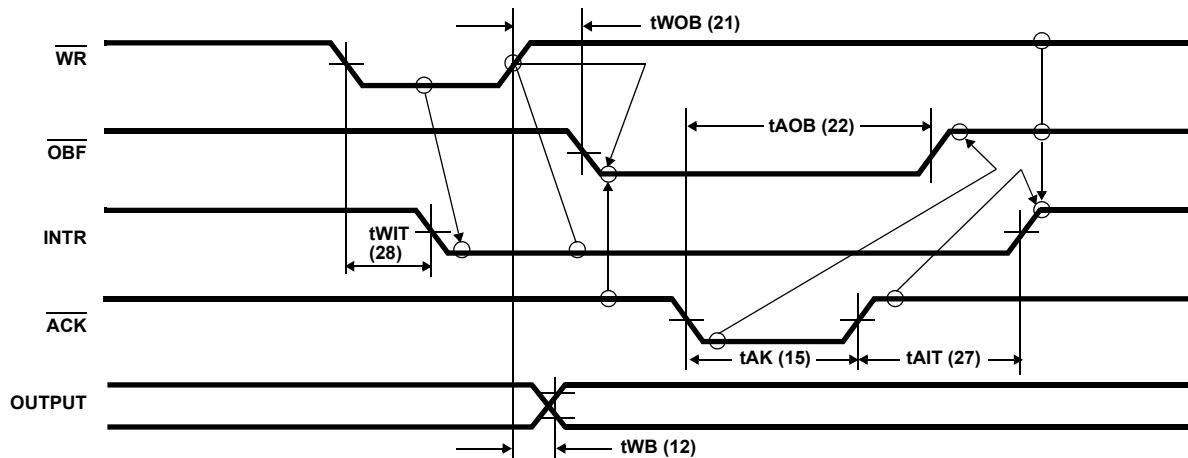
Timing Waveforms (Continued)

FIGURE 28. MODE 1 (STROBED OUTPUT)

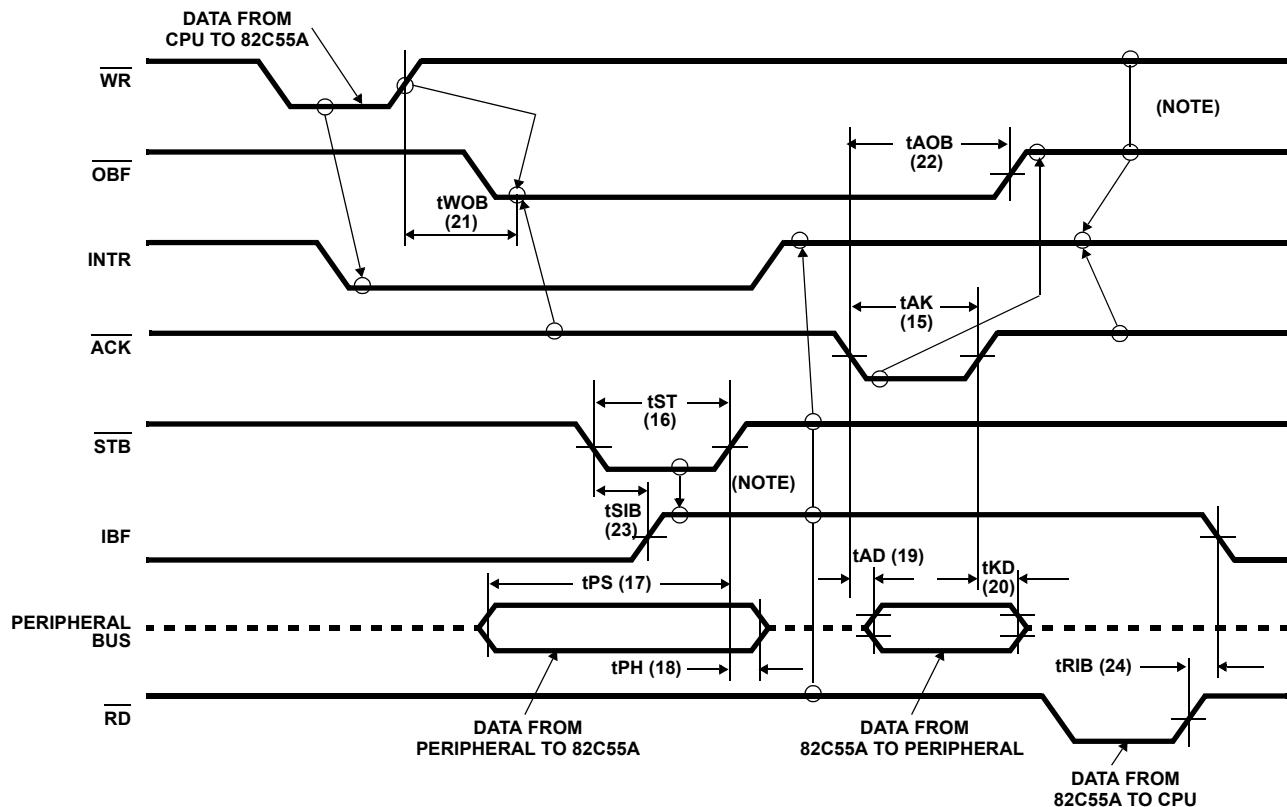


FIGURE 29. MODE 2 (BIDIRECTIONAL)

NOTE: Any sequence where **WR** occurs before **ACK** and **STB** occurs before **RD** is permissible. (**INTR** = **IBF** • **MASK** • **STB** • **RD** + **OBF** • **MASK** • **ACK** • **WR**)

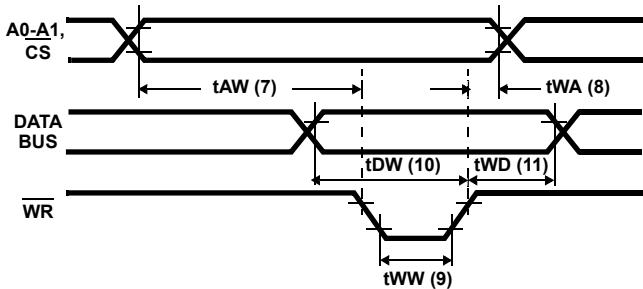
Timing Waveforms (Continued)

FIGURE 30. WRITE TIMING

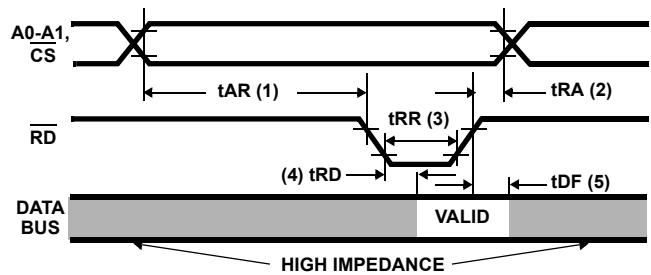
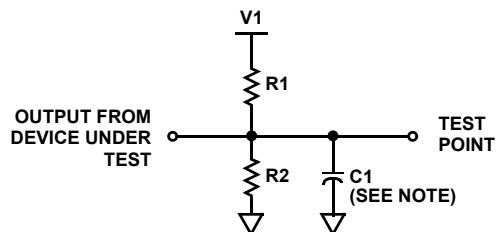
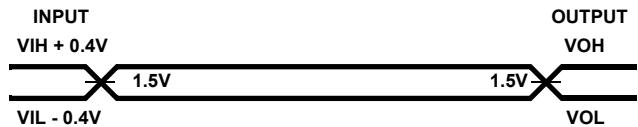


FIGURE 31. READ TIMING

AC Test Circuit

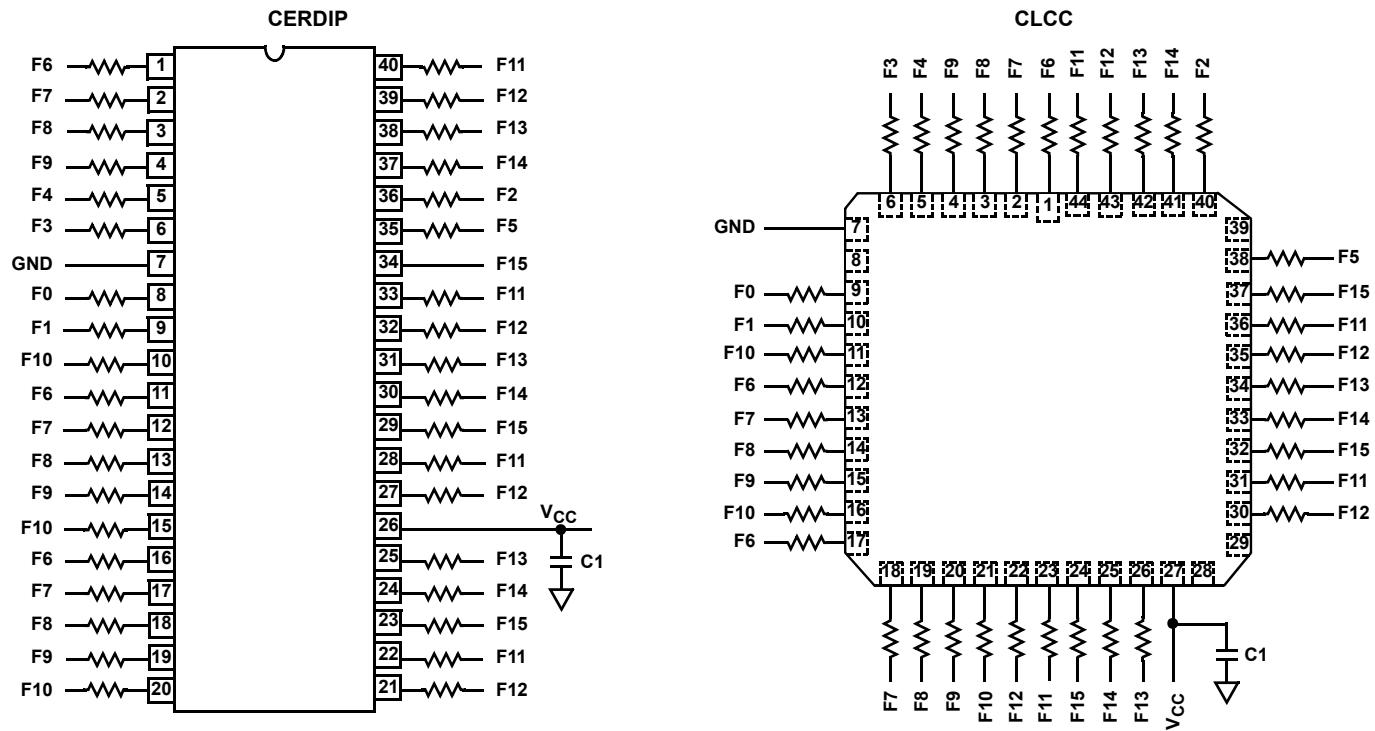
NOTE: Includes STRAY and JIG Capacitance

AC Testing Input, Output Waveforms

AC Testing: All AC Parameters tested as per test circuits. Input RISE and FALL times are driven at 1ns/V.

TEST CONDITION DEFINITION TABLE

| TEST CONDITION | V1 | R1 | R2 | C1 |
|----------------|-----------------|------|-------|-------|
| 1 | 1.7V | 523Ω | Open | 150pF |
| 2 | V _{CC} | 2kΩ | 1.7kΩ | 50pF |
| 3 | 1.5V | 750Ω | Open | 50pF |

Burn-In Circuits

NOTES:

1. V_{CC} = 5.5V ± 0.5V
2. VIH = 4.5V ± 10%
3. Vil = -0.2V to 0.4V
4. GND = 0V

NOTES:

1. C1 = 0.01µF minimum
2. All resistors are 47kΩ ± 5%
3. f0 = 100kHz ± 10%
4. f1 = f0 ÷ 2; f2 = f1 ÷ 2; . . . ; f15 = f14 ÷ 2

Die Characteristics**METALLIZATION:**

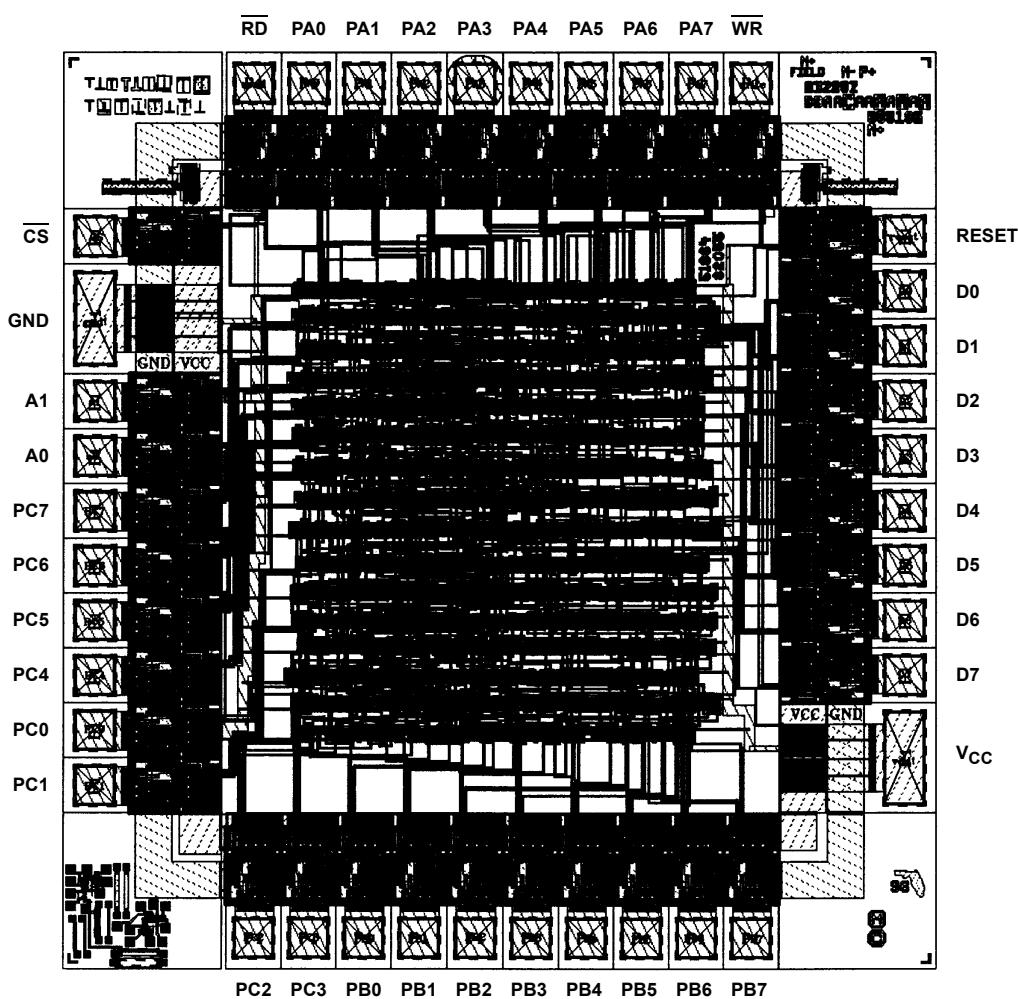
Type: Silicon - Aluminum
Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2
Thickness: $8\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Metallization Mask Layout

82C55A



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|------------------|-----------|--|
| December 8, 2015 | FN2969.11 | - Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. |

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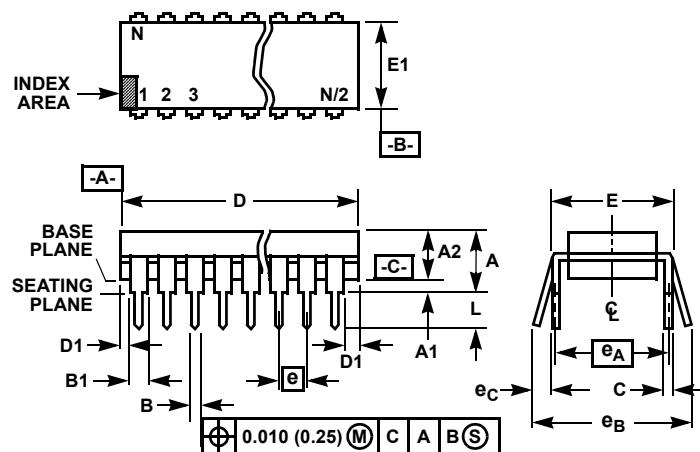
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Dual-In-Line Plastic Packages (PDIP)

NOTES:

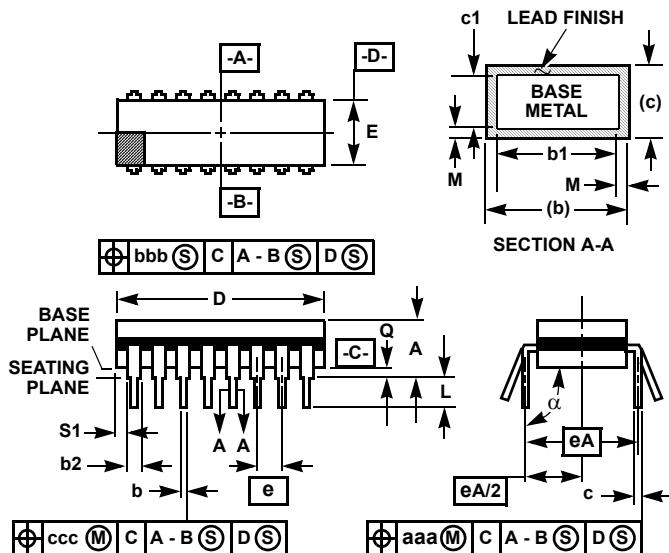
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.250 | - | 6.35 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.125 | 0.195 | 3.18 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.030 | 0.070 | 0.77 | 1.77 | 8 |
| C | 0.008 | 0.015 | 0.204 | 0.381 | - |
| D | 1.980 | 2.095 | 50.3 | 53.2 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.600 | 0.625 | 15.24 | 15.87 | 6 |
| E1 | 0.485 | 0.580 | 12.32 | 14.73 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| e_A | 0.600 BSC | | 15.24 BSC | | 6 |
| e_B | - | 0.700 | - | 17.78 | 7 |
| L | 0.115 | 0.200 | 2.93 | 5.08 | 4 |
| N | 40 | | 40 | | 9 |

Rev. 0 12/93

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



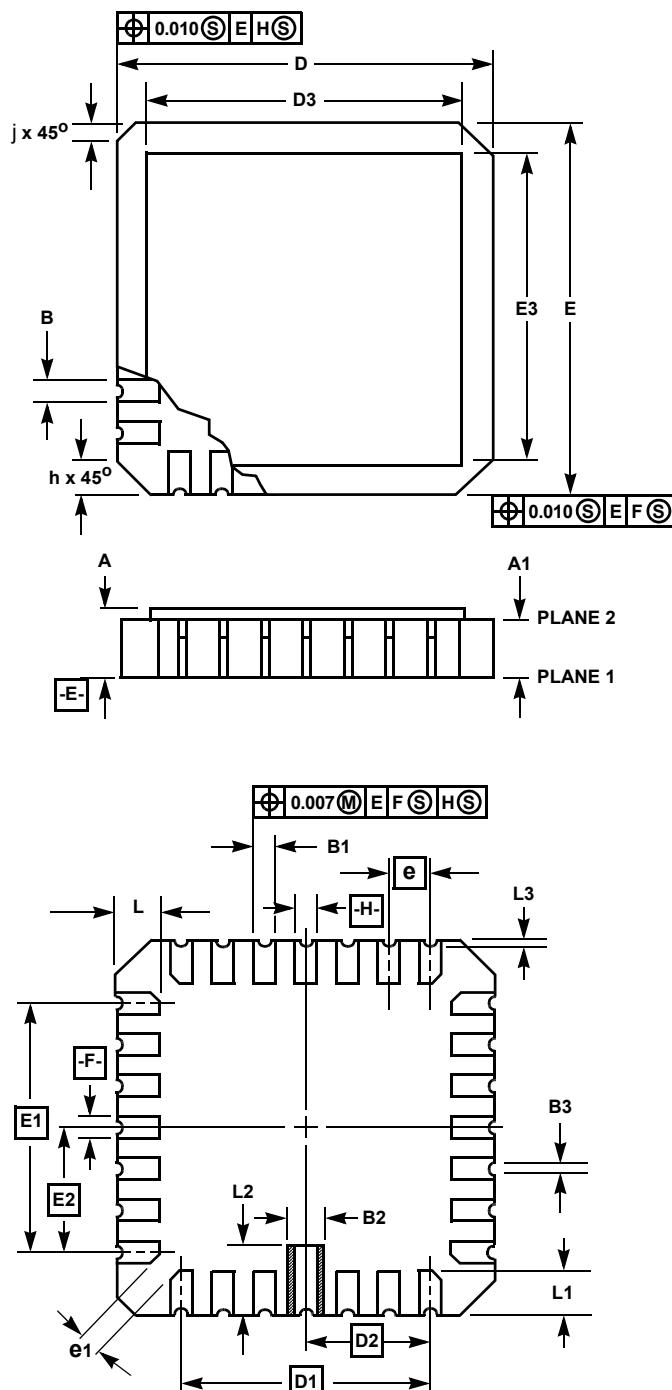
NOTES:

- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- This dimension allows for off-center lid, meniscus, and glass overrun.
- Dimension Q shall be measured from the seating plane to the base plane.
- Measure dimension S1 at all four corners.
- N is the maximum number of terminal positions.
- Dimensioning and tolerancing per ANSI Y14.5M - 1982.
- Controlling dimension: INCH.

**F40.6 MIL-STD-1835 GDIP1-T40 (D-5, CONFIGURATION A)
40 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.225 | - | 5.72 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 2.096 | - | 53.24 | 5 |
| E | 0.510 | 0.620 | 12.95 | 15.75 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.600 BSC | | 15.24 BSC | | - |
| eA/2 | 0.300 BSC | | 7.62 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.070 | 0.38 | 1.78 | 6 |
| S1 | 0.005 | - | 0.13 | - | 7 |
| alpha | 90° | 105° | 90° | 105° | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2, 3 |
| N | 40 | | 40 | | 8 |

Rev. 0 4/94

Ceramic Leadless Chip Carrier Packages (CLCC)

**J44.A MIL-STD-1835 CQCC1-N44 (C-5)
44 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE**

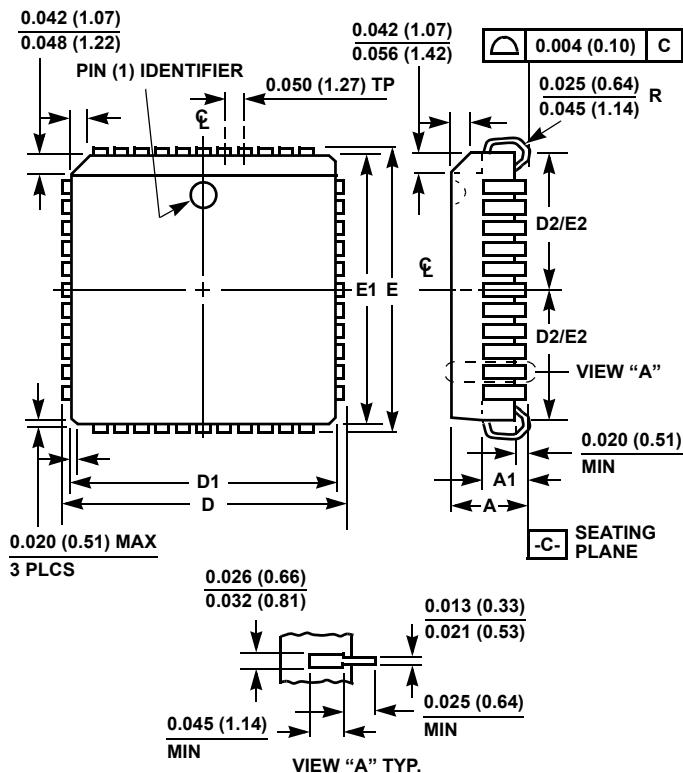
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.064 | 0.120 | 1.63 | 3.05 | 6, 7 |
| A1 | 0.054 | 0.088 | 1.37 | 2.24 | - |
| B | 0.033 | 0.039 | 0.84 | 0.99 | 4 |
| B1 | 0.022 | 0.028 | 0.56 | 0.71 | 2, 4 |
| B2 | 0.072 REF | | 1.83 REF | | - |
| B3 | 0.006 | 0.022 | 0.15 | 0.56 | - |
| D | 0.640 | 0.662 | 16.26 | 16.81 | - |
| D1 | 0.500 BSC | | 12.70 BSC | | - |
| D2 | 0.250 BSC | | 6.35 BSC | | - |
| D3 | - | 0.662 | - | 16.81 | 2 |
| E | 0.640 | 0.662 | 16.26 | 16.81 | - |
| E1 | 0.500 BSC | | 12.70 BSC | | - |
| E2 | 0.250 BSC | | 6.35 BSC | | - |
| E3 | - | 0.662 | - | 16.81 | 2 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| e1 | 0.015 | - | 0.38 | - | 2 |
| h | 0.040 REF | | 1.02 REF | | 5 |
| j | 0.020 REF | | 0.51 REF | | 5 |
| L | 0.045 | 0.055 | 1.14 | 1.40 | - |
| L1 | 0.045 | 0.055 | 1.14 | 1.40 | - |
| L2 | 0.075 | 0.095 | 1.90 | 2.41 | - |
| L3 | 0.003 | 0.015 | 0.08 | 0.38 | - |
| ND | 11 | | 11 | | 3 |
| NE | 11 | | 11 | | 3 |
| N | 44 | | 44 | | 3 |

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Plastic Leaded Chip Carrier Packages (PLCC)



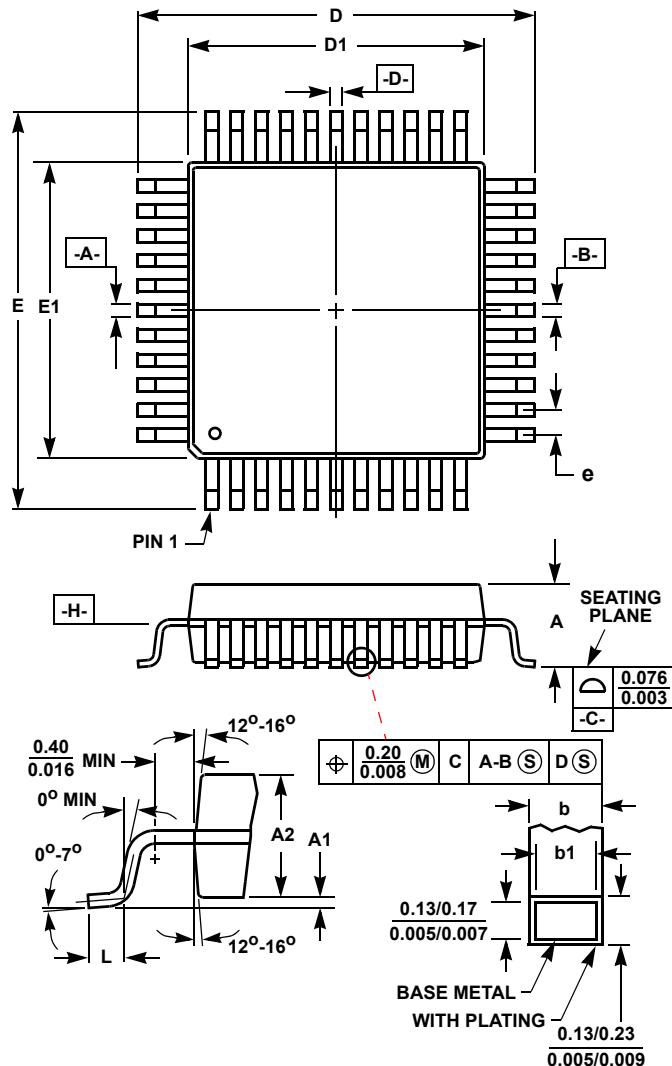
N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.165 | 0.180 | 4.20 | 4.57 | - |
| A1 | 0.090 | 0.120 | 2.29 | 3.04 | - |
| D | 0.685 | 0.695 | 17.40 | 17.65 | - |
| D1 | 0.650 | 0.656 | 16.51 | 16.66 | 3 |
| D2 | 0.291 | 0.319 | 7.40 | 8.10 | 4, 5 |
| E | 0.685 | 0.695 | 17.40 | 17.65 | - |
| E1 | 0.650 | 0.656 | 16.51 | 16.66 | 3 |
| E2 | 0.291 | 0.319 | 7.40 | 8.10 | 4, 5 |
| N | 44 | | 44 | | 6 |

Rev. 2 11/97

NOTES:

- Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
- Dimensions and tolerancing per ANSI Y14.5M-1982.
- Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
- To be measured at seating plane [-C-] contact point.
- Centerline to be determined where center leads exit plastic body.
- "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)

**Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.096 | - | 2.45 | - |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 | - |
| A2 | 0.077 | 0.083 | 1.95 | 2.10 | - |
| b | 0.012 | 0.018 | 0.30 | 0.45 | 6 |
| b1 | 0.012 | 0.016 | 0.30 | 0.40 | - |
| D | 0.515 | 0.524 | 13.08 | 13.32 | 3 |
| D1 | 0.389 | 0.399 | 9.88 | 10.12 | 4, 5 |
| E | 0.516 | 0.523 | 13.10 | 13.30 | 3 |
| E1 | 0.390 | 0.398 | 9.90 | 10.10 | 4, 5 |
| L | 0.029 | 0.040 | 0.73 | 1.03 | - |
| N | 44 | | 44 | | 7 |
| e | 0.032 BSC | | 0.80 BSC | | - |

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane [-C-].
4. Dimensions D1 and E1 to be determined at datum plane [-H-].
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

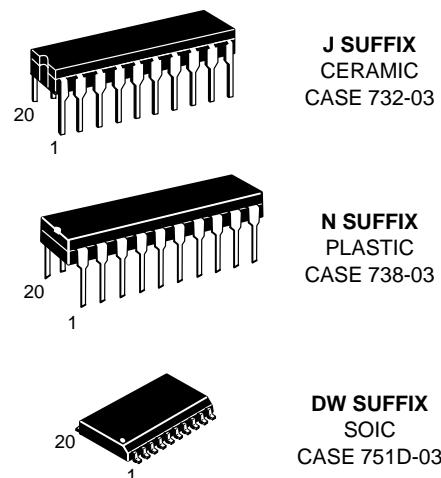
| | | LOADING (Note a) | |
|--------------------------------|--------------------------------------|------------------|---------------|
| | | HIGH | LOW |
| D ₀ -D ₇ | Data Inputs | 0.5 U.L. | 0.25 U.L. |
| LE | Latch Enable (Active HIGH) Input | 0.5 U.L. | 0.25 U.L. |
| CP | Clock (Active HIGH going edge) Input | 0.5 U.L. | 0.25 U.L. |
| OE | Output Enable (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| O ₀ -O ₇ | Outputs (Note b) | 65 (25) U.L. | 15 (7.5) U.L. |

NOTES:

- 1 TTL Units Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS373 SN54/74LS374

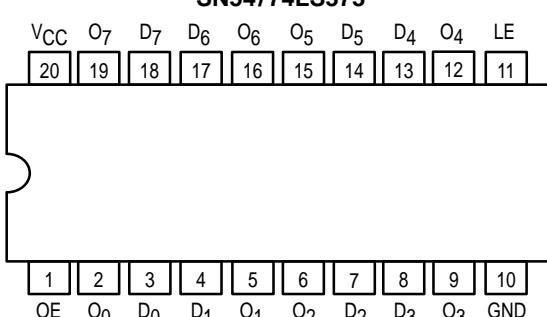
OCTAL TRANSPARENT LATCH
WITH 3-STATE OUTPUTS;
OCTAL D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUT
LOW POWER SCHOTTKY



ORDERING INFORMATION

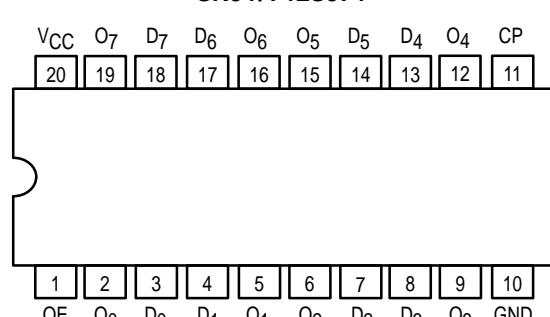
SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

SN54/74LS373



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram)
as the Dual In-Line Package.

SN54/74LS374



SN54/74LS373 • SN54/74LS374

TRUTH TABLE

LS373

| D _n | LE | OE | O _n |
|----------------|----|----|----------------|
| H | H | L | H |
| L | H | L | L |
| X | L | L | Q ₀ |
| X | X | H | Z* |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

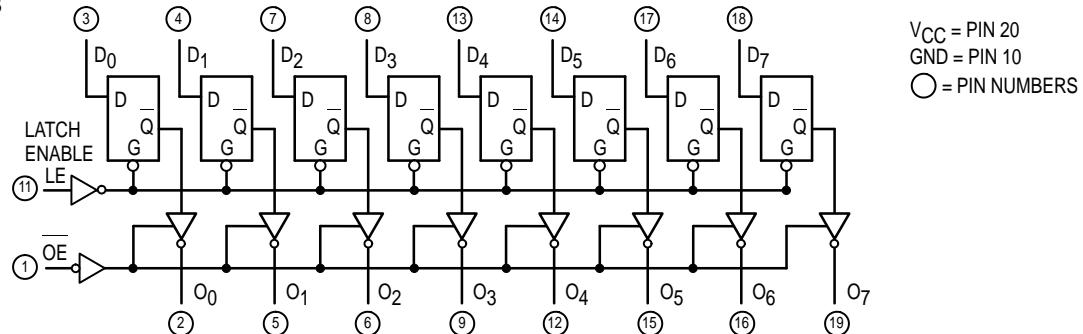
LS374

| D _n | LE | OE | O _n |
|----------------|----|----|----------------|
| H | — | L | H |
| L | — | L | L |
| X | X | H | Z* |

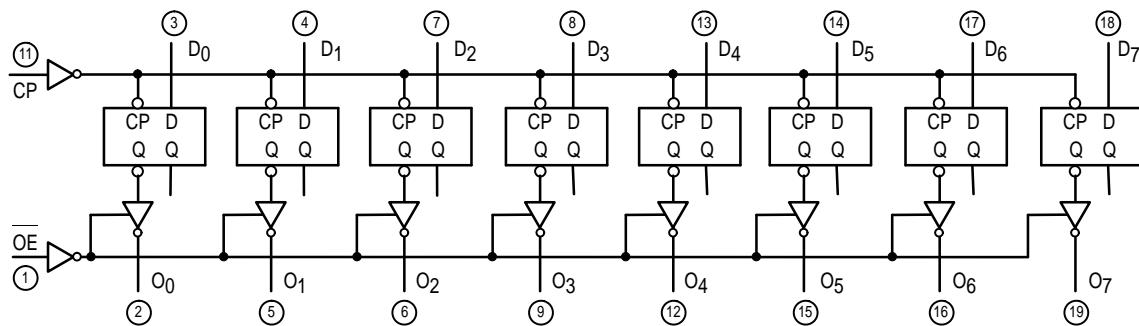
* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

LOGIC DIAGRAMS

SN54LS/74LS373



SN54LS/74LS374



GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|--|----------|-------------|--------------|------|
| V _{CC} | Supply Voltage | | 54 74 | 4.5 4.75 | 5.0 5.0 | V |
| T _A | Operating Ambient Temperature Range | | 54 74 | -55 0 | 25 25 | °C |
| I _{OH} | Output Current — High | | 54 74 | | -1.0 -2.6 | mA |
| I _{OL} | Output Current — Low | | 54 74 | | 12 24 | mA |

SN54/74LS373 • SN54/74LS374

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|------------------|--------------------------------|--------|-------|------|------|--|
| | | Min | Typ | Max | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| V _{IL} | Input LOW Voltage | 54 | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs |
| | | 74 | | 0.8 | | |
| V _{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 54 | 2.4 | 3.4 | V | V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table |
| | | 74 | 2.4 | 3.1 | | |
| V _{OL} | Output LOW Voltage | 54, 74 | | 0.25 | V | I _{OL} = 12 mA |
| | | 74 | | 0.35 | V | I _{OL} = 24 mA |
| I _{OZH} | Output Off Current HIGH | | | 20 | µA | V _{CC} = MAX, V _{OUT} = 2.7 V |
| I _{OZL} | Output Off Current LOW | | | -20 | µA | V _{CC} = MAX, V _{OUT} = 0.4 V |
| I _{IH} | Input HIGH Current | | | 20 | µA | V _{CC} = MAX, V _{IN} = 2.7 V |
| | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V |
| I _{IL} | Input LOW Current | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V |
| I _{OS} | Short Circuit Current (Note 1) | -30 | | -130 | mA | V _{CC} = MAX |
| I _{CC} | Power Supply Current | | | 40 | mA | V _{CC} = MAX |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

| Symbol | Parameter | Limits | | | | | | Unit | Test Conditions | | |
|--------------------------------------|--------------------------------------|--------|----------|----------|-------|----------|----------|------|---|--|--|
| | | LS373 | | | LS374 | | | | | | |
| | | Min | Typ | Max | Min | Typ | Max | | | | |
| f _{MAX} | Maximum Clock Frequency | | | | 35 | 50 | | MHz | $C_L = 45 \text{ pF}$, $R_L = 667 \Omega$ | | |
| t _{PLH} t _{PHL} | Propagation Delay, Data to Output | | 12 12 | 18 18 | | | | ns | | | |
| t _{PLH} t _{PHL} | Clock or Enable to Output | | 20 18 | 30 30 | | 15 19 | 28 28 | ns | | | |
| t _{PZH} t _{PZL} | Output Enable Time | | 15 25 | 28 36 | | 20 21 | 28 28 | ns | | | |
| t _{PHZ} t _{PLZ} | Output Disable Time | | 12 15 | 20 25 | | 12 15 | 20 25 | ns | $C_L = 5.0 \text{ pF}$ | | |

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

| Symbol | Parameter | Limits | | | | | | Unit | |
|----------------|-------------------|--------|-----|-----|-------|-----|-----|------|--|
| | | LS373 | | | LS374 | | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| t _W | Clock Pulse Width | | 15 | | | 15 | | ns | |
| t _S | Setup Time | | 5.0 | | | 20 | | ns | |
| t _H | Hold Time | | 20 | | | 0 | | ns | |

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN54/74LS373

AC WAVEFORMS

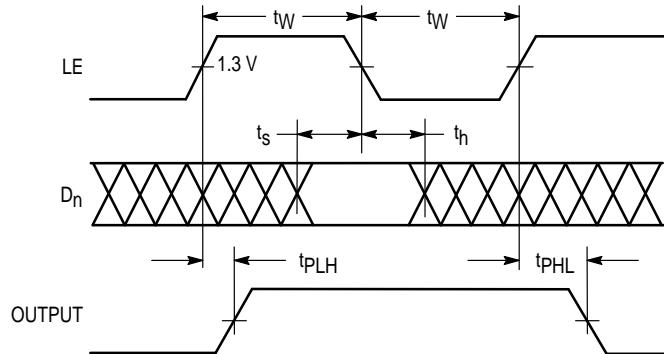


Figure 1

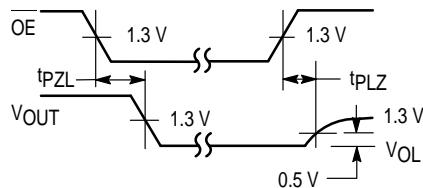


Figure 2

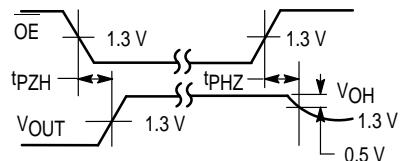
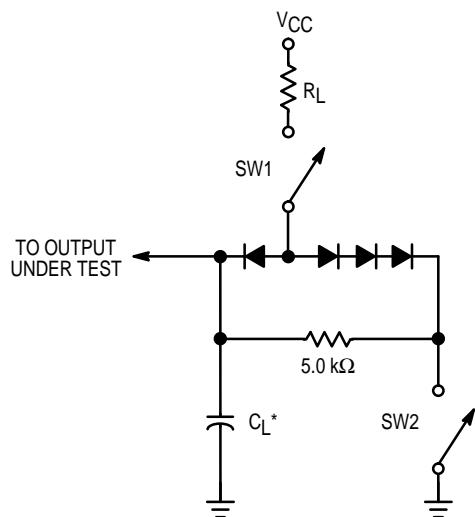


Figure 3

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

| SYMBOL | SW1 | SW2 |
|-----------|--------|--------|
| t_{PZH} | Open | Closed |
| t_{PZL} | Closed | Open |
| t_{PLZ} | Closed | Closed |
| t_{PHZ} | Closed | Closed |

Figure 4

SN54/74LS374

AC WAVEFORMS

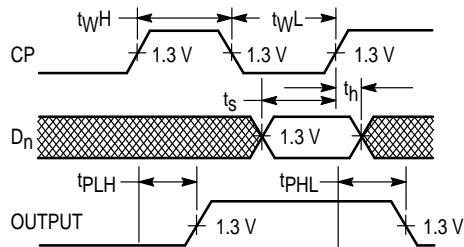


Figure 5

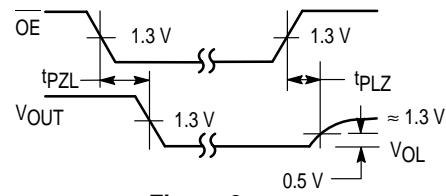


Figure 6

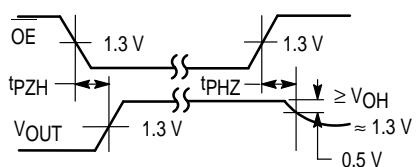
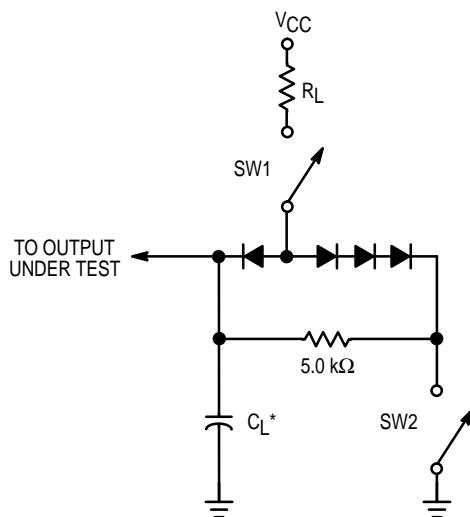


Figure 7

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

| SYMBOL | SW1 | SW2 |
|------------------|--------|--------|
| t _{PZH} | Open | Closed |
| t _{PZL} | Closed | Open |
| t _{PLZ} | Closed | Closed |
| t _{PHZ} | Closed | Closed |

Figure 8

LM016L

- 16 Character x 2 lines
 - Built-in control LSI HD44780 type (see page 23)
 - +5V single power supply

MECHANICAL DATA (Nominal dimensions)

| | |
|---------------------------------------|---------------------------|
| Module size | 84W x 44H x 12D (max.) mm |
| Effective display area | 61W x 15.8H mm |
| Character size (5 x 7 dots) | 2.96W x 4.86H mm |
| Pitch | 3.55 mm |
| Dot size | 0.56W x 0.66H mm |
| Weight | about 25 g |

ABSOLUTE MAXIMUM RATINGS

| SOLUTE MAXIMUM RATINGS | min. | max. |
|--|----------|----------|
| Power supply for logic ($V_{DD} - V_{SS}$) | 0 | 7.0 V |
| Power supply for LCD drive ($V_{DD} - V_O$) | 0 | 13.5 V |
| Input voltage (V_i) | V_{SS} | V_{DD} |
| Operating temeprature (T_a) | 0 | 50°C |
| Storage temperature (T_{stg}) | -20 | 70°C |

ELECTRICAL CHARACTERISTICS

| | |
|---|----------------------------|
| Ta = 25°C, V _{DD} = 5.0 V ± 0.25 V | |
| Input "high" voltage (V _{iH}) | 2.2 V min. |
| Input "low" voltage (V _{iL}) | 0.6 V max. |
| Output high voltage (V _{OH}) (-I _{OH} = 0.2 mA) . . | 2.4 V min. |
| Output low voltage (V _{OL}) (I _{OL} = 1.2 mA) . . . | 0.4 V max. |
| Power supply current (I _{DD}) (V _{DD} = 5.0 V) . . . | 1.0 mA typ. 3.0 mA max. |
| Power supply for LCD drive (Recommended) (V _{DD} -V _O) | Du=1/16 |
| at Ta = 0°C | 4.6 V typ. |
| at Ta = 25°C | 4.4 V typ. |
| at Ta = 50°C | 4.2 V typ. |

OPTICAL DATA See page 8

INTERNAL PIN CONNECTION

| Pin No. | Symbol | Level | Function | |
|---------|----------|----------------------|--|--------------|
| 1 | V_{SS} | — | 0V | Power supply |
| 2 | V_{DD} | — | +5V | |
| 3 | V_O | — | — | |
| 4 | RS | H/L | L: Instruction code input H: Data input | |
| 5 | R/W | H/L | H: Data read (LCD module \rightarrow MPU) L: Data write (LCD module \leftarrow MPU) | |
| 6 | E | H, H \rightarrow L | Enable signal | |
| 7 | DB0 | H/L | Data bus line Note (1), Note (2) | |
| 8 | DB1 | H/L | | |
| 9 | DB2 | H/L | | |
| 10 | DB3 | H/L | | |
| 11 | DB4 | H/L | | |
| 12 | DB5 | H/L | | |
| 13 | DB6 | H/L | | |
| 14 | DB7 | H/L | | |

Note:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

- (1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$, and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$, when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).
 - (2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

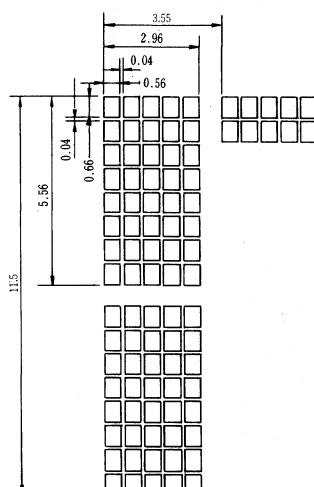
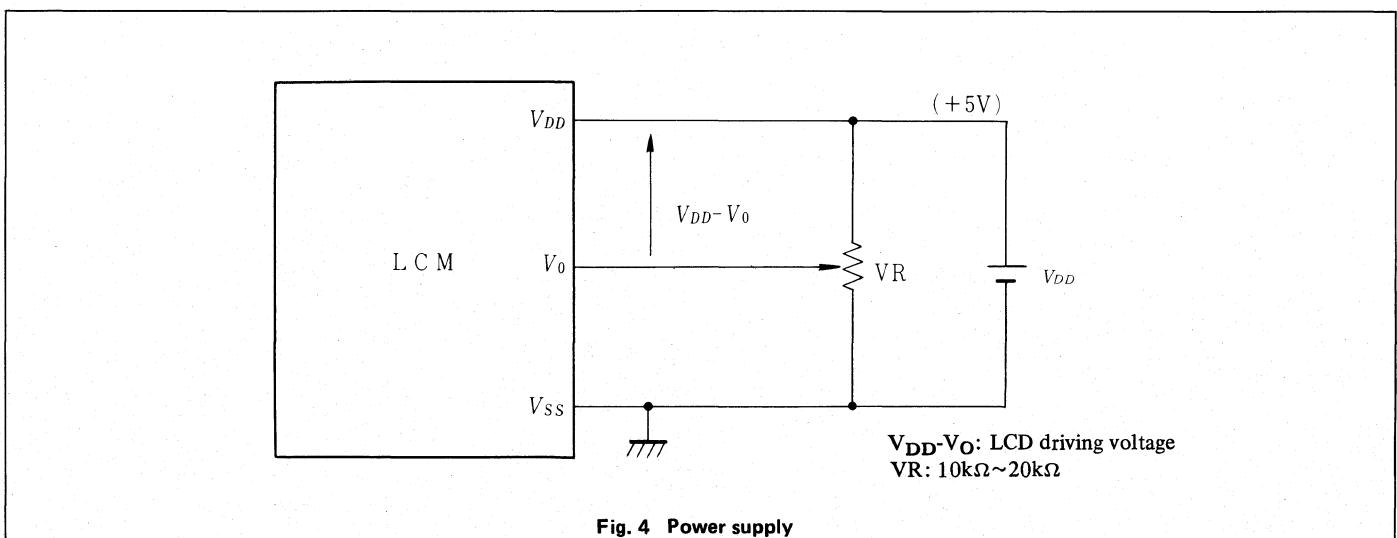
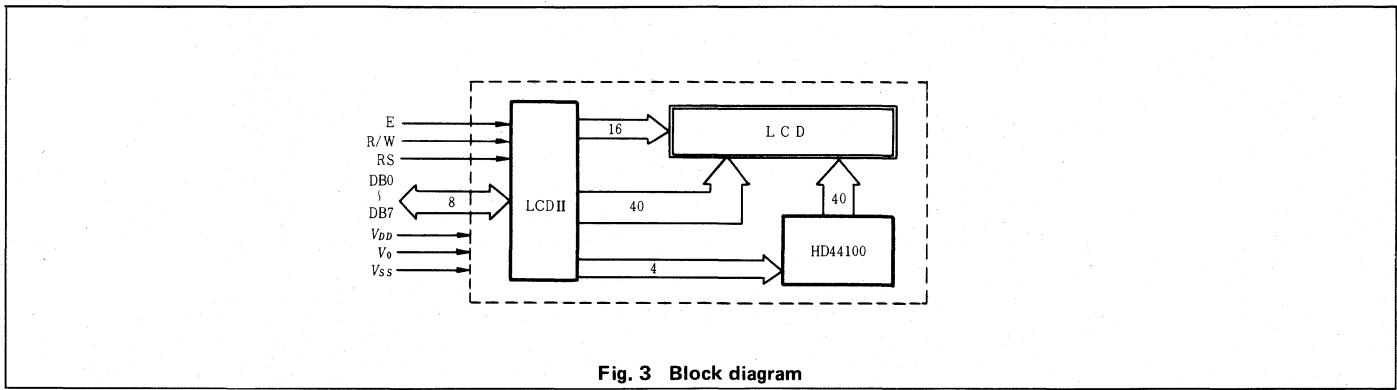
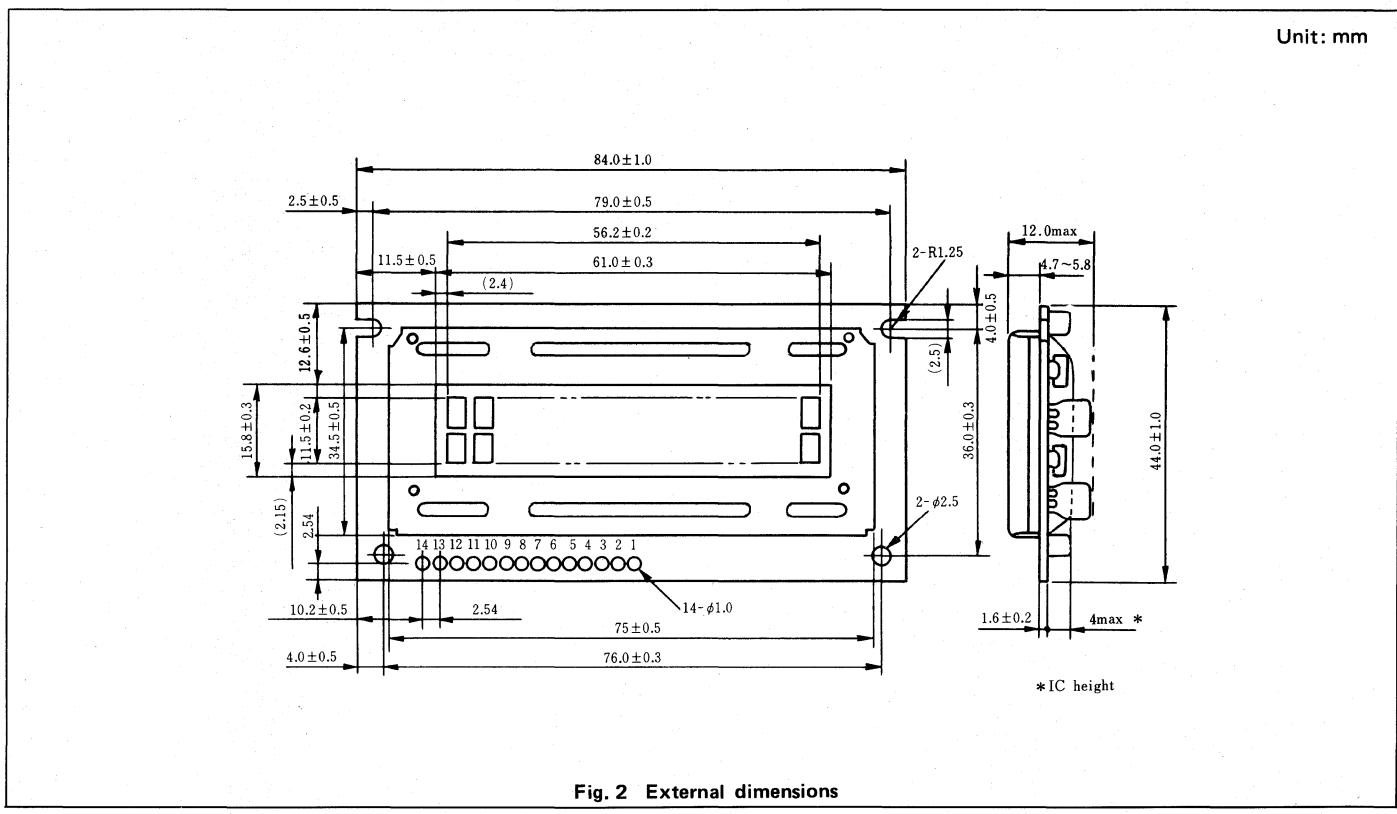


Fig. 1 Display pattern



TIMING CHARACTERISTICS

| Item | Symbol | Test condition | min. | typ. | max. | Unit |
|-----------------------|------------------|----------------|------|------|------|---------|
| Enable cycle time | t_{cyc} | Fig. 5, Fig. 6 | 1.0 | — | — | μs |
| Enable pulse width | P_{WEH} | Fig. 5, Fig. 6 | 450 | — | — | ns |
| Enable rise/fall time | t_{Er}, t_{Ef} | Fig. 5, Fig. 6 | — | — | 25 | ns |
| RS, R/W set up time | t_{AS} | Fig. 5, Fig. 6 | 140 | — | — | ns |
| Data delay time | t_{DDR} | Fig. 6 | — | — | 320 | ns |
| Data set up time | t_{DSW} | Fig. 5 | 195 | — | — | ns |
| Hold time | t_H | Fig. 5, Fig. 6 | 20 | — | — | ns |

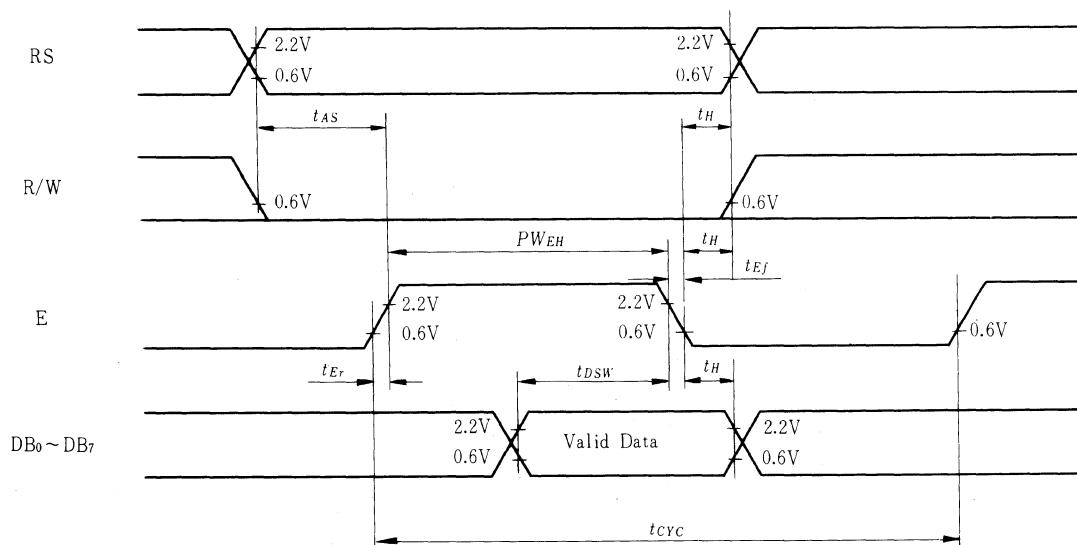


Fig. 5 Interface timing (data write)

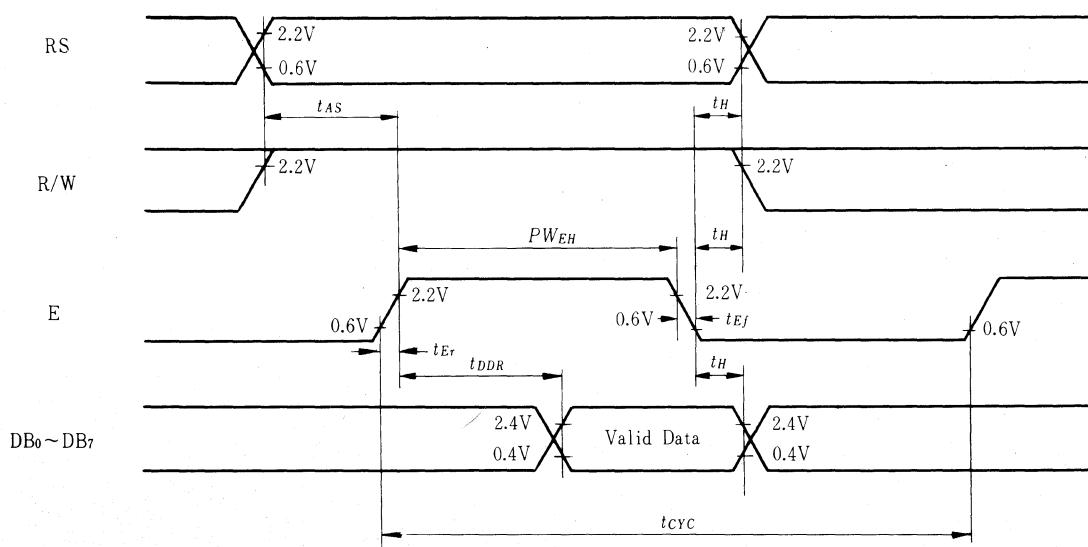


Fig. 6 Interface timing (data read)