Tsao-Lun Chen

Contact Information

TEL: +886-912-711-870
Mail: a870128rlen@gmail.com
Github: github.com/wahahahaya
Web: wahahahaya.github.io/

Education

Yuan Ze University Taoyuan, Taiwan
Bachelor of Electrical Engineering *Sep 2016 - Jun 2020*

- GPA: 3.82
- Conference: Automatic Reference Current Architecture in Computing in Memory by MRAM
- Conference: Based on deep learning analyze brainwave signals of hand movements
- Award: IEEE ECICE best conference paper award

National Taiwan University of Science and Technology Taipei, Taiwan
Master of Electrical Engineering *Sep 2020 - present*

- Advisor: Shun-Feng Su

Work Experience

Student Inter May 2019 – Oct 2019
Industrial Technology Research Institute *Hsinchu, Taiwan*

- Digital IC design
- STT-MRAM/Computing in Memory/Sense Amplifier

Publish

Conference

- **Chen, Tsao-Lun**, and Wei-Tang Tseng. "Automatic Reference Current Architecture in Computing in Memory by MRAM." 2019 IEEE Eurasia Conference on IOT, Communication and Engineering (ECICE). IEEE, 2019.
- **Chen, Tsao-Lun**, and Chien-Cheng Lee. "Based on deep learning analyze brainwave signals of hand movements." 2019 Mobile Computing Workshop. MC2019.

Projects

Zero-shot Learning | *Python* Sep 2020 – Present

- end-to-end zero-shot learning model

OPG Decomposition | *Python* Oct 2021 – Present

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Image Noise Distribute | *Python* Sep 2020 – May 2021

- Use GAN to generate the clear image by inputting the mixed noise(AWGN, SPIN, RVIN).

Technical Skills

Programming Languages: Python, C/C++, R, Hspice
Domain Expertise: Computer Vision, Deep Learning, Zero-shot Learning, VLSI

Award

- Best conference paper in IEEE ECICE: Automatic Reference Current Architecture in Computing in Memory by MRAM

Professional Experience

Podcast Producer

- Writing interviews
- Inviting guests
- Recording
- Editing

Teaching Assistant

- Introduction to Intelligent Control, NTUST, Fall 2021
- Decision Support and Recommender Systems, NTUST, Fall 2021
- Programming Language, YZU, Spring and Fall 2020, Fall 2019

Research Assistant

- Logic Circuit Lab., YZU, Fall 2019