CME 341: Latches and Flip-flops

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Today's agenda

1. Review of Latches and Flip-flops

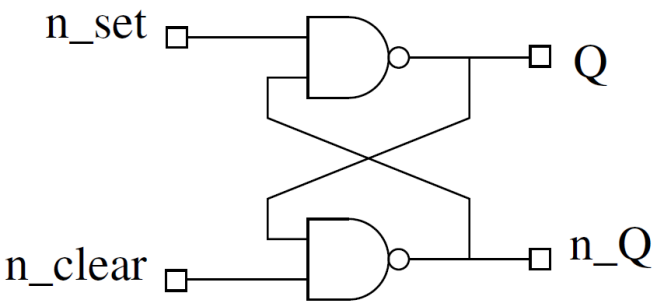
Review of Latches and Flip-flops

Latches and Flip-flops

- Latches and flip-flops are circuits that can store state information in a digital circuit
- Latches are not clocked, but can be used to create flip-flops (which are clocked)
- Some examples and early assignment questions in CME 341 involve latches
- Latches can be dangerous and generally shouldn't be used in actual designs in CME 341 (or ever)
  - ▷ 99.9% of the time, you really want a flip-flop
  - ▷ Quartus will sometimes generate latches if you use incorrect coding styles; we will study how to avoid this later

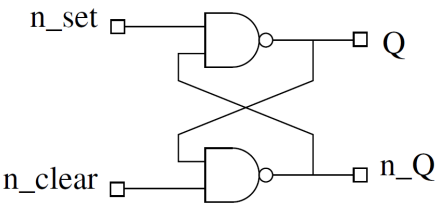
Set-clear latch

Practice: Try to generate a truth table for this circuit



Verilog code for the s-c latch

Try to write it yourself before peeking



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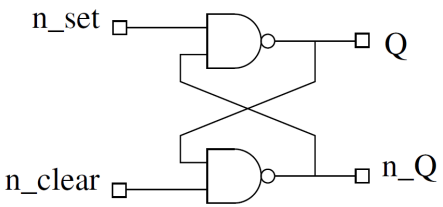
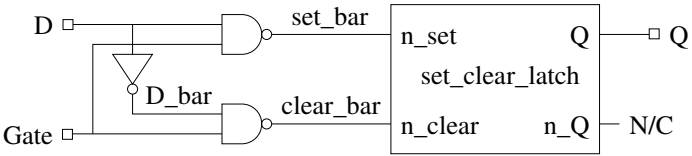



```
module set_clear_latch (
  input wire n_set,
  input wire n_clear,
  output wire Q,
  output wire n_Q
);

assign Q   = ~(n_set & n_Q);
assign n_Q = ~(n_clear & Q);

endmodule
```

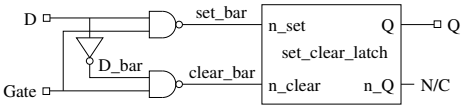
Transparent latch

Practice: Try to generate a truth table for this circuit

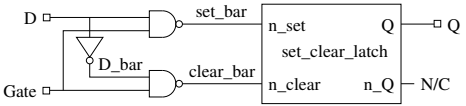


Verilog code for the transparent latch

Try to write it yourself before peeking



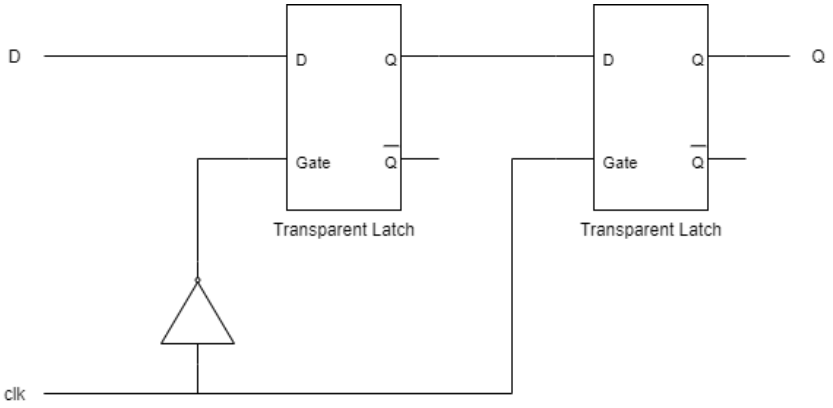
Verilog code for the transparent latch




```
module transparent_latch(D, Gate, Q);
input D, Gate;
output Q;

wire D_bar, set_bar, clear_bar;

assign set_bar = ~(D & Gate);
assign clear_bar = ~((~D) & Gate);

set_clear_latch latch_1(.n_set(set_bar),
.n_clear(clear_bar),
.Q(Q)); // n_Q output not used

endmodule
```

A D-flip-flop can be built from transparent latches

Positive edge-triggered logic



Thank you!
Have a great day!