CME341 Assignment 1

1. Generate a schematic diagram for a D flipflop with clock enable. Use only standard gates like and, nand, xnor, etc. and a regular d-flipflop, that is a d-flipflop that does not have a clock enable. A d-flipflop with clock enable acts like a regular d-flipflop when the enable is high. When the enable is low, Q stays as it was on the last positive clock edge prior to the enable going low. Q does not get the value of d on a positive clock edge while the enable is low. NB: When the enable changes state it should not generate an additional clock edge or delay the time of a positive going clock edge.

2. For the purpose of learning what it means to fully annotate a block diagram, draw a block diagram consisting of 4 blocks in total, but with three of the four blocks being the same block. To provide focus for this activity, assume that the function of the circuit is that of a "12 input nand". It should also be assumed that the block used three times has the function of a "4 input and" and the block used once has the function of a "3 input nand". Appropriate prototype names for the blocks might be "and_function" and "nand_function". In addition to the function name (prototype name) each block should have a unique instance name. The ports (inputs and outputs) for each block must also be named inside the block. These names are associated with a prototype. The wires that interconnect the blocks must be named as well.

   Note that this is not a question on the use primitives. The block diagram will consist of four **rectangular** blocks with interconnecting signals and a lot of annotation.

3. Specify the prototypes for the blocks used in question 2. Name the modules "and_function" and "nand_function". Use an explicit structural description (instantiate primitives) for the four input "and" function and an implicit structural description (use the assign statement) for the three input "nand" function.