CME341 Assignment 8

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Revised Nov. 12, 2020: Added Question 2 to take efffect
                       starting 2021
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1. Design, debug and test the instruction decoder circuit for the CME341 Microprocessor.

   You have the freedom to use any programming style you like, but there may be consequences. Some possible consequences for a couple of different design styles are explained below.

   In this case the prototype will be sufficiently simple that it can, and in industry most likely would, be implemented in one hierarchical level. I.e., **the prototype for the instruction decoder would not instantiate any other prototypes**. If you choose to build some of the functionality of your instruction decoder in other prototypes and then instantiate them it will likely put you at a disadvantage when writing the exams. The exams are designed under the assumption that the instruction decoder does not instantiate any prototypes.

   The best way to design this module is with one always procedure for each output. That is, do not use any begin-end wrappers.

   It is certainly possible to build the combinational logic circuit by parsing the input with a *"case (ir)"* construct. However, this approach will produce a very large Verilog HDL description that is generally more difficult to debug. It is believed that most engineers debug their circuits one output at a time. Constructing each output in a separate always procedure works well for this debugging style.

2. Complete the preamble for the second midterm exam as per the instructions on the class website. Doing so builds a prototype that connects the program sequencer, the program memory and the instruction decoder.

   The prototype will be used in the second midterm so it is essential it be built and verified exactly as described.