CME341 - October, 2019 Midterm
Material up to end of Assignment 5

```
Date: Wednesday, October 9, 2019
Time = 1.00 hours
Text Books, Notes and Computer Files Only
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(1)

1. Re-design prototype `student_circuit` to describe an 8-flip/flop ring counter. Make the eight flip/flops as an 8-bit Verilog HDL vector called `ring_counter`. `ring_counter` is to be synchronously set to `ring_counter = 8'b1000_0000` when `clear==1'b1`. Otherwise `ring_counter` is to count in the sequence given below:

   ```
   8'b1000_0000
   8'b0100_0000
   8'b0010_0000
   8'b0001_0000
   8'b0000_1000
   8'b0000_0100
   8'b0000_0010
   8'b0000_0001
   8'b1000_0000
     etcetera
   ```

   Make `cct_output = ring_counter`.

   Note this circuit does not use `cct_input`.

   The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'HE8D4`.
   Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(2) 2. Re-design prototype `student_circuit` to make it describe a combinational logic circuit that uses the input to do the following:

Sets `cct_output` to zero while `clear` is high. Otherwise

If `cct_input` is equal to 8'H14 `cct_output` is to be the ones complement of `cct_input` (i.e. all bits inverted).

If `cct_input` is greater than 66 (in decimal) `cct_output` is to be the sum of the least significant 4 bits of the input (the sum of the individual bits). This means `cct_output` will be between 8'd0 and 8'd4, inclusive.

Otherwise `cct_output` is to be `cct_input`.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'H32BF`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(1) 3. Make an asynchronous circuit that sets `cct_output` to be the reverse order of the bits of `cct_input`. For example, if the input is *10100000*, then the output should be *00000101*.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'HCC7D`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(1) 4. Redesign prototype "student_circuit" to implement a sequential logic circuit that has:

- a new clock called *new_clock* that has a frequency equal to $\frac{clk}{2}$
- an 8-bit counter that is synchronously cleared when clear is high, and counts on the positive edge of *new_clock*.
- `cct_output` equal to the 8-bit counter value.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'H3767`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(1) 5. Design the circuit shown in Figure 1.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'HA18A`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

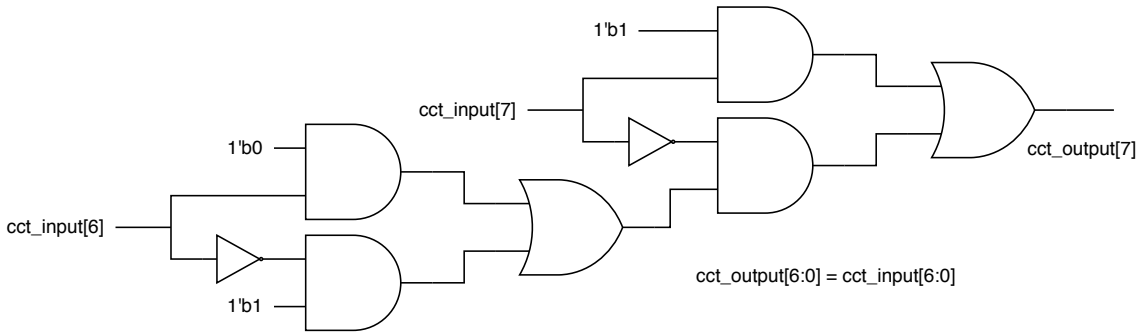

Figure 1: Question 5