CME341 - October, 2017 Midterm
Material up to end of Assignment 5

`Date: Wednesday, October 11, 2017`
`Time = 1.00 hours`
`Text Books, Notes and Computer Files Only`

Before starting the exam modify the second "initial" procedure in the test bench so that `exam_dependent_seed` is assigned the value on your answer sheet.

(2)

1. Consider the Verilog HDL below:

```
module exam_ques (
input clk,
input [7:0] exam_dependent_seed,
output reg [15:0] Q4
                  );
reg [15:0] Q1, Q2, Q3;
always @ (posedge clk)
begin
    Q1 = {8'HFF, exam_dependent_seed};
    Q4 = Q1 | 16'h5555;
    Q2 = Q3;
    Q3 =  | (16'hA337 |  Q1);
    Q4 = (Q1 | 16'h5555)^Q3;
end
endmodule
```

   Report the 16 bit input to the `Q4` register (For those that may not know, in this case the word "register" means a bank of 16 flip/flops.). For `exam_dependent_seed` = `8'HAA`, `Q4` = 16'HFFFE.

   For this question the test bench is not used.

(2)

2. Re-design prototype `student_circuit` to make it describe a combinational logic circuit that uses the most significant 4 bits of the input to specify the function of the circuit as follows:

   Sets `cct_output` to zero while `clear` is high. Otherwise

   - If the most significant 4 bits of the input are equal to 4'b11 it sets `cct_output` equal to the ones complement of `cct_input`.
   - If the most significant bit of the input is 1'b1 it makes `cct_output` the sum of the bits of the input. This means `cct_output` will be between 8'd1 and 8'd8.

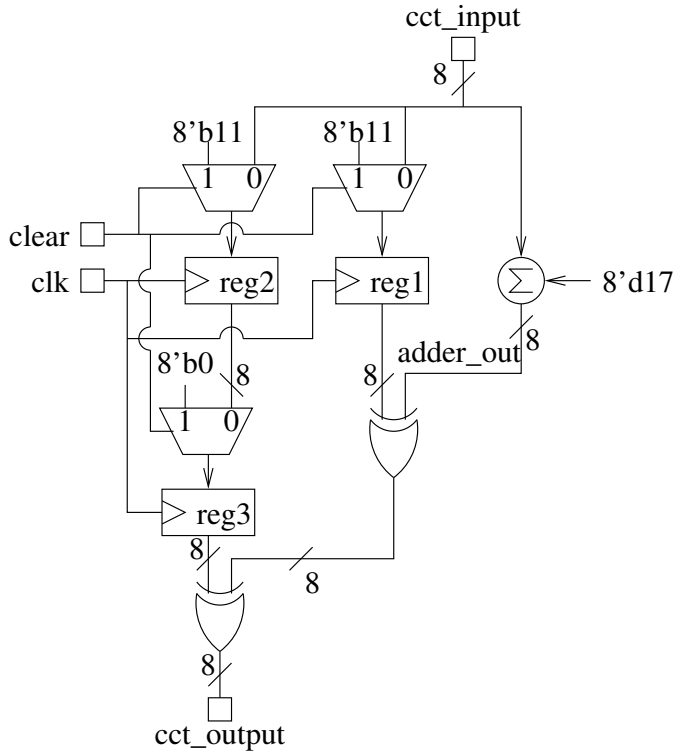

Figure 1: Circuit for Question 3

Otherwise sets `cct_output` to `cct_input`.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'H9CC9`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(2) 3. Re-design the Verilog HDL prototype `student_circuit` to construct the circuit described in Figure 1.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'H1476`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(2) 4. Re-design prototype `student_circuit` to describe an 8-flip/flop ring counter. Make the eight flip/flops as an 8-bit Verilog HDL vector called `ring_counter`. `ring_counter` is to be synchronously set to `ring_counter = 8'b0000_0001` when `clear==1'b1`. Otherwise `ring_counter` is to count in the sequence given below:

```
8'b0000_0001
8'b0000_0010
8'b0000_0100
8'b0000_1000
8'b0001_0000
8'b0010_0000
8'b0100_0000
8'b1000_0000
8'b0000_0001
  etcetera
```

Make `cct_output = ring_counter`.

Note this circuit does not use `cct_input`.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'78c2`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.

(2) 5. Re-design prototype `student_circuit` to make `cct_output` the middle 8 bits of the square of `cct_input`.

Note neither `clk` nor `clear` is used.

The accumulator output, i.e. `accumulator_output`, when `counter_full_bar` is low for `seed = 8'HAA` should be `16'He820`.
Once `accumulator_output` is correct for `seed = 8'HAA` report it for the seed on your answer sheet.