CME341 - Preamble for the first Midterm Material up to end of Assignment 5

`Created: October 3, 2014`
`modified: September 27, 2021`

In preparation for the exam (i.e. prior to entering the exam) do the following:

1. Using a lab computer (in Linux mode), create a directory called `first_midterm_CME341`. Make a Quartus project within that directory called `student_circuit` and the make the top entity in that project `student_circuit`. Use the Cyclone IVe FPGA that is used on the DE2-115 boards, which has part number EP4CE115F29C7.

2. Download the files `student_circuit.sv`, `student_circuit_preamble.sv`, and `student_circuit.sdc` and place them in the project directory.

3. Add the files `student_circuit.sv` and `student_circuit_preamble.sv` to the Quartus project: **Project $\longrightarrow$ add/remove files in project**

4. If you forgot to make `student_circuit.sv` the top-level entity when establishing the project with the project wizard it can be after the project is created by opening `student_circuit.sv` and then selecting **Project $\longrightarrow$ Set as top-level entity**.

5. Compile the project.

6. Download the file `midterm_1_testbench.sv` and place it in the subdirectory of the Quartus project: **simulation $\rightarrow$ modelsim**.

7. Make a Modelsim project in the subdirectory and add files `student_circuit.vo` and `midterm_1_testbench.sv`.

8. Compile all.

9. Start the simulation. Remember to include the required simulation libraries: `altera_mf_ver`, `altera_ver`, and `cycloneive_ver`

10. Add signals `clk`, `clear`, `seed`, `stimulus`, `student_output`, counter_full_bar and `accumulator_output` to the wave window.

11. Make the radix of all signals hexadecimal.

12. Change the grid & timeline properties of the horizontal axis to have units of microseconds.

13. **Save the format of the wave window in a `wave.do` file so the wave window can be quickly set up in the exam**.

14. Run the simulation with the `-all` option.

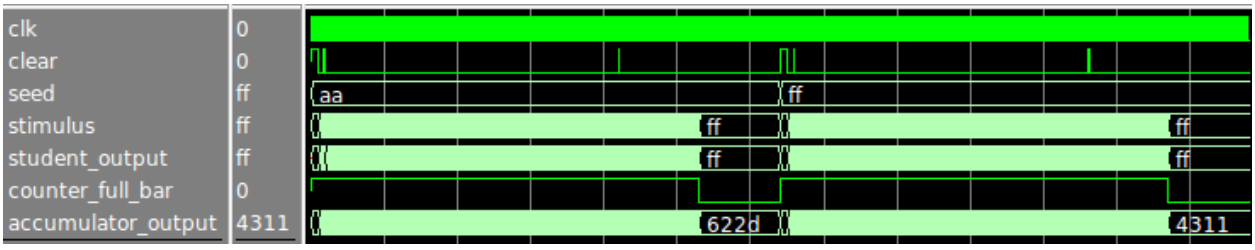

Figure 1: Full view of wave window

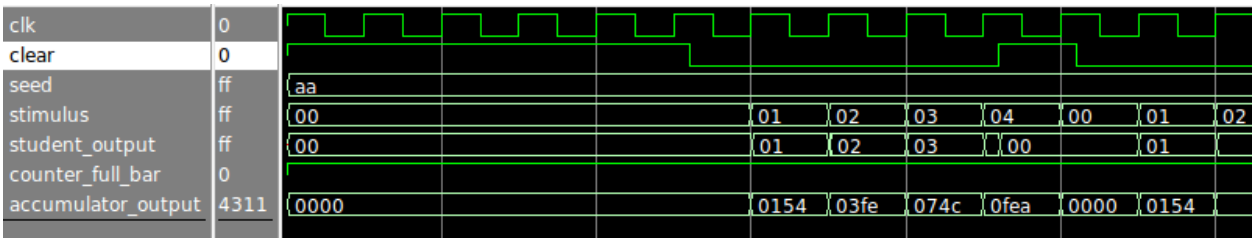

Figure 2: Zoomed in view at the beginning of the wave window

15. After "full-zooming" the wave window it should be as shown in Figure 1. A closer view near the beginning is shown in Figure 2. A close look at Figure 1 shows four clear pulse, two or which are narrower than the other two. A zoomed in view of one of the narrow clear pulses is shown in Figure 3.

16. Notice from observing the wave window that the value of variable `seed` changes at 320 microseconds from 8'AA to 8'HFF. The reason for this is important and is explained below.

17. The results of the simulation are coded in the 16 bit variable `accumulator_output`. The result, i.e. the value of `accumulator_output`, is valid only at the times when binary variable `counter_full_bar` is low. The value of `accumulator_output` depends on: the prototype `student_circuit.sv` (and any submodules) and the value of the variable `seed`. The variable `seed` changes at time 320 μs from 8'hAA to the value of a variable named `exam_dependent_seed`. In the posted version of

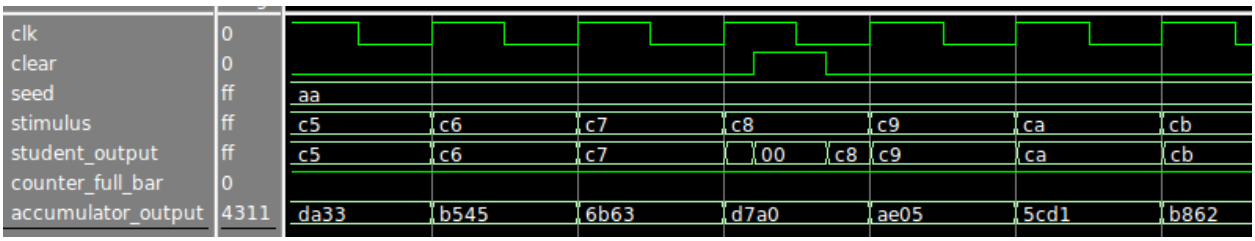

Figure 3: Zoomed in view showing one of the two narrow clear pulses

`midterm_1_testbench.sv` `exam_dependent_seed` is set to 8'HFF. The two"valid result" values of `accumulator_output` should be 16'H622D and 16'H4311 for seeds 8'HAA and 8'HFF, respectively. Please check your wave window to make sure this is the case.

18. The very first thing you must do in the exam is change the value of variable `exam_dependent_seed` in `midterm_1_testbench.sv` to the seed given on your answer sheet. To be sure you will do that correctly in the exam modify `midterm_1_testbench.sv` so that `exam_dependent_seed` is set to `8'HAA`. Then recompile `midterm_1_testbench.sv`. Then check the wave window to make sure `seed` is 8'HAA for the entire 640 μs and the two " valid" values of `accumulator_output`, (i.e. the values at the two times `counter_full_bar` is low) are both `16'H622D`.

Example Exam Question

Modify the modelsim testbench `midterm_1_testbench.sv` so that `exam_dependent_seed` is set to `8'H11`.

Then modify `student_circuit` to make it a combinational logic circuit whose output is `8'H00` while `clear` is high and is otherwise the "exclusive or" of the input and the constant 8'H3C.

Recompile the Quartus project.

Compile and load the Modelsim project. Then add the appropriate signals to the wave window (easiest way is to execute `do wave.do`).

If your circuit is working properly `accumulator_output` should be `16'H62DE` when `counter_full_bar` is low for `seed = 8'HAA`.

Once your circuit is working properly report the value of `accumulator_output` when `counter_full_bar` is low for the seed on your exam sheet, which for this example is `8'H11`.