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CME 331 – Embedded Systems – Fall 2025
Assignment 2

This assignment contains 3 sections of questions related to Stellaris Launchpad usage and memory mapped architectures. Completed assignments must be submitted as a .pdf, on Canvas, by the specified due date. Late or missed assignments will not be marked (i.e., graded as zero).

Preprocessor Definition Usage

Complete the preprocessor definitions and/or use them to configure a Stellaris Launchpad as requested:

1. With a single line of code, define a symbolic name for accessing port F data, using the advanced peripheral bus, with access to all bits. (1 point)

Answer: `#define GPIO_PORTF_DATA_R (*((volatile unsigned long *)0x400253FC))`

2. With a single line of code, use the definition from question 1 to turn on the red, green, and blue LEDs, assuming positive logic. (1 point)

Answer: `GPIO_PORTF_DATA_R |= 0x0E;`

3. With a single line of code, define a symbolic name for accessing port A alternate functions, using the advanced peripheral bus. (1 point)

Answer: `#define GPIO_PORTA_AFSEL_R (*((volatile unsigned long *)0x40004420))`

4. With a single line of code, use the definition from question 3 to enable the alternate functions for bits 0 and 1. (1 point)

Answer: `GPIO_PORTA_AFSEL_R |= 0x03;`

5. Assume GPIO_PORTA_PCTL has been defined as the port control register for port A. With a single line of code, use the definition to enable UART0. (1 point)

Answer:

TM4C123 Memory-mapped Locations

Use the TM4C123 data sheet to find the 32-bit memory address (in hexadecimal) for the following locations:

6. The register required to load a starting count value for general purpose timer 2, assuming its timer A has been configured as an independent 32-bit timer counting down. (2 points)

Answer: 0x4003.2000

7. The register required to write data into the transmit FIFO for UART 2, assuming the transmit and receive FIFOs have been enabled. (2 points)

Answer: 0x4000.E000

8. The register required to set the data frame size of the synchronous serial interface, module 2, to 8-bits wide. (2 points)

Answer: 0x4000.A000

9. The register required to enable the output of pulse-width modulator 0, on M0PWM pin 2, assuming configuration has been completed. (2 points)

Answer: 0x4002.8008

10. The register required to connect the output of pulse-width modulator 0 on pin 2 (M0PWM2) to port B pin 4. (2 points)

Answer: 0x4000.552C

Memory Map Design

As a new engineer working at ARM, you receive the following email:

I need you to lay out the memory map for the Media Access Controller (MAC) of a new Ethernet peripheral we're creating for our 32-bit microcontrollers. Make sure you group similar registers together by function and leave reserved space for expansion. We'll figure out the base address later, but you have from 0x00 to 0xFF to fit everything in.

For configuration, off the top of my head, 1 revision register for the peripheral version, a scratch register that does nothing, but we can read and write for test purposes, probably 1 register with all the enable and reset bits, definitely a MAC address that's 48-bits so it will need more than 1 register to

hold the address, definitely Ethernet frame length and inter-packet gap length. That's all that comes to mind, but leave room for at least 32 registers in the configuration space

We'll need a lot of statistics counters. We always keep a count of things like Ethernet frames transmitted and received, multicast packets received, broadcast packets received, I won't list them all, but we already have a list of 32 32-bit counters that we need, leave room for more.

We need space for 64 multicast addresses. They're 48-bit, but we can use a hash function to map them to 32-bit registers, so just 64 32-bit registers. That's a fixed amount, no need for extra space for those.

We're also going to put the physical layer (PHY) configuration in your address space. This block needs to start at 0xA0. Reads or writes to this section will cause an MDIO bus transaction to the PHY. For now, treat it just like the config space for the MAC.

Thanks,
Your Supervisor

11. There is a lot of irrelevant information in the email from your supervisor, but there is also enough information given to create a memory map. Generate a table like memory map table 2-4 in the TM4C123 datasheet. You may not need all of the rows in the provided table below. (5 points)

Word Offset (start)	Word Offset (end)	Description
0x00	0x00	Revision
0x01	0x01	Scratch
0x02	0x02	Enable and Reset
0x03	0x04	MAC address
0x05	0x05	Ethernet frame length
0x06	0x06	Inter-packet gap length
0x07	0x26	Configuration
0x29	0x46	Counters
0x47	0x86	Multicast addresses
0x87	0x9F	Reserved
0xA0	0xC8	PHY configuration
0xC9	0xFF	Reserved