**Part 1**:

MAX_AREA 3000000

MAX_DYNAMIC_POWER 70.0

MAX_FANOUT 8

MAX_OUTPUT_load 57.462

max_capacitance 5

min_capacitance 0

MAX_INPUT_DELAY 5

MIN_INPUT_DELAY 4

OUTPUT_MAX_DELAY 5

OUTPUT_MIN_DELAY 4

Power:

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.0000           0.0000            0.0000            0.0000  (   0.00%)
sequential         1.7686        3.7732e-03        4.3085e-03           1.7767  (  76.79%)
combinational      0.1681           0.3687         3.3584e-04           0.5371  (  23.21%)
--------------------------------------------------------------------------------------------------
Total              1.9368 mW        0.3724 mW     4.6443e-03 mW         2.3139 mW
1
```

Area:

```
    vlvl_tsmc180 (File: /home/tgy/Desktop/test/fpgaEx3/vscale/src/main

Number of ports:                          403
Number of nets:                         17022
Number of cells:                        16766
Number of combinational cells:          14771
Number of sequential cells:              1995
Number of macros/black boxes:               0
Number of buf/inv:                       1481
Number of references:                      37

Combinational area:             648209.010532
Buf/Inv area:                    42032.828339
Noncombinational area:          348172.583542
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                996381.594074
Total area:                 undefined
1
```

Min_timing

```
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
vscale_core        10x10                 vtvt_tsmc180

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
input external delay                     4.00       4.00 r
imem_hready (in)                        60.73      64.73 r
U12128/op (nand2_1)                     71.09     135.82 f
U12130/op (nand2_1)                     84.44     220.26 r
U12131/op (nor2_1)                     142.82     363.07 f
U15385/op (inv_1)                       45.68     408.75 r
U15386/op (nor2_1)                      73.46     482.21 f
U15387/op (and2_1)                     146.64     628.85 f
U11835/op (xor2_1)                     190.02     818.87 f
U10859/op (xor2_2)                     262.88    1081.75 f
imem_haddr[2] (out)                      0.00    1081.75 f
data arrival time                                1081.75

clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
output external delay                   -4.00      -4.00
data required time                                 -4.00
-----------------------------------------------------------
data required time                                 -4.00
data arrival time                                -1081.75
-----------------------------------------------------------
slack (MET)                                       1085.75
```

Max_timing:

```
-----------------------------------------------------------
data required time                                4995.00
data arrival time                                -4994.60
-----------------------------------------------------------
slack (MET)                                          0.40
```

**Part 2**:

MAX_INPUT_DELAY 6

MIN_INPUT_DELAY 4

OUTPUT_MAX_DELAY 6

OUTPUT_MIN_DELAY 4

Power:

| Power Group | Internal Power | Switching Power | Leakage Power | Total Power | ( % ) | Attrs |
|---|---|---|---|---|---|---|
| io_pad | 0.0000 | 0.0000 | 0.0000 | 0.0000 | ( 0.00%) | |
| memory | 0.0000 | 0.0000 | 0.0000 | 0.0000 | ( 0.00%) | |
| black_box | 0.0000 | 0.0000 | 0.0000 | 0.0000 | ( 0.00%) | |
| clock_network | 0.0000 | 0.0000 | 0.0000 | 0.0000 | ( 0.00%) | |
| register | 0.0000 | 0.0000 | 0.0000 | 0.0000 | ( 0.00%) | |
| sequential | 1.7687 | 3.8030e-03 | 4.3085e-03 | 1.7768 | ( 76.44%) | |
| combinational | 0.1741 | 0.3731 | 3.3593e-04 | 0.5475 | ( 23.56%) | |
| Total | 1.9428 mW | 0.3769 mW | 4.6444e-03 mW | 2.3244 mW | | |

Max_timing:

| | | |
|---|---|---|
| clock clk (rise edge) | 5000.00 | 5000.00 |
| clock network delay (ideal) | 0.00 | 5000.00 |
| output external delay | -6.00 | 4994.00 |
| data required time | | 4994.00 |
| data required time | | 4994.00 |
| data arrival time | | -4992.55 |
| slack (MET) | | 1.45 |

Min_timing:

| Des/Clust/Port | Wire Load Model | Library |
|---|---|---|
| vscale_core | 10x10 | vtvt_tsmc180 |

| Point | Incr | Path | |
|---|---|---|---|
| clock clk (rise edge) | 0.00 | 0.00 | |
| clock network delay (ideal) | 0.00 | 0.00 | |
| input external delay | 4.00 | 4.00 | r |
| imem_hready (in) | 46.24 | 50.24 | r |
| U11988/op (nand2_1) | 69.47 | 119.72 | f |
| U11990/op (and2_1) | 138.61 | 258.33 | f |
| U15090/op (nand2_1) | 49.92 | 308.25 | r |
| U10806/op (and2_1) | 126.32 | 434.56 | r |
| U15091/op (nand2_2) | 109.13 | 543.70 | f |
| U15092/op (inv_4) | 69.97 | 613.66 | r |
| U15109/op (buf_4) | 111.13 | 724.79 | r |
| U20100/op (nand2_1) | 74.21 | 799.00 | f |
| U20101/op (nand3_1) | 218.07 | 1017.07 | r |
| imem_haddr[0] (out) | 0.00 | 1017.07 | r |
| data arrival time | | 1017.07 | |
| clock clk (rise edge) | 0.00 | 0.00 | |
| clock network delay (ideal) | 0.00 | 0.00 | |
| output external delay | -4.00 | -4.00 | |
| data required time | | -4.00 | |
| data required time | | -4.00 | |
| data arrival time | | -1017.07 | |
| slack (MET) | | 1021.07 | |

Area:

```
Number of ports:                          403
Number of nets:                         16849
Number of cells:                        16593
Number of combinational cells:          14598
Number of sequential cells:              1995
Number of macros/black boxes:               0
Number of buf/inv:                       1475
Number of references:                      38

Combinational area:             642696.166763
Buf/Inv area:                    42146.552315
Noncombinational area:          348172.583542
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                990868.750305
Total area:                 undefined
1
```

**Part3:**

MAX_AREA 1000000

Area:

```
Number of ports:                          403
Number of nets:                         16849
Number of cells:                        16593
Number of combinational cells:          14598
Number of sequential cells:              1995
Number of macros/black boxes:               0
Number of buf/inv:                       1475
Number of references:                      38

Combinational area:             642696.166763
Buf/Inv area:                    42146.552315
Noncombinational area:          348172.583542
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                990868.750305
Total area:                 undefined
1
```

Power:

```
  Cell Internal Power  =   1.9428 mW   (84%)
  Net Switching Power  = 376.8939 uW   (16%)
                         ---------
Total Dynamic Power    =   2.3197 mW  (100%)

Cell Leakage Power     =   4.6444 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.0000           0.0000            0.0000            0.0000  (   0.00%)
sequential         1.7687        3.8030e-03        4.3085e-03            1.7768  (  76.44%)
combinational      0.1741           0.3731         3.3593e-04            0.5475  (  23.56%)
--------------------------------------------------------------------------------------------------
Total              1.9428 mW        0.3769 mW     4.6444e-03 mW         2.3244 mW
1
```

**Part4:**

MAX_OUTPUT_load 50

Power:

```
  Cell Internal Power  =   1.9385 mW   (84%)
  Net Switching Power  = 377.7948 uW   (16%)
                         ---------
Total Dynamic Power    =   2.3163 mW  (100%)

Cell Leakage Power     =   4.6424 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.0000           0.0000            0.0000            0.0000  (   0.00%)
sequential         1.7699        3.9539e-03        4.3085e-03            1.7782  (  76.61%)
combinational      0.1687           0.3738         3.3399e-04            0.5429  (  23.39%)
--------------------------------------------------------------------------------------------------
Total              1.9386 mW        0.3778 mW     4.6424e-03 mW         2.3210 mW
```

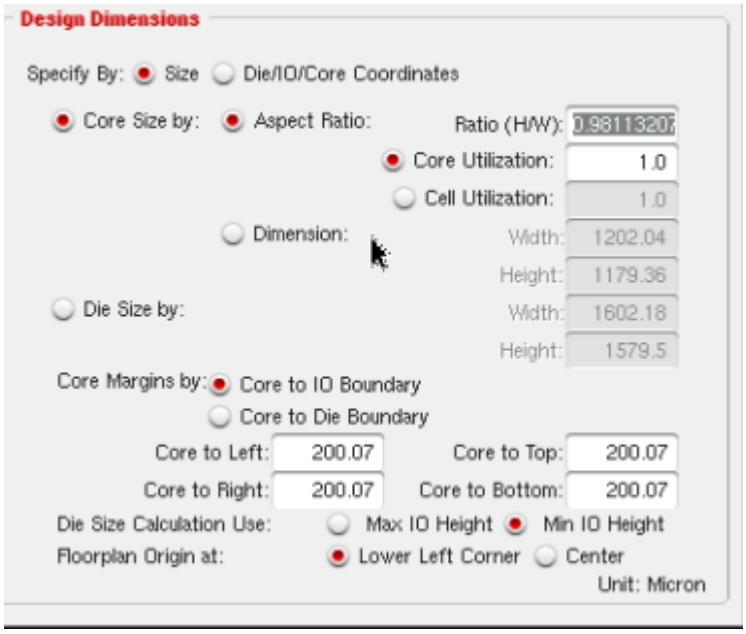
Area:

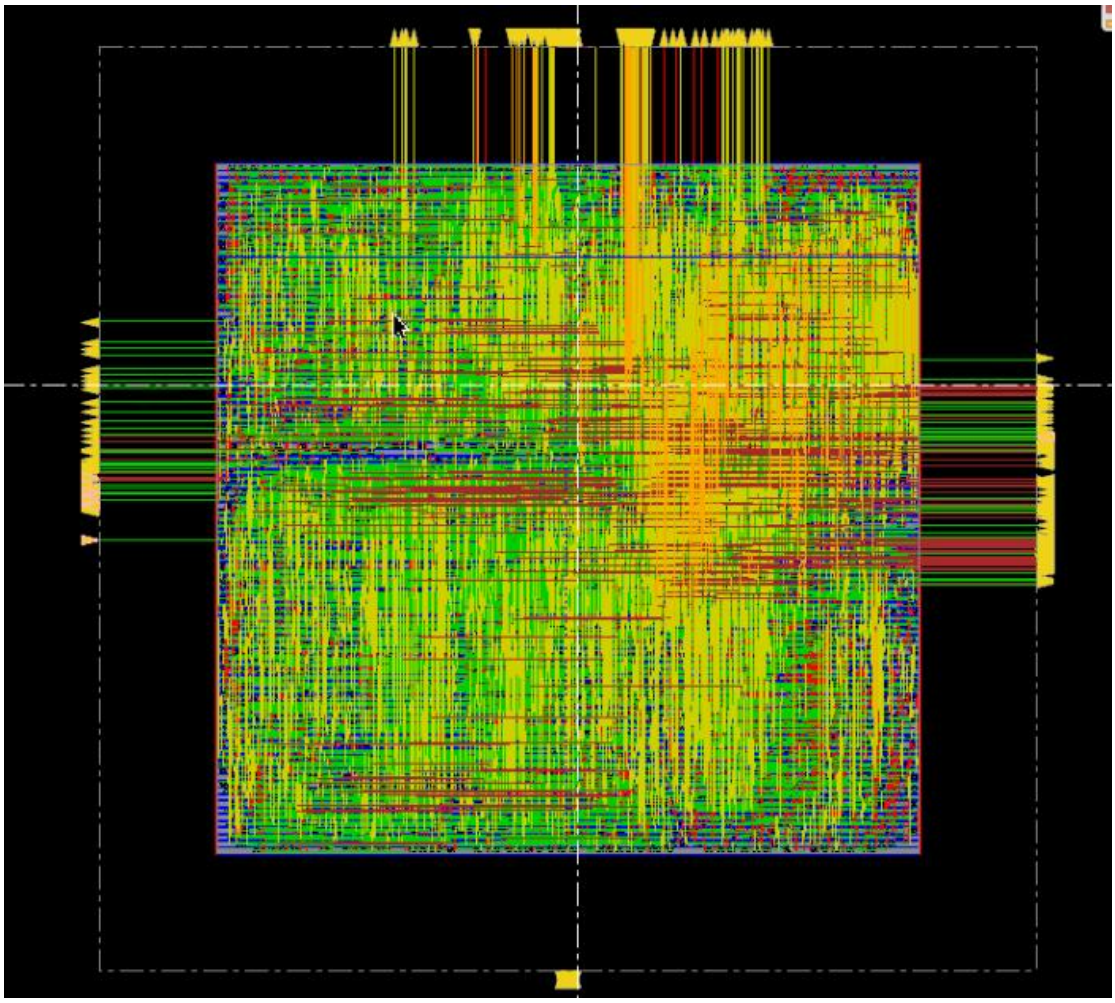
```
Number of ports:                          403
Number of nets:                         16903
Number of cells:                        16647
Number of combinational cells:          14652
Number of sequential cells:              1995
Number of macros/black boxes:               0
Number of buf/inv:                       1430
Number of references:                      35

Combinational area:             644541.630301
Buf/Inv area:                    40716.910418
Noncombinational area:          348172.583542
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                992714.213842
Total area:                 undefined
1
```

Part1:





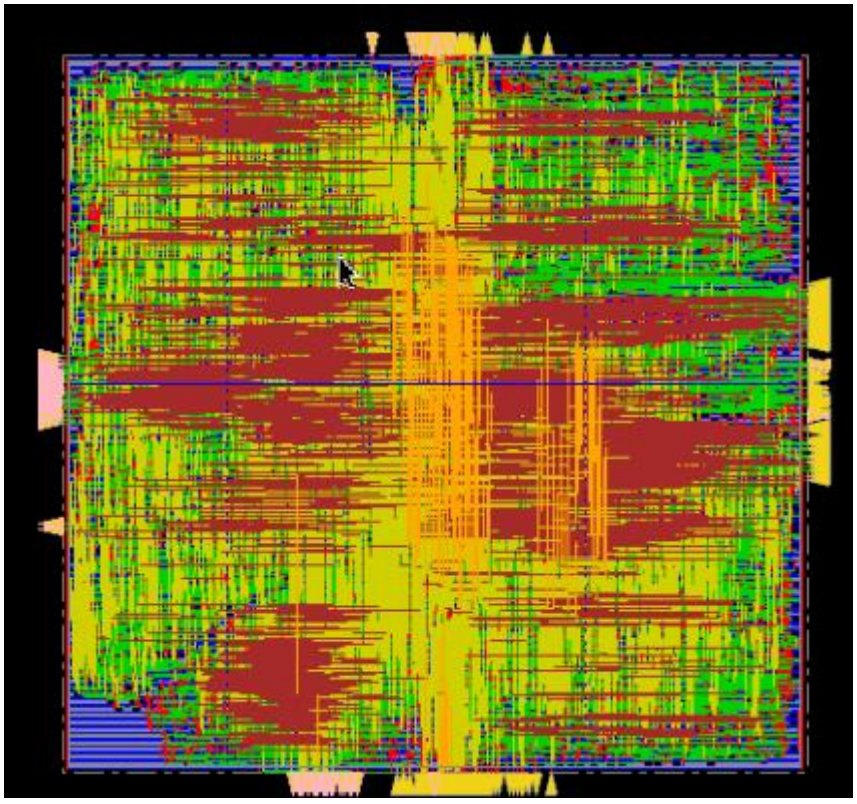
```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.509  |   N/A   | -0.509  |
|           TNS (ns):| -9.832  |   N/A   | -9.832  |
|    Violating Paths:|   28    |   N/A   |   28    |
|          All Paths:|   64    |   N/A   |   64    |
+--------------------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |               Real                |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  | Worst Vio      |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      1 (1)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      0 (0)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 74.923%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

Part2:



optDesign Final Summary

| Setup mode | all | reg2reg | default |
|---|---|---|---|
| WNS (ns): | 0.000 | N/A | 0.000 |
| TNS (ns): | 0.000 | N/A | 0.000 |
| Violating Paths: | 0 | N/A | 0 |
| All Paths: | 0 | N/A | 0 |

| DRVs | Real | | Total | |
|---|---|---|---|---|
| | Nr nets(terms) | Worst Vio | Nr nets(terms) | |
| max_cap | 0 (0) | 0.000 | 1 (1) | |
| max_tran | 0 (0) | 0.000 | 0 (0) | |
| max_fanout | 0 (0) | 0 | 0 (0) | |
| max_length | 0 (0) | 0 | 0 (0) | |

Density: 71.115%
Routing Overflow: 0.00% H and 0.00% V