



Note When in CXL1.1 mode, all the registers are considered as memory mapped registers, but this does not have any impact on how these registers are mapped in APB port register address space

4.2 Register summary

The register summary tables list the registers in CMN-700.

4.2.1 APB register summary

This section lists the APB registers used in CMN-700.

APB register summary

The following table shows the APB registers in offset order from the base memory address

Table 4-2: APB register summary

Offset	Name	Type	Description
16'h0	por_apb_node_info	RO	4.3.1.1 por_apb_node_info on page 284
16'h80	por_apb_child_info	RO	4.3.1.2 por_apb_child_info on page 285
16'h980	por_apb_only_access	RW	4.3.1.3 por_apb_only_access on page 286
16'h988	por-axu-control	RW	4.3.1.4 por_axu_control on page 287

4.2.2 CCG_HA register summary

This section lists the CCG_HA registers used in CMN-700.

CCG_HA register summary

The following table shows the CCG_HA registers in offset order from the base memory address

Table 4-3: CCG_HA register summary

Offset	Name	Type	Description
16'h0	por_ccg_ha_node_info	RO	4.3.2.1 por_ccg_ha_node_info on page 289
16'h8	por_ccg_ha_id	RW	4.3.2.2 por_ccg_ha_id on page 289
16'h80	por_ccg_ha_child_info	RO	4.3.2.3 por_ccg_ha_child_info on page 290
16'hA00	por_ccg_ha_cfg_ctl	RW	4.3.2.4 por_ccg_ha_cfg_ctl on page 291
16'hA08	por_ccg_ha_aux_ctl	RW	4.3.2.5 por_ccg_ha_aux_ctl on page 292
16'hA10	por_ccg_ha_mpam_control_link0	RW	4.3.2.6 por_ccg_ha_mpam_control_link0 on page 294
16'hA18	por_ccg_ha_mpam_control_link1	RW	4.3.2.7 por_ccg_ha_mpam_control_link1 on page 295
16'hA20	por_ccg_ha_mpam_control_link2	RW	4.3.2.8 por_ccg_ha_mpam_control_link2 on page 297

Offset	Name	Type	Description
16'h980	por_ccg_ha_secure_register_groups_override	RW	4.3.2.9 por_ccg_ha_secure_register_groups_override on page 298
16'h900	por_ccg_ha_unit_info	RO	4.3.2.10 por_ccg_ha_unit_info on page 299
16'h908	por_ccg_ha_unit_info2	RO	4.3.2.11 por_ccg_ha_unit_info2 on page 300
16'h910	por_ccg_ha_unit_info3	RO	4.3.2.12 por_ccg_ha_unit_info3 on page 301
16'h1F00	por_ccg_ha_agentid_to_linkid_reg0	RW	4.3.2.13 por_ccg_ha_agentid_to_linkid_reg0 on page 302
16'h1F08	por_ccg_ha_agentid_to_linkid_reg1	RW	4.3.2.14 por_ccg_ha_agentid_to_linkid_reg1 on page 303
16'h1F10	por_ccg_ha_agentid_to_linkid_reg2	RW	4.3.2.15 por_ccg_ha_agentid_to_linkid_reg2 on page 305
16'h1F18	por_ccg_ha_agentid_to_linkid_reg3	RW	4.3.2.16 por_ccg_ha_agentid_to_linkid_reg3 on page 306
16'h1F20	por_ccg_ha_agentid_to_linkid_reg4	RW	4.3.2.17 por_ccg_ha_agentid_to_linkid_reg4 on page 307
16'h1F28	por_ccg_ha_agentid_to_linkid_reg5	RW	4.3.2.18 por_ccg_ha_agentid_to_linkid_reg5 on page 309
16'h1F30	por_ccg_ha_agentid_to_linkid_reg6	RW	4.3.2.19 por_ccg_ha_agentid_to_linkid_reg6 on page 310
16'h1F38	por_ccg_ha_agentid_to_linkid_reg7	RW	4.3.2.20 por_ccg_ha_agentid_to_linkid_reg7 on page 311
16'h1FF8	por_ccg_ha_agentid_to_linkid_val	RW	4.3.2.21 por_ccg_ha_agentid_to_linkid_val on page 313
16'hC00 : 16'h13F8	por_ccg_ha_rnf_exp_raid_to_ldid_reg_0-255	RW	4.3.2.22 por_ccg_ha_rnf_exp_raid_to_ldid_reg_0-255 on page 314
16'h2000	por_ccg_ha_pmu_event_sel	RW	4.3.2.23 por_ccg_ha_pmu_event_sel on page 315
16'h1C00	por_ccg_ha_cxprtcl_link0_ctl	RW	4.3.2.24 por_ccg_ha_cxprtcl_link0_ctl on page 317
16'h1C08	por_ccg_ha_cxprtcl_link0_status	RO	4.3.2.25 por_ccg_ha_cxprtcl_link0_status on page 319
16'h1C10	por_ccg_ha_cxprtcl_link1_ctl	RW	4.3.2.26 por_ccg_ha_cxprtcl_link1_ctl on page 320
16'h1C18	por_ccg_ha_cxprtcl_link1_status	RO	4.3.2.27 por_ccg_ha_cxprtcl_link1_status on page 323
16'h1C20	por_ccg_ha_cxprtcl_link2_ctl	RW	4.3.2.28 por_ccg_ha_cxprtcl_link2_ctl on page 324
16'h1C28	por_ccg_ha_cxprtcl_link2_status	RO	4.3.2.29 por_ccg_ha_cxprtcl_link2_status on page 326

4.2.3 CCG_RA register summary

This section lists the CCG_RA registers used in CMN-700.

CCG_RA register summary

The following table shows the CCG_RA registers in offset order from the base memory address

Table 4-4: CCG_RA register summary

Offset	Name	Type	Description
16'h0	por_ccg_ra_node_info	RO	4.3.3.1 por_ccg_ra_node_info on page 328
16'h80	por_ccg_ra_child_info	RO	4.3.3.2 por_ccg_ra_child_info on page 329
16'h980	por_ccg_ra_secure_register_groups_override	RW	4.3.3.3 por_ccg_ra_secure_register_groups_override on page 330
16'h900	por_ccg_ra_unit_info	RO	4.3.3.4 por_ccg_ra_unit_info on page 331
16'hA00	por_ccg_ra_cfg_ctl	RW	4.3.3.5 por_ccg_ra_cfg_ctl on page 332
16'hA08	por_ccg_ra_aux_ctl	RW	4.3.3.6 por_ccg_ra_aux_ctl on page 334
16'hA18	por_ccg_ra_cbusy_limit_ctl	RW	4.3.3.7 por_ccg_ra_cbusy_limit_ctl on page 337

Offset	Name	Type	Description
16'hC00 : 16'hC38	por_ccg_ra_sam_addr_reg0-7on_reg0-7ndex	RW	4.3.3.8 por_ccg_ra_sam_addr_reg0-7on_reg0-7ndex on page 338
16'hD00	por_ccg_ra_agentid_to_linkid_val	RW	4.3.3.9 por_ccg_ra_agentid_to_linkid_val on page 339
16'hD10 : 16'hD48	por_ccg_ra_agent0-7d_to_l0-7nk0-7d_reg0-7ndex	RW	4.3.3.10 por_ccg_ra_agent0-7d_to_l0-7nk0-7d_reg0-7ndex on page 340
16'hE00 : 16'hEF8	por_ccg_ra_rn0-31_ld0-31d_to_exp_ra0-31d_reg0-31ndex	RW	4.3.3.11 por_ccg_ra_rn0-31_ld0-31d_to_exp_ra0-31d_reg0-31ndex on page 341
16'hF00 : 16'hFF8	por_ccg_ra_rnd_ld0-31d_to_exp_ra0-31d_reg0-31ndex	RW	4.3.3.12 por_ccg_ra_rnd_ld0-31d_to_exp_ra0-31d_reg0-31ndex on page 342
16'h1000 : 16'h13F8	por_ccg_ra_rnf_ld0-127d_to_exp_ra0-127d_reg0-127ndex	RW	4.3.3.13 por_ccg_ra_rnf_ld0-127d_to_exp_ra0-127d_reg0-127ndex on page 343
16'h1400 : 16'h1478	por_ccg_ra_ha_ld0-15d_to_exp_ra0-15d_reg0-15ndex	RW	4.3.3.14 por_ccg_ra_ha_ld0-15d_to_exp_ra0-15d_reg0-15ndex on page 345
16'h1480 : 16'h1480	por_ccg_ra_hns_ld0-0d_to_exp_ra0-0d_reg0-0ndex	RW	4.3.3.15 por_ccg_ra_hns_ld0-0d_to_exp_ra0-0d_reg0-0ndex on page 346
16'h1500 : 16'h18F8	por_ccg_ra_rnf_ld0-127d_to_ovrd_ld0-127d_reg0-127ndex	RW	4.3.3.16 por_ccg_ra_rnf_ld0-127d_to_ovrd_ld0-127d_reg0-127ndex on page 347
16'h2000	por_ccg_ra_pmu_event_sel	RW	4.3.3.17 por_ccg_ra_pmu_event_sel on page 348
16'h1C00	por_ccg_ra_ccprtcl_link0_ctl	RW	4.3.3.18 por_ccg_ra_ccprtcl_link0_ctl on page 350
16'h1C08	por_ccg_ra_ccprtcl_link0_status	RO	4.3.3.19 por_ccg_ra_ccprtcl_link0_status on page 353
16'h1C10	por_ccg_ra_ccprtcl_link1_ctl	RW	4.3.3.20 por_ccg_ra_ccprtcl_link1_ctl on page 354
16'h1C18	por_ccg_ra_ccprtcl_link1_status	RO	4.3.3.21 por_ccg_ra_ccprtcl_link1_status on page 357
16'h1C20	por_ccg_ra_ccprtcl_link2_ctl	RW	4.3.3.22 por_ccg_ra_ccprtcl_link2_ctl on page 358
16'h1C28	por_ccg_ra_ccprtcl_link2_status	RO	4.3.3.23 por_ccg_ra_ccprtcl_link2_status on page 361

4.2.4 CCLA register summary

This section lists the CCLA registers used in CMN-700.

CCLA register summary

The following table shows the CCLA registers in offset order from the base memory address

Table 4-5: CCLA register summary

Offset	Name	Type	Description
16'h0	por_ccla_node_info	RO	4.3.4.1 por_ccla_node_info on page 363
16'h80	por_ccla_child_info	RO	4.3.4.2 por_ccla_child_info on page 364
16'h988	por_ccla_secure_register_groups_override	RW	4.3.4.3 por_ccla_secure_register_groups_override on page 365
16'h910	por_ccla_unit_info	RO	4.3.4.4 por_ccla_unit_info on page 366

Offset	Name	Type	Description
16'hB00	por_ccla_cfg_ctl	RW	4.3.4.5 por_ccla_cfg_ctl on page 367
16'hB08	por_ccla_aux_ctl	RW	4.3.4.6 por_ccla_aux_ctl on page 369
16'hC00	por_ccla_ccix_prop_capabilities	RO	4.3.4.7 por_ccla_ccix_prop_capabilities on page 370
16'hC08	por_ccla_cxs_attr_capabilities	RO	4.3.4.8 por_ccla_cxs_attr_capabilities on page 372
16'hD00	por_ccla_permmsg_pyld_0_63	RW	4.3.4.9 por_ccla_permmsg_pyld_0_63 on page 374
16'hD08	por_ccla_permmsg_pyld_64_127	RW	4.3.4.10 por_ccla_permmsg_pyld_64_127 on page 374
16'hD10	por_ccla_permmsg_pyld_128_191	RW	4.3.4.11 por_ccla_permmsg_pyld_128_191 on page 375
16'hD18	por_ccla_permmsg_pyld_192_255	RW	4.3.4.12 por_ccla_permmsg_pyld_192_255 on page 376
16'hD20	por_ccla_permmsg_ctl	RW	4.3.4.13 por_ccla_permmsg_ctl on page 377
16'hD28	por_ccla_err_agent_id	RW	4.3.4.14 por_ccla_err_agent_id on page 378
16'hD30	por_ccla_agentid_to_portid_reg0	RW	4.3.4.15 por_ccla_agentid_to_portid_reg0 on page 379
16'hD38	por_ccla_agentid_to_portid_reg1	RW	4.3.4.16 por_ccla_agentid_to_portid_reg1 on page 380
16'hD40	por_ccla_agentid_to_portid_reg2	RW	4.3.4.17 por_ccla_agentid_to_portid_reg2 on page 382
16'hD48	por_ccla_agentid_to_portid_reg3	RW	4.3.4.18 por_ccla_agentid_to_portid_reg3 on page 383
16'hD50	por_ccla_agentid_to_portid_reg4	RW	4.3.4.19 por_ccla_agentid_to_portid_reg4 on page 384
16'hD58	por_ccla_agentid_to_portid_reg5	RW	4.3.4.20 por_ccla_agentid_to_portid_reg5 on page 386
16'hD60	por_ccla_agentid_to_portid_reg6	RW	4.3.4.21 por_ccla_agentid_to_portid_reg6 on page 387
16'hD68	por_ccla_agentid_to_portid_reg7	RW	4.3.4.22 por_ccla_agentid_to_portid_reg7 on page 388
16'hD70	por_ccla_agentid_to_portid_val	RW	4.3.4.23 por_ccla_agentid_to_portid_val on page 390
16'hD78	por_ccla_portfwd_en	RW	4.3.4.24 por_ccla_portfwd_en on page 391
16'hD80	por_ccla_portfwd_status	RO	4.3.4.25 por_ccla_portfwd_status on page 391
16'hD88	por_ccla_portfwd_req	RW	4.3.4.26 por_ccla_portfwd_req on page 392
16'hD90	por_ccla_linkid_to_hops	RW	4.3.4.27 por_ccla_linkid_to_hops on page 393
16'hE00	por_ccla_cxl_link_rx_credit_ctl	RW	4.3.4.28 por_ccla_cxl_link_rx_credit_ctl on page 394
16'hE08	por_ccla_cxl_link_rx_credit_return_stat	RO	4.3.4.29 por_ccla_cxl_link_rx_credit_return_stat on page 395
16'hE10	por_ccla_cxl_link_tx_credit_stat	RO	4.3.4.30 por_ccla_cxl_link_tx_credit_stat on page 396
16'hE50	por_ccla_cxl_security_policy	RW	4.3.4.31 por_ccla_cxl_security_policy on page 397
16'hE78	por_ccla_cxl_hdm_decoder_capability	RO	4.3.4.32 por_ccla_cxl_hdm_decoder_capability on page 398
16'hE80	por_ccla_cxl_hdm_decoder_global_control	RW	4.3.4.33 por_ccla_cxl_hdm_decoder_global_control on page 400
16'hE88	por_ccla_cxl_hdm_decoder_O_base_low	RWL	4.3.4.34 por_ccla_cxl_hdm_decoder_O_base_low on page 401
16'hE90	por_ccla_cxl_hdm_decoder_O_base_high	RWL	4.3.4.35 por_ccla_cxl_hdm_decoder_O_base_high on page 402
16'hE98	por_ccla_cxl_hdm_decoder_O_size_low	RWL	4.3.4.36 por_ccla_cxl_hdm_decoder_O_size_low on page 403
16'hEA0	por_ccla_cxl_hdm_decoder_O_size_high	RWL	4.3.4.37 por_ccla_cxl_hdm_decoder_O_size_high on page 404
16'hEA8	por_ccla_cxl_hdm_decoder_O_control	RWL	4.3.4.38 por_ccla_cxl_hdm_decoder_O_control on page 405
16'hEC0	por_ccla_cxl_hdm_decoder_O_dpa_skip_low	RWL	4.3.4.39 por_ccla_cxl_hdm_decoder_O_dpa_skip_low on page 406
16'hEC8	por_ccla_cxl_hdm_decoder_O_dpa_skip_high	RWL	4.3.4.40 por_ccla_cxl_hdm_decoder_O_dpa_skip_high on page 407
16'hED0	por_ccla_snoop_filter_group_id	RW	4.3.4.41 por_ccla_snoop_filter_group_id on page 408
16'hED8	por_ccla_snoop_filter_effective_size	RW	4.3.4.42 por_ccla_snoop_filter_effective_size on page 409
16'hEE0	por_ccla_kvsec_cxl_range_1_base_high	RWL	4.3.4.43 por_ccla_kvsec_cxl_range_1_base_high on page 410
16'hEE8	por_ccla_kvsec_cxl_range_1_base_low	RWL	4.3.4.44 por_ccla_kvsec_cxl_range_1_base_low on page 411

Offset	Name	Type	Description
16'hEF0	por_ccla_dvsec_cxl_range_2_base_high	RWL	4.3.4.45 por_ccla_dvsec_cxl_range_2_base_high on page 412
16'hEF8	por_ccla_dvsec_cxl_range_2_base_low	RWL	4.3.4.46 por_ccla_dvsec_cxl_range_2_base_low on page 413
16'hF00	por_ccla_dvsec_cxl_control	RWL	4.3.4.47 por_ccla_dvsec_cxl_control on page 414
16'hF08	por_ccla_dvsec_cxl_control2	RW	4.3.4.48 por_ccla_dvsec_cxl_control2 on page 415
16'hF10	por_ccla_dvsec_cxl_lock	RW	4.3.4.49 por_ccla_dvsec_cxl_lock on page 417
16'hF18	por_ccla_dvsec_flex_bus_port_control	RW	4.3.4.50 por_ccla_dvsec_flex_bus_port_control on page 418
16'hF40	por_ccla_err_capabilities_control	RW	4.3.4.51 por_ccla_err_capabilities_control on page 419
16'hF58	por_ccla_IDE_key_refresh_time_control	RW	4.3.4.52 por_ccla_IDE_key_refresh_time_control on page 420
16'hF60	por_ccla_IDE_truncation_transmit_delay_control	RW	4.3.4.53 por_ccla_IDE_truncation_transmit_delay_control on page 421
16'hF70	por_ccla_ll_to_ull_msg	RW	4.3.4.54 por_ccla_ll_to_ull_msg on page 422
16'hF80	por_ccla_cxl_timeout_isolation_control	RW	4.3.4.55 por_ccla_cxl_timeout_isolation_control on page 422
16'hF28	por_ccla_root_port_n_security_policy	RW	4.3.4.56 por_ccla_root_port_n_security_policy on page 424
16'hF30	por_ccla_root_port_n_id	RW	4.3.4.57 por_ccla_root_port_n_id on page 425
16'hE18	por_ccla_cxl_link_layer_defeature	RW	4.3.4.58 por_ccla_cxl_link_layer_defeature on page 426
16'hE20	por_ccla_ull_ctl	RW	4.3.4.59 por_ccla_ull_ctl on page 427
16'hE28	por_ccla_ull_status	RO	4.3.4.60 por_ccla_ull_status on page 428
16'hE30	por_ccla_cxl_ll_errinject_ctl	RW	4.3.4.61 por_ccla_cxl_ll_errinject_ctl on page 429
16'hE38	por_ccla_cxl_ll_errinject_stat	RO	4.3.4.62 por_ccla_cxl_ll_errinject_stat on page 430
16'hE40	por_ccla_cxl_viral_prop_en	RW	4.3.4.63 por_ccla_cxl_viral_prop_en on page 431
16'h2008	por_ccla_pmu_event_sel	RW	4.3.4.64 por_ccla_pmu_event_sel on page 432
16'h3000	por_ccla_errfr	RO	4.3.4.65 por_ccla_errfr on page 433
16'h3008	por_ccla_errctlr	RW	4.3.4.66 por_ccla_errctlr on page 435
16'h3010	por_ccla_errstatus	W1C	4.3.4.67 por_ccla_errstatus on page 436
16'h3018	por_ccla_erraddr	RW	4.3.4.68 por_ccla_erraddr on page 438
16'h3020	por_ccla_errmisc	RW	4.3.4.69 por_ccla_errmisc on page 439
16'h3100	por_ccla_errfr_NS	RO	4.3.4.70 por_ccla_errfr_NS on page 440
16'h3108	por_ccla_errctlr_NS	RW	4.3.4.71 por_ccla_errctlr_NS on page 441
16'h3110	por_ccla_errstatus_NS	W1C	4.3.4.72 por_ccla_errstatus_NS on page 442
16'h3118	por_ccla_erraddr_NS	RW	4.3.4.73 por_ccla_erraddr_NS on page 444
16'h3120	por_ccla_errmisc_NS	RW	4.3.4.74 por_ccla_errmisc_NS on page 445

4.2.5 Configuration manager register summary

This section lists the configuration manager registers used in CMN-700.

CFGM register summary

The following table shows the CFGM registers in offset order from the base memory address

Table 4-6: CFGM register summary

Offset	Name	Type	Description
16'h0	por_cfgm_node_info	RO	4.3.5.1 por_cfgm_node_info on page 446
16'h8	por_cfgm_periph_id_0_periph_id_1	RO	4.3.5.2 por_cfgm_periph_id_0_periph_id_1 on page 447
16'h10	por_cfgm_periph_id_2_periph_id_3	RO	4.3.5.3 por_cfgm_periph_id_2_periph_id_3 on page 448
16'h18	por_cfgm_periph_id_4_periph_id_5	RO	4.3.5.4 por_cfgm_periph_id_4_periph_id_5 on page 449
16'h20	por_cfgm_periph_id_6_periph_id_7	RO	4.3.5.5 por_cfgm_periph_id_6_periph_id_7 on page 450
16'h28	por_cfgm_component_id_0_component_id_1	RO	4.3.5.6 por_cfgm_component_id_0_component_id_1 on page 451
16'h30	por_cfgm_component_id_2_component_id_3	RO	4.3.5.7 por_cfgm_component_id_2_component_id_3 on page 452
16'h80	por_cfgm_child_info	RO	4.3.5.8 por_cfgm_child_info on page 453
16'h980	por_cfgm_secure_access	RW	4.3.5.9 por_cfgm_secure_access on page 454
16'h988	por_cfgm_secure_register_groups_override	RW	4.3.5.10 por_cfgm_secure_register_groups_override on page 455
16'h3000 : 16'h3038	por_cfgm_errgsr_mxp_0-7	RO	4.3.5.11 por_cfgm_errgsr_mxp_0-7 on page 456
16'h3040 : 16'h3078	por_cfgm_errgsr_mxp_0-7_NS	RO	4.3.5.12 por_cfgm_errgsr_mxp_0-7_NS on page 457
16'h3080 : 16'h30B8	por_cfgm_errgsr_hni_0-7	RO	4.3.5.13 por_cfgm_errgsr_hni_0-7 on page 458
16'h30C0 : 16'h30F8	por_cfgm_errgsr_hni_0-7_NS	RO	4.3.5.14 por_cfgm_errgsr_hni_0-7_NS on page 459
16'h3100 : 16'h3138	por_cfgm_errgsr_hnf_0-7	RO	4.3.5.15 por_cfgm_errgsr_hnf_0-7 on page 459
16'h3140 : 16'h3178	por_cfgm_errgsr_hnf_0-7_NS	RO	4.3.5.16 por_cfgm_errgsr_hnf_0-7_NS on page 460
16'h3180 : 16'h31B8	por_cfgm_errgsr_sbsx_0-7	RO	4.3.5.17 por_cfgm_errgsr_sbsx_0-7 on page 461
16'h31C0 : 16'h31F8	por_cfgm_errgsr_sbsx_0-7_NS	RO	4.3.5.18 por_cfgm_errgsr_sbsx_0-7_NS on page 462
16'h3200 : 16'h3238	por_cfgm_errgsr_cxg_0-7	RO	4.3.5.19 por_cfgm_errgsr_cxg_0-7 on page 463
16'h3240 : 16'h3278	por_cfgm_errgsr_cxg_0-7_NS	RO	4.3.5.20 por_cfgm_errgsr_cxg_0-7_NS on page 464
16'h3280 : 16'h32B8	por_cfgm_errgsr_mtsx_0-7	RO	4.3.5.21 por_cfgm_errgsr_mtsx_0-7 on page 465
16'h32C0 : 16'h32F8	por_cfgm_errgsr_mtsx_0-7_NS	RO	4.3.5.22 por_cfgm_errgsr_mtsx_0-7_NS on page 466
16'h3FA8	por_cfgm_errdevaff	RO	4.3.5.23 por_cfgm_errdevaff on page 467
16'h3FB8	por_cfgm_errdevarch	RO	4.3.5.24 por_cfgm_errdevarch on page 468
16'h3FC8	por_cfgm_erridr	RO	4.3.5.25 por_cfgm_erridr on page 469
16'h3FD0	por_cfgm_errpidr45	RO	4.3.5.26 por_cfgm_errpidr45 on page 470
16'h3FD8	por_cfgm_errpidr67	RO	4.3.5.27 por_cfgm_errpidr67 on page 471
16'h3FE0	por_cfgm_errpidr01	RO	4.3.5.28 por_cfgm_errpidr01 on page 472
16'h3FE8	por_cfgm_errpidr23	RO	4.3.5.29 por_cfgm_errpidr23 on page 473

Offset	Name	Type	Description
16'h3FF0	por_cfgm_errcidr01	RO	4.3.5.30 por_cfgm_errcidr01 on page 474
16'h3FF8	por_cfgm_errcidr23	RO	4.3.5.31 por_cfgm_errcidr23 on page 475
16'h900	por_info_global	RO	4.3.5.32 por_info_global on page 476
16'h908	por_info_global_1	RO	4.3.5.33 por_info_global_1 on page 478
16'h1C00	por_ppu_int_enable	RW	4.3.5.34 por_ppu_int_enable on page 479
16'h1C08	por_ppu_int_enable_1	RW	4.3.5.35 por_ppu_int_enable_1 on page 480
16'h1C10	por_ppu_int_status	W1C	4.3.5.36 por_ppu_int_status on page 481
16'h1C18	por_ppu_int_status_1	W1C	4.3.5.37 por_ppu_int_status_1 on page 482
16'h1C20	por_ppu_qactive_hyst	RW	4.3.5.38 por_ppu_qactive_hyst on page 483
16'h1C28	por_mpam_s_err_int_status	W1C	4.3.5.39 por_mpam_s_err_int_status on page 483
16'h1C30	por_mpam_s_err_int_status_1	W1C	4.3.5.40 por_mpam_s_err_int_status_1 on page 484
16'h1C38	por_mpam_ns_err_int_status	W1C	4.3.5.41 por_mpam_ns_err_int_status on page 485
16'h1C40	por_mpam_ns_err_int_status_1	W1C	4.3.5.42 por_mpam_ns_err_int_status_1 on page 486
16'h100 : 16'h8F8	por_cfgm_child_pointer_0-255	RO	4.3.5.43 por_cfgm_child_pointer_0-255 on page 487

4.2.6 CXLAPB register summary

This section lists the CXLAPB registers used in CMN-700

CXLAPB register summary

The following table shows the CXLAPB registers in offset order from the base memory address

Table 4-7: por_cxlapb_cfg register summary

Offset	Name	Type	Description
16'h1110	por_cxlapb_link_rx_credit_ctl	RW	4.3.6.1 por_cxlapb_link_rx_credit_ctl on page 488
16'h1118	por_cxlapb_link_rx_credit_return_stat	RO	4.3.6.2 por_cxlapb_link_rx_credit_return_stat on page 489
16'h1120	por_cxlapb_link_tx_credit_stat	RO	4.3.6.3 por_cxlapb_link_tx_credit_stat on page 490
16'h1060	por_cxlapb_cxl_security_policy	RW	4.3.6.4 por_cxlapb_cxl_security_policy on page 491
16'h1200	por_cxlapb_cxl_hdm_decoder_capability	RO	4.3.6.5 por_cxlapb_cxl_hdm_decoder_capability on page 492
16'h1204	por_cxlapb_cxl_hdm_decoder_global_control	RW	4.3.6.6 por_cxlapb_cxl_hdm_decoder_global_control on page 494
16'h1210	por_cxlapb_cxl_hdm_decoder_0_base_low	RWL	4.3.6.7 por_cxlapb_cxl_hdm_decoder_0_base_low on page 495
16'h1214	por_cxlapb_cxl_hdm_decoder_0_base_high	RWL	4.3.6.8 por_cxlapb_cxl_hdm_decoder_0_base_high on page 495
16'h1218	por_cxlapb_cxl_hdm_decoder_0_size_low	RWL	4.3.6.9 por_cxlapb_cxl_hdm_decoder_0_size_low on page 496
16'h121C	por_cxlapb_cxl_hdm_decoder_0_size_high	RWL	4.3.6.10 por_cxlapb_cxl_hdm_decoder_0_size_high on page 497
16'h1220	por_cxlapb_cxl_hdm_decoder_0_control	RWL	4.3.6.11 por_cxlapb_cxl_hdm_decoder_0_control on page 498
16'h1224	por_cxlapb_cxl_hdm_decoder_0_dpa_skip_low	RWL	4.3.6.12 por_cxlapb_cxl_hdm_decoder_0_dpa_skip_low on page 499
16'h1228	por_cxlapb_cxl_hdm_decoder_0_dpa_skip_high	RWL	4.3.6.13 por_cxlapb_cxl_hdm_decoder_0_dpa_skip_high on page 500
16'h1800	por_cxlapb_snoop_filter_group_id	RO	4.3.6.14 por_cxlapb_snoop_filter_group_id on page 501
16'h1804	por_cxlapb_snoop_filter_effective_size	RO	4.3.6.15 por_cxlapb_snoop_filter_effective_size on page 502

Offset	Name	Type	Description
16'h120	por_cxlapb_dvsec_cxl_range_1_base_high	RWL	4.3.6.16 por_cxlapb_dvsec_cxl_range_1_base_high on page 503
16'h124	por_cxlapb_dvsec_cxl_range_1_base_low	RWL	4.3.6.17 por_cxlapb_dvsec_cxl_range_1_base_low on page 504
16'h130	por_cxlapb_dvsec_cxl_range_2_base_high	RWL	4.3.6.18 por_cxlapb_dvsec_cxl_range_2_base_high on page 505
16'h134	por_cxlapb_dvsec_cxl_range_2_base_low	RWL	4.3.6.19 por_cxlapb_dvsec_cxl_range_2_base_low on page 506
16'h10C	por_cxlapb_dvsec_cxl_control	RWL	4.3.6.20 por_cxlapb_dvsec_cxl_control on page 507
16'h110	por_cxlapb_dvsec_cxl_control2	RW	4.3.6.21 por_cxlapb_dvsec_cxl_control2 on page 508
16'h114	por_cxlapb_dvsec_cxl_lock	RW	4.3.6.22 por_cxlapb_dvsec_cxl_lock on page 509
16'h20C	por_cxlapb_dvsec_flex_bus_port_control	RW	4.3.6.23 por_cxlapb_dvsec_flex_bus_port_control on page 510
16'h1014	por_cxlapb_err_capabilities_control	RW	4.3.6.24 por_cxlapb_err_capabilities_control on page 511
16'h18	por_cxlapb_IDE_key_refresh_time_control	RW	4.3.6.25 por_cxlapb_IDE_key_refresh_time_control on page 512
16'h24	por_cxlapb_IDE_truncation_transmit_delay_control	RW	4.3.6.26 por_cxlapb_IDE_truncation_transmit_delay_control on page 513
16'h0	por_cxlapb_ll_to_ull_msg	RW	4.3.6.27 por_cxlapb_ll_to_ull_msg on page 514
16'h8	por_cxlapb_cxl_timeout_isolation_control	RW	4.3.6.28 por_cxlapb_cxl_timeout_isolation_control on page 515
16'h1130	por_cxlapb_link_layer_defeature	RW	4.3.6.29 por_cxlapb_link_layer_defeature on page 516

4.2.7 Debug and trace register summary

This section lists the debug and trace registers used in CMN-700.

DT register summary

The following table shows the DT registers in offset order from the base memory address

Table 4-8: DT register summary

Offset	Name	Type	Description
16'h0	por_dt_node_info	RO	4.3.7.1 por_dt_node_info on page 517
16'h80	por_dt_child_info	RO	4.3.7.2 por_dt_child_info on page 518
16'h980	por_dt_secure_access	RW	4.3.7.3 por_dt_secure_access on page 519
16'hA00	por_dt_dtc_ctl	RW	4.3.7.4 por_dt_dtc_ctl on page 520
16'hA10	por_dt_trigger_status	RO	4.3.7.5 por_dt_trigger_status on page 522
16'hA20	por_dt_trigger_status_clr	WO	4.3.7.6 por_dt_trigger_status_clr on page 522
16'hA30	por_dt_trace_control	RW	4.3.7.7 por_dt_trace_control on page 523
16'hA48	por_dt_traceid	RW	4.3.7.8 por_dt_traceid on page 524
16'h2000	por_dt_pmevcntAB	RW	4.3.7.9 por_dt_pmevcntAB on page 525
16'h2010	por_dt_pmevcntCD	RW	4.3.7.10 por_dt_pmevcntCD on page 526
16'h2020	por_dt_pmevcntEF	RW	4.3.7.11 por_dt_pmevcntEF on page 527
16'h2030	por_dt_pmevcntGH	RW	4.3.7.12 por_dt_pmevcntGH on page 528
16'h2040	por_dt_pmccntr	RW	4.3.7.13 por_dt_pmccntr on page 529
16'h2050	por_dt_pmevcntsAB	RW	4.3.7.14 por_dt_pmevcntsAB on page 529
16'h2060	por_dt_pmevcntsCD	RW	4.3.7.15 por_dt_pmevcntsCD on page 530
16'h2070	por_dt_pmevcntsEF	RW	4.3.7.16 por_dt_pmevcntsEF on page 531

Offset	Name	Type	Description
16'h2080	por_dt_pmevcntsrGH	RW	4.3.7.17 por_dt_pmevcntsrGH on page 532
16'h2090	por_dt_pmccntrs	RW	4.3.7.18 por_dt_pmccntrs on page 533
16'h2100	por_dt_pmcr	RW	4.3.7.19 por_dt_pmcr on page 534
16'h2118	por_dt_pmovsr	RO	4.3.7.20 por_dt_pmovsr on page 535
16'h2120	por_dt_pmovsr_clr	WO	4.3.7.21 por_dt_pmovsr_clr on page 536
16'h2128	por_dt_pmssr	RO	4.3.7.22 por_dt_pmssr on page 537
16'h2130	por_dt_pmsrr	WO	4.3.7.23 por_dt_pmsrr on page 538
16'hFA0	por_dt_claim	RW	4.3.7.24 por_dt_claim on page 538
16'hFA8	por_dt_devaff	RO	4.3.7.25 por_dt_devaff on page 539
16'hFB0	por_dt_lsr	RO	4.3.7.26 por_dt_lsr on page 540
16'hFB8	por_dt_authstatus_devarch	RO	4.3.7.27 por_dt_authstatus_devarch on page 541
16'hFC0	por_dt_devid	RO	4.3.7.28 por_dt_devid on page 542
16'hFC8	por_dt_devtype	RO	4.3.7.29 por_dt_devtype on page 543
16'hFD0	por_dt_pidr45	RO	4.3.7.30 por_dt_pidr45 on page 544
16'hFD8	por_dt_pidr67	RO	4.3.7.31 por_dt_pidr67 on page 545
16'hFE0	por_dt_pidr01	RO	4.3.7.32 por_dt_pidr01 on page 546
16'hFE8	por_dt_pidr23	RO	4.3.7.33 por_dt_pidr23 on page 547
16'hFF0	por_dt_cidr01	RO	4.3.7.34 por_dt_cidr01 on page 548
16'hFF8	por_dt_cidr23	RO	4.3.7.35 por_dt_cidr23 on page 549

4.2.8 DN register summary

This section lists the DN registers used in CMN-700.

DN register summary

The following table shows the DN registers in offset order from the base memory address

Table 4-9: DN register summary

Offset	Name	Type	Description
16'h0	por_dn_node_info	RO	4.3.8.1 por_dn_node_info on page 550
16'h80	por_dn_child_info	RO	4.3.8.2 por_dn_child_info on page 551
16'h900	por_dn_build_info	RO	4.3.8.3 por_dn_build_info on page 552
16'h980	por_dn_secure_register_groups_override	RW	4.3.8.4 por_dn_secure_register_groups_override on page 553
16'hA00	por_dn_cfg_ctl	RW	4.3.8.5 por_dn_cfg_ctl on page 554
16'hA08	por_dn_aux_ctl	RW	4.3.8.6 por_dn_aux_ctl on page 555
16'hC00 + #{{56}*index}	por_dn_vmf0-15_ctrl	RW	4.3.8.7 por_dn_vmf0-15_ctrl on page 556
16'hC00 + #{{56}*index + 8}	por_dn_vmf0-15_rnf0	RW	4.3.8.8 por_dn_vmf0-15_rnf0 on page 557
16'hC00 + #{{56}*index + 16}	por_dn_vmf0-15_rnf1	RW	4.3.8.9 por_dn_vmf0-15_rnf1 on page 558

Offset	Name	Type	Description
16'hC00 + #{{56}*index + 24}	por_dn_vmf0-15_rnf2	RW	4.3.8.10 por_dn_vmf0-15_rnf2 on page 559
16'hC00 + #{{56}*index + 32}	por_dn_vmf0-15_rnf3	RW	4.3.8.11 por_dn_vmf0-15_rnf3 on page 560
16'hC00 + #{{56}*index + 40}	por_dn_vmf0-15_rnd0	RW	4.3.8.12 por_dn_vmf0-15_rnd0 on page 561
16'hC00 + #{{56}*index + 48}	por_dn_vmf0-15(cxra)	RW	4.3.8.13 por_dn_vmf0-15(cxra) on page 562
16'hF80 : 16'hF98	por_dn_domain_rnf0-3	RW	4.3.8.14 por_dn_domain_rnf0-3 on page 563
16'hFA0	por_dn_domain_rnd0	RW	4.3.8.15 por_dn_domain_rnd0 on page 564
16'hFA8	por_dn_domain_cxra	RW	4.3.8.16 por_dn_domain_cxra on page 565
16'hFB0 : 16'h1028	por_dn_vmf0-15_rnd1	RW	4.3.8.17 por_dn_vmf0-15_rnd1 on page 566
16'h1030	por_dn_domain_rnd1	RW	4.3.8.18 por_dn_domain_rnd1 on page 567
16'h2000	por_dn_pmu_event_sel	RW	4.3.8.19 por_dn_pmu_event_sel on page 568

4.2.9 HN-F register summary

This section lists the HN-F registers used in CMN-700.

HN-F register summary

The following table shows the HN-F registers in offset order from the base memory address

Table 4-10: HN-F register summary

Offset	Name	Type	Description
16'h0	cmn_hns_node_info	RO	4.3.10.1 cmn_hns_node_info on page 599
16'h80	cmn_hns_child_info	RO	4.3.10.2 cmn_hns_child_info on page 600
16'h980	cmn_hns_secure_register_groups_override	RW	4.3.10.3 cmn_hns_secure_register_groups_override on page 601
16'h900	cmn_hns_unit_info	RO	4.3.10.4 cmn_hns_unit_info on page 602
16'h908	cmn_hns_unit_info_1	RO	4.3.10.5 cmn_hns_unit_info_1 on page 605
16'hA00	cmn_hns_cfg_ctl	RW	4.3.10.6 cmn_hns_cfg_ctl on page 606
16'hA08	cmn_hns_aux_ctl	RW	4.3.10.7 cmn_hns_aux_ctl on page 609
16'hA10	cmn_hns_aux_ctl_1	RW	4.3.10.8 cmn_hns_aux_ctl_1 on page 613
16'hA18	cmn_hns_cbusy_limit_ctl	RW	4.3.10.9 cmn_hns_cbusy_limit_ctl on page 616
16'hA20	cmn_hns_txrsp_arb_weight_ctl	RW	4.3.10.10 cmn_hns_txrsp_arb_weight_ctl on page 617
16'hA28	cmn_hns_cbusy_mode_ctl	RW	4.3.10.11 cmn_hns_cbusy_mode_ctl on page 618
16'hA30	cmn_hns_lbt_cfg_ctl	RW	4.3.10.12 cmn_hns_lbt_cfg_ctl on page 620
16'hA38	cmn_hns_lbt_aux_ctl	RW	4.3.10.13 cmn_hns_lbt_aux_ctl on page 621
16'h1C00	cmn_hns_ppu_pwpr	RW	4.3.10.14 cmn_hns_ppu_pwpr on page 624
16'h1C08	cmn_hns_ppu_pwsr	RO	4.3.10.15 cmn_hns_ppu_pwsr on page 625
16'h1C14	cmn_hns_ppu_misr	RO	4.3.10.16 cmn_hns_ppu_misr on page 627
16'h2BB0	cmn_hns_ppu_idr0	RO	4.3.10.17 cmn_hns_ppu_idr0 on page 628

Offset	Name	Type	Description
16'h2BB4	cmn_hns_ppu_idr1	RO	4.3.10.18 cmn_hns_ppu_idr1 on page 630
16'h2BC8	cmn_hns_ppu_iidr	RO	4.3.10.19 cmn_hns_ppu_iidr on page 630
16'h2BCC	cmn_hns_ppu_aidr	RO	4.3.10.20 cmn_hns_ppu_aidr on page 631
16'h1D00	cmn_hns_ppu_dyn_ret_threshold	RW	4.3.10.21 cmn_hns_ppu_dyn_ret_threshold on page 632
16'hA80	cmn_hns_qos_band	RO	4.3.10.22 cmn_hns_qos_band on page 633
16'h3000	cmn_hns_errfr	RO	4.3.10.23 cmn_hns_errfr on page 635
16'h3008	cmn_hns_errctlr	RW	4.3.10.24 cmn_hns_errctlr on page 636
16'h3010	cmn_hns_errstatus	W1C	4.3.10.25 cmn_hns_errstatus on page 637
16'h3018	cmn_hns_erraddr	RW	4.3.10.26 cmn_hns_erraddr on page 639
16'h3020	cmn_hns_errmisc	RW	4.3.10.27 cmn_hns_errmisc on page 640
16'h3030	cmn_hns_err_inj	RW	4.3.10.28 cmn_hns_err_inj on page 642
16'h3038	cmn_hns_byte_par_err_inj	WO	4.3.10.29 cmn_hns_byte_par_err_inj on page 643
16'h3100	cmn_hns_errfr_NS	RO	4.3.10.30 cmn_hns_errfr_NS on page 644
16'h3108	cmn_hns_errctlr_NS	RW	4.3.10.31 cmn_hns_errctlr_NS on page 645
16'h3110	cmn_hns_errstatus_NS	W1C	4.3.10.32 cmn_hns_errstatus_NS on page 646
16'h3118	cmn_hns_erraddr_NS	RW	4.3.10.33 cmn_hns_erraddr_NS on page 648
16'h3120	cmn_hns_errmisc_NS	RW	4.3.10.34 cmn_hns_errmisc_NS on page 649
16'hC00	cmn_hns_slc_lock_ways	RW	4.3.10.35 cmn_hns_slc_lock_ways on page 650
16'hC08	cmn_hns_slc_lock_base0	RW	4.3.10.36 cmn_hns_slc_lock_base0 on page 651
16'hC10	cmn_hns_slc_lock_base1	RW	4.3.10.37 cmn_hns_slc_lock_base1 on page 652
16'hC18	cmn_hns_slc_lock_base2	RW	4.3.10.38 cmn_hns_slc_lock_base2 on page 653
16'hC20	cmn_hns_slc_lock_base3	RW	4.3.10.39 cmn_hns_slc_lock_base3 on page 654
16'hC28	cmn_hns_rni_region_vec	RW	4.3.10.40 cmn_hns_rni_region_vec on page 655
16'hC30	cmn_hns_rnd_region_vec	RW	4.3.10.41 cmn_hns_rnd_region_vec on page 656
16'hC38	cmn_hns_rnf_region_vec	RW	4.3.10.42 cmn_hns_rnf_region_vec on page 657
16'hC40	cmn_hns_rnf_region_vec1	RW	4.3.10.43 cmn_hns_rnf_region_vec1 on page 658
16'hC48	cmn_hns_slcway_partition0_rnf_vec	RW	4.3.10.44 cmn_hns_slcway_partition0_rnf_vec on page 659
16'hC50	cmn_hns_slcway_partition1_rnf_vec	RW	4.3.10.45 cmn_hns_slcway_partition1_rnf_vec on page 660
16'hC58	cmn_hns_slcway_partition2_rnf_vec	RW	4.3.10.46 cmn_hns_slcway_partition2_rnf_vec on page 661
16'hC60	cmn_hns_slcway_partition3_rnf_vec	RW	4.3.10.47 cmn_hns_slcway_partition3_rnf_vec on page 662
16'hCB0	cmn_hns_slcway_partition0_rnf_vec1	RW	4.3.10.48 cmn_hns_slcway_partition0_rnf_vec1 on page 663
16'hCB8	cmn_hns_slcway_partition1_rnf_vec1	RW	4.3.10.49 cmn_hns_slcway_partition1_rnf_vec1 on page 664
16'hCC0	cmn_hns_slcway_partition2_rnf_vec1	RW	4.3.10.50 cmn_hns_slcway_partition2_rnf_vec1 on page 665
16'hCC8	cmn_hns_slcway_partition3_rnf_vec1	RW	4.3.10.51 cmn_hns_slcway_partition3_rnf_vec1 on page 666

Offset	Name	Type	Description
16'hC68	cmn_hns_slcway_partition0_rni_vec	RW	4.3.10.52 cmn_hns_slcway_partition0_rni_vec on page 667
16'hC70	cmn_hns_slcway_partition1_rni_vec	RW	4.3.10.53 cmn_hns_slcway_partition1_rni_vec on page 668
16'hC78	cmn_hns_slcway_partition2_rni_vec	RW	4.3.10.54 cmn_hns_slcway_partition2_rni_vec on page 669
16'hC80	cmn_hns_slcway_partition3_rni_vec	RW	4.3.10.55 cmn_hns_slcway_partition3_rni_vec on page 670
16'hC88	cmn_hns_slcway_partition0_rnd_vec	RW	4.3.10.56 cmn_hns_slcway_partition0_rnd_vec on page 671
16'hC90	cmn_hns_slcway_partition1_rnd_vec	RW	4.3.10.57 cmn_hns_slcway_partition1_rnd_vec on page 672
16'hC98	cmn_hns_slcway_partition2_rnd_vec	RW	4.3.10.58 cmn_hns_slcway_partition2_rnd_vec on page 673
16'hCA0	cmn_hns_slcway_partition3_rnd_vec	RW	4.3.10.59 cmn_hns_slcway_partition3_rnd_vec on page 674
16'hCA8	cmn_hns_rn_region_lock	RW	4.3.10.60 cmn_hns_rn_region_lock on page 675
16'hCD0	cmn_hns_sf_cxg_blocked_ways	RW	4.3.10.61 cmn_hns_sf_cxg_blocked_ways on page 676
16'hCE0	cmn_hns_cxg_ha_metadata_exclusion_list	RW	4.3.10.62 cmn_hns_cxg_ha_metadata_exclusion_list on page 677
16'hCD8	cmn_hns_cxg_ha_smp_exclusion_list	RW	4.3.10.63 cmn_hns_cxg_ha_smp_exclusion_list on page 678
16'hCF0	hn_sam_hash_addr_mask_reg	RW	4.3.10.64 hn_sam_hash_addr_mask_reg on page 679
16'hCF8	hn_sam_region_cmp_addr_mask_reg	RW	4.3.10.65 hn_sam_region_cmp_addr_mask_reg on page 680
16'hD48	cmn_hns_sam_cfg1_def_hashed_region	RW	4.3.10.66 cmn_hns_sam_cfg1_def_hashed_region on page 681
16'hD50	cmn_hns_sam_cfg2_def_hashed_region	RW	4.3.10.67 cmn_hns_sam_cfg2_def_hashed_region on page 682
16'hD00	cmn_hns_sam_control	RW	4.3.10.68 cmn_hns_sam_control on page 683
16'hD28	cmn_hns_sam_control2	RW	4.3.10.69 cmn_hns_sam_control2 on page 685
16'hD08	cmn_hns_sam_memregion0	RW	4.3.10.70 cmn_hns_sam_memregion0 on page 686
16'hD38	cmn_hns_sam_memregion0_end_addr	RW	4.3.10.71 cmn_hns_sam_memregion0_end_addr on page 687
16'hD10	cmn_hns_sam_memregion1	RW	4.3.10.72 cmn_hns_sam_memregion1 on page 688
16'hD40	cmn_hns_sam_memregion1_end_addr	RW	4.3.10.73 cmn_hns_sam_memregion1_end_addr on page 689
16'hD18	cmn_hns_sam_sn_properties	RW	4.3.10.74 cmn_hns_sam_sn_properties on page 690
16'hD20	cmn_hns_sam_6sn_nodeid	RW	4.3.10.75 cmn_hns_sam_6sn_nodeid on page 693
16'hCE8	cmn_hns_sam_sn_properties1	RW	4.3.10.76 cmn_hns_sam_sn_properties1 on page 695
16'hD30	cmn_hns_sam_sn_properties2	RW	4.3.10.77 cmn_hns_sam_sn_properties2 on page 697
16'hF80 : 16'hFA0	cmn_hns_cml_port_aggr_grp0-4_add_mask	RW	4.3.10.78 cmn_hns_cml_port_aggr_grp0-4_add_mask on page 699
16'h6028 : 16'h60F8	cmn_hns_cml_port_aggr_grp5-31_add_mask	RW	4.3.10.79 cmn_hns_cml_port_aggr_grp5-31_add_mask on page 700

Offset	Name	Type	Description
{0-1} 16'hF80 : 16'hFB8	cmn_hns_cml_port_aggr_grp_reg0-12	RW	4.3.10.80 cmn_hns_cml_port_aggr_grp_reg0-12 on page 701
{2-12} 16'h6110 : 16'h6160			
16'hF00	cmn_hns_cml_port_aggr_ctrl_reg	RW	4.3.10.81 cmn_hns_cml_port_aggr_ctrl_reg on page 702
16'h6208 : 16'h6230	cmn_hns_cml_port_aggr_ctrl_reg1-6	RW	4.3.10.82 cmn_hns_cml_port_aggr_ctrl_reg1-6 on page 704
16'hF50	cmn_hns_abf_lo_addr	RW	4.3.10.83 cmn_hns_abf_lo_addr on page 707
16'hF58	cmn_hns_abf_hi_addr	RW	4.3.10.84 cmn_hns_abf_hi_addr on page 708
16'hF60	cmn_hns_abf_pr	RW	4.3.10.85 cmn_hns_abf_pr on page 709
16'hF68	cmn_hns_abf_sr	RO	4.3.10.86 cmn_hns_abf_sr on page 710
16'h1000	cmn_hns_cbusy_write_limit_ctl	RW	4.3.10.87 cmn_hns_cbusy_write_limit_ctl on page 711
16'h1008	cmn_hns_cbusy_resp_ctl	RW	4.3.10.88 cmn_hns_cbusy_resp_ctl on page 712
16'h1010	cmn_hns_cbusy_sn_ctl	RW	4.3.10.89 cmn_hns_cbusy_sn_ctl on page 714
16'h1018	cmn_hns_lbt_cbusy_ctl	RW	4.3.10.90 cmn_hns_lbt_cbusy_ctl on page 715
16'h1020	cmn_hns_pocq_alloc_class_dedicated	RW	4.3.10.91 cmn_hns_pocq_alloc_class_dedicated on page 716
16'h1028	cmn_hns_pocq_alloc_class_max_allowed	RW	4.3.10.92 cmn_hns_pocq_alloc_class_max_allowed on page 718
16'h1030	cmn_hns_pocq_alloc_class_contented_min	RW	4.3.10.93 cmn_hns_pocq_alloc_class_contented_min on page 719
16'h1038	cmn_hns_pocq_alloc_misc_max_allowed	RW	4.3.10.94 cmn_hns_pocq_alloc_misc_max_allowed on page 720
16'h1040	cmn_hns_class_ctl	RW	4.3.10.95 cmn_hns_class_ctl on page 721
16'h1048	cmn_hns_pocq_qos_class_ctl	RW	4.3.10.96 cmn_hns_pocq_qos_class_ctl on page 722
16'h1050	cmn_hns_class_pocq_arb_weight_ctl	RW	4.3.10.97 cmn_hns_class_pocq_arb_weight_ctl on page 723
16'h1058	cmn_hns_class_retry_weight_ctl	RW	4.3.10.98 cmn_hns_class_retry_weight_ctl on page 724
16'h1060	cmn_hns_pocq_misc_retry_weight_ctl	RW	4.3.10.99 cmn_hns_pocq_misc_retry_weight_ctl on page 725
16'hFE0	cmn_hns_partner_scratch_reg0	RW	4.3.10.100 cmn_hns_partner_scratch_reg0 on page 727
16'hFE8	cmn_hns_partner_scratch_reg1	RW	4.3.10.101 cmn_hns_partner_scratch_reg1 on page 728
16'hB80	cmn_hns_cfg_slcsf_dbgrd	WO	4.3.10.102 cmn_hns_cfg_slcsf_dbgrd on page 729
16'hB88	cmn_hns_slc_cache_access_slc_tag	RO	4.3.10.103 cmn_hns_slc_cache_access_slc_tag on page 730
16'hB90	cmn_hns_slc_cache_access_slc_tag1	RO	4.3.10.104 cmn_hns_slc_cache_access_slc_tag1 on page 731
16'hB98	cmn_hns_slc_cache_access_slc_data	RO	4.3.10.105 cmn_hns_slc_cache_access_slc_data on page 732
16'hBC0	cmn_hns_slc_cache_access_slc_mte_tag	RO	4.3.10.106 cmn_hns_slc_cache_access_slc_mte_tag on page 733
16'hBA0	cmn_hns_slc_cache_access_sf_tag	RO	4.3.10.107 cmn_hns_slc_cache_access_sf_tag on page 734
16'hBA8	cmn_hns_slc_cache_access_sf_tag1	RO	4.3.10.108 cmn_hns_slc_cache_access_sf_tag1 on page 735

Offset	Name	Type	Description
16'hB00	cmn_hns_slc_cache_access_sf_tag2	RO	4.3.10.109 cmn_hns_slc_cache_access_sf_tag2 on page 736
16'h2000	cmn_hns_pmu_event_sel	RW	4.3.10.110 cmn_hns_pmu_event_sel on page 737
16'h2008	cmn_hns_pmu_mpam_sel	RW	4.3.10.111 cmn_hns_pmu_mpam_sel on page 741
16'h2010 : 16'h2048	cmn_hns_pmu_mpam_pardid_mask0-7	RW	4.3.10.112 cmn_hns_pmu_mpam_pardid_mask0-7 on page 742
16'h3C00 + #{{index}*32}	cmn_hns_rn_cluster0-63_physid_reg0	RW	4.3.10.113 cmn_hns_rn_cluster0-63_physid_reg0 on page 743
16'h3C00 + #{{index}*32}	cmn_hns_rn_cluster64-127_physid_reg0	RW	4.3.10.114 cmn_hns_rn_cluster64-127_physid_reg0 on page 746
16'h3C08 + #{{index}*32}	cmn_hns_rn_cluster0-127_physid_reg1	RW	4.3.10.115 cmn_hns_rn_cluster0-127_physid_reg1 on page 748
16'h3C10 + #{{index}*32}	cmn_hns_rn_cluster0-127_physid_reg2	RW	4.3.10.116 cmn_hns_rn_cluster0-127_physid_reg2 on page 750
16'h3C18 + #{{index}*32}	cmn_hns_rn_cluster0-127_physid_reg3	RW	4.3.10.117 cmn_hns_rn_cluster0-127_physid_reg3 on page 752
16'h5010 : 16'h51F8	cmn_hns_sam_nonhash_cfg1_memregion2-63	RW	4.3.10.118 cmn_hns_sam_nonhash_cfg1_memregion2-63 on page 754
16'h5210 : 16'h53F8	cmn_hns_sam_nonhash_cfg2_memregion2-63	RW	4.3.10.119 cmn_hns_sam_nonhash_cfg2_memregion2-63 on page 755
16'h5400 : 16'h5478	cmn_hns_sam_htg_cfg1_memregion0-15	RW	4.3.10.120 cmn_hns_sam_htg_cfg1_memregion0-15 on page 756
16'h5480 : 16'h54F8	cmn_hns_sam_htg_cfg2_memregion0-15	RW	4.3.10.121 cmn_hns_sam_htg_cfg2_memregion0-15 on page 758
16'h5500 : 16'h5578	cmn_hns_sam_htg_cfg3_memregion0-15	RW	4.3.10.122 cmn_hns_sam_htg_cfg3_memregion0-15 on page 759
16'h5600 : 16'h5678	cmn_hns_sam_htg_sn_nodeid_reg0-15	RW	4.3.10.123 cmn_hns_sam_htg_sn_nodeid_reg0-15 on page 761
16'h5680 : 16'h56F8	cmn_hns_sam_htg_sn_attr0-15	RW	4.3.10.124 cmn_hns_sam_htg_sn_attr0-15 on page 762
16'h5700 : 16'h5718	cmn_hns_sam_ccg_sa_nodeid_reg0-3	RW	4.3.10.125 cmn_hns_sam_ccg_sa_nodeid_reg0-3 on page 766
16'h5740 : 16'h5758	cmn_hns_sam_ccg_sa_attr0-3	RW	4.3.10.126 cmn_hns_sam_ccg_sa_attr0-3 on page 767
16'h5780 : 16'h57B8	hns_generic_regs0-7	RW	4.3.10.127 hns_generic_regs0-7 on page 771
16'h5900	cmn_hns_pa2setaddr_slc	RW	4.3.10.128 cmn_hns_pa2setaddr_slc on page 772
16'h5908	cmn_hns_pa2setaddr_sf	RW	4.3.10.129 cmn_hns_pa2setaddr_sf on page 776
16'h5910	cmn_hns_pa2setaddr_flex_slc	RW	4.3.10.130 cmn_hns_pa2setaddr_flex_slc on page 780
16'h5918	cmn_hns_pa2setaddr_flex_sf	RW	4.3.10.131 cmn_hns_pa2setaddr_flex_sf on page 781
16'h7000 : 16'h70F8	lcn_hashed_tgt_grp_cfg1_region0-31	RW	4.3.10.132 lcn_hashed_tgt_grp_cfg1_region0-31 on page 782
16'h7100 : 16'h71F8	lcn_hashed_tgt_grp_cfg2_region0-31	RW	4.3.10.133 lcn_hashed_tgt_grp_cfg2_region0-31 on page 784
16'h7200 : 16'h72F8	lcn_hashed_target_grp_secondary_cfg1_reg0-31	RW	4.3.10.134 lcn_hashed_target_grp_secondary_cfg1_reg0-31 on page 785

Offset	Name	Type	Description
16'h7300 : 16'h73F8	lcn_hashed_target_grp_secondary_cfg2_rego-31	RW	4.3.10.135 lcn_hashed_target_grp_secondary_cfg2_rego-31 on page 787
16'h7400 : 16'h74F8	lcn_hashed_target_grp_hash_cntl_reg0-31	RW	4.3.10.136 lcn_hashed_target_grp_hash_cntl_reg0-31 on page 788
16'h7500 : 16'h7518	lcn_hashed_target_group_hn_count_reg0-3	RW	4.3.10.137 lcn_hashed_target_group_hn_count_reg0-3 on page 790
16'h7520 : 16'h7558	lcn_hashed_target_grp_cal_mode_reg0-7	RW	4.3.10.138 lcn_hashed_target_grp_cal_mode_reg0-7 on page 791
16'h7560 : 16'h7568	lcn_hashed_target_grp_hnf_cpa_en_reg0-1	RW	4.3.10.139 lcn_hashed_target_grp_hnf_cpa_en_reg0-1 on page 793
16'h7580 : 16'h75F8	lcn_hashed_target_grp_cpag_perhnf_reg0-15	RW	4.3.10.140 lcn_hashed_target_grp_cpag_perhnf_reg0-15 on page 794
16'h7700 : 16'h77F8	lcn_hashed_target_grp_compact_cpag_ctrl0-31	RW	4.3.10.141 lcn_hashed_target_grp_compact_cpag_ctrl0-31 on page 796
16'h7800 : 16'h78F8	lcn_hashed_target_grp_compact_hash_ctrl0-31	RW	4.3.10.142 lcn_hashed_target_grp_compact_hash_ctrl0-31 on page 797

4.2.10 HN-F MPAM_NS register summary

This section lists the HN-F MPAM_NS registers used in CMN-700.

HNF_MPAM_NS register summary

The following table shows the HNF_MPAM_NS registers in offset order from the base memory address

Table 4-11: HNF_MPAM_NS register summary

Offset	Name	Type	Description
16'h0	cmn_hns_mpam_ns_node_info	RO	4.3.11.1 cmn_hns_mpam_ns_node_info on page 799
16'h80	cmn_hns_mpam_ns_child_info	RO	4.3.11.2 cmn_hns_mpam_ns_child_info on page 800
16'h1000	cmn_hns_mpam_idr	RO	4.3.11.3 cmn_hns_mpam_idr on page 801
16'h1018	cmn_hns_mpam_iidr	RO	4.3.11.4 cmn_hns_mpam_iidr on page 802
16'h1020	cmn_hns_mpam_aidr	RO	4.3.11.5 cmn_hns_mpam_aidr on page 803
16'h1028	cmn_hns_mpam_impl_idr	RO	4.3.11.6 cmn_hns_mpam_impl_idr on page 804
16'h1030	cmn_hns_mpam_cpor_idr	RO	4.3.11.7 cmn_hns_mpam_cpor_idr on page 805
16'h1038	cmn_hns_mpam_ccap_idr	RO	4.3.11.8 cmn_hns_mpam_ccap_idr on page 806
16'h1040	cmn_hns_mpam_mbw_idr	RO	4.3.11.9 cmn_hns_mpam_mbw_idr on page 807
16'h1048	cmn_hns_mpam_pri_idr	RO	4.3.11.10 cmn_hns_mpam_pri_idr on page 808
16'h1050	cmn_hns_mpam_partid_nrw_idr	RO	4.3.11.11 cmn_hns_mpam_partid_nrw_idr on page 810
16'h1080	cmn_hns_mpam_msmon_idr	RO	4.3.11.12 cmn_hns_mpam_msmon_idr on page 811
16'h1088	cmn_hns_mpam_csumon_idr	RO	4.3.11.13 cmn_hns_mpam_csumon_idr on page 812
16'h1090	cmn_hns_mpam_mbwumon_idr	RO	4.3.11.14 cmn_hns_mpam_mbwumon_idr on page 813
16'h10F0	cmn_hns_ns_mpam_ecr	RW	4.3.11.15 cmn_hns_ns_mpam_ecr on page 814

Offset	Name	Type	Description
16'h10F8	cmn_hns_ns_mpam_esr	RW	4.3.11.16 cmn_hns_ns_mpam_esr on page 815
16'h1100	cmn_hns_ns_mpamcfg_part_sel	RW	4.3.11.17 cmn_hns_ns_mpamcfg_part_sel on page 816
16'h1108	cmn_hns_ns_mpamcfg_cmax	RW	4.3.11.18 cmn_hns_ns_mpamcfg_cmax on page 817
16'h1200	cmn_hns_ns_mpamcfg_mbw_min	RW	4.3.11.19 cmn_hns_ns_mpamcfg_mbw_min on page 818
16'h1208	cmn_hns_ns_mpamcfg_mbw_max	RW	4.3.11.20 cmn_hns_ns_mpamcfg_mbw_max on page 819
16'h1220	cmn_hns_ns_mpamcfg_mbw_winwd	RW	4.3.11.21 cmn_hns_ns_mpamcfg_mbw_winwd on page 820
16'h1400	cmn_hns_ns_mpamcfg_pri	RW	4.3.11.22 cmn_hns_ns_mpamcfg_pri on page 821
16'h1500	cmn_hns_ns_mpamcfg_mbw_prop	RW	4.3.11.23 cmn_hns_ns_mpamcfg_mbw_prop on page 823
16'h1600	cmn_hns_ns_mpamcfg_intpartid	RW	4.3.11.24 cmn_hns_ns_mpamcfg_intpartid on page 824
16'h1800	cmn_hns_ns_msmon_cfg_mon_sel	RW	4.3.11.25 cmn_hns_ns_msmon_cfg_mon_sel on page 825
16'h1808	cmn_hns_ns_msmon_capt_evnt	RW	4.3.11.26 cmn_hns_ns_msmon_capt_evnt on page 826
16'h1810	cmn_hns_ns_msmon_cfg_csuflt	RW	4.3.11.27 cmn_hns_ns_msmon_cfg_csuflt on page 827
16'h1818	cmn_hns_ns_msmon_cfg_csu_ctl	RW	4.3.11.28 cmn_hns_ns_msmon_cfg_csu_ctl on page 828
16'h1820	cmn_hns_ns_msmon_cfg_mbwuflt	RW	4.3.11.29 cmn_hns_ns_msmon_cfg_mbwuflt on page 830
16'h1828	cmn_hns_ns_msmon_cfg_mbwu_ctl	RW	4.3.11.30 cmn_hns_ns_msmon_cfg_mbwu_ctl on page 831
16'h1840	cmn_hns_ns_msmon_csu	RW	4.3.11.31 cmn_hns_ns_msmon_csu on page 833
16'h1848	cmn_hns_ns_msmon_csu_capture	RW	4.3.11.32 cmn_hns_ns_msmon_csu_capture on page 834
16'h1860	cmn_hns_ns_msmon_mbwu	RW	4.3.11.33 cmn_hns_ns_msmon_mbwu on page 835
16'h1868	cmn_hns_ns_msmon_mbwu_capture	RW	4.3.11.34 cmn_hns_ns_msmon_mbwu_capture on page 836
16'h2000	cmn_hns_ns_mpamcfg_cpmbm	RW	4.3.11.35 cmn_hns_ns_mpamcfg_cpmbm on page 837

4.2.11 HN-F MPAM_S register summary

This section lists the HN-F MPAM_S registers used in CMN-700.

HNF_MPAM_S register summary

The following table shows the HNF_MPAM_S registers in offset order from the base memory address

Table 4-12: HNF_MPAM_S register summary

Offset	Name	Type	Description
16'h0	cmn_hns_mpam_s_node_info	RO	4.3.12.1 cmn_hns_mpam_s_node_info on page 838
16'h80	cmn_hns_mpam_s_child_info	RO	4.3.12.2 cmn_hns_mpam_s_child_info on page 839
16'h980	cmn_hns_mpam_s_secure_register_groups_override	RW	4.3.12.3 cmn_hns_mpam_s_secure_register_groups_override on page 840
16'h1000	cmn_hns_s_mpam_idr	RO	4.3.12.4 cmn_hns_s_mpam_idr on page 841
16'h1008	cmn_hns_mpam_sidr	RO	4.3.12.5 cmn_hns_mpam_sidr on page 842
16'h1018	cmn_hns_s_mpam_iidr	RO	4.3.12.6 cmn_hns_s_mpam_iidr on page 843
16'h1020	cmn_hns_s_mpam_aidr	RO	4.3.12.7 cmn_hns_s_mpam_aidr on page 844
16'h1028	cmn_hns_s_mpam_impl_idr	RO	4.3.12.8 cmn_hns_s_mpam_impl_idr on page 845
16'h1030	cmn_hns_s_mpam_cpor_idr	RO	4.3.12.9 cmn_hns_s_mpam_cpor_idr on page 846

Offset	Name	Type	Description
16'h1038	cmn_hns_s_mpam_ccap_idr	RO	4.3.12.10 cmn_hns_s_mpam_ccap_idr on page 847
16'h1040	cmn_hns_s_mpam_mbw_idr	RO	4.3.12.11 cmn_hns_s_mpam_mbw_idr on page 848
16'h1048	cmn_hns_s_mpam_pri_idr	RO	4.3.12.12 cmn_hns_s_mpam_pri_idr on page 849
16'h1050	cmn_hns_s_mpam_partid_nrw_idr	RO	4.3.12.13 cmn_hns_s_mpam_partid_nrw_idr on page 851
16'h1080	cmn_hns_s_mpam_msmon_idr	RO	4.3.12.14 cmn_hns_s_mpam_msmon_idr on page 852
16'h1088	cmn_hns_s_mpam_csumon_idr	RO	4.3.12.15 cmn_hns_s_mpam_csumon_idr on page 853
16'h1090	cmn_hns_s_mpam_mbwumon_idr	RO	4.3.12.16 cmn_hns_s_mpam_mbwumon_idr on page 854
16'h10F0	cmn_hns_s_mpam_ecr	RW	4.3.12.17 cmn_hns_s_mpam_ecr on page 855
16'h10F8	cmn_hns_s_mpam_esr	RW	4.3.12.18 cmn_hns_s_mpam_esr on page 856
16'h1100	cmn_hns_s_mpamcfg_part_sel	RW	4.3.12.19 cmn_hns_s_mpamcfg_part_sel on page 857
16'h1108	cmn_hns_s_mpamcfg_cmax	RW	4.3.12.20 cmn_hns_s_mpamcfg_cmax on page 858
16'h1200	cmn_hns_s_mpamcfg_mbw_min	RW	4.3.12.21 cmn_hns_s_mpamcfg_mbw_min on page 859
16'h1208	cmn_hns_s_mpamcfg_mbw_max	RW	4.3.12.22 cmn_hns_s_mpamcfg_mbw_max on page 861
16'h1220	cmn_hns_s_mpamcfg_mbw_winwd	RW	4.3.12.23 cmn_hns_s_mpamcfg_mbw_winwd on page 862
16'h1400	cmn_hns_s_mpamcfg_pri	RW	4.3.12.24 cmn_hns_s_mpamcfg_pri on page 863
16'h1500	cmn_hns_s_mpamcfg_mbw_prop	RW	4.3.12.25 cmn_hns_s_mpamcfg_mbw_prop on page 864
16'h1600	cmn_hns_s_mpamcfg_intpartid	RW	4.3.12.26 cmn_hns_s_mpamcfg_intpartid on page 865
16'h1800	cmn_hns_s_msmon_cfg_mon_sel	RW	4.3.12.27 cmn_hns_s_msmon_cfg_mon_sel on page 866
16'h1808	cmn_hns_s_msmon_capt_evnt	RW	4.3.12.28 cmn_hns_s_msmon_capt_evnt on page 867
16'h1810	cmn_hns_s_msmon_cfg_csu_flt	RW	4.3.12.29 cmn_hns_s_msmon_cfg_csu_flt on page 868
16'h1818	cmn_hns_s_msmon_cfg_csu_ctl	RW	4.3.12.30 cmn_hns_s_msmon_cfg_csu_ctl on page 870
16'h1820	cmn_hns_s_msmon_cfg_mbwu_flt	RW	4.3.12.31 cmn_hns_s_msmon_cfg_mbwu_flt on page 872
16'h1828	cmn_hns_s_msmon_cfg_mbwu_ctl	RW	4.3.12.32 cmn_hns_s_msmon_cfg_mbwu_ctl on page 873
16'h1840	cmn_hns_s_msmon_csu	RW	4.3.12.33 cmn_hns_s_msmon_csu on page 875
16'h1848	cmn_hns_s_msmon_csu_capture	RW	4.3.12.34 cmn_hns_s_msmon_csu_capture on page 876
16'h1860	cmn_hns_s_msmon_mbwu	RW	4.3.12.35 cmn_hns_s_msmon_mbwu on page 877
16'h1868	cmn_hns_s_msmon_mbwu_capture	RW	4.3.12.36 cmn_hns_s_msmon_mbwu_capture on page 878
16'h2000	cmn_hns_s_mpamcfg_cpbm	RW	4.3.12.37 cmn_hns_s_mpamcfg_cpbm on page 879

4.2.12 HN-I register summary

This section lists the HN-I registers used in CMN-700.

HN-I register summary

The following table shows the HN-I registers in offset order from the base memory address

Table 4-13: HN-I register summary

Offset	Name	Type	Description
16'h0	por_hni_node_info	RO	4.3.9.1 por_hni_node_info on page 570
16'h80	por_hni_child_info	RO	4.3.9.2 por_hni_child_info on page 570

Offset	Name	Type	Description
16'h980	por_hni_secure_register_groups_override	RW	4.3.9.3 por_hni_secure_register_groups_override on page 571
16'h900	por_hni_unit_info	RO	4.3.9.4 por_hni_unit_info on page 572
16'h908	por_hni_unit_info_1	RO	4.3.9.5 por_hni_unit_info_1 on page 574
16'hC00	por_hni_sam_addrregion0_cfg	RW	4.3.9.6 por_hni_sam_addrregion0_cfg on page 575
16'hC08	por_hni_sam_addrregion1_cfg	RW	4.3.9.7 por_hni_sam_addrregion1_cfg on page 576
16'hC10	por_hni_sam_addrregion2_cfg	RW	4.3.9.8 por_hni_sam_addrregion2_cfg on page 578
16'hC18	por_hni_sam_addrregion3_cfg	RW	4.3.9.9 por_hni_sam_addrregion3_cfg on page 579
16'hA00	por_hni_cfg_ctl	RW	4.3.9.10 por_hni_cfg_ctl on page 581
16'hA08	por_hni_aux_ctl	RW	4.3.9.11 por_hni_aux_ctl on page 582
16'h3000	por_hni_errfr	RO	4.3.9.12 por_hni_errfr on page 583
16'h3008	por_hni_errctlr	RW	4.3.9.13 por_hni_errctlr on page 584
16'h3010	por_hni_errstatus	W1C	4.3.9.14 por_hni_errstatus on page 585
16'h3018	por_hni_erraddr	RW	4.3.9.15 por_hni_erraddr on page 587
16'h3020	por_hni_errmisc	RW	4.3.9.16 por_hni_errmisc on page 588
16'h3100	por_hni_errfr_NS	RO	4.3.9.17 por_hni_errfr_NS on page 590
16'h3108	por_hni_errctlr_NS	RW	4.3.9.18 por_hni_errctlr_NS on page 591
16'h3110	por_hni_errstatus_NS	W1C	4.3.9.19 por_hni_errstatus_NS on page 592
16'h3118	por_hni_erraddr_NS	RW	4.3.9.20 por_hni_erraddr_NS on page 594
16'h3120	por_hni_errmisc_NS	RW	4.3.9.21 por_hni_errmisc_NS on page 595
16'h2000	por_hni_pmu_event_sel	RW	4.3.9.22 por_hni_pmu_event_sel on page 596
16'h2008	por_hnp_pmu_event_sel	RW	4.3.9.23 por_hnp_pmu_event_sel on page 598

4.2.13 MXP register summary

This section lists the MXP registers used in CMN-700.

MXP register summary

The following table shows the MXP registers in offset order from the base memory address

Table 4-14: MXP register summary

Offset	Name	Type	Description
16'h0	por_mxp_node_info	RO	4.3.13.1 por_mxp_node_info on page 880
16'h8 : 16'h30	por_mxp_device_port_connect_info_p0-5	RO	4.3.13.2 por_mxp_device_port_connect_info_p0-5 on page 881
16'h38	por_mxp_mesh_port_connect_info_east	RO	4.3.13.3 por_mxp_mesh_port_connect_info_east on page 883
16'h40	por_mxp_mesh_port_connect_info_north	RO	4.3.13.4 por_mxp_mesh_port_connect_info_north on page 884

Offset	Name	Type	Description
16'h48 : 16'h70	por_mxp_device_port_connect_lid_info_p0-5	RO	4.3.13.5 por_mxp_device_port_connect_lid_info_p0-5 on page 885
16'h80	por_mxp_child_info	RO	4.3.13.6 por_mxp_child_info on page 886
16'h100 : 16'h1F8	por_mxp_child_pointer_0-31	RO	4.3.13.7 por_mxp_child_pointer_0-31 on page 887
16'h900 + #{16*index}	por_mxp_p0-5_info	RO	4.3.13.8 por_mxp_p0-5_info on page 888
16'h908 + #{16*index}	por_mxp_p0-5_info_1	RO	4.3.13.9 por_mxp_p0-5_info_1 on page 889
16'h960	por_dtm_unit_info	RO	4.3.13.10 por_dtm_unit_info on page 891
16'h968 : 16'h978	por_dtm_unit_info_dt1-3	RO	4.3.13.11 por_dtm_unit_info_dt1-3 on page 891
16'h980	por_mxp_secure_register_groups_override	RW	4.3.13.12 por_mxp_secure_register_groups_override on page 892
16'hA00	por_mxp_aux_ctl	RW	4.3.13.13 por_mxp_aux_ctl on page 894
16'hA08	por_mxp_device_port_ctl	RW	4.3.13.14 por_mxp_device_port_ctl on page 894
16'hA10 : 16'hA38	por_mxp_p0-5_mpam_override	RW	4.3.13.15 por_mxp_p0-5_mpam_override on page 896
16'hA40 : 16'hA68	por_mxp_p0-5_lid_override	RW	4.3.13.16 por_mxp_p0-5_lid_override on page 897
16'hA80 + #{32*index}	por_mxp_p0-5_qos_control	RW	4.3.13.17 por_mxp_p0-5_qos_control on page 899
16'hA88 + #{32*index}	por_mxp_p0-5_qos_lat_tgt	RW	4.3.13.18 por_mxp_p0-5_qos_lat_tgt on page 900
16'hA90 + #{32*index}	por_mxp_p0-5_qos_lat_scale	RW	4.3.13.19 por_mxp_p0-5_qos_lat_scale on page 901
16'hA98 + #{32*index}	por_mxp_p0-5_qos_lat_range	RW	4.3.13.20 por_mxp_p0-5_qos_lat_range on page 902
16'h2000	por_mxp_pmu_event_sel	RW	4.3.13.21 por_mxp_pmu_event_sel on page 903
16'h3000	por_mxp_errfr	RO	4.3.13.22 por_mxp_errfr on page 905
16'h3008	por_mxp_errctlr	RW	4.3.13.23 por_mxp_errctlr on page 906
16'h3010	por_mxp_errstatus	W1C	4.3.13.24 por_mxp_errstatus on page 907
16'h3028	por_mxp_errmisc	RW	4.3.13.25 por_mxp_errmisc on page 909
16'h3030 : 16'h3058	por_mxp_p0-5_byte_par_err_inj	WO	4.3.13.26 por_mxp_p0-5_byte_par_err_inj on page 911
16'h3100	por_mxp_errfr_NS	RO	4.3.13.27 por_mxp_errfr_NS on page 912
16'h3108	por_mxp_errctlr_NS	RW	4.3.13.28 por_mxp_errctlr_NS on page 913
16'h3110	por_mxp_errstatus_NS	W1C	4.3.13.29 por_mxp_errstatus_NS on page 914
16'h3128	por_mxp_errmisc_NS	RW	4.3.13.30 por_mxp_errmisc_NS on page 916
16'h1C00 + #{16*index}	por_mxp_p0-5_syscoreq_ctl	RW	4.3.13.31 por_mxp_p0-5_syscoreq_ctl on page 918
16'h1C08 + #{16*index}	por_mxp_p0-5_syscoack_status	RO	4.3.13.32 por_mxp_p0-5_syscoack_status on page 919

Offset	Name	Type	Description
16'h2100	por_dtm_control	RW	4.3.13.33 por_dtm_control on page 920
16'h2118	por_dtm_fifo_entry_ready	W1C	4.3.13.34 por_dtm_fifo_entry_ready on page 921
16'h2120 + #{24*index}	por_dtm_fifo_entry0-3_0	RO	4.3.13.35 por_dtm_fifo_entry0-3_0 on page 922
16'h2128 + #{24*index}	por_dtm_fifo_entry0-3_1	RO	4.3.13.36 por_dtm_fifo_entry0-3_1 on page 923
16'h2130 + #{24*index}	por_dtm_fifo_entry0-3_2	RO	4.3.13.37 por_dtm_fifo_entry0-3_2 on page 924
16'h21A0 + #{24*index}	por_dtm_wp0-3_config	RW	4.3.13.38 por_dtm_wp0-3_config on page 925
16'h21A8 + #{24*index}	por_dtm_wp0-3_val	RW	4.3.13.39 por_dtm_wp0-3_val on page 926
16'h21B0 + #{24*index}	por_dtm_wp0-3_mask	RW	4.3.13.40 por_dtm_wp0-3_mask on page 927
16'h2200	por_dtm_pmsicr	RW	4.3.13.41 por_dtm_pmsicr on page 928
16'h2208	por_dtm_pmsirr	RW	4.3.13.42 por_dtm_pmsirr on page 929
16'h2210	por_dtm_pmu_config	RW	4.3.13.43 por_dtm_pmu_config on page 930
16'h2220	por_dtm_pmevcnt	RW	4.3.13.44 por_dtm_pmevcnt on page 934
16'h2240	por_dtm_pmevcntsr	RW	4.3.13.45 por_dtm_pmevcntsr on page 935
16'h2100 + #{512*index}	por_dtm_control_dt1-3	RW	4.3.13.46 por_dtm_control_dt1-3 on page 935
16'h2118 + #{512*index}	por_dtm_fifo_entry_ready_dt1-3	W1C	4.3.13.47 por_dtm_fifo_entry_ready_dt1-3 on page 937
16'h2120 + #{24*(index%4)} + #{512*((index/4)+1)}	por_dtm_fifo_entry0-11%4_0_dt(0-11/4)+1	RO	4.3.13.48 por_dtm_fifo_entry0-11%4_0_dt(0-11/4)+1 on page 938
16'h2128 + #{24*(index%4)} + #{512*((index/4)+1)}	por_dtm_fifo_entry0-11%4_1_dt(0-11/4)+1	RO	4.3.13.49 por_dtm_fifo_entry0-11%4_1_dt(0-11/4)+1 on page 938
16'h2130 + #{24*(index%4)} + #{512*((index/4)+1)}	por_dtm_fifo_entry0-11%4_2_dt(0-11/4)+1	RO	4.3.13.50 por_dtm_fifo_entry0-11%4_2_dt(0-11/4)+1 on page 939
16'h21A0 + #{24*(index%4)} + #{512*((index/4)+1)}	por_dtm_wp0-11%4_config_dt(0-11/4)+1	RW	4.3.13.51 por_dtm_wp0-11%4_config_dt(0-11/4)+1 on page 940
16'h21A8 + #{24*(index%4)} + #{512*((index/4)+1)}	por_dtm_wp0-11%4_val_dt(0-11/4)+1	RW	4.3.13.52 por_dtm_wp0-11%4_val_dt(0-11/4)+1 on page 941
16'h21B0 + #{24*(index%4)} + #{512*((index/4)+1)}	por_dtm_wp0-11%4_mask_dt(0-11/4)+1	RW	4.3.13.53 por_dtm_wp0-11%4_mask_dt(0-11/4)+1 on page 942
16'h2200 + #{512*index}	por_dtm_pmsicr_dt1-3	RW	4.3.13.54 por_dtm_pmsicr_dt1-3 on page 943
16'h2208 + #{512*index}	por_dtm_pmsirr_dt1-3	RW	4.3.13.55 por_dtm_pmsirr_dt1-3 on page 944
16'h2210 + #{512*index}	por_dtm_pmu_config_dt1-3	RW	4.3.13.56 por_dtm_pmu_config_dt1-3 on page 945

Offset	Name	Type	Description
16'h2220 + #{512*index}	por_dtm_pmevcnt_dt1-3	RW	4.3.13.57 por_dtm_pmevcnt_dt1-3 on page 948
16'h2240 + #{512*index}	por_dtm_pmevcntsr_dt1-3	RW	4.3.13.58 por_dtm_pmevcntsr_dt1-3 on page 949
16'hC00 : 16'hC78	por_mxp_multi_mesh_chn_sel_0-15	RW	4.3.13.59 por_mxp_multi_mesh_chn_sel_0-15 on page 950
16'hC80	por_mxp_multi_mesh_chn_ctrl	RW	4.3.13.60 por_mxp_multi_mesh_chn_ctrl on page 953
16'hC90 : 16'hCC8	por_mxp_xy_override_sel_0-7	RW	4.3.13.61 por_mxp_xy_override_sel_0-7 on page 954
16'hCD0 + #{32*index}	por_mxp_p0-5_pa2setaddr_slc	RW	4.3.13.62 por_mxp_p0-5_pa2setaddr_slc on page 956
16'hCD8 + #{32*index}	por_mxp_p0-5_pa2setaddr_sf	RW	4.3.13.63 por_mxp_p0-5_pa2setaddr_sf on page 960
16'hCE0 + #{32*index}	por_mxp_p0-5_pa2setaddr_flex_slc	RW	4.3.13.64 por_mxp_p0-5_pa2setaddr_flex_slc on page 964
16'hCE8 + #{32*index}	por_mxp_p0-5_pa2setaddr_flex_sf	RW	4.3.13.65 por_mxp_p0-5_pa2setaddr_flex_sf on page 965

4.2.14 RN-D register summary

This section lists the RN-D registers used in CMN-700.

RN-D register summary

The following table shows the RND registers in offset order from the base memory address

Table 4-15: RN-D register summary

Offset	Name	Type	Description
16'h0	por_rnd_node_info	RO	4.3.14.1 por_rnd_node_info on page 966
16'h80	por_rnd_child_info	RO	4.3.14.2 por_rnd_child_info on page 967
16'h980	por_rnd_secure_register_groups_override	RW	4.3.14.3 por_rnd_secure_register_groups_override on page 968
16'h900	por_rnd_unit_info	RO	4.3.14.4 por_rnd_unit_info on page 969
16'h908	por_rnd_unit_info2	RO	4.3.14.5 por_rnd_unit_info2 on page 970
16'hA00	por_rnd_cfg_ctl	RW	4.3.14.6 por_rnd_cfg_ctl on page 971
16'hA08	por_rnd_aux_ctl	RW	4.3.14.7 por_rnd_aux_ctl on page 974
16'hA10 : 16'hA20	por_rnd_s0-2_port_control	RW	4.3.14.8 por_rnd_s0-2_port_control on page 977
16'hA28 : 16'hA38	por_rnd_s0-2_mpam_control	RW	4.3.14.9 por_rnd_s0-2_mpam_control on page 979
16'hA80 + #{index*32}	por_rnd_s0-2_qos_control	RW	4.3.14.10 por_rnd_s0-2_qos_control on page 980
16'hA88 + #{index*32}	por_rnd_s0-2_qos_lat_tgt	RW	4.3.14.11 por_rnd_s0-2_qos_lat_tgt on page 982
16'hA90 + #{index*32}	por_rnd_s0-2_qos_lat_scale	RW	4.3.14.12 por_rnd_s0-2_qos_lat_scale on page 983

Offset	Name	Type	Description
16'hA98 + #{{index}*32}	por_rnd_s0-2_qos_lat_range	RW	4.3.14.13 por_rnd_s0-2_qos_lat_range on page 984
16'h2000	por_rnd_pmu_event_sel	RW	4.3.14.14 por_rnd_pmu_event_sel on page 985
16'h1C00	por_rnd_syscoreq_ctl	RW	4.3.14.15 por_rnd_syscoreq_ctl on page 987
16'h1C08	por_rnd_syscoack_status	RO	4.3.14.16 por_rnd_syscoack_status on page 988

4.2.15 RN-I register summary

This section lists the RN-I registers used in CMN-700.

RN-I register summary

The following table shows the RN-I registers in offset order from the base memory address

Table 4-16: RN-I register summary

Offset	Name	Type	Description
16'h0	por_rni_node_info	RO	4.3.15.1 por_rni_node_info on page 989
16'h80	por_rni_child_info	RO	4.3.15.2 por_rni_child_info on page 990
16'h980	por_rni_secure_register_groups_override	RW	4.3.15.3 por_rni_secure_register_groups_override on page 991
16'h900	por_rni_unit_info	RO	4.3.15.4 por_rni_unit_info on page 992
16'h908	por_rni_unit_info2	RO	4.3.15.5 por_rni_unit_info2 on page 993
16'hA00	por_rni_cfg_ctl	RW	4.3.15.6 por_rni_cfg_ctl on page 994
16'hA08	por_rni_aux_ctl	RW	4.3.15.7 por_rni_aux_ctl on page 997
16'hA10 : 16'hA20	por_rni_s0-2_port_control	RW	4.3.15.8 por_rni_s0-2_port_control on page 1000
16'hA28 : 16'hA38	por_rni_s0-2_mpam_control	RW	4.3.15.9 por_rni_s0-2_mpam_control on page 1002
16'hA80 + #{{index}*32}	por_rni_s0-2_qos_control	RW	4.3.15.10 por_rni_s0-2_qos_control on page 1003
16'hA88 + #{{index}*32}	por_rni_s0-2_qos_lat_tgt	RW	4.3.15.11 por_rni_s0-2_qos_lat_tgt on page 1005
16'hA90 + #{{index}*32}	por_rni_s0-2_qos_lat_scale	RW	4.3.15.12 por_rni_s0-2_qos_lat_scale on page 1006
16'hA98 + #{{index}*32}	por_rni_s0-2_qos_lat_range	RW	4.3.15.13 por_rni_s0-2_qos_lat_range on page 1007
16'h2000	por_rni_pmu_event_sel	RW	4.3.15.14 por_rni_pmu_event_sel on page 1008

4.2.16 RN SAM register summary

This section lists the RN SAM registers used in CMN-700.

RNSAM register summary

The following table shows the RNSAM registers in offset order from the base memory address

Table 4-17: RNSAM register summary

Offset	Name	Type	Description
16'h0	por_rnsam_node_info	RO	4.3.16.1 por_rnsam_node_info on page 1010
16'h80	por_rnsam_child_info	RO	4.3.16.2 por_rnsam_child_info on page 1011

Offset	Name	Type	Description
16'h980	por_rnsam_secure_register_groups_override	RW	4.3.16.3 por_rnsam_secure_register_groups_override on page 1012
16'h900	por_rnsam_unit_info	RO	4.3.16.4 por_rnsam_unit_info on page 1013
16'h908	por_rnsam_unit_info1	RO	4.3.16.5 por_rnsam_unit_info1 on page 1014
{0-23} 16'hC00 : 16'hCB8	non_hash_mem_region_reg0-63	RW	4.3.16.6 non_hash_mem_region_reg0-63 on page 1016
{24-63} 16'h20C0 : 16'h24B8			
{0-23} 16'hCC0 : 16'hD78	non_hash_mem_region_cfg2_reg0-63	RW	4.3.16.7 non_hash_mem_region_cfg2_reg0-63 on page 1018
{24-63} 16'h24C0 : 16'h28D8			
16'hD80 : 16'hDF8	non_hash_tgt_nodeid0-15	RW	4.3.16.8 non_hash_tgt_nodeid0-15 on page 1019
16'h11A0	cml_port_aggr_mode_ctrl_reg	RW	4.3.16.9 cml_port_aggr_mode_ctrl_reg on page 1020
{1-3} 16'h11A8 : 16'h11B8	cml_port_aggr_mode_ctrl_reg1-6	RW	4.3.16.10 cml_port_aggr_mode_ctrl_reg1-6 on page 1021
{4-6} 16'h2A20 : 16'h2A30			
16'hE00 : 16'hE18	sys_cache_grp_region0-3	RW	4.3.16.11 sys_cache_grp_region0-3 on page 1024
{4-7} 16'hE20 : 16'hE38	hashed_tgt_grp_cfg1_region4-31	RW	4.3.16.12 hashed_tgt_grp_cfg1_region4-31 on page 1025
{8-31} 16'h3040 : 16'h30F8			
16'h3100 : 16'h31F8	hashed_tgt_grp_cfg2_region0-31	RW	4.3.16.13 hashed_tgt_grp_cfg2_region0-31 on page 1027
16'hE40 : 16'hE58	sys_cache_grp_secondary_reg0-3	RW	4.3.16.14 sys_cache_grp_secondary_reg0-3 on page 1028
{4-7} 16'hE60 : 16'hE78	hashed_target_grp_secondary_cfg1_reg4-31	RW	4.3.16.15 hashed_target_grp_secondary_cfg1_reg4-31 on page 1030
{8-31} 16'h3240 : 16'h32F8			
16'h3300 : 16'h33F8	hashed_target_grp_secondary_cfg2_reg0-31	RW	4.3.16.16 hashed_target_grp_secondary_cfg2_reg0-31 on page 1032
16'h3400 : 16'h34F8	hashed_target_grp_hash_ctrl_reg0-31	RW	4.3.16.17 hashed_target_grp_hash_ctrl_reg0-31 on page 1033
16'hEA0	sys_cache_group_hn_count	RW	4.3.16.18 sys_cache_group_hn_count on page 1035

Offset	Name	Type	Description
{1} 16'hEA8	hashed_target_group_hn_count_reg1-3	RW	4.3.16.19 hashed_target_group_hn_count_reg1-3 on page 1036
{2-3} 16'h3710 : 16'h3718			
16'hEC0	sys_cache_grp_nonhash_nodeid	RW	4.3.16.20 sys_cache_grp_nonhash_nodeid on page 1037
{0-5} 16'hEC8 : 16'hEE8	hashed_target_grp_nonhash_nodeid_reg1-6	RW	4.3.16.21 hashed_target_grp_nonhash_nodeid_reg1-6 on page 1038
{6} 16'h3800			
16'hF00 : 16'hF78	sys_cache_grp_hn_nodeid_reg0-15	RW	4.3.16.22 sys_cache_grp_hn_nodeid_reg0-15 on page 1039
16'hF80 : 16'hFF8	hashed_target_grp_hnf_nodeid_reg16-31	RW	4.3.16.23 hashed_target_grp_hnf_nodeid_reg16-31 on page 1041
16'h3600 : 16'h3678	hashed_target_grp_hnp_nodeid_reg0-15	RW	4.3.16.24 hashed_target_grp_hnp_nodeid_reg0-15 on page 1042
16'h1120	sys_cache_grp_cal_mode_reg	RW	4.3.16.25 sys_cache_grp_cal_mode_reg on page 1043
{1-3} 16'h1128 : 16'h1138	hashed_target_grp_cal_mode_reg1-7	RW	4.3.16.26 hashed_target_grp_cal_mode_reg1-7 on page 1045
{4-7} 16'h37A0 : 16'h37B8			
16'h1180	sys_cache_grp_hn_cpa_en_reg	RW	4.3.16.27 sys_cache_grp_hn_cpa_en_reg on page 1047
16'h1188	hashed_target_grp_hnf_cpa_en_reg1-1	RW	4.3.16.28 hashed_target_grp_hnf_cpa_en_reg1-1 on page 1048
16'h3900 : 16'h3978	hashed_target_grp_cpag_perhnf_reg0-15	RW	4.3.16.29 hashed_target_grp_cpag_perhnf_reg0-15 on page 1049
16'h1190	sys_cache_grp_hn_cpa_grp_reg	RW	4.3.16.30 sys_cache_grp_hn_cpa_grp_reg on page 1050
{1} 16'h1198	hashed_target_grp_cpa_grp_reg1-7	RW	4.3.16.31 hashed_target_grp_cpa_grp_reg1-7 on page 1052
{2-7} 16'h3750 : 16'h3778			
16'h37C0 : 16'h37C8	hashed_target_grp_hnf_lcn_bound_cfg_reg0-1	RW	4.3.16.32 hashed_target_grp_hnf_lcn_bound_cfg_reg0-1 on page 1054
16'h37E0 : 16'h37E8	hashed_target_grp_hnf_target_type_override_cfg_reg0-1	RW	4.3.16.33 hashed_target_grp_hnf_target_type_override_cfg_reg0-1 on page 1054
16'h3A00 : 16'h3AF8	hashed_target_grp_compact_cpag_ctrl0-31	RW	4.3.16.34 hashed_target_grp_compact_cpag_ctrl0-31 on page 1055
16'h3B00 : 16'h3BF8	hashed_target_grp_compact_hash_ctrl0-31	RW	4.3.16.35 hashed_target_grp_compact_hash_ctrl0-31 on page 1057
16'hE80	rnsam_hash_addr_mask_reg	RW	4.3.16.36 rnsam_hash_addr_mask_reg on page 1061
16'hE88	rnsam_hash_axi_id_mask_reg	RW	4.3.16.37 rnsam_hash_axi_id_mask_reg on page 1062
16'hE90	rnsam_region_cmp_addr_mask_reg	RW	4.3.16.38 rnsam_region_cmp_addr_mask_reg on page 1063

Offset	Name	Type	Description
{0-5} 16'h11C0 : 16'h11E8	cml_port_aggr_grp0-31_add_mask	RW	4.3.16.39 cml_port_aggr_grp0-31_add_mask on page 1063
{6-31} 16'h2B30 : 16'h2BF8			
16'h2B00 : 16'h2B18	cml_cpag_base_idx_grp0-3	RW	4.3.16.40 cml_cpag_base_idx_grp0-3 on page 1064
{0-2} 16'h11F0 : 16'h1200	cml_port_aggr_grp_reg0-12	RW	4.3.16.41 cml_port_aggr_grp_reg0-12 on page 1066
{3-12} 16'h2C18 : 16'h2C60			
16'h1208	cml_port_aggr_ctrl_reg	RW	4.3.16.42 cml_port_aggr_ctrl_reg on page 1067
16'h1210 : 16'h1238	cml_port_aggr_ctrl_reg1-6	RW	4.3.16.43 cml_port_aggr_ctrl_reg1-6 on page 1070
16'hEB0	sys_cache_grp_sn_attr	RW	4.3.16.44 sys_cache_grp_sn_attr on page 1073
16'hEB8	sys_cache_grp_sn_attr1	RW	4.3.16.45 sys_cache_grp_sn_attr1 on page 1076
16'h1140 : 16'h1158	sys_cache_grp_sn_sam_cfg0-3	RW	4.3.16.46 sys_cache_grp_sn_sam_cfg0-3 on page 1079
16'h1280 : 16'h12F8	sam_qos_mem_region_reg0-15	RW	4.3.16.47 sam_qos_mem_region_reg0-15 on page 1080
16'h1340 : 16'h13B8	sam_qos_mem_region_cfg2_reg0-15	RW	4.3.16.48 sam_qos_mem_region_cfg2_reg0-15 on page 1082
16'h4000 : 16'h4FF8	sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg1_reg0-511%64	RW	4.3.16.49 sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg1_reg0-511%64 on page 1083
16'h5000 : 16'h5FF8	sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg2_reg0-511%64	RW	4.3.16.50 sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg2_reg0-511%64 on page 1084
16'h6000 : 16'h61F8	sam_scg0-63/8_prefetch_hashed_region_cfg1_reg0-63%8	RW	4.3.16.51 sam_scg0-63/8_prefetch_hashed_region_cfg1_reg0-63%8 on page 1086
16'h6200 : 16'h63F8	sam_scg0-63/8_prefetch_hashed_region_cfg2_reg0-63%8	RW	4.3.16.52 sam_scg0-63/8_prefetch_hashed_region_cfg2_reg0-63%8 on page 1087
16'h6400 : 16'h65F8	sam_scg0-63/8_prefetch_hashed_region_cfg3_reg0-63%8	RW	4.3.16.53 sam_scg0-63/8_prefetch_hashed_region_cfg3_reg0-63%8 on page 1088
16'h1000 : 16'h10F8	sys_cache_grp_sn_nodeid_reg0-31	RW	4.3.16.54 sys_cache_grp_sn_nodeid_reg0-31 on page 1090
16'h1400 : 16'h15F8	sys_cache_grp_region0-63/32_sn_nodeid_reg0-63%32	RW	4.3.16.55 sys_cache_grp_region0-63/32_sn_nodeid_reg0-63%32 on page 1091
16'h6600 : 16'h6678	sys_cache_grp_hashed_regions_sn_nodeid_reg0-15	RW	4.3.16.56 sys_cache_grp_hashed_regions_sn_nodeid_reg0-15 on page 1093
16'h1100	rnsam_status	RW	4.3.16.57 rnsam_status on page 1094
16'h1108	gic_mem_region_reg	RW	4.3.16.58 gic_mem_region_reg on page 1095

Offset	Name	Type	Description
16'h1600 : 16'h1638	sam_generic_regs0-7	RW	4.3.16.59 sam_generic_regs0-7 on page 1097

4.2.17 SBSX register summary

This section lists the SBSX registers used in CMN-700.

SBSX register summary

The following table shows the SBSX registers in offset order from the base memory address

Table 4-18: SBSX register summary

Offset	Name	Type	Description
16'h0	por_sbsx_node_info	RO	4.3.17.1 por_sbsx_node_info on page 1098
16'h80	por_sbsx_child_info	RO	4.3.17.2 por_sbsx_child_info on page 1099
16'h980	por_sbsx_secure_register_groups_override	RW	4.3.17.3 por_sbsx_secure_register_groups_override on page 1100
16'h900	por_sbsx_unit_info	RO	4.3.17.4 por_sbsx_unit_info on page 1101
16'hA00	por_sbsx_cfg_ctl	RW	4.3.17.5 por_sbsx_cfg_ctl on page 1102
16'hA08	por_sbsx_aux_ctl	RW	4.3.17.6 por_sbsx_aux_ctl on page 1104
16'hA18	por_sbsx_cbusy_limit_ctl	RW	4.3.17.7 por_sbsx_cbusy_limit_ctl on page 1105
16'h3000	por_sbsx_errfr	RO	4.3.17.8 por_sbsx_errfr on page 1106
16'h3008	por_sbsx_errctlr	RW	4.3.17.9 por_sbsx_errctlr on page 1107
16'h3010	por_sbsx_errstatus	W1C	4.3.17.10 por_sbsx_errstatus on page 1108
16'h3018	por_sbsx_erraddr	RW	4.3.17.11 por_sbsx_erraddr on page 1110
16'h3020	por_sbsx_errmisc	RW	4.3.17.12 por_sbsx_errmisc on page 1111
16'h3100	por_sbsx_errfr_NS	RO	4.3.17.13 por_sbsx_errfr_NS on page 1112
16'h3108	por_sbsx_errctlr_NS	RW	4.3.17.14 por_sbsx_errctlr_NS on page 1113
16'h3110	por_sbsx_errstatus_NS	W1C	4.3.17.15 por_sbsx_errstatus_NS on page 1114
16'h3118	por_sbsx_erraddr_NS	RW	4.3.17.16 por_sbsx_erraddr_NS on page 1116
16'h3120	por_sbsx_errmisc_NS	RW	4.3.17.17 por_sbsx_errmisc_NS on page 1117
16'h2000	por_sbsx_pmu_event_sel	RW	4.3.17.18 por_sbsx_pmu_event_sel on page 1118

4.3 Register descriptions

This section contains register descriptions.

4.3.1 APB register descriptions

This section lists the APB registers.

4.3.1.1 por_apb_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-3: por_apb_node_info

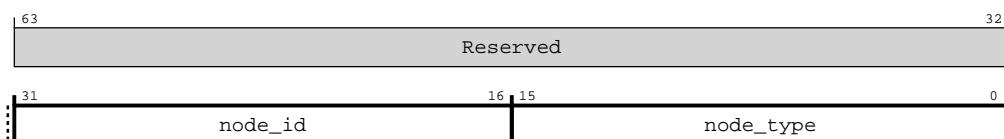


Table 4-19: por_apb_node_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h1000

4.3.1.2 por_apb_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-4: por_apb_child_info

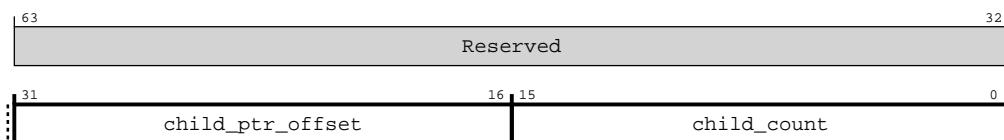


Table 4-20: por_apb_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0000
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.1.3 por_apb_only_access

Functions as the CMN access control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-5: por_apb_only_access

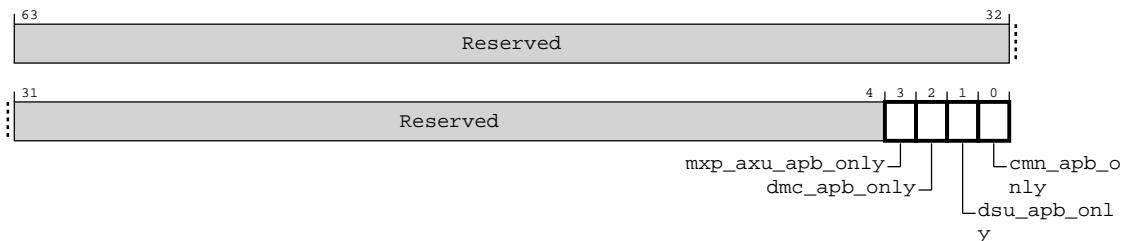


Table 4-21: por_apb_only_access attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	mpx_axu_apb_only	MXP AXI utility bus access by APB only 1'b0 MXP AXU accessible via CHI/AXI in addition to APB 1'b1 MXP AXU accessible only via APB	RW	1'b0
[2]	dmc_apb_only	DMC AXI utility bus access by APB only 1'b0 DMC AXU accessible via CHI/AXI in addition to APB 1'b1 DMC AXU accessible only via APB	RW	1'b0
[1]	dsu_apb_only	DSU AXI utility bus access by APB only 1'b0 DSU AXU accessible via CHI/AXI in addition to APB 1'b1 DSU AXU accessible only via APB	RW	1'b0
[0]	cmn_apb_only	CMN config access by APB only 1'b0 CMN config accessible via CHI/AXI in addition to APB 1'b1 CMN config accessible only via APB	RW	1'b0

4.3.1.4 por_axu_control

Functions as the CMN AXU interface control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h988

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-6: por_axu_control

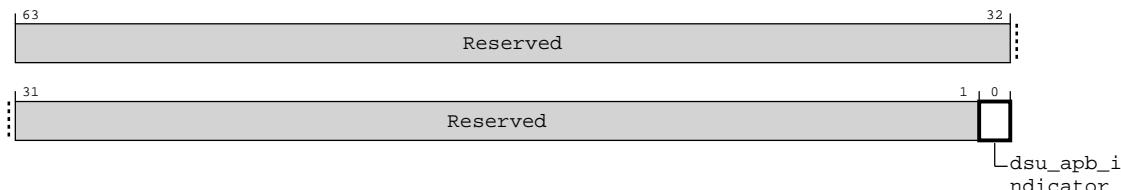


Table 4-22: por_axu_control attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	dsu_apb_indicator	DSU AxADDRU[23] access indicator enable 1'b1 AxADDRU[23] will carry source indicator (0: from CHI / 1: from APB) 1'b0 AxADDRU[23] behaves as default	RW	1'b0

4.3.2 CCG_HA register descriptions

This section lists the CCG_HA registers.

4.3.2.1 por_ccg_ha_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-7: por_ccg_ha_node_info

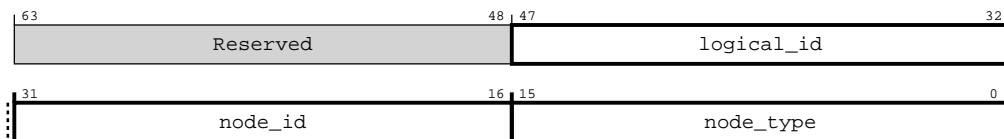


Table 4-23: por_ccg_ha_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0104

4.3.2.2 por_ccg_ha_id

Contains the CCIX-assigned HAID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h8

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-8: por_ccg_ha_id

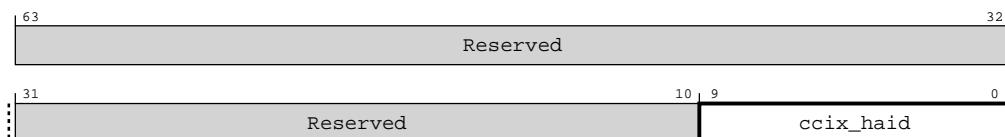


Table 4-24: por_ccg_ha_id attributes

Bits	Name	Description	Type	Reset
[63:10]	Reserved	Reserved	RO	-
[9:0]	ccix_haid	CCIX HAID	RW	10'h0

4.3.2.3 por_ccg_ha_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-9: por_ccg_ha_child_info

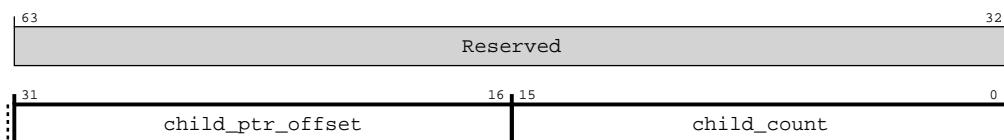


Table 4-25: por_ccg_ha_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'h0

4.3.2.4 por_ccg_ha_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ha_secure_register_groups_override.cfg_ctl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-10: por_ccg_ha_cfg_ctl

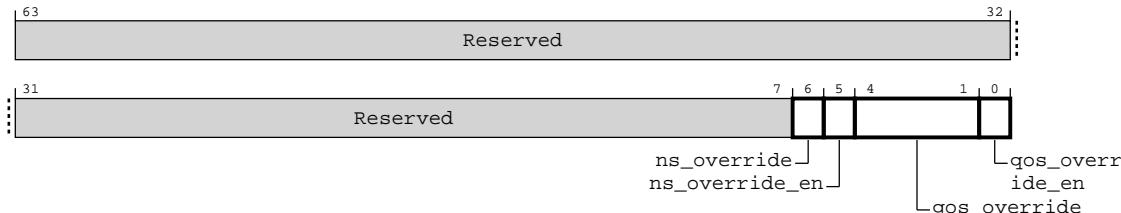


Table 4-26: por_ccg_ha_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6]	ns_override	NS override value	RW	1'b0
[5]	ns_override_en	NS override en When set, NS(Non-secure) value on CHI side is driven from NS override value in this register	RW	1'b0
[4:1]	qos_override	QoS override value	RW	4'b0
[0]	qos_override_en	QoS override en When set, QoS value on CHI side is driven from QoS override value in this register	RW	1'b0

4.3.2.5 por_ccg_ha_aux_ctl

Functions as the auxiliary control register for CXHA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-11: por_ccg_ha_aux_ctl

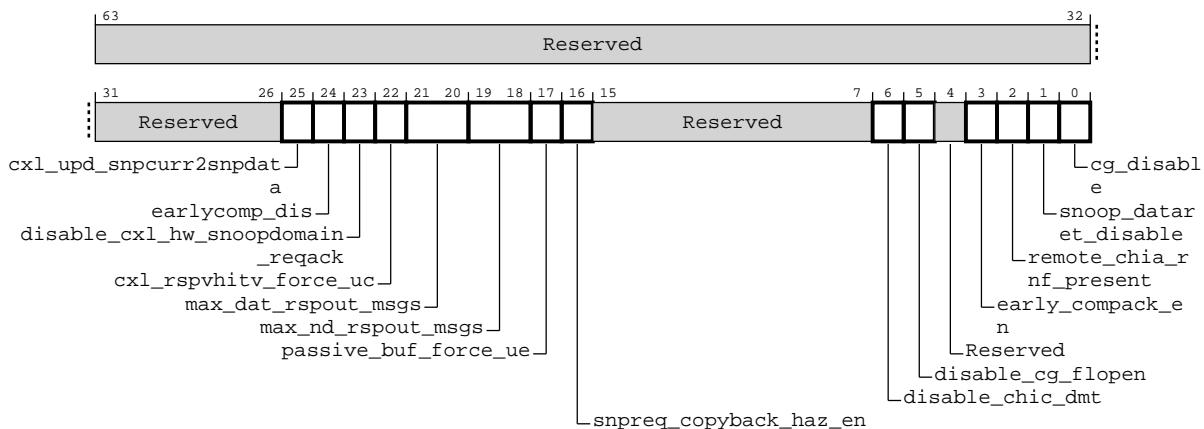


Table 4-27: por_ccg_ha_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25]	cxl_upd_snpcurr2snpdata	When set, updates SnpCurr to SnpData on CXL.Cache	RW	1'b0
[24]	earlycomp_dis	When set, disables sending early completions for requests	RW	1'b0
[23]	disable_cxl_hw_snoopdomain_reqack	When set, disables CXL Hardware based Snoop domain handshake	RW	1'b0
[22]	cxl_rspvhitv_force_uc	When set, forces UC response state for Snoop response on CHI when D2H RspVHitV response is received on CXL	RW	1'b0

Bits	Name	Description	Type	Reset
[21:20]	max_dat_rspout_msgs	<p>Used to configure the maximum number of response data messages (Read Data) presented to CCLA's packing logic.</p> <p>2'b00 one message 2'b01 two messages 2'b10 three messages 2'b11 four messages</p> <p>Note: The max is further limited by max allowed by the given protocol (CCIX2.0/CXL.mem/CXL.cache)</p>	RW	2'b11
[19:18]	max_nd_rspout_msgs	<p>Used to configure the maximum number of non-data response messages (Completions/GO/WritePulls) presented to CCLA's packing logic.</p> <p>2'b00 one message 2'b01 two messages 2'b10 three messages 2'b11 four messages</p> <p>Note: The max is further limited by max allowed by the given protocol (CCIX2.0/CXL.mem/CXL.cache)</p>	RW	2'b11
[17]	passive_buf_force_ue	When set, forces all DE's originating in Passive Buffer to be reported as UEs	RW	1'b0
[16]	snpreq_copyback_haz_en	When set enables Snoop-CopyBack hazarding at incoming Snoop Request pipe	RW	1'b0
[15:7]	Reserved	Reserved	RO	-
[6]	disable_chic_dmt	When set disables CHI-C style DMT	RW	1'b0
[5]	disable_cg_flopen	Disables enhanced flop enable control for dynamic power savings	RW	1'b0
[4]	Reserved	Reserved	RO	-
[3]	early_compack_en	Early CompAck enable; enables sending early CompAck on CCIX for requests that require CompAck	RW	1'b1
[2]	remote_chia_rnf_present	<p>Indicates existence of CHIA RN-F in system; HA uses this indication to send SnpToS or SnpToSC</p> <p>1'b0 HA converts SnpShared, SnpClean, and SnpNotSharedDirty to SnpToSC 1'b1 HA converts SnpShared, SnpClean, and SnpNotSharedDirty to SnpToS</p>	RW	1'b0
[1]	snoop_dataret_disable	Disables setting data return for CCIX snoop requests for all CHI snoop opcodes	RW	1'b0
[0]	cg_disable	Disables clock gating when set	RW	1'b0

4.3.2.6 por_ccg_ha_mpam_control_link0

Controls MPAM override values on incoming CCIX Request in non-SMP mode for Link0

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA10

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.mpam_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-12: por_ccg_ha_mpam_control_link0

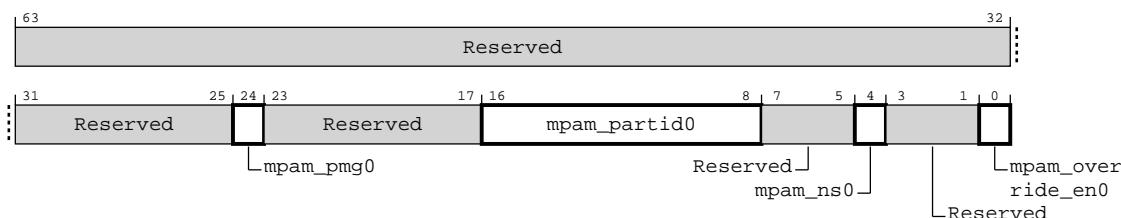


Table 4-28: por_ccg_ha_mpam_control_link0 attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	mpam_pmg0	MPAM_PMG value	RW	1'b0
[23:17]	Reserved	Reserved	RO	-
[16:8]	mpam_partid0	MPAM_PARTID value	RW	9'b0
[7:5]	Reserved	Reserved	RO	-
[4]	mpam_ns0	MPAM_NS value	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	mpam_override_en0	MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Applicable only in non-SMP mode	RW	1'b0

4.3.2.7 por_ccg_ha_mpam_control_link1

Controls MPAM override values on incoming CCIX Request in non-SMP mode for Link1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA18

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.mpam_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-13: por_ccg_ha_mpam_control_link1

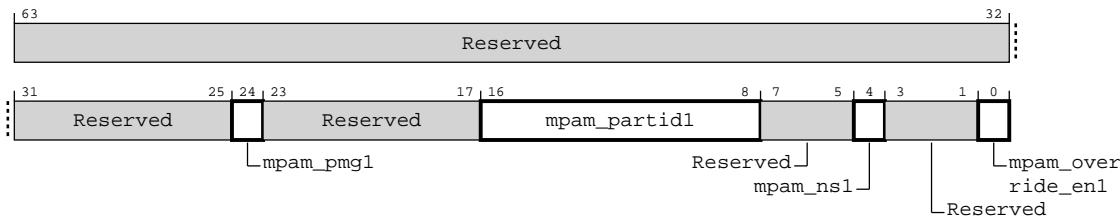


Table 4-29: por_ccg_ha_mpam_control_link1 attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	mpam_pmg1	MPAM_PMG value	RW	1'b0
[23:17]	Reserved	Reserved	RO	-
[16:8]	mpam_partid1	MPAM_PARTID value	RW	9'b0
[7:5]	Reserved	Reserved	RO	-
[4]	mpam_ns1	MPAM_NS value	RW	1'b0

Bits	Name	Description	Type	Reset
[3:1]	Reserved	Reserved	RO	-
[0]	mpam_override_en1	MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Applicable only in non-SMP mode	RW	1'b0

4.3.2.8 por_ccg_ha_mpam_control_link2

Controls MPAM override values on incoming CCIX Request in non-SMP mode for Link2

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA20

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.mpam_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-14: por_ccg_ha_mpam_control_link2

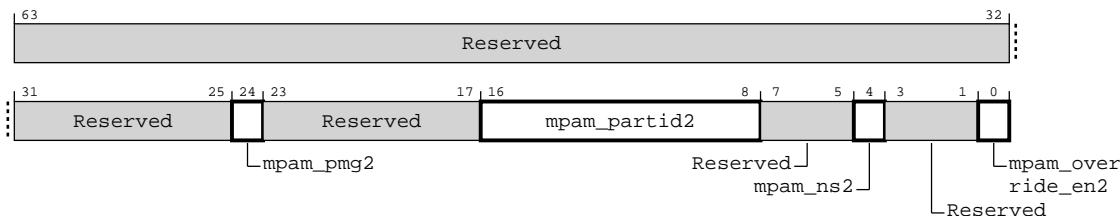


Table 4-30: por_ccg_ha_mpam_control_link2 attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	mpam_pmg2	MPAM_PMG value	RW	1'b0
[23:17]	Reserved	Reserved	RO	-
[16:8]	mpam_partid2	MPAM_PARTID value	RW	9'b0
[7:5]	Reserved	Reserved	RO	-
[4]	mpam_ns2	MPAM_NS value	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	mpam_override_en2	MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Applicable only in non-SMP mode	RW	1'b0

4.3.2.9 por_ccg_ha_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-15: por_ccg_ha_secure_register_groups_override

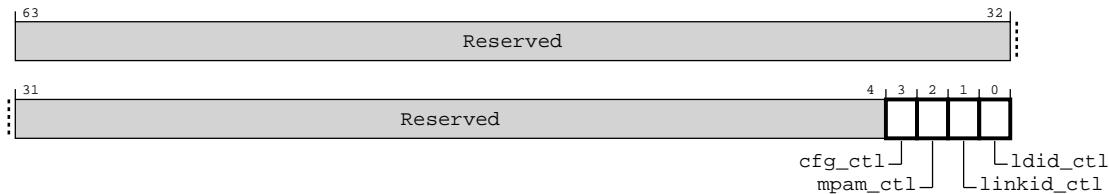


Table 4-31: por_ccg_ha_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	cfg_ctl	Allows Non-secure access to Secure HA config control registers	RW	1'b0
[2]	mpam_ctl	Allows Non-secure access to Secure HA MPAM override registers	RW	1'b0
[1]	linkid_ctl	Allows Non-secure access to Secure HA Link ID registers	RW	1'b0
[0]	ldid_ctl	Allows Non-secure access to Secure HA LDID registers	RW	1'b0

4.3.2.10 por_ccg_ha_unit_info

Provides component identification information for CXHA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-16: por_ccg_ha_unit_info

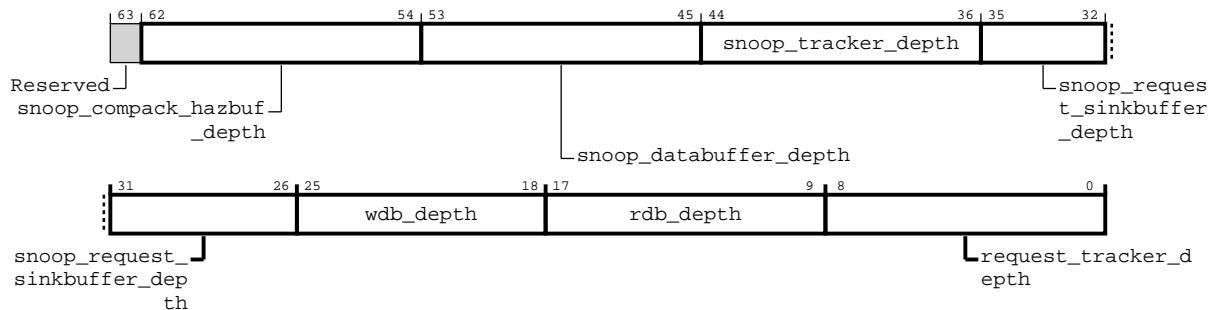


Table 4-32: por_ccg_ha_unit_info attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:54]	snoop_compack_hazbuf_depth	Depth of CompAck snoop hazard buffer	RO	Configuration dependent
[53:45]	snoop_databuffer_depth	Depth of snoop data buffer	RO	Configuration dependent
[44:36]	snoop_tracker_depth	Depth of snoop tracker; number of outstanding SNP requests on CCIX	RO	Configuration dependent
[35:26]	snoop_request_sinkbuffer_depth	Depth of snoop request sink buffer; number of CHI SNP requests that can be sunk by CXHA	RO	Configuration dependent
[25:18]	wdb_depth	Depth of write data buffer	RO	Configuration dependent
[17:9]	rdb_depth	Depth of read data buffer	RO	Configuration dependent
[8:0]	request_tracker_depth	Depth of request tracker	RO	Configuration dependent

4.3.2.11 por_ccg_ha_unit_info2

Provides additional component identification information for CXHA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-17: por_ccg_ha_unit_info2

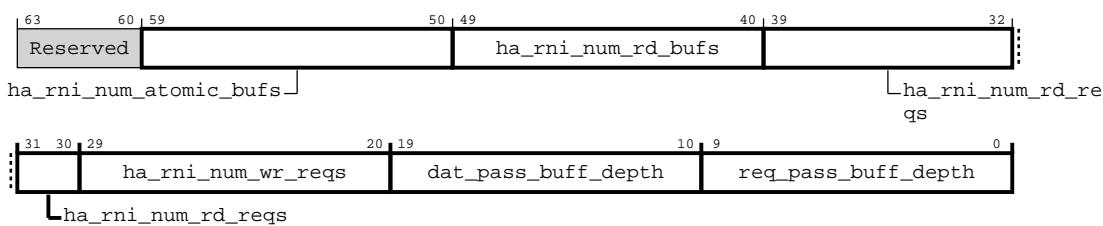


Table 4-33: por_ccg_ha_unit_info2 attributes

Bits	Name	Description	Type	Reset
[63:60]	Reserved	Reserved	RO	-
[59:50]	ha_rni_num_atomic_bufs	Number of HA_RNI atomic data buffers	RO	Configuration dependent
[49:40]	ha_rni_num_rd_bufs	Number of HA_RNI read data buffers	RO	Configuration dependent
[39:30]	ha_rni_num_rd_reqs	Number of HA_RNI outstanding read requests	RO	Configuration dependent
[29:20]	ha_rni_num_wr_reqs	Number of HA_RNI outstanding write requests	RO	Configuration dependent
[19:10]	dat_pass_buff_depth	Depth of DAT Passive Buffer	RO	Configuration dependent
[9:0]	req_pass_buff_depth	Depth of REQ Passive Buffer	RO	Configuration dependent

4.3.2.12 por_ccg_ha_unit_info3

Provides additional component identification information for CXHA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h910

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-18: por_ccg_ha_unit_info3

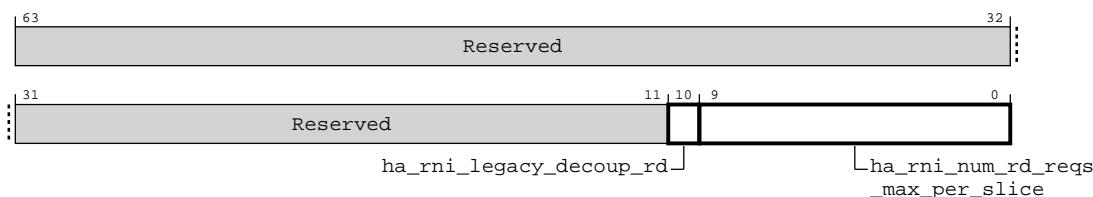


Table 4-34: por_ccg_ha_unit_info3 attributes

Bits	Name	Description	Type	Reset
[63:11]	Reserved	Reserved	RO	-
[10]	ha_rni_legacy_decoup_rd	Legacy decoupled read mode, no read burst propagation	RO	Configuration dependent
[9:0]	ha_rni_num_rd_reqs_max_per_slice	Number of HA_RNI read request entries per slice	RO	Configuration dependent

4.3.2.13 por_ccg_ha_agentid_to_linkid_reg0

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F00

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-19: por_ccg_ha_agentid_to_linkid_reg0

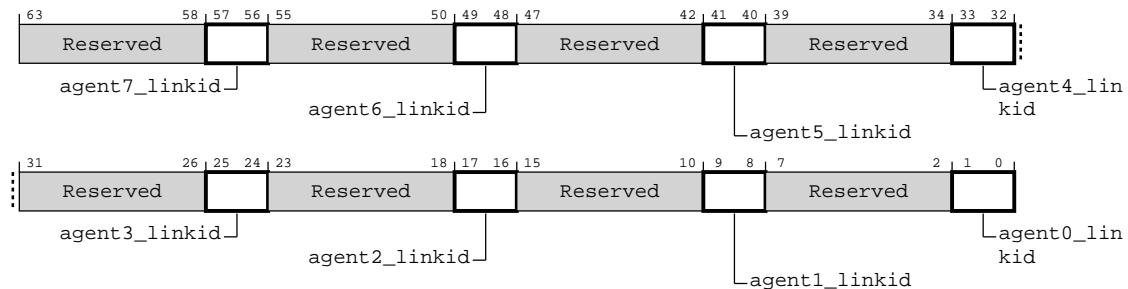


Table 4-35: por_ccg_ha_agentid_to_linkid_reg0 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent7_linkid	Specifies Link ID 7	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent6_linkid	Specifies Link ID 6	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent5_linkid	Specifies Link ID 5	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent4_linkid	Specifies Link ID 4	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent3_linkid	Specifies Link ID 3	RW	2'h0
[23:18]	Reserved	Reserved	RO	-
[17:16]	agent2_linkid	Specifies Link ID 2	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent1_linkid	Specifies Link ID 1	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent0_linkid	Specifies Link ID 0	RW	2'h0

4.3.2.14 por_ccg_ha_agentid_to_linkid_reg1

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F08

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-20: por_ccg_ha_agentid_to_linkid_reg1

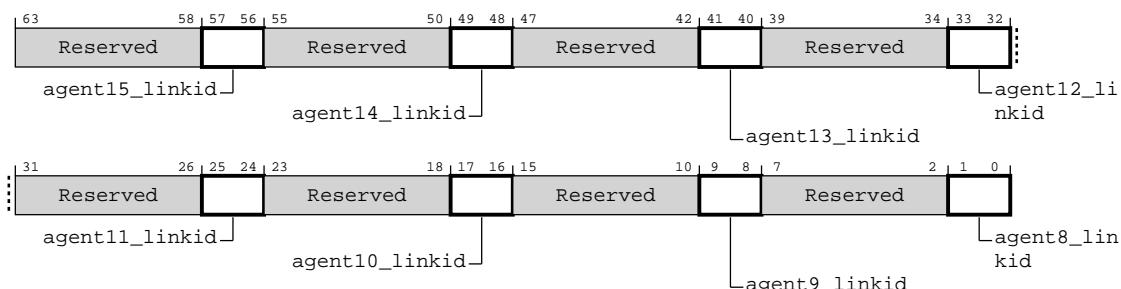


Table 4-36: por_ccg_ha_agentid_to_linkid_reg1 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent15_linkid	Specifies Link ID 15	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent14_linkid	Specifies Link ID 14	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent13_linkid	Specifies Link ID 13	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent12_linkid	Specifies Link ID 12	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent11_linkid	Specifies Link ID 11	RW	2'h0
[23:18]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[17:16]	agent10_linkid	Specifies Link ID 10	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent9_linkid	Specifies Link ID 9	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent8_linkid	Specifies Link ID 8	RW	2'h0

4.3.2.15 por_ccg_ha_agentid_to_linkid_reg2

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F10

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-21: por_ccg_ha_agentid_to_linkid_reg2

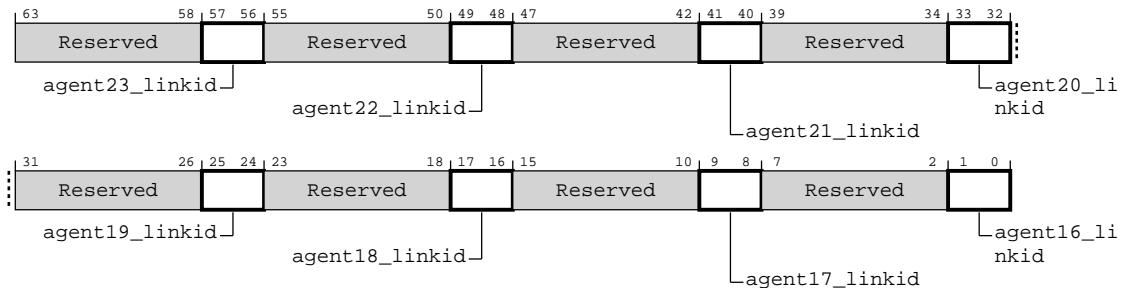


Table 4-37: por_ccg_ha_agentid_to_linkid_reg2 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent23_linkid	Specifies Link ID 23	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent22_linkid	Specifies Link ID 22	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent21_linkid	Specifies Link ID 21	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent20_linkid	Specifies Link ID 20	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent19_linkid	Specifies Link ID 19	RW	2'h0
[23:18]	Reserved	Reserved	RO	-
[17:16]	agent18_linkid	Specifies Link ID 18	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent17_linkid	Specifies Link ID 17	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent16_linkid	Specifies Link ID 16	RW	2'h0

4.3.2.16 por_ccg_ha_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F18

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-22: por_ccg_ha_agentid_to_linkid_reg3

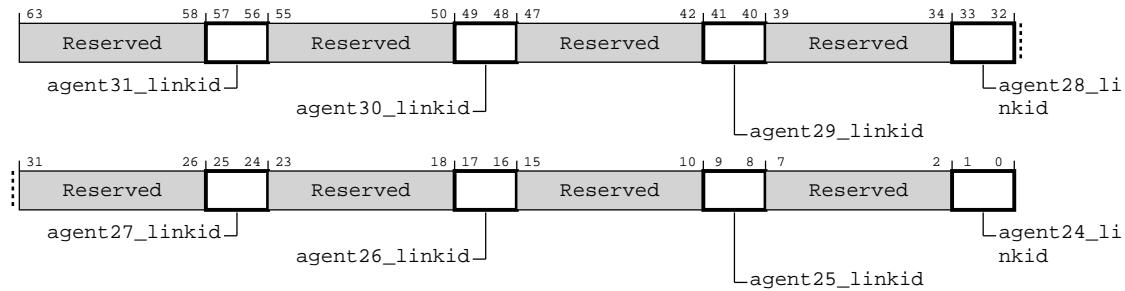


Table 4-38: por_ccg_ha_agentid_to_linkid_reg3 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent31_linkid	Specifies Link ID 31	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent30_linkid	Specifies Link ID 30	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent29_linkid	Specifies Link ID 29	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent28_linkid	Specifies Link ID 28	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent27_linkid	Specifies Link ID 27	RW	2'h0
[23:18]	Reserved	Reserved	RO	-
[17:16]	agent26_linkid	Specifies Link ID 26	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent25_linkid	Specifies Link ID 25	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent24_linkid	Specifies Link ID 24	RW	2'h0

4.3.2.17 por_ccg_ha_agentid_to_linkid_reg4

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F20

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-23: por_ccg_ha_agentid_to_linkid_reg4

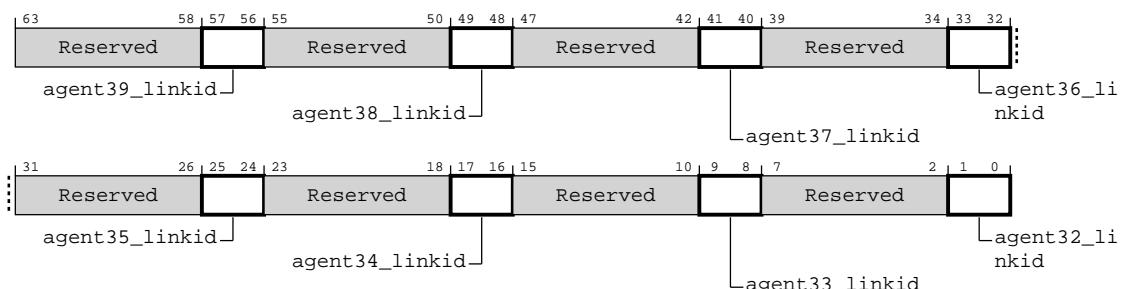


Table 4-39: por_ccg_ha_agentid_to_linkid_reg4 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent39_linkid	Specifies Link ID 39	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent38_linkid	Specifies Link ID 38	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent37_linkid	Specifies Link ID 37	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent36_linkid	Specifies Link ID 36	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent35_linkid	Specifies Link ID 35	RW	2'h0
[23:18]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[17:16]	agent34_linkid	Specifies Link ID 34	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent33_linkid	Specifies Link ID 33	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent32_linkid	Specifies Link ID 32	RW	2'h0

4.3.2.18 por_ccg_ha_agentid_to_linkid_reg5

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F28

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-24: por_ccg_ha_agentid_to_linkid_reg5

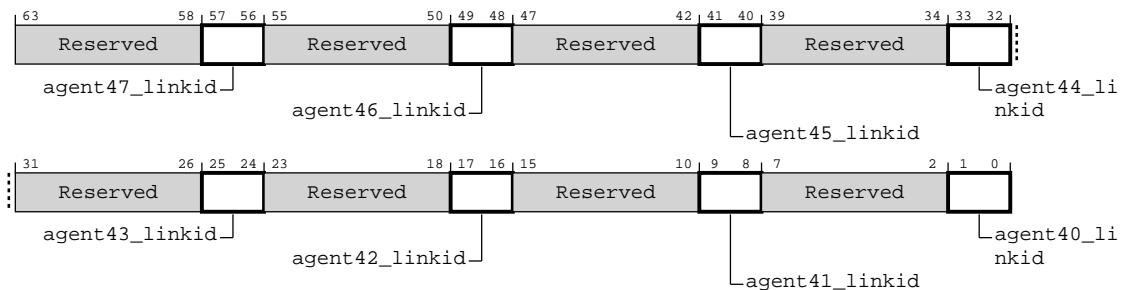


Table 4-40: por_ccg_ha_agentid_to_linkid_reg5 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent47_linkid	Specifies Link ID 47	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent46_linkid	Specifies Link ID 46	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent45_linkid	Specifies Link ID 45	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent44_linkid	Specifies Link ID 44	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent43_linkid	Specifies Link ID 43	RW	2'h0
[23:18]	Reserved	Reserved	RO	-
[17:16]	agent42_linkid	Specifies Link ID 42	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent41_linkid	Specifies Link ID 41	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent40_linkid	Specifies Link ID 40	RW	2'h0

4.3.2.19 por_ccg_ha_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F30

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-25: por_ccg_ha_agentid_to_linkid_reg6

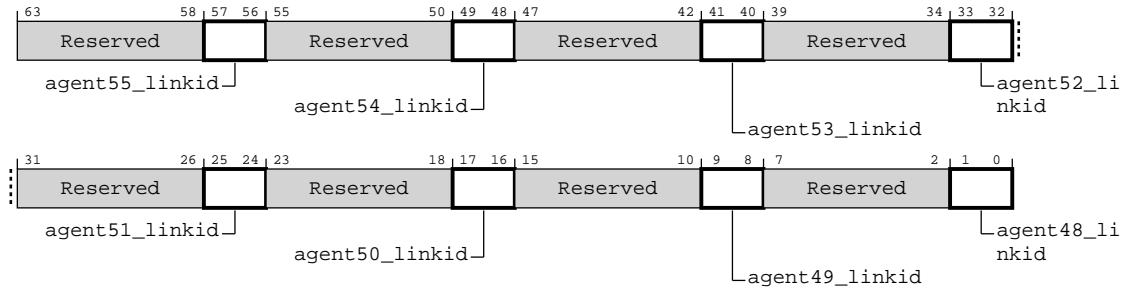


Table 4-41: por_ccg_ha_agentid_to_linkid_reg6 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent55_linkid	Specifies Link ID 55	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent54_linkid	Specifies Link ID 54	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent53_linkid	Specifies Link ID 53	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent52_linkid	Specifies Link ID 52	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent51_linkid	Specifies Link ID 51	RW	2'h0
[23:18]	Reserved	Reserved	RO	-
[17:16]	agent50_linkid	Specifies Link ID 50	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent49_linkid	Specifies Link ID 49	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent48_linkid	Specifies Link ID 48	RW	2'h0

4.3.2.20 por_ccg_ha_agentid_to_linkid_reg7

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1F38

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-26: por_ccg_ha_agentid_to_linkid_reg7

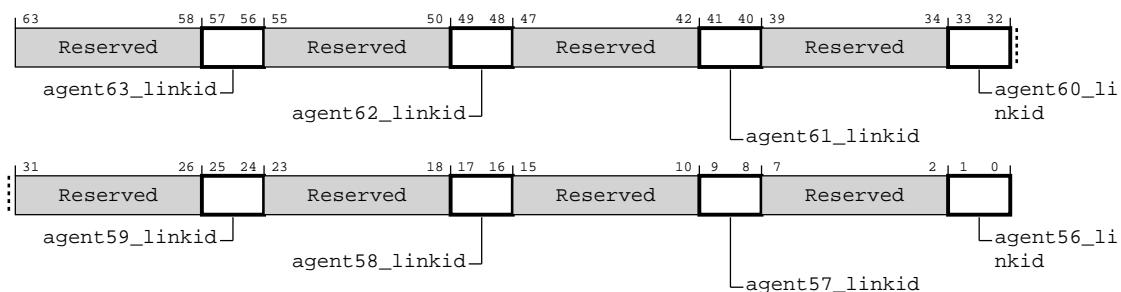


Table 4-42: por_ccg_ha_agentid_to_linkid_reg7 attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent63_linkid	Specifies Link ID 63	RW	2'h0
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent62_linkid	Specifies Link ID 62	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent61_linkid	Specifies Link ID 61	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent60_linkid	Specifies Link ID 60	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent59_linkid	Specifies Link ID 59	RW	2'h0
[23:18]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[17:16]	agent58_linkid	Specifies Link ID 58	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent57_linkid	Specifies Link ID 57	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent56_linkid	Specifies Link ID 56	RW	2'h0

4.3.2.21 por_ccg_ha_agentid_to_linkid_val

Specifies which Agent ID to Link ID mappings are valid.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1FF8

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ha_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-27: por_ccg_ha_agentid_to_linkid_val

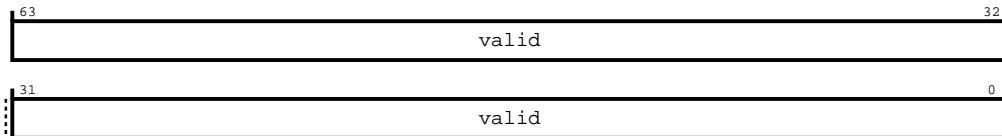


Table 4-43: por_ccg_ha_agentid_to_linkid_val attributes

Bits	Name	Description	Type	Reset
[63:0]	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

4.3.2.22 por_ccg_ha_rnf_exp_raid_to_ldid_reg_0-255

There are 256 iterations of this register. The index ranges from 0 to 255. Specifies the mapping of Expanded RAID to RN-F LDID for Expanded RAIDs $\#\{index*4\}$ to $\#\{index*4+3\}$.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16'hC00 + \#\{8*index\}$

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ha_secure_register_groups_override.ldid_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-28: por_ccg_ha_rnf_exp_raid_to_ldid_reg_0-255

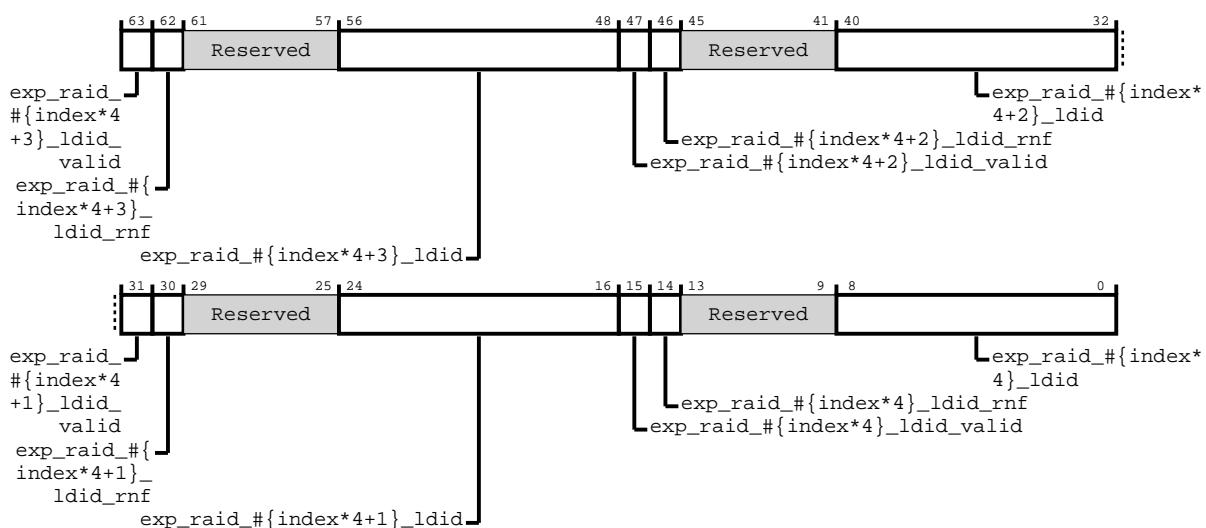


Table 4-44: por_ccg_ha_rnf_exp_raid_to_ldid_reg_0-255 attributes

Bits	Name	Description	Type	Reset
[63]	exp_raid_#{index*4+3}_ldid_valid	Specifies if LDID for Expanded RAID #{index*4+3} is valid	RW	1'b0
[62]	exp_raid_#{index*4+3}_ldid_rnf	Specifies if Expanded RAID #{index*4+3} is RN-F	RW	1'b0
[61:57]	Reserved	Reserved	RO	-
[56:48]	exp_raid_#{index*4+3}_ldid	Specifies the LDID for Expanded RAID #{index*4+3}	RW	9'h0
[47]	exp_raid_#{index*4+2}_ldid_valid	Specifies if LDID for Expanded RAID #{index*4+2} is valid	RW	1'b0
[46]	exp_raid_#{index*4+2}_ldid_rnf	Specifies if Expanded RAID #{index*4+2} is RN-F	RW	1'b0
[45:41]	Reserved	Reserved	RO	-
[40:32]	exp_raid_#{index*4+2}_ldid	Specifies the LDID for Expanded RAID #{index*4+2}	RW	9'h0
[31]	exp_raid_#{index*4+1}_ldid_valid	Specifies if LDID for Expanded RAID #{index*4+1} is valid	RW	1'b0
[30]	exp_raid_#{index*4+1}_ldid_rnf	Specifies if Expanded RAID #{index*4+1} is RN-F	RW	1'b0
[29:25]	Reserved	Reserved	RO	-
[24:16]	exp_raid_#{index*4+1}_ldid	Specifies the LDID for Expanded RAID #{index*4+1}	RW	9'h0
[15]	exp_raid_#{index*4}_ldid_valid	Specifies if LDID for Expanded RAID #{index*4} is valid	RW	1'b0
[14]	exp_raid_#{index*4}_ldid_rnf	Specifies if Expanded RAID #{index*4} is RN-F	RW	1'b0
[13:9]	Reserved	Reserved	RO	-
[8:0]	exp_raid_#{index*4}_ldid	Specifies the LDID for Expanded RAID #{index*4}	RW	9'h0

4.3.2.23 por_ccg_ha_pmu_event_sel

Specifies the PMU event to be counted as a 8-bit ID with the following encodings:

8'h00	CXHA_PMU_EVENT_NULL
8'h61	CXHA_PMU_EVENT_RDDATBYP
8'h62	CXHA_PMU_EVENT_CHIRSP_UP_STALL
8'h63	CXHA_PMU_EVENT_CHIDAT_UP_STALL
8'h64	CXHA_PMU_EVENT_SNPPCRD_LNK0_STALL
8'h65	CXHA_PMU_EVENT_SNPPCRD_LNK1_STALL
8'h66	CXHA_PMU_EVENT_SNPPCRD_LNK2_STALL
8'h67	CXHA_PMU_EVENT_REQTRK_OCC
8'h68	CXHA_PMU_EVENT_RDB_OCC
8'h69	CXHA_PMU_EVENT_RDBBYP_OCC
8'h6A	CXHA_PMU_EVENT_WDB_OCC
8'h6B	CXHA_PMU_EVENT_SNPTRK_OCC
8'h6C	CXHA_PMU_EVENT_SDB_OCC
8'h6D	CXHA_PMU_EVENT_SNPHAZ_OCC
8'h6E	CXHA_PMU_EVENT_REQTRK_ALLOC
8'h6F	CXHA_PMU_EVENT_RDB_ALLOC
8'h70	CXHA_PMU_EVENT_RDBBYP_ALLOC
8'h71	CXHA_PMU_EVENT_WDB_ALLOC
8'h72	CXHA_PMU_EVENT_SNPTRK_ALLOC
8'h73	CXHA_PMU_EVENT_SDB_ALLOC
8'h74	CXHA_PMU_EVENT_SNPHAZ_ALLOC

8'h75	CCHA_PMU_EVENT_PB_RHU_REQ_OCC
8'h76	CCHA_PMU_EVENT_PB_RHU_REQ_ALLOC
8'h77	CCHA_PMU_EVENT_PB_RHU_PCIE_REQ_OCC
8'h78	CCHA_PMU_EVENT_PB_RHU_PCIE_REQ_ALLOC
8'h79	CCHA_PMU_EVENT_PB_PCIE_WR_REQ_OCC
8'h7A	CCHA_PMU_EVENT_PB_PCIE_WR_REQ_ALLOC
8'h7B	CCHA_PMU_EVENT_PB_PCIE_REG_REQ_OCC
8'h7C	CCHA_PMU_EVENT_PB_PCIE_REG_REQ_ALLOC
8'h7D	CCHA_PMU_EVENT_PB_PCIE_RSVD_REQ_OCC
8'h7E	CCHA_PMU_EVENT_PB_PCIE_RSVD_REQ_ALLOC
8'h7F	CCHA_PMU_EVENT_PB_RHU_DAT_OCC
8'h80	CCHA_PMU_EVENT_PB_RHU_DAT_ALLOC
8'h81	CCHA_PMU_EVENT_PB_RHU_PCIE_DAT_OCC
8'h82	CCHA_PMU_EVENT_PB_RHU_PCIE_DAT_ALLOC
8'h83	CCHA_PMU_EVENT_PB_PCIE_WR_DAT_OCC
8'h84	CCHA_PMU_EVENT_PB_PCIE_WR_DAT_ALLOC

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-29: por_ccg_ha_pmu_event_sel

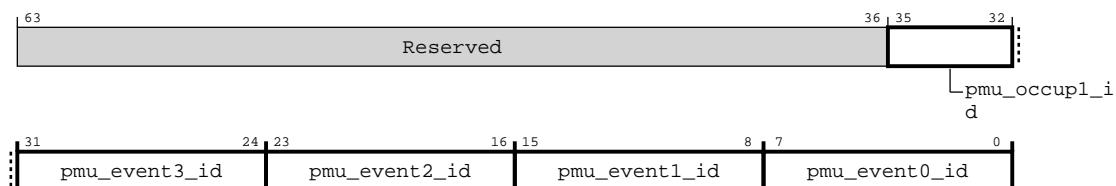


Table 4-45: por_ccg_ha_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:36]	Reserved	Reserved	RO	-
[35:32]	pmu_occup1_id	CXHA PMU occupancy event selector ID	RW	4'b0
[31:24]	pmu_event3_id	CXHA PMU Event 3 ID	RW	8'b0
[23:16]	pmu_event2_id	CXHA PMU Event 2 ID	RW	8'b0
[15:8]	pmu_event1_id	CXHA PMU Event 1 ID	RW	8'b0
[7:0]	pmu_event0_id	CXHA PMU Event 0 ID	RW	8'b0

4.3.2.24 por_ccg_ha_cxprtcl_link0_ctl

Functions as the CXHA CCIX Protocol Link 0 control register. Works with por_ccg_ha_cxprtcl_link0_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C00

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-30: por_ccg_ha_cxprtcl_link0_ctl

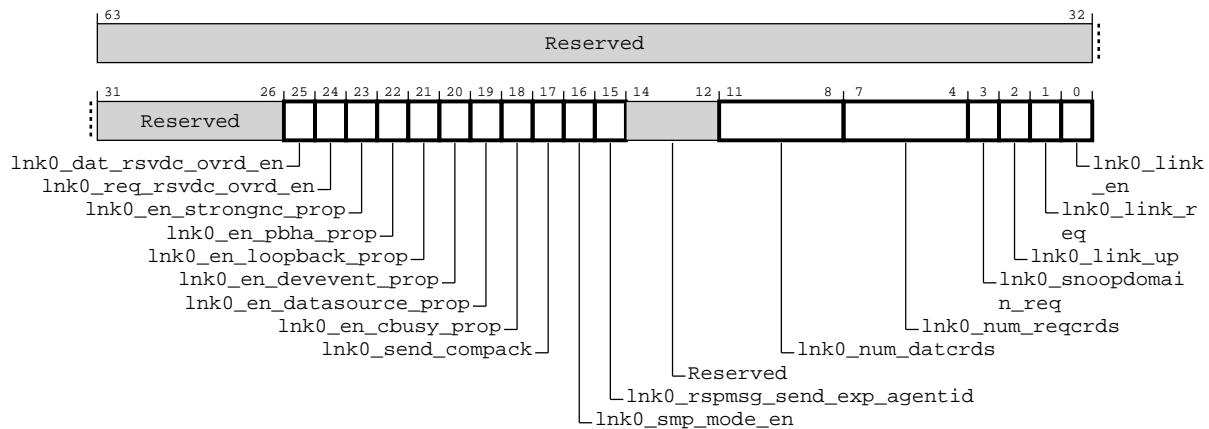


Table 4-46: por_ccg_ha_cxprtcl_link0_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25]	lnk0_dat_rsvdc_ovrd_en	When set, overrides CHI DAT RSVDC field with dat rsvdc strap input for incoming data on CCIX Link 0. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[24]	lnk0_req_rsvdc_ovrd_en	When set, overrides CHI REQ RSVDC field with req rsvdc strap input for incoming requests on CCIX Link 0. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[23]	lnk0_en_strongnc_prop	When set, enables propagation of StrongNC on CCIX Link 0.	RW	1'b0
[22]	lnk0_en_pbha_prop	When set, enables propagation of PBHA on CCIX Link 0.	RW	1'b0
[21]	lnk0_en_loopback_prop	When set, enables propagation of LoopBack on CCIX Link 0.	RW	1'b0
[20]	lnk0_en_devevent_prop	When set, enables propagation of DevEvent on CCIX Link 0.	RW	1'b1
[19]	lnk0_en_datasource_prop	When set, enables propagation of DataSource on CCIX Link 0.	RW	1'b1
[18]	lnk0_en_cbusy_prop	When set, enables propagation of CBusy on CCIX Link 0.	RW	1'b1
[17]	lnk0_send_compack	When set, sends CompAck for CCIX Link 0.	RW	1'b0
[16]	lnk0_smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode for CCIX Link 0.	RW	Configuration dependent
[15]	lnk0_rspmsg_send_exp_agentid	When set sends Expanded Agent ID on CCIX Response Messages for CCIX Link 0	RW	1'b0
[14:12]	Reserved	Reserved	RO	-
[11:8]	lnk0_num_datcrds	Controls the number of CCIX data credits assigned to Link 0 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0

Bits	Name	Description	Type	Reset
[7:4]	lnk0_num_reqcrds	<p>Controls the number of CCIX request credits assigned to Link 0</p> <p>4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned</p>	RW	4'b0
[3]	lnk0_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 0	RW	1'b0
[2]	lnk0_link_up	<p>Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent</p> <p>1'b0 Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1 Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent</p>	RW	1'b0
[1]	lnk0_link_req	<p>Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent</p> <p>1'b0 Link Down request 1'b1 Link Up request</p> <p>The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state.</p>	RW	1'b0
[0]	lnk0_link_en	Enables CCIX Link 0 when set	RW	1'b0
		1'b0 Link is disabled 1'b1 Link is enabled		

4.3.2.25 por_ccg_ha_cxprtcl_link0_status

Functions as the CXHA CCIX Protocol Link 0 status register. Works with por_ccg_ha_cxprtcl_link0_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C08

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-31: por_ccg_ha_cxprtcl_link0_status

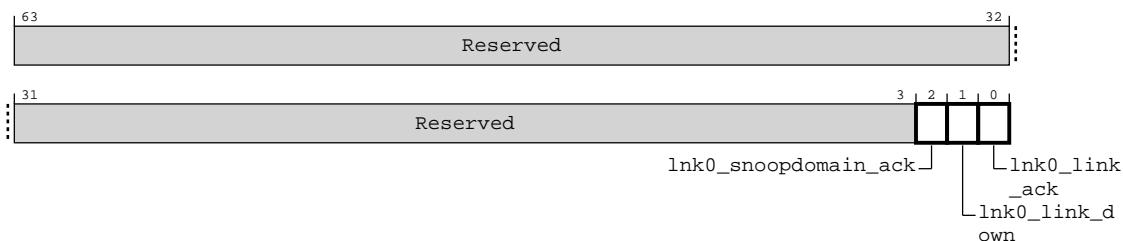


Table 4-47: por_ccg_ha_cxprtcl_link0_status attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	lnk0_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 0	RO	1'b0
[1]	lnk0_link_down	<p>Link Down status; hardware updates this register bit to indicate Link Down status</p> <p>1'b0 Link is not Down; hardware clears Link_DN when it receives a Link Up request</p> <p>1'b1 Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear</p>	RO	1'b1
[0]	lnk0_link_ack	<p>Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request</p> <p>1'b0 Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear</p> <p>1'b1 Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent</p> <p>NOTE: The local agent must clear Link_DN before setting Link_ACK.</p>	RO	1'b0

4.3.2.26 por_ccg_ha_cxprtcl_link1_ctl

Functions as the CXHA CCIX Protocol Link 1 control register. Works with por_ccg_ha_cxprtcl_link1_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C10

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-32: por_ccg_ha_cxprtcl_link1_ctl

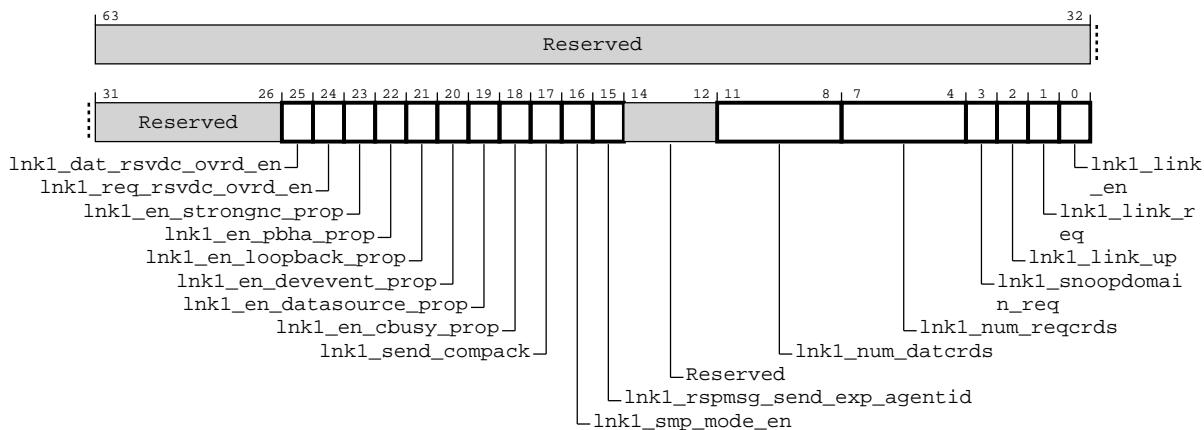


Table 4-48: por_ccg_ha_cxprtcl_link1_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[25]	lnk1_dat_rsvdc_ovrd_en	When set, overrides CHI DAT RSVDC field with dat rsvdc strap input for incoming data on CCIX Link 1. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[24]	lnk1_req_rsvdc_ovrd_en	When set, overrides CHI REQ RSVDC field with req rsvdc strap input for incoming requests on CCIX Link 1. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[23]	lnk1_en_strongnc_prop	When set, enables propagation of StrongNC on CCIX Link 1.	RW	1'b0
[22]	lnk1_en_pbha_prop	When set, enables propagation of PBHA on CCIX Link 1.	RW	1'b0
[21]	lnk1_en_loopback_prop	When set, enables propagation of LoopBack on CCIX Link 1.	RW	1'b0
[20]	lnk1_en_devevent_prop	When set, enables propagation of DevEvent on CCIX Link 1.	RW	1'b1
[19]	lnk1_en_datasource_prop	When set, enables propagation of DataSource on CCIX Link 1.	RW	1'b1
[18]	lnk1_en_cbusy_prop	When set, enables propagation of CBusy on CCIX Link 1.	RW	1'b1
[17]	lnk1_send_compack	When set, sends CompAck for CCIX Link 1.	RW	1'b0
[16]	lnk1_smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode for CCIX Link 1.	RW	Configuration dependent
[15]	lnk1_rspmsg_send_exp_agentid	When set sends Expanded Agent ID on CCIX Response Messages for CCIX Link 1	RW	1'b0
[14:12]	Reserved	Reserved	RO	-
[11:8]	lnk1_num_datcrds	Controls the number of CCIX data credits assigned to Link 1 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0
[7:4]	lnk1_num_reqrnds	Controls the number of CCIX request credits assigned to Link 1 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0
[3]	lnk1_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 1	RW	1'b0
[2]	lnk1_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_UP and Link_DN status in the remote agent 1'b0 Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1 Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0

Bits	Name	Description	Type	Reset
[1]	lnk1_link_req	<p>Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent</p> <p>1'b0 Link Down request 1'b1 Link Up request</p> <p>The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state.</p>	RW	1'b0
[0]	lnk1_link_en	<p>Enables CCIX Link 1 when set</p> <p>1'b0 Link is disabled 1'b1 Link is enabled</p>	RW	1'b0

4.3.2.27 por_ccg_ha_cxprtcl_link1_status

Functions as the CXHA CCIX Protocol Link 1 status register. Works with por_ccg_ha_cxprtcl_link1_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C18

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-33: por_ccg_ha_cxprtcl_link1_status

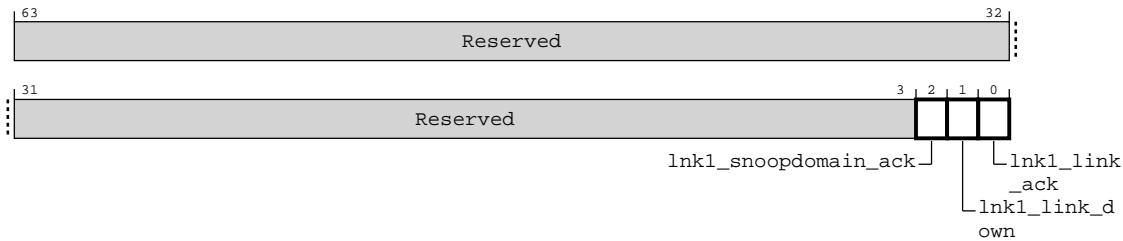


Table 4-49: por_ccg_ha_cxprtcl_link1_status attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	Lnk1_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 1	RO	1'b0
[1]	Lnk1_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0 Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1 Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
[0]	Lnk1_link_ack	Link Up/Down Acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0 Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1 Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

4.3.2.28 por_ccg_ha_cxprtcl_link2_ctl

Functions as the CXHA CCIX Protocol Link 2 control register. Works with por_ccg_ha_cxprtcl_link2_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C20

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-34: por_ccg_ha_cxprtcl_link2_ctl

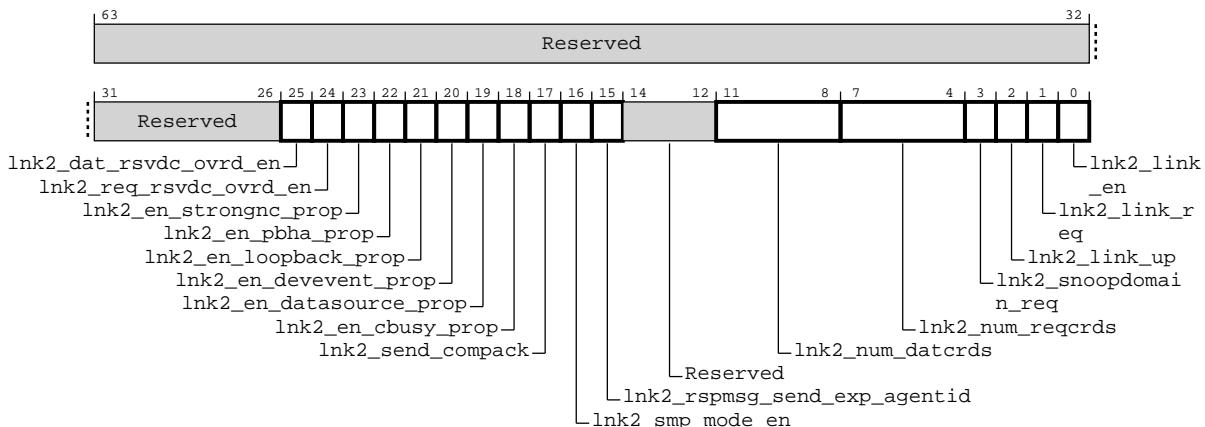


Table 4-50: por_ccg_ha_cxprtcl_link2_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25]	lnk2_dat_rsvdc_ovrd_en	When set, overrides CHI DAT RSVDC field with dat rsvdc strap input for incoming data on CCIX Link 2. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[24]	lnk2_req_rsvdc_ovrd_en	When set, overrides CHI REQ RSVDC field with req rsvdc strap input for incoming requests on CCIX Link 2. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[23]	lnk2_en_strongnc_prop	When set, enables propagation of StrongNC on CCIX Link 2.	RW	1'b0
[22]	lnk2_en_pbha_prop	When set, enables propagation of PBHA on CCIX Link 2.	RW	1'b0
[21]	lnk2_en_loopback_prop	When set, enables propagation of LoopBack on CCIX Link 2.	RW	1'b0
[20]	lnk2_en_devevent_prop	When set, enables propagation of DevEvent on CCIX Link 2.	RW	1'b1
[19]	lnk2_en_datasource_prop	When set, enables propagation of DataSource on CCIX Link 2.	RW	1'b1
[18]	lnk2_en_cbusy_prop	When set, enables propagation of CBusy on CCIX Link 2.	RW	1'b1
[17]	lnk2_send_compack	When set, sends CompAck for CCIX Link 2.	RW	1'b0
[16]	lnk2_smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode for CCIX Link 2.	RW	Configuration dependent

Bits	Name	Description	Type	Reset
[15]	lnk2_rspmsg_send_exp_agentid	When set sends Expanded Agent ID on CCIX Response Messages for CCIX Link 2	RW	1'b0
[14:12]	Reserved	Reserved	RO	-
[11:8]	lnk2_num_datcrds	Controls the number of CCIX data credits assigned to Link 2 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0
[7:4]	lnk2_num_reqcrds	Controls the number of CCIX request credits assigned to Link 2 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0
[3]	lnk2_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 2	RW	1'b0
[2]	lnk2_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0 Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1 Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
[1]	lnk2_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0 Link Down request 1'b1 Link Up request The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state.	RW	1'b0
[0]	lnk2_link_en	Enables CCIX Link 2 when set 1'b0 Link is disabled 1'b1 Link is enabled	RW	1'b0

4.3.2.29 por_ccg_ha_cxprtcl_link2_status

Functions as the CXHA CCIX Protocol Link 2 status register. Works with por_ccg_ha_cxprtcl_link2_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C28

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-35: por_ccg_ha_cxprtcl_link2_status

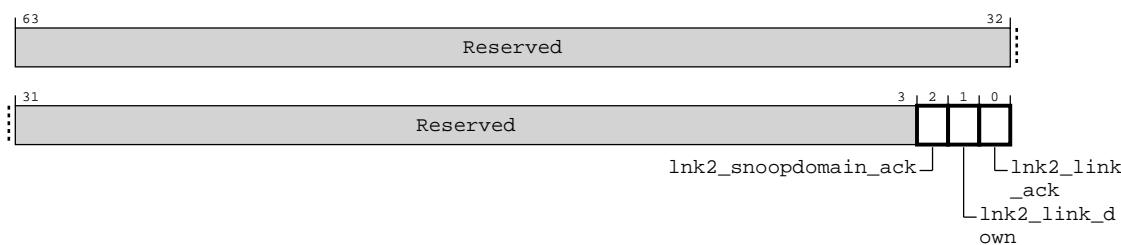


Table 4-51: por_ccg_ha_cxprtcl_link2_status attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	lnk2_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 2	RO	1'b0
[1]	lnk2_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0 Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1 Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1

Bits	Name	Description	Type	Reset
[0]	lnk2_link_ack	<p>Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request</p> <p>1'b0 Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear</p> <p>1'b1 Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent</p> <p>NOTE: The local agent must clear Link_DN before setting Link_ACK.</p>	RO	1'b0

4.3.3 CCG_RA register descriptions

This section lists the CCG_RA registers.

4.3.3.1 por_ccg_ra_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-36: por_ccg_ra_node_info

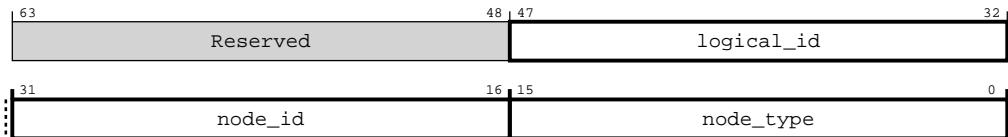


Table 4-52: por_ccg_ra_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0103

4.3.3.2 por_ccg_ra_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-37: por_ccg_ra_child_info

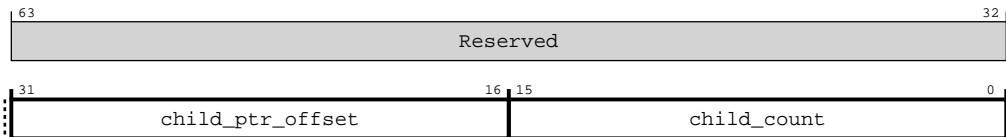


Table 4-53: por_ccg_ra_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'h0

4.3.3.3 por_ccg_ra_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-38: por_ccg_ra_secure_register_groups_override

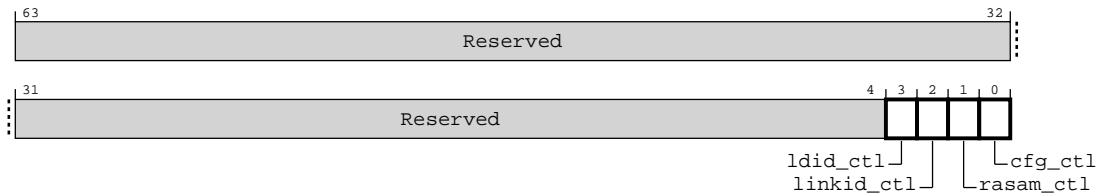


Table 4-54: por_ccg_ra_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	ldid_ctl	Allows Non-secure access to Secure RA LDID registers	RW	1'b0
[2]	linkid_ctl	Allows Non-secure access to Secure RA Link ID registers	RW	1'b0
[1]	rasam_ctl	Allows Non-secure access to Secure RA SAM control registers	RW	1'b0
[0]	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

4.3.3.4 por_ccg_ra_unit_info

Provides component identification information for CXRA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-39: por_ccg_ra_unit_info

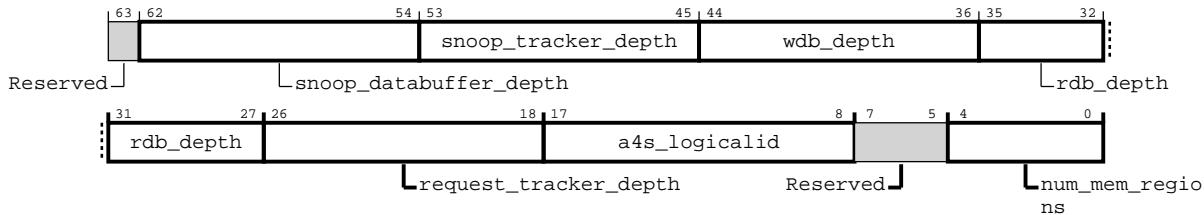


Table 4-55: por_ccg_ra_unit_info attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:54]	snoop_databuffer_depth	Depth of Snoop Data Buffer - number of outstanding SNP requests on CHI	RO	Configuration dependent
[53:45]	snoop_tracker_depth	Depth of Snoop Tracker - number of outstanding SNP requests on CCIX	RO	Configuration dependent
[44:36]	wdb_depth	Depth of Write Data Buffer	RO	Configuration dependent
[35:27]	rdb_depth	Depth of Read Data Buffer	RO	Configuration dependent
[26:18]	request_tracker_depth	Depth of Request Tracker - number of outstanding Memory requests on CCIX	RO	Configuration dependent
[17:8]	a4s_logicalid	AXI4Stream interfaces logical ID	RO	Configuration dependent
[7:5]	Reserved	Reserved	RO	-
[4:0]	num_mem_regions	Number of memory regions supported	RO	Configuration dependent

4.3.3.5 por_ccg_ra_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ra_secure_register_groups_override.cfg_ctl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-40: por_ccg_ra_cfg_ctl

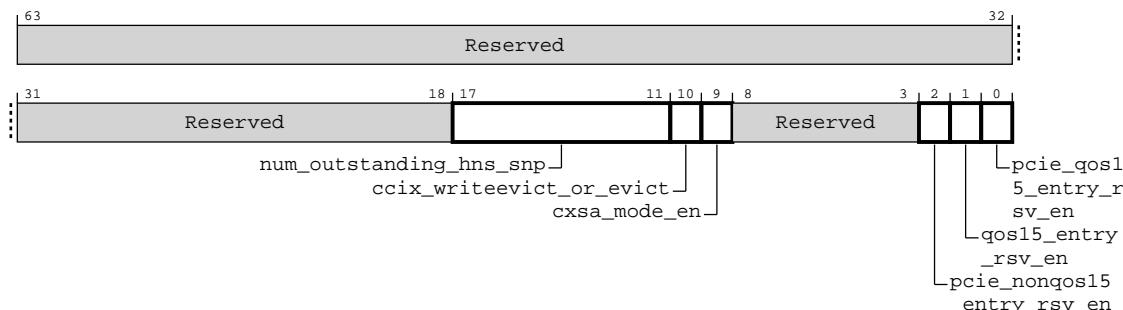


Table 4-56: por_ccg_ra_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:18]	Reserved	Reserved	RO	-
[17:11]	num_outstanding_hns_snp	Specifies the Max number of outstanding snoops from the given RA to each HNS to guarantee snoop sink and deadlock prevention. Must be set to (HNS_NUM_ENTRIES_SNPOQ_PARAM)/(NUM_NON_CXSA_RA).	RW	7'h2
[10]	ccix_writeevict_or_evict	When set, downgrades WriteEvictOrEvict to Evict 1'b1 Evict is sent 1'b0 WriteEvict is sent	RW	1'b0
[9]	cxa_mode_en	When set, enables the CCIX Subordinate Agent mode. In this mode RA functions as a CCIX Subordinate Agent 1'b1 CCIX Subordinate Agent 1'b0 CCIX Requesting Agent	RW	1'b0
[8:3]	Reserved	Reserved	RO	-
[2]	pcie_nongos15_entry_rsv_en	Enables entry reservation for non QoS15 traffic from PCIe RN-I/RN-D 1'b1 Reserves tracker entry for non QoS15 requests from PCIe RN-I/RN-D 1'b0 Does not reserve tracker entry for non QoS15 requests from PCIe RN-I/RN-D	RW	1'b1

Bits	Name	Description	Type	Reset
[1]	qos15_entry_rsv_en	<p>Enables entry reservation for QoS15 traffic</p> <p>1'b1 Reserves tracker entry for QoS15 requests</p> <p>1'b0 Does not reserve tracker entry for QoS15 requests</p>	RW	1'b1
[0]	pcie_qos15_entry_rsv_en	<p>Enables entry reservation for QoS15 traffic from PCIe RN-I/RN-D</p> <p>1'b1 Reserves tracker entry for QoS15 requests from PCIe RN-I/RN-D</p> <p>1'b0 Does not reserve tracker entry for QoS15 requests from PCIe RN-I/RN-D</p>	RW	1'b1

4.3.3.6 por_ccg_ra_aux_ctl

Functions as the auxiliary control register for CXRA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-41: por_ccg_ra_aux_ctl

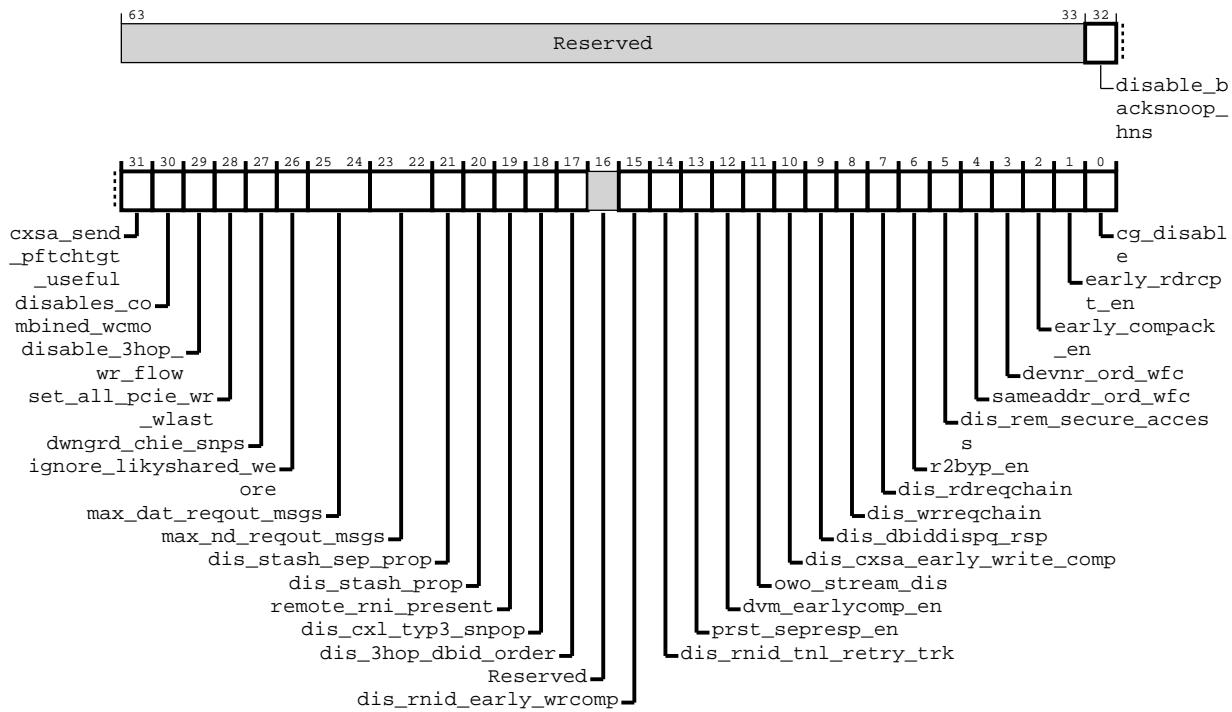


Table 4-57: por_ccg_ra_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:33]	Reserved	Reserved	RO	-
[32]	disable_backsnoop_hns	When set, disables back snooping on an HNS/LCN initiated WriteClean request which is due to LLC eviction	RW	1'b1
[31]	cxsa_send_pftchtgt_useful	When set, sends PreFetch Usefull indication on CHI datasource field in CXSA mode	RW	1'b0
[30]	disables_combined_wcmo	When set, disables sending combined W+CMO to remote HA. Applicable only in SMP mode	RW	1'b1
[29]	disable_3hop_wr_flow	When set, disables 3-hop write flow to remote HA. Applicable only in SMP mode	RW	1'b0
[28]	set_all_pcnie_wr_wlast	When set, sets WLAST indication for all PCIe writes going to HA RNI	RW	1'b0
[27]	dwngrd_chie_snps	When set, downgrades CHIE SnpPreferUnique to SnpNotSharedDirty	RW	1'b0
[26]	ignore_likyshared_weore	<p>When set, disables the use of LikelyShared(LS) bit to make a decision for WriteEvictOrEvict</p> <p>1'b0 Send WriteEvict when LS= 0 and send Evict when LS=1</p> <p>1'b1 Ignore LS bit. WriteEvict is sent. Further static decision can be made using ccix_writeevict_or_evict in cfg_ctl register</p>	RW	1'b0

Bits	Name	Description	Type	Reset
[25:24]	max_dat_reqout_msgs	<p>Used to configure the maximum number of data requests messages (writes, atomics etc.) presented to CCLA's packing logic.</p> <p>2'b00 one message 2'b01 two messages 2'b10 three messages 2'b11 four messages</p> <p>Note: The max is further limited by max allowed by the given protocol (CCIX2.0/CXL.mem/CXL.cache)</p>	RW	2'b11
[23:22]	max_nd_reqout_msgs	<p>Used to configure the maximum number of non-data requests messages (reads, dataless) presented to CCLA's packing logic.</p> <p>2'b00 one message 2'b01 two messages 2'b10 three messages 2'b11 four messages</p> <p>Note: The max is further limited by max allowed by the given protocol (CCIX2.0/CXL.mem/CXL.cache)</p>	RW	2'b11
[21]	dis_stash_sep_prop	When set, disables propagation of StashSep opcodes on CCIX. StashSep opcodes are sent as Stash opcodes when set. Applicable only in SMP mode	RW	1'b0
[20]	dis_stash_prop	When set, disables propagation of stash opcodes on CCIX. Applicable only in SMP mode	RW	1'b0
[19]	remote_rni_present	When set, Enables TXNID coloring to enable traffic to remote RNI	RW	1'b1
[18]	dis_cxl_typ3_snpop	When set, drives SnpType= NOP on CXL Type3 M2S Req and RwD messages	RW	1'b1
[17]	dis_3hop_dbid_order	When set, disables ordered dispatch of DBIDs for 3-hop writes. By default, 3-hop DBIDs are dispatched in order. Applicable only if 3-hop write flow is enabled	RW	1'b0
[16]	Reserved	Reserved	RO	-
[15]	dis_rnid_early_wrcomp	When set, disables early write completions for tunneled writes from RNI.	RW	1'b0
[14]	dis_rnid_tnl_retry_trk	When set, disables RNID write request tunneling retry tracker.	RW	1'b0
[13]	prst_sepresp_en	When set, enables separate persist response on CCIX for persistent cache maintenance (PCMO2) operation Note: this bit is applicable only in SMP mode.	RW	1'b1
[12]	dvm_earlycomp_en	When set, enables early DVM Op completion responses from RA.	RW	1'b1
[11]	owo_stream_dis	When set, disables CompAck dependency to dispatch an ordered PCIe write.	RW	1'b1
[10]	dis_cxsa_early_write_comp	When set, disables early write completions in CCIX Subordinate Agent mode.	RW	1'b0
[9]	dis_dbiddispq_rsp	When set, disables the dispatch of DBID responses from a separate DispatchQ.	RW	1'b0
[8]	dis_wreqchain	When set, disables chaining of write requests.	RW	1'b0
[7]	dis_rdreqchain	When set, disables chaining of read and dataless requests.	RW	1'b0
[6]	r2byp_en	When set, enables request bypass. Applies to read and dataless requests only. Note: When set will affect the capability to chain a request on the TX side	RW	1'b1
[5]	dis_rem_secure_access	When set, treats all the incoming snoops as Non-secure and forces the NS bit to 1	RW	1'b0
[4]	sameaddr_ord_wfc	When set, enables waiting for completion (COMP) before dispatching next same Addr dependent transaction (TXN)	RW	1'b0
[3]	devnr_ord_wfc	When set, enables waiting for completion (COMP) before dispatching next Device-nR dependent transaction (TXN)	RW	1'b0
[2]	early_compack_en	Early CompAck enable; enables sending early CompAck on CCIX for requests that require CompAck	RW	1'b1

Bits	Name	Description	Type	Reset
[1]	early_rdrcpt_en	Early ReadReceipt enable; enables sending early ReadReceipt for ordered read requests	RW	1'b1
[0]	cg_disable	Disables clock gating when set	RW	1'b0

4.3.3.7 por_ccg_ra_cbusy_limit_ctl

Cbusy threshold limits for RHT entries.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA18

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-42: por_ccg_ra_cbusy_limit_ctl

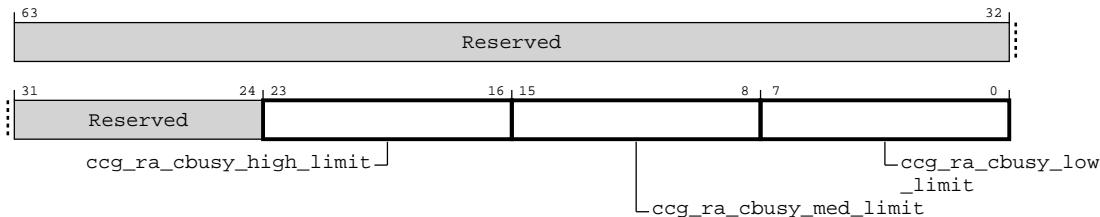


Table 4-58: por_ccg_ra_cbusy_limit_ctl attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	ccg_ra_cbusy_high_limit	RHT limit for CBusy High	RW	Configuration dependent
[15:8]	ccg_ra_cbusy_med_limit	RHT limit for CBusy Med	RW	Configuration dependent

Bits	Name	Description	Type	Reset
[7:0]	ccg_ra_cbusy_low_limit	RHT limit for CBusy Low	RW	Configuration dependent

4.3.3.8 por_ccg_ra_sam_addr_reg0-7on_reg0-7ndex

There are 8 iterations of this register. The index ranges from 0 to 7. Configures Address Region #{{index}} for RA SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
16'hC00 + #{8*index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por ccg ra secure register groups override.rasam ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-43: por ccg ra sam addr reg0-7on reg0-7ndex

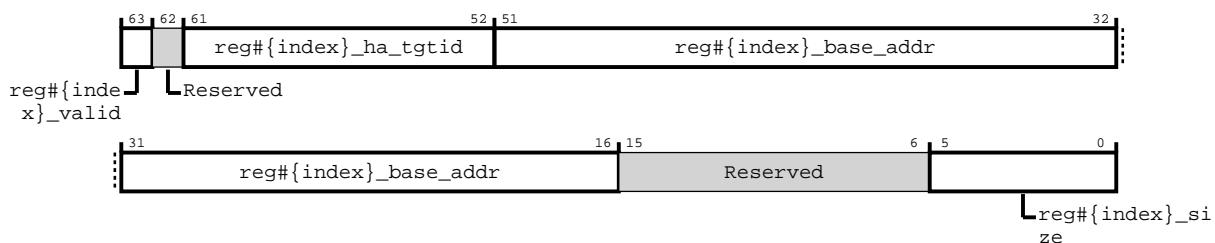


Table 4-59: por_ccg_ra_sam_addr_reg0-7on_reg0-7ndex attributes

Bits	Name	Description	Type	Reset
[63]	reg#{index}_valid	Specifies if the memory region is valid	RW	1'b0

Bits	Name	Description	Type	Reset
[62]	Reserved	Reserved	RO	-
[61:52]	reg#{index}_ha_tgtid	Specifies the target HAID	RW	10'b0
[51:16]	reg#{index}_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	36'h0
[15:6]	Reserved	Reserved	RO	-
[5:0]	reg#{index}_size	Specifies the size of the memory region	RW	1'b0

4.3.3.9 por_ccg_ra_agentid_to_linkid_val

Specifies which Agent ID to Link ID mappings are valid.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD00

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ra_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-44: por_ccg_ra_agentid_to_linkid_val

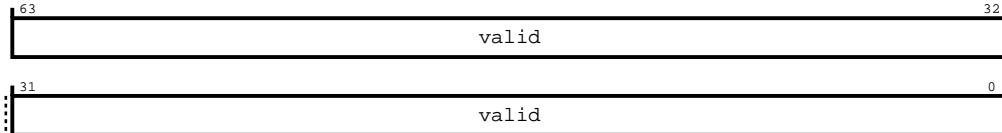


Table 4-60: por_ccg_ra_agentid_to_linkid_val attributes

Bits	Name	Description	Type	Reset
[63:0]	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

4.3.3.10 por_ccg_ra_agent0-7d_to_l0-7nk0-7d_reg0-7ndex

There are 8 iterations of this register. The index ranges from 0 to 7. Specifies the mapping of Agent ID to Link ID for Agent IDs #{{index}*8} to #{{index}*8+7}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD10 + #{index*8}

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ra_secure_register_groups_override.linkid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-45: por_ccg_ra_agent0-7d_to_l0-7nk0-7d_reg0-7ndex

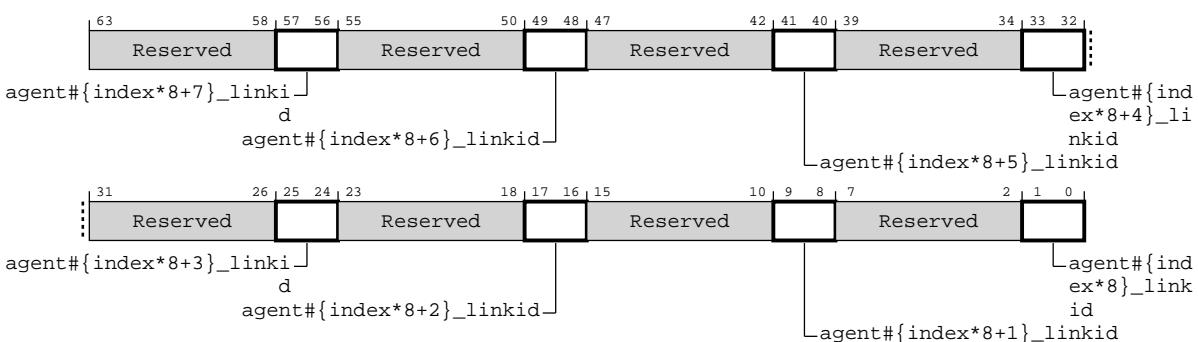


Table 4-61: por_ccg_ra_agent0-7d_to_l0-7nk0-7d_reg0-7ndex attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:56]	agent#{index*8+7}_linkid	Specifies the Link ID for Agent ID #{{index}*8+7}	RW	2'h0

Bits	Name	Description	Type	Reset
[55:50]	Reserved	Reserved	RO	-
[49:48]	agent#{index*8+6}_linkid	Specifies the Link ID for Agent ID #{index*8+6}	RW	2'h0
[47:42]	Reserved	Reserved	RO	-
[41:40]	agent#{index*8+5}_linkid	Specifies the Link ID for Agent ID #{index*8+5}	RW	2'h0
[39:34]	Reserved	Reserved	RO	-
[33:32]	agent#{index*8+4}_linkid	Specifies the Link ID for Agent ID #{index*8+4}	RW	2'h0
[31:26]	Reserved	Reserved	RO	-
[25:24]	agent#{index*8+3}_linkid	Specifies the Link ID for Agent ID #{index*8+3}	RW	2'h0
[23:18]	Reserved	Reserved	RO	-
[17:16]	agent#{index*8+2}_linkid	Specifies the Link ID for Agent ID #{index*8+2}	RW	2'h0
[15:10]	Reserved	Reserved	RO	-
[9:8]	agent#{index*8+1}_linkid	Specifies the Link ID for Agent ID #{index*8+1}	RW	2'h0
[7:2]	Reserved	Reserved	RO	-
[1:0]	agent#{index*8}_linkid	Specifies the Link ID for Agent ID #{index*8}	RW	2'h0

4.3.3.11 por_ccg_ra_rn0-31_ld0-31d_to_exp_ra0-31d_reg0-31ndex

There are 32 iterations of this register. The index ranges from 0 to 31. Specifies the mapping of RN-I's LDID to Expanded RAID for LDIDs #{i*4} to #{index*4+3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE00 + #{index*8}

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ra_secure_register_groups_override.ldid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-46: por_ccg_ra_rn0-31_Id0-31d_to_exp_ra0-31d_reg0-31index

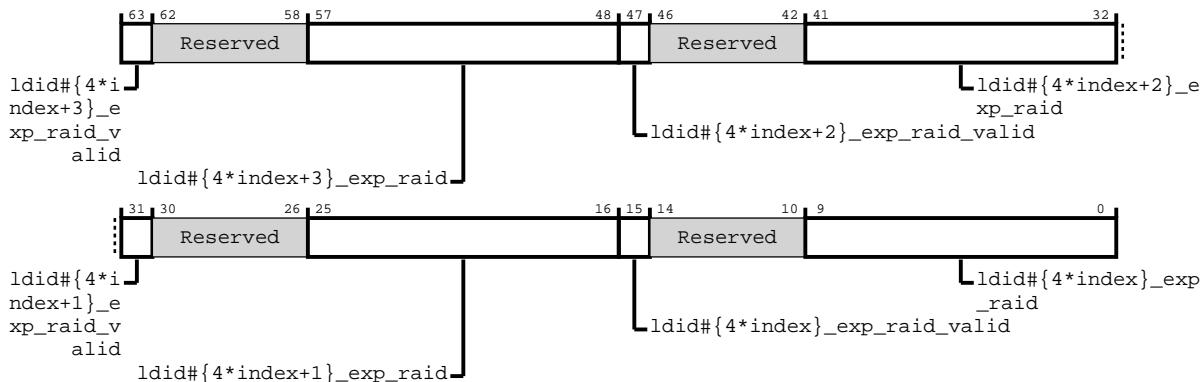


Table 4-62: por_ccg_ra_rn0-31_Id0-31d_to_exp_ra0-31d_reg0-31index attributes

Bits	Name	Description	Type	Reset
[63]	ldid#{4*index+3}_exp_raid_valid	Specifies whether the Expanded RAID for LDID#{4*index+3} is valid;	RW	1'h0
[62:58]	Reserved	Reserved	RO	-
[57:48]	ldid#{4*index+3}_xp_raid	Specifies the Expanded RAID for LDID #{4*index+3}	RW	10'h0
[47]	ldid#{4*index+2}_xp_raid	Specifies whether the Expanded RAID for LDID#{4*index+2} is valid;	RW	1'h0
[46:42]	Reserved	Reserved	RO	-
[41:32]	ldid#{4*index+2}_exp_raid	Specifies the Expanded RAID for LDID #{4*index+2}	RW	10'h0
[31]	ldid#{4*index+1}_exp_raid_valid	Specifies whether the Expanded RAID for LDID#{4*index+1} is valid;	RW	1'h0
[30:26]	Reserved	Reserved	RO	-
[25:16]	ldid#{4*index+1}_xp_raid	Specifies the Expanded RAID for LDID #{4*index+1}	RW	10'h0
[15]	ldid#{4*index}_xp_raid	Specifies whether the Expanded RAID for LDID#{4*index} is valid;	RW	1'h0
[14:10]	Reserved	Reserved	RO	-
[9:0]	ldid#{4*index}_exp_raid	Specifies the Expanded RAID for LDID #{4*index}	RW	10'h0

4.3.3.12 por_ccg_ra_rnd_Id0-31d_to_exp_ra0-31d_reg0-31index

There are 32 iterations of this register. The index ranges from 0 to 31. Specifies the mapping of RN-D's LDID to Expanded RAID for LDIDs #{{index}*4} to #{{index}*4+3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF00 + #{{index}*8}

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ra_secure_register_groups_override.ldid_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-47: por_ccg_ra_rnd_Id0-31d_to_exp_ra0-31d_reg0-31ndex

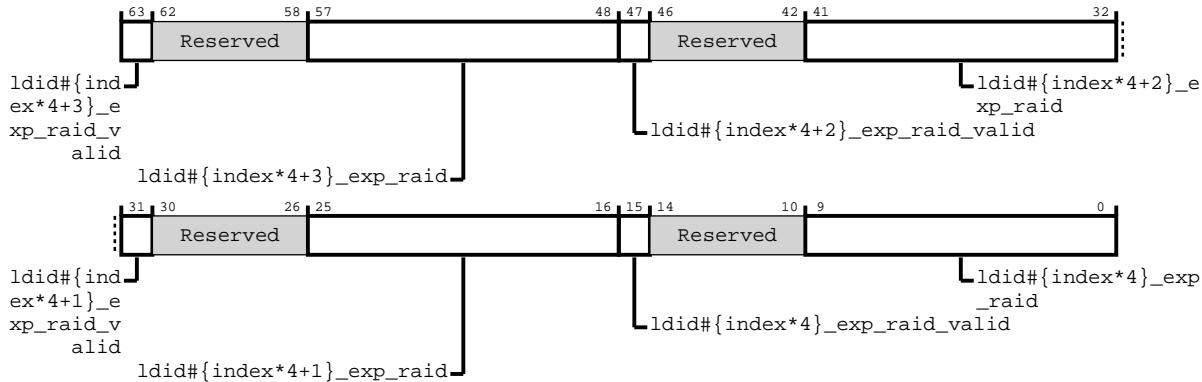


Table 4-63: por_ccg_ra_rnd_Id0-31d_to_exp_ra0-31d_reg0-31ndex attributes

Bits	Name	Description	Type	Reset
[63]	ldid#[index*4+3]_exp_raid_valid	Specifies whether the Expanded RAID for LDID#[index*4+3] is valid;	RW	1'h0
[62:58]	Reserved	Reserved	RO	-
[57:48]	ldid#[index*4+3]_exp_raid	Specifies the Expanded RAID for LDID #[index*4+3]	RW	10'h0
[47]	ldid#[index*4+2]_exp_raid_valid	Specifies whether the Expanded RAID for LDID#[index*4+2] is valid;	RW	1'h0
[46:42]	Reserved	Reserved	RO	-
[41:32]	ldid#[index*4+2]_exp_raid	Specifies the Expanded RAID for LDID #[index*4+2]	RW	10'h0
[31]	ldid#[index*4+1]_exp_raid_valid	Specifies whether the Expanded RAID for LDID#[index*4+1] is valid;	RW	1'h0
[30:26]	Reserved	Reserved	RO	-
[25:16]	ldid#[index*4+1]_exp_raid	Specifies the Expanded RAID for LDID #[index*4+1]	RW	10'h0
[15]	ldid#[index*4]_exp_raid_valid	Specifies whether the Expanded RAID for LDID#[index*4] is valid;	RW	1'h0
[14:10]	Reserved	Reserved	RO	-
[9:0]	ldid#[index*4]_exp_raid	Specifies the Expanded RAID for LDID #[index*4]	RW	10'h0

4.3.3.13 por_ccg_ra_rnf_ld0-127d_to_exp_ra0-127d_reg0-127ndex

There are 128 iterations of this register. The index ranges from 0 to 127. Specifies the mapping of RN-F's LDID to Expanded RAID for LDIDs # $\{index^*4\}$ to # $\{index^*4+3\}$.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h1000 + #{index*8}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ra_secure_register_groups_override.ldid_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-48: por_ccg_ra_rnf_ld0-127d_to_exp_ra0-127d_reg0-127ndex

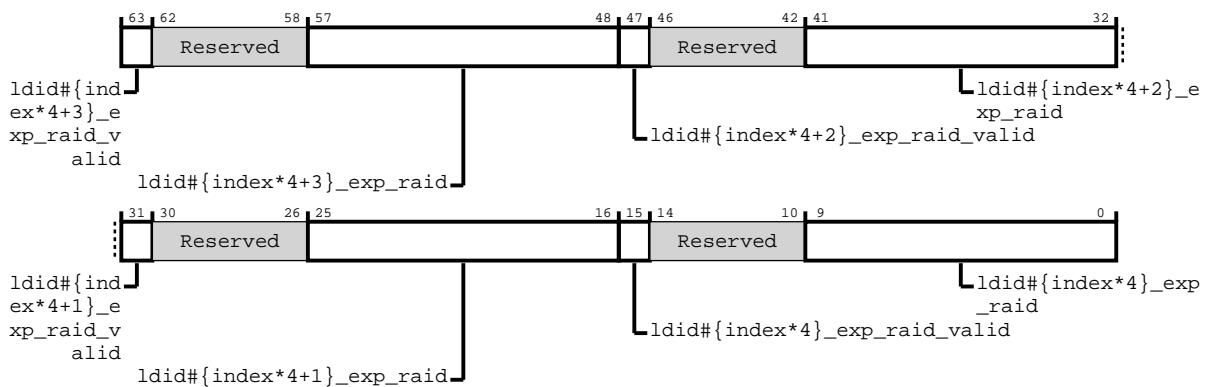


Table 4-64: por_ccg_ra_rnf_ld0-127d_to_exp_ra0-127d_reg0-127ndex attributes

Bits	Name	Description	Type	Reset
[63]	ldid#{index*4+3}_exp_raid_valid	Specifies whether the look table entry for default LDID# $\{index^*4+3\}$ is valid;	RW	<code>1'h0</code>
[62:58]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[57:48]	ldid#{index*4+3}_exp_raid	Specifies the Expanded RAID for LDID #{index*4+3}	RW	10'h0
[47]	ldid#{index*4+2}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4+2} is valid;	RW	1'h0
[46:42]	Reserved	Reserved	RO	-
[41:32]	ldid#{index*4+2}_exp_raid	Specifies the Expanded RAID for LDID #{index*4+2}	RW	10'h0
[31]	ldid#{index*4+1}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4+1} is valid;	RW	1'h0
[30:26]	Reserved	Reserved	RO	-
[25:16]	ldid#{index*4+1}_exp_raid	Specifies the Expanded RAID for LDID #{index*4+1}	RW	10'h0
[15]	ldid#{index*4}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4} is valid;	RW	1'h0
[14:10]	Reserved	Reserved	RO	-
[9:0]	ldid#{index*4}_exp_raid	Specifies the Expanded RAID for LDID #{index*4}	RW	10'h0

4.3.3.14 por_ccg_ra_ha_ld0-15d_to_exp_ra0-15d_reg0-15ndex

There are 16 iterations of this register. The index ranges from 0 to 15. Specifies the mapping of HA's LDID to Expanded RAID for LDIDs #{{index}*4} to #{{index}*4+3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1400 + #{index*8}

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccg_ra_secure_register_groups_override.ldid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-49: por_ccg_ra_ha_Id0-15d_to_exp_ra0-15d_reg0-15ndex

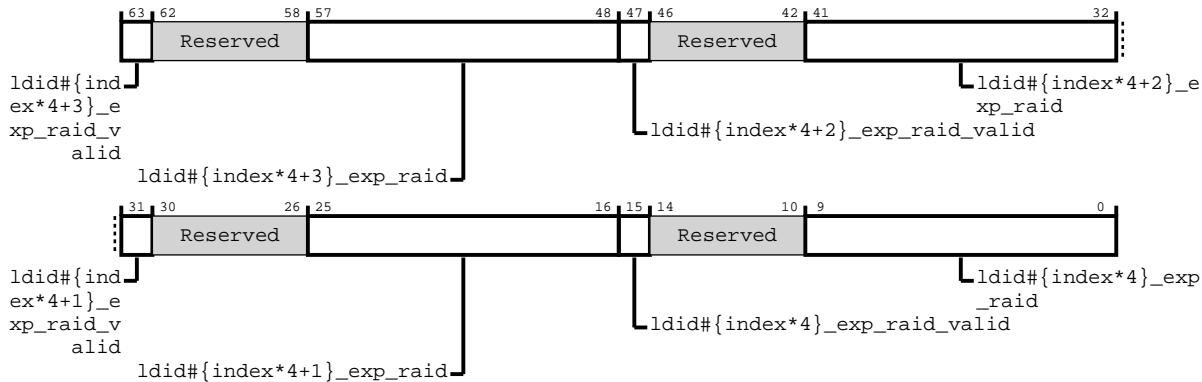


Table 4-65: por_ccg_ra_ha_Id0-15d_to_exp_ra0-15d_reg0-15ndex attributes

Bits	Name	Description	Type	Reset
[63]	ldid#{index*4+3}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4+3} is valid;	RW	1'h0
[62:58]	Reserved	Reserved	RO	-
[57:48]	ldid#{index*4+3}_exp_raid	Specifies the Expanded RAID for LDID #{index*4+3}	RW	10'h0
[47]	ldid#{index*4+2}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4+2} is valid;	RW	1'h0
[46:42]	Reserved	Reserved	RO	-
[41:32]	ldid#{index*4+2}_exp_raid	Specifies the Expanded RAID for LDID #{index*4+2}	RW	10'h0
[31]	ldid#{index*4+1}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4+1} is valid;	RW	1'h0
[30:26]	Reserved	Reserved	RO	-
[25:16]	ldid#{index*4+1}_exp_raid	Specifies the Expanded RAID for LDID #{index*4+1}	RW	10'h0
[15]	ldid#{index*4}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4} is valid;	RW	1'h0
[14:10]	Reserved	Reserved	RO	-
[9:0]	ldid#{index*4}_exp_raid	Specifies the Expanded RAID for LDID #{index*4}	RW	10'h0

4.3.3.15 por_ccg_ra_hns_Id0-0d_to_exp_ra0-0d_reg0-0ndex

There are 1 iterations of this register. The index ranges from 0 to 0. Specifies the mapping of HNS's LDID to Expanded RAID for LDIDs #{index*4} to #{index*4+3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1480 + #{index*8}

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ra_secure_register_groups_override.ldid_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-50: por_ccg_ra_hns_Id0-0d_to_exp_ra0-0d_reg0-0ndex

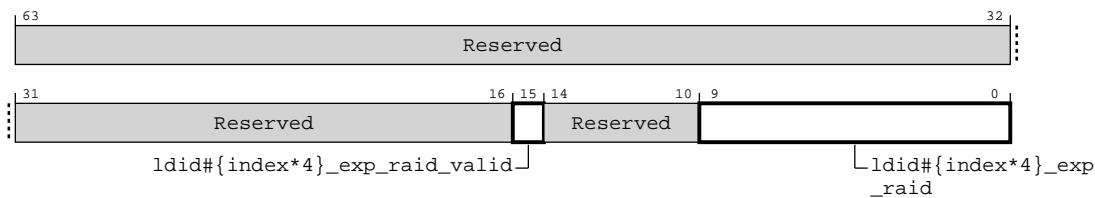


Table 4-66: por_ccg_ra_hns_Id0-0d_to_exp_ra0-0d_reg0-0ndex attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15]	ldid#{index*4}_exp_raid_valid	Specifies whether the look table entry for default LDID#{index*4} is valid;	RW	1'h0
[14:10]	Reserved	Reserved	RO	-
[9:0]	ldid#{index*4}_exp_raid	Specifies the Expanded RAID for LDID #{index*4}	RW	10'h0

4.3.3.16 por_ccg_ra_rnf_Id0-127d_to_ovrd_Id0-127d_reg0-127ndex

There are 128 iterations of this register. The index ranges from 0 to 127. Specifies the mapping of RN-F's overridden LDID for default LDIDs #{index*4} to #{index*4+3}. Valid only if POR_MXP_RNF_CLUSTER_EN_PARAM is 1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h1500 + #{index*8}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccg_ra_secure_register_groups_override.ldid_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-51: por_ccg_ra_rnf_Id0-127d_to_ovrd_Id0-127d_reg0-127ndex

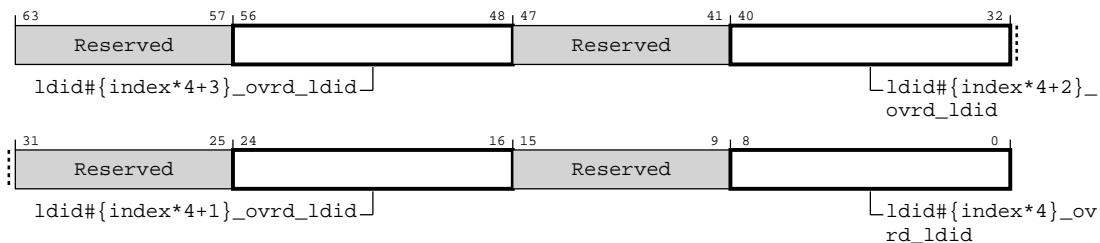


Table 4-67: por_ccg_ra_rnf_Id0-127d_to_ovrd_Id0-127d_reg0-127ndex attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:48]	ldid#{index*4+3}_ovrd_ldid	Specifies the Overridden LDID for Default LDID #{index*4+3}	RW	Configuration dependent
[47:41]	Reserved	Reserved	RO	-
[40:32]	ldid#{index*4+2}_ovrd_ldid	Specifies the Overridden LDID for Default LDID #{index*4+2}	RW	Configuration dependent
[31:25]	Reserved	Reserved	RO	-
[24:16]	ldid#{index*4+1}_ovrd_ldid	Specifies the Overridden LDID for Default LDID #{index*4+1}	RW	Configuration dependent
[15:9]	Reserved	Reserved	RO	-
[8:0]	ldid#{index*4}_ovrd_ldid	Specifies the Overridden LDID for Default LDID #{index*4}	RW	Configuration dependent

4.3.3.17 por_ccg_ra_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-52: por_ccg_ra_pmu_event_sel

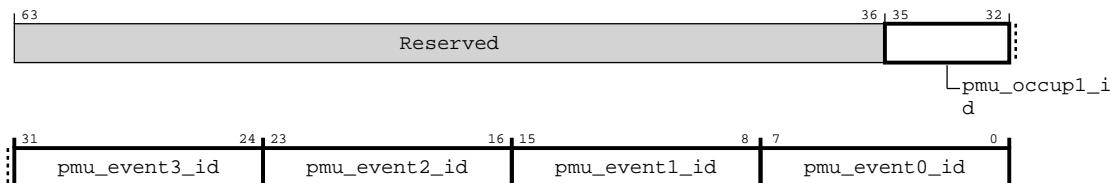


Table 4-68: por_ccg_ra_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:36]	Reserved	Reserved	RO	-
[35:32]	pmu_occup1_id	PMU occupancy event selector ID	RW	4'b0
[31:24]	pmu_event3_id	CXRA PMU Event 3 ID; see pmu_event0_id for encodings	RW	8'b0
[23:16]	pmu_event2_id	CXRA PMU Event 2 ID; see pmu_event0_id for encodings	RW	8'b0
[15:8]	pmu_event1_id	CXRA PMU Event 1 ID; see pmu_event0_id for encodings	RW	8'b0

Bits	Name	Description	Type	Reset
[7:0]	pmu_event0_id	CXRA PMU Event 0 ID	RW	8'b0
	8'h00	No event		
	8'h41	Request Tracker (RHT) occupancy count overflow		
	8'h42	Snoop Tracker (SHT) occupancy count overflow		
	8'h43	Read Data Buffer (RDB) occupancy count overflow		
	8'h44	Write Data Buffer (WDB) occupancy count overflow		
	8'h45	Snoop Sink Buffer (SSB) occupancy count overflow		
	8'h46	CCIX RX broadcast snoops		
	8'h47	CCIX TX request chain		
	8'h48	CCIX TX request chain average length		
	8'h49	CHI internal RSP stall		
	8'h4A	CHI internal DAT stall		
	8'h4B	CCIX REQ Protocol credit Link 0 stall		
	8'h4C	CCIX REQ Protocol credit Link 1 stall		
	8'h4D	CCIX REQ Protocol credit Link 2 stall		
	8'h4E	CCIX DAT Protocol credit Link 0 stall		
	8'h4F	CCIX DAT Protocol credit Link 1 stall		
	8'h50	CCIX DAT Protocol credit Link 2 stall		
	8'h51	CHI external RSP stall		
	8'h52	CHI external DAT stall		
	8'h53	CCIX MISC Protocol credit Link 0 stall		
	8'h54	CCIX MISC Protocol credit Link 1 stall		
	8'h55	CCIX MISC Protocol credit Link 2 stall		
	8'h56	Request Tracker (RHT) allocations		
	8'h57	Snoop Tracker (SHT) allocations		
	8'h58	Read Data Buffer (RDB) allocations		
	8'h59	Write Data Buffer (WDB) allocations		
	8'h5A	Snoop Sink Buffer (SSB) allocations		

4.3.3.18 por_ccg_ra_ccprtcl_link0_ctl

Functions as the CXRA CCIX Protocol Link 0 control register. Works with por_ccg_ra_ccprtcl_link0_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C00

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-53: por_ccg_ra_ccprtcl_link0_ctl

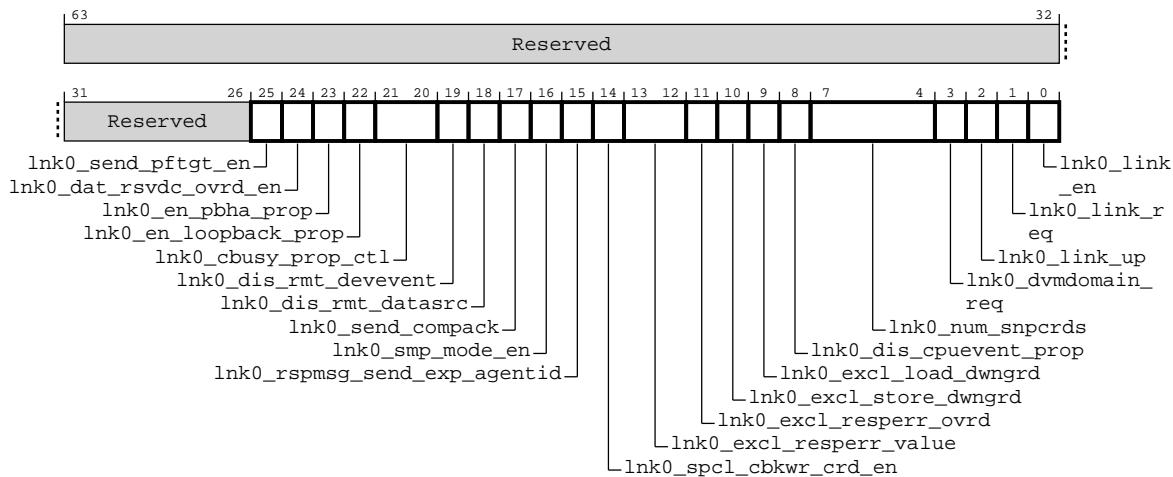


Table 4-69: por_ccg_ra_ccprtcl_link0_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25]	lnk0_send_pftgt_en	When set, enables sending Prefetch Target (CHI) or MemSpecRd (CXL) over link 0.	RW	1'b1
[24]	lnk0_dat_rsvdc_ovrd_en	When set, overrides CHI DAT RSVDC field with dat rsvdc strap input for incoming data on CCIX Link 0. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[23]	lnk0_en_pbha_prop	When set, enables propagation of PBHA on CCIX Link 0.	RW	1'b1
[22]	lnk0_en_loopback_prop	When set, enables propagation of LoopBack on CCIX Link 0.	RW	1'b1
[21:20]	lnk0_cbusy_prop_ctl	Controls the propagation of Cbusy field for CCIX Link 0. 2'b00 Send RA Cbusy on all responses based on the limits programmed in por_ccg_ra_cbusy_limit_ctl 2'b01 Pass through remote CBusy on late completion responses (CompData, Comp) 2'b10 Greater of RA Cbusy or remote Cbusy. Applicable to responses where remote Cbusy can be sent NOTE: This field is applicable SMP and CXL modes	RW	2'b0
[19]	lnk0_dis_rmt_devevent	When set, disables propagation of remote Dev Event field for CCIX Link 0. NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0

Bits	Name	Description	Type	Reset
[18]	lnk0_dis_rmt_datasrc	When set, disables propagation of remote data source for CCIX Link 0. NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[17]	lnk0_send_compack	When set, sends CompAck for CCIX Link 0.	RW	1'b0
[16]	lnk0_smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode for CCIX Link 0.	RW	Configuration dependent
[15]	lnk0_rspmsg_send_exp_agentid	When set sends Expanded Agent ID on CCIX Response Messages for CCIX Link 0	RW	1'b0
[14]	lnk0_spcl_cbkwr_crd_en	When set, notifies RA to use special credits from HA to send CopyBack writes on CCIX Link 0 NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[13:12]	lnk0_excl_resperr_value	Two bit value to override RespErr field of an exclusive response. Applicable only if lnk0_excl_resperr_ovrd bit is set. NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	2'b0
[11]	lnk0_excl_resperr_ovrd	When set, overrides the RespErr field of exclusive response with the lnk0_excl_resperr_value field NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[10]	lnk0_excl_store_dwgnd	When set, downgrades shareable exclusive store to shareable store when sending on CCIX Link 0 NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[9]	lnk0_excl_load_dwgnd	When set, downgrades shareable exclusive load to shareable load when sending on CCIX Link 0 NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[8]	lnk0_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 0 NOTE: This field is applicable only when SMP Mode enable is set.	RW	1'b0
[7:4]	lnk0_num_snpcrds	Controls the number of CCIX snoop credits assigned to Link 0 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0
[3]	lnk0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 0	RW	1'b0
[2]	lnk0_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0 Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1 Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0

Bits	Name	Description	Type	Reset
[1]	lnk0_link_req	<p>Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent</p> <p>1'b0 Link Down request 1'b1 Link Up request</p> <p>The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state.</p>	RW	1'b0
[0]	lnk0_link_en	<p>Enables CCIX Link 0 when set</p> <p>1'b0 Link is disabled 1'b1 Link is enabled</p>	RW	1'b0

4.3.3.19 por_ccg_ra_ccprtcl_link0_status

Functions as the CXRA CCIX Protocol Link 0 status register. Works with por_ccg_ra_ccprtcl_link0_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C08

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-54: por_ccg_ra_ccprtcl_link0_status

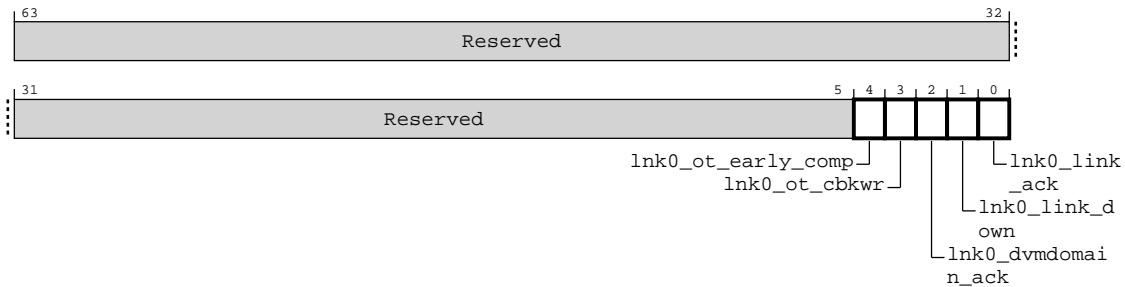


Table 4-70: por_ccg_ra_ccprtcl_link0_status attributes

Bits	Name	Description	Type	Reset
[63:5]	Reserved	Reserved	RO	-
[4]	lnk0_ot_early_comp	Set, if there is an outstanding request for which early completion has been given for CCIX Link0	RO	1'b0
[3]	lnk0_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link0	RO	1'b0
[2]	lnk0_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 0	RO	1'b0
[1]	lnk0_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0 Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1 Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
[0]	lnk0_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0 Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops granting protocol credits and starts returning protocol credits to the remote agent when Link_ACK is clear 1'b1 Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

4.3.3.20 por_ccg_ra_ccprtcl_link1_ctl

Functions as the CXRA CCIX Protocol Link 1 control register. Works with por_ccg_ra_ccprtcl_link1_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C10

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-55: por_ccg_ra_ccprtcl_link1_ctl

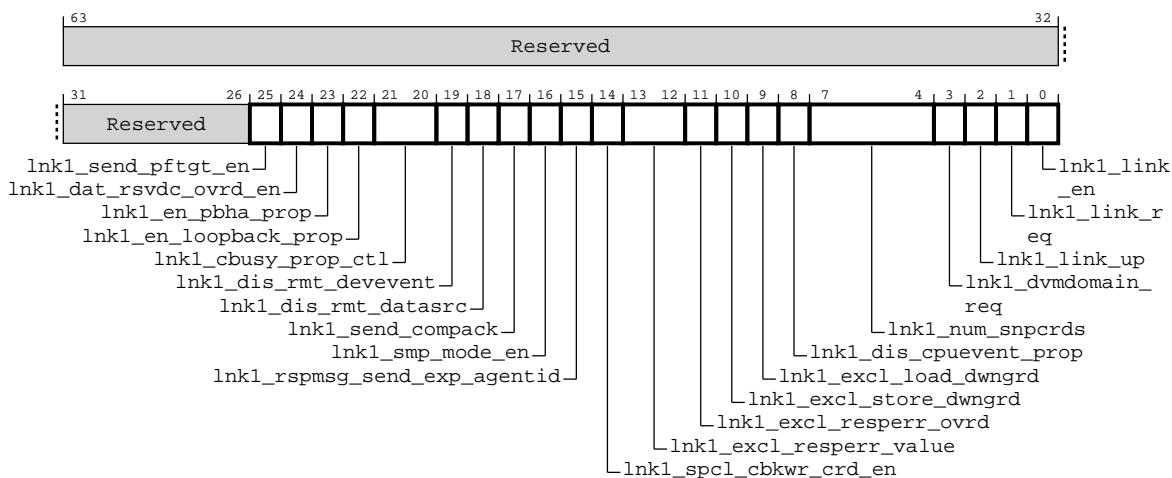


Table 4-71: por_ccg_ra_ccprtcl_link1_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25]	lnk1_send_pftgt_en	When set, enables sending Prefetch Target (CHI) over link 1. Note: This field is not-applicable in CXL mode for link1	RW	1'b1
[24]	lnk1_dat_rsvdc_ovrd_en	When set, overrides CHI DAT RSVDC field with dat rsvdc strap input for incoming data on CCIX Link 1. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[23]	lnk1_en_pbha_prop	When set, enables propagation of PBHA on CCIX Link 1.	RW	1'b1
[22]	lnk1_en_loopback_prop	When set, enables propagation of LoopBack on CCIX Link 1.	RW	1'b1

Bits	Name	Description	Type	Reset
[21:20]	lnk1_cbusy_prop_ctl	<p>Controls the propagation of Cbusy field for CCIX Link 1.</p> <p>2'b00 Send RA Cbusy on all responses based on the limits programmed in por_ccg_ra_cbusy_limit_ctl</p> <p>2'b01 Pass through remote CBusy on late completion responses (CompData, Comp)</p> <p>2'b10 Greater of RA Cbusy or remote Cbusy. Applicable to responses where remote Cbusy can be sent</p> <p>NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)</p>	RW	2'b0
[19]	lnk1_dis_rmt_deevent	When set, disables propagation of remote Dev Event field for CCIX Link 1. NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[18]	lnk1_dis_rmt_datasrc	When set, disables propagation of remote data source for CCIX Link 1. NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[17]	lnk1_send_compack	When set, sends CompAck for CCIX Link 1.	RW	1'b0
[16]	lnk1_smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode for CCIX Link 1.	RW	Configuration dependent
[15]	lnk1_rspmsg_send_exp_agentid	When set sends Expanded Agent ID on CCIX Response Messages for CCIX Link 1	RW	1'b0
[14]	lnk1_spcl_cbkwr_crd_en	When set, notifies RA to use special credits from HA to send CopyBack writes on CCIX Link 1 NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[13:12]	lnk1_excl_resperr_value	Two bit value to override RespErr field of an exclusive response. Applicable only if lnk1_excl_resperr_ovrd bit is set. NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	2'b0
[11]	lnk1_excl_resperr_ovrd	When set, overrides the RespErr field of exclusive response with the lnk1_excl_resperr_value field NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[10]	lnk1_excl_store_dwngrd	When set, downgrades shareable exclusive store to shareable store when sending on CCIX Link 1 NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[9]	lnk1_excl_load_dwngrd	When set, downgrades shareable exclusive load to shareable load when sending on CCIX Link 1 NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[8]	lnk1_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 1 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0

Bits	Name	Description	Type	Reset
[7:4]	lnk1_num_snpcrds	<p>Controls the number of CCIX snoop credits assigned to Link 1</p> <p>4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned</p>	RW	4'b0
[3]	lnk1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 1	RW	1'b0
[2]	lnk1_link_up	<p>Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent</p> <p>1'b0 Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1 Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent</p>	RW	1'b0
[1]	lnk1_link_req	<p>Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent</p> <p>1'b0 Link Down request 1'b1 Link Up request</p> <p>The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state.</p>	RW	1'b0
[0]	lnk1_link_en	Enables CCIX Link 1 when set	RW	1'b0
		1'b0 Link is disabled 1'b1 Link is enabled		

4.3.3.21 por_ccg_ra_ccprtcl_link1_status

Functions as the CXRA CCIX Protocol Link 1 status register. Works with por_ccg_ra_ccprtcl_link1_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C18

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-56: por_ccg_ra_ccprtcl_link1_status

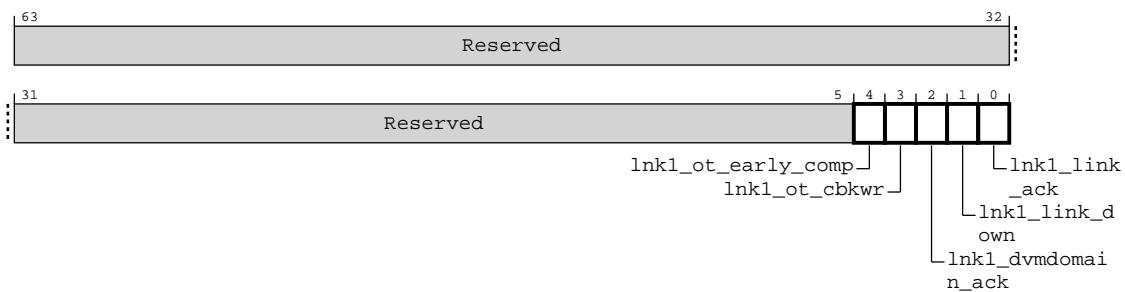


Table 4-72: por_ccg_ra_ccprtcl_link1_status attributes

Bits	Name	Description	Type	Reset
[63:5]	Reserved	Reserved	RO	-
[4]	Lnk1_ot_early_comp	Set, if there is an outstanding request for which early completion has been given for CCIX Link1	RO	1'b0
[3]	Lnk1_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link1	RO	1'b0
[2]	Lnk1_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 1	RO	1'b0
[1]	Lnk1_link_down	<p>Link Down status; hardware updates this register bit to indicate Link Down status</p> <p>1'b0 Link is not Down; hardware clears Link_DN when it receives a Link Up request</p> <p>1'b1 Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear</p>	RO	1'b1
[0]	Lnk1_link_ack	<p>Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request</p> <p>1'b0 Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear</p> <p>1'b1 Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent</p> <p>NOTE: The local agent must clear Link_DN before setting Link_ACK.</p>	RO	1'b0

4.3.3.22 por_ccg_ra_ccprtcl_link2_ctl

Functions as the CXRA CCIX Protocol Link 2 control register. Works with por_ccg_ra_ccprtcl_link2_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C20

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-57: por_ccg_ra_ccprtcl_link2_ctl

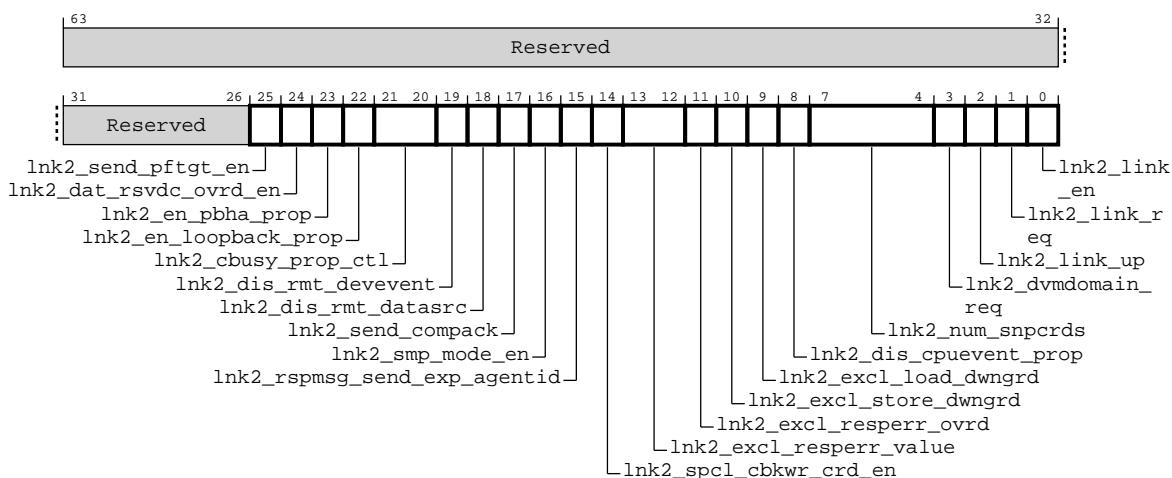


Table 4-73: por_ccg_ra_ccprtcl_link2_ctl attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[25]	lnk2_send_pftgt_en	When set, enables sending Prefetch Target (CHI) over link 2. Note: This field is not-applicable in CXL mode for link2	RW	1'b1
[24]	lnk2_dat_rsvdc_ovrd_en	When set, overrides CHI DAT RSVDC field with dat rsvdc strap input for incoming data on CCIX Link 2. Note: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode)	RW	1'b0
[23]	lnk2_en_pbha_prop	When set, enables propagation of PBHA on CCIX Link 2.	RW	1'b1
[22]	lnk2_en_loopback_prop	When set, enables propagation of LoopBack on CCIX Link 2.	RW	1'b1
[21:20]	lnk2_cbusy_prop_ctl	<p>Controls the propagation of Cbusy field for CCIX Link 2.</p> <p>2'b00 Send RA Cbusy on all responses based on the limits programmed in por_ccg_ra_cbusy_limit_ctl</p> <p>2'b01 Pass through remote CBusy on late completion responses (CompData, Comp)</p> <p>2'b10 Greater of RA Cbusy or remote Cbusy. Applicable to responses where remote Cbusy can be sent</p> <p>NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)</p>	RW	2'b0
[19]	lnk2_dis_rmt_devevent	When set, disables propagation of remote Dev Event field for CCIX Link 2. NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[18]	lnk2_dis_rmt_datasrc	When set, disables propagation of remote data source for CCIX Link 2. NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[17]	lnk2_send_compack	When set, sends CompAck for CCIX Link 2.	RW	1'b0
[16]	lnk2_smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode for CCIX Link 2.	RW	Configuration dependent
[15]	lnk2_rspmsg_send_exp_agentid	When set sends Expanded Agent ID on CCIX Response Messages for CCIX Link 2	RW	1'b0
[14]	lnk2_spcl_cbkwr_crd_en	When set, notifies RA to use special credits from HA to send CopyBack writes on CCIX Link 2 NOTE: This field is applicable only if the link programmed for SMP mode (i.e. SMP Mode enable bit is set)	RW	1'b0
[13:12]	lnk2_excl_resperr_value	Two bit value to override RespErr field of an exclusive response. Applicable only if lnk2_excl_resperr_ovrd bit is set. NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	2'b0
[11]	lnk2_excl_resperr_ovrd	When set, overrides the RespErr field of exclusive response with the lnk2_excl_resperr_value field NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[10]	lnk2_excl_store_dwngrd	When set, downgrades shareable exclusive store to shareable store when sending on CCIX Link 2 NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0
[9]	lnk2_excl_load_dwngrd	When set, downgrades shareable exclusive load to shareable load when sending on CCIX Link 2 NOTE: This field is applicable only when SMP Mode enable bit is clear (i.e. Non-SMP mode) and must only be used if the corresponding link end pair does not support exclusive monitoring	RW	1'b0

Bits	Name	Description	Type	Reset
[8]	lnk2_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 2 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0
[7:4]	lnk2_num_snpcrds	Controls the number of CCIX snoop credits assigned to Link 2 4'h0 Total credits are equally divided across all links 4'h1 25% of credits assigned 4'h2 50% of credits assigned 4'h3 75% of credits assigned 4'h4 100% of credits assigned 4'hF 0% of credits assigned	RW	4'b0
[3]	lnk2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 2	RW	1'b0
[2]	lnk2_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0 Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1 Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
[1]	lnk2_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0 Link Down request 1'b1 Link Up request The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state.	RW	1'b0
[0]	lnk2_link_en	Enables CCIX Link 2 when set 1'b0 Link is disabled 1'b1 Link is enabled	RW	1'b0

4.3.3.23 por_ccg_ra_ccprtcl_link2_status

Functions as the CXRA CCIX Protocol Link 2 status register. Works with por_ccg_ra_ccprtcl_link2_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C28

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-58: por_ccg_ra_ccprtcl_link2_status

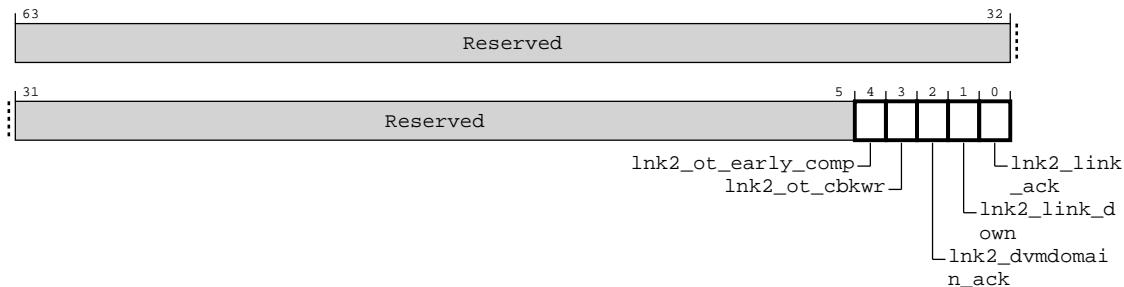


Table 4-74: por_ccg_ra_ccprtcl_link2_status attributes

Bits	Name	Description	Type	Reset
[63:5]	Reserved	Reserved	RO	-
[4]	Lnk2_ot_early_comp	Set, if there is an outstanding request for which early completion has been given for CCIX Link2	RO	1'b0
[3]	Lnk2_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link2	RO	1'b0
[2]	Lnk2_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 2	RO	1'b0
[1]	Lnk2_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0 Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1 Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1

Bits	Name	Description	Type	Reset
[0]	lnk2_link_ack	<p>Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request</p> <p>1'b0 Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear</p> <p>1'b1 Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent</p> <p>NOTE: The local agent must clear Link_DN before setting Link_ACK.</p>	RO	1'b0

4.3.4 CCLA register descriptions

This section lists the CCLA registers.

4.3.4.1 por_ccla_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-59: por_ccla_node_info

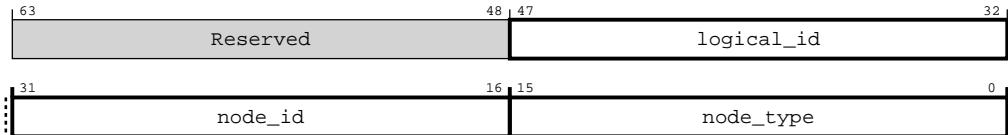


Table 4-75: por_ccla_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0105

4.3.4.2 por_ccla_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-60: por_ccla_child_info

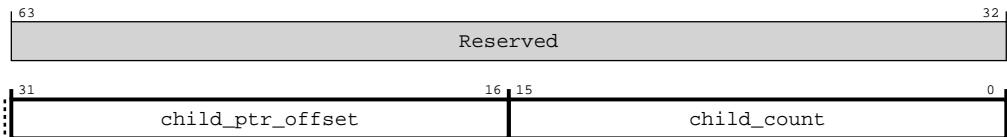


Table 4-76: por_ccla_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.4.3 por_ccla_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h988

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-61: por_ccla_secure_register_groups_override

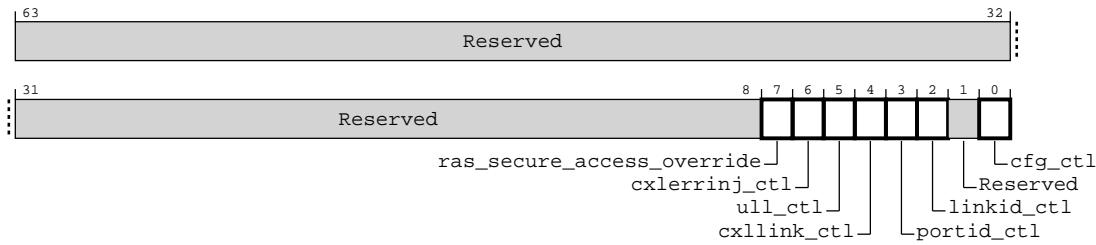


Table 4-77: por_ccla_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7]	ras_secure_access_override	Allow Non-secure access to Secure RAS registers	RW	1'b0
[6]	cxlerrinj_ctl	Allows Non-secure access to Secure CXL error injection registers	RW	1'b0
[5]	ull_ctl	Allows Non-secure access to Secure upper link layer control registers	RW	1'b0
[4]	cxllink_ctl	Allows Non-secure access to Secure CXL link layer registers	RW	1'b0
[3]	portid_ctl	Allows Non-secure access to Secure LA Port ID registers	RW	1'b0
[2]	linkid_ctl	Allows Non-secure access to Secure LA Link ID registers	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

4.3.4.4 por_ccla_unit_info

Provides component identification information for CCLA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h910

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-62: por_ccla_unit_info

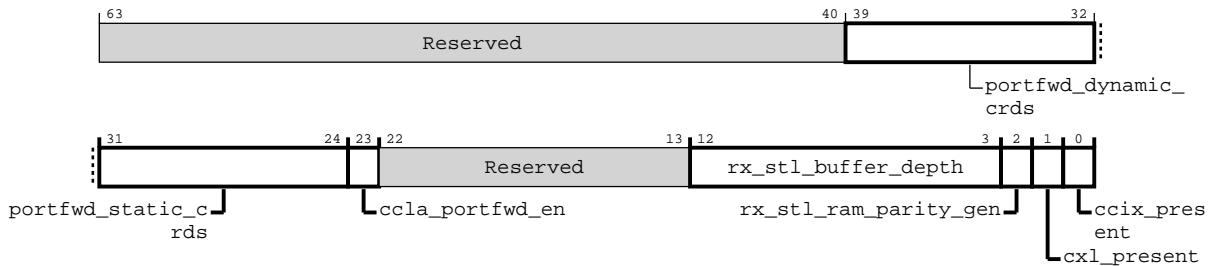


Table 4-78: por_ccla_unit_info attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	portfwd_dynamic_crds	Number of dynamic credits granted by this CCLA port for port forwarded traffic	RO	Configuration dependent
[31:24]	portfwd_static_crds	Number of static credits granted by this CCLA port for port forwarded traffic	RO	Configuration dependent
[23]	ccla_portfwd_en	Port forwarding is enabled at this CCLA port	RO	Configuration dependent
[22:13]	Reserved	Reserved	RO	-
[12:3]	rx_stl_buffer_depth	Depth of CCL stalling channel RX buffer for CXS RSP with data messages	RO	Configuration dependent
[2]	rx_stl_ram_parity_gen	Option to generate parity bits for the RX STL buffer	RO	Configuration dependent
[1]	cxl_present	Option to generate CXL support over CXS	RO	Configuration dependent
[0]	ccix_present	Option to generate CCIX support over CXS	RO	Configuration dependent

4.3.4.5 por_ccla_cfg_ctl

Functions as the configuration control register for CCLA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16' hB00

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-63: por_ccla_cfg_ctl

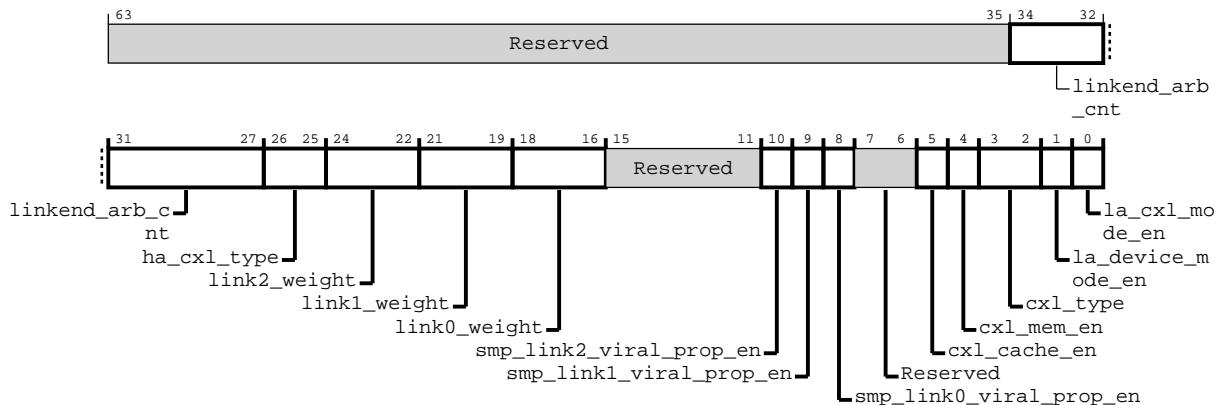


Table 4-79: por_ccla_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:35]	Reserved	Reserved	RO	-
[34:27]	linkend_arb_cnt	The count for how long each linkend is selected during linkend arbitration. If linkend_arb_cnt=8, each linkend is active for 8 cycles before switching to the next linkend	RW	8'h10
[26:25]	ha_cxl_type	Used to program CXL Type for HA 2'b00 Reserved 2'b01 Type1 2'b10 Type2 2'b11 Type3	RW	2'b01
[24:22]	link2_weight	Determines weight of link2 in CCL linkend arbitration	RW	3'b001
[21:19]	link1_weight	Determines weight of link1 in CCL linkend arbitration	RW	3'b001
[18:16]	link0_weight	Determines weight of link0 in CCL linkend arbitration	RW	3'b001

Bits	Name	Description	Type	Reset
[15:11]	Reserved	Reserved	RO	-
[10]	smp_link2_viral_prop_en	When set, enables viral propagation on SMP link2	RW	1'b0
[9]	smp_link1_viral_prop_en	When set, enables viral propagation on SMP link1	RW	1'b0
[8]	smp_link0_viral_prop_en	When set, enables viral propagation on SMP link0	RW	1'b0
[7:6]	Reserved	Reserved	RO	-
[5]	cxl_cache_en	Enable CXL .cache mode, by default is disabled	RW	1'b0
[4]	cxl_mem_en	Enable CXL .mem mode, by default is enabled	RW	1'b1
[3:2]	cxl_type	Used to program CXL Type for RA	RW	2'b11
		2'b00 Reserved 2'b01 Type1 2'b10 Type2 2'b11 Type3		
[1]	la_device_mode_en	Enable the Device mode, by default set to Host mode	RW	1'b0
[0]	la_cxl_mode_en	When set enables CXL mode	RW	1'b0

4.3.4.6 por_ccla_aux_ctl

Functions as the auxiliary control register for CCLA.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hB08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-64: por_ccla_aux_ctl

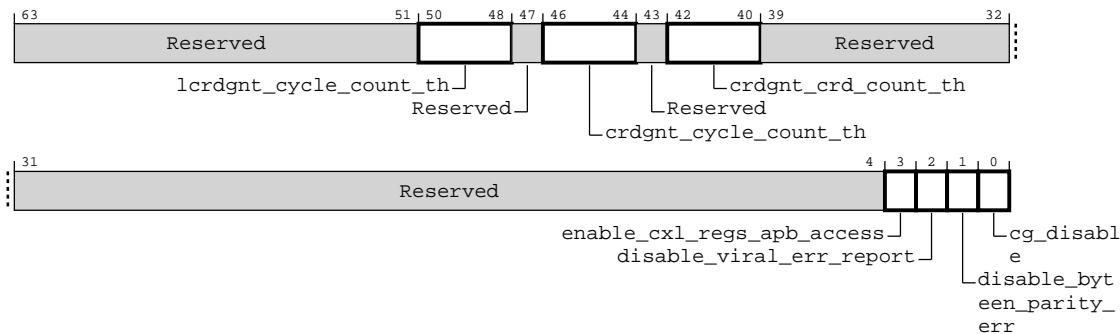


Table 4-80: por_ccla_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:51]	Reserved	Reserved	RO	-
[50:48]	lcrdgnt_cycle_count_th	Maximum number of cycles that need to be elapsed since previous piggyback credits were sent, to send a link credit grant message	RW	3'b001
	3'b000	8 cycles		
	3'b001	16 cycles		
	3'b010	32 cycles		
	3'b011	64 cycles		
[47]	Reserved	Reserved	RO	-
[46:44]	crdgnt_cycle_count_th	Maximum number of cycles that need to be elapsed since previous piggyback credits were sent, to send a protocol (Req, Dat, Snp..) credit grant message	RW	3'b010
	3'b000	32 cycles		
	3'b001	64 cycles		
	3'b010	128 cycles		
	3'b011	256 cycles		
[43]	Reserved	Reserved	RO	-
[42:40]	crdgnt_crd_count_th	Maximum number of protocol credits (i.e. Req, Dat, Snp..) that need to be accumulated to send a credit grant message	RW	3'b010
	3'b000	16 cycles		
	3'b001	32 cycles		
	3'b010	64 cycles		
	3'b011	128 cycles		
[39:4]	Reserved	Reserved	RO	-
[3]	enable_cxl_regs_apb_access	When set, Enables the APB access to the CXL registers and Disables the CMN access	RW	1'b0
[2]	disable_viral_err_report	When set, disables viral error reporting through CMN's error reporting mechanism	RW	1'b1
[1]	disable_byteen_parity_err	Disables CCLA RX RAM byte enable parity errors	RW	1'b0
[0]	cg_disable	Disables CCLA architectural clock gates	RW	1'b0

4.3.4.7 por_ccla_ccix_prop_capabilities

Contains CCIX-supported properties.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC00

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-65: por_ccla_ccix_prop_capabilities

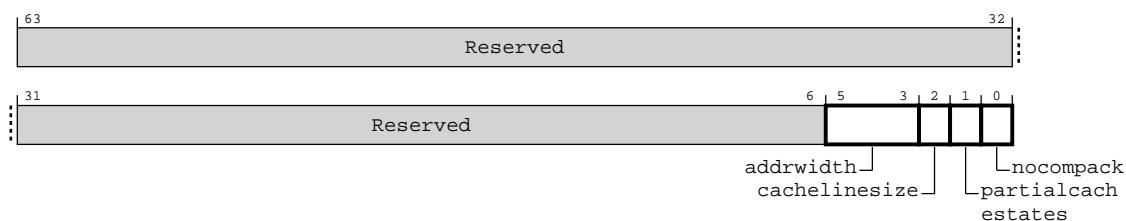


Table 4-81: por_ccla_ccix_prop_capabilities attributes

Bits	Name	Description	Type	Reset
[63:6]	Reserved	Reserved	RO	-
[5:3]	addrwidth	Address width supported 3'b000 48b 3'b001 52b 3'b010 56b 3'b011 60b 3'b100 64b	RO	3'b001

Bits	Name	Description	Type	Reset
[2]	cachelinesize	Cacheline size supported 1'b0 64B 1'b1 128B	RO	1'b0
[1]	partialcachestates	Partial cache states supported 1'b0 False 1'b1 True	RO	1'b0
[0]	nocompack	No CompAck supported 1'b0 False 1'b1 True	RO	1'b1

4.3.4.8 por_ccla_cxs_attr_capabilities

Contains CXS supported attributes.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC08

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-66: por_ccla_cxs_attr_capabilities

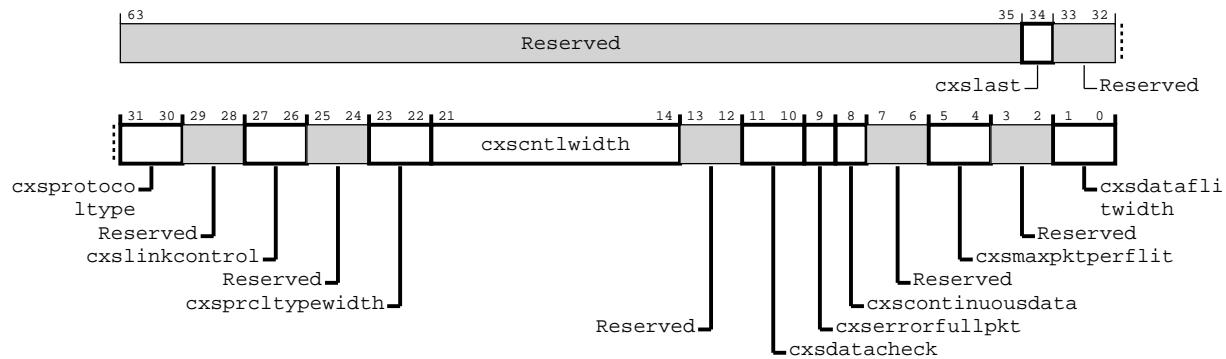


Table 4-82: por_ccla_cxs_attr_capabilities attributes

Bits	Name	Description	Type	Reset
[63:35]	Reserved	Reserved	RO	-
[34]	cxslast	CXS LAST signal is supported	RO	Configuration dependent
[33:32]	Reserved	Reserved	RO	-
[31:30]	cxsprotoctype	CXS Protocol type signal is supported	RO	Configuration dependent
[29:28]	Reserved	Reserved	RO	-
[27:26]	cxslinkcontrol	Set to Explicit Credit Return.	RO	Configuration dependent
[25:24]	Reserved	Reserved	RO	-
[23:22]	cxspctrltypewidth	Width of CXS TX/RX control	RO	Configuration dependent
[21:14]	cxscntlwidth	Width of CXS TX/RX control	RO	Configuration dependent
[13:12]	Reserved	Reserved	RO	-
[11:10]	cxsdatabflitwidth	CXS datacheck supported 2'b00 None 2'b01 Parity 2'b10 SECDED	RO	Configuration dependent
[9]	cxserrofullpkt	CXS error full packet supported 1'b0 False 1'b1 True	RO	Configuration dependent
[8]	cxsscontinuousdata	CXS continuous data supported 1'b0 False 1'b1 True	RO	Configuration dependent
[7:6]	Reserved	Reserved	RO	-
[5:4]	cxsmaxpktperflit	CXS maximum packets per flit supported 2'b00 2 2'b01 3 2'b10 4	RO	Configuration dependent
[3:2]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[1:0]	cxsdataflitwidth	CXS data flit width supported 2'b00 256b 2'b01 512b 2'b10 1024b	RO	2'b01

4.3.4.9 por_ccla_permmsg_pyld_0_63

Contains bits[63:0] of CCIX Protocol Error (PER) Message payload.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD00

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-67: por_ccla_permmsg_pyld_0_63

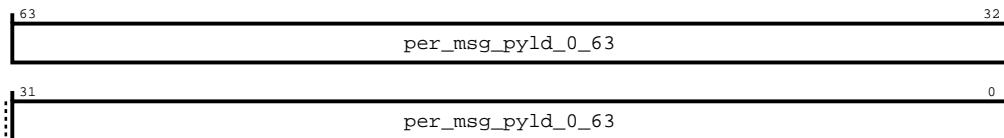


Table 4-83: por_ccla_permmsg_pyld_0_63 attributes

Bits	Name	Description	Type	Reset
[63:0]	per_msg_pyld_0_63	Protocol Error Msg Payload[63:0]	RW	64'b0

4.3.4.10 por_ccla_permmsg_pyld_64_127

Contains bits[127:64] of CCIX Protocol Error (PER) Message payload.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD08

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-68: por_ccla_permmsg_pyld_64_127

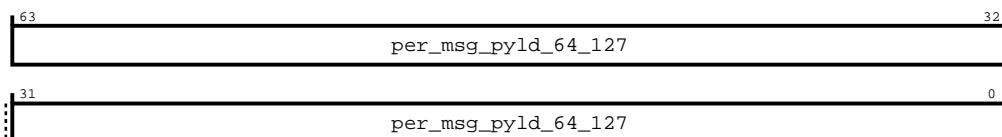


Table 4-84: por_ccla_permmsg_pyld_64_127 attributes

Bits	Name	Description	Type	Reset
[63:0]	per_msg_pyld_64_127	Protocol Error Msg Payload[127:64]	RW	64'b0

4.3.4.11 por_ccla_permmsg_pyld_128_191

Contains bits[192:128] of CCIX Protocol Error (PER) Message payload.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD10

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-69: por_ccla_permmsg_pyld_128_191

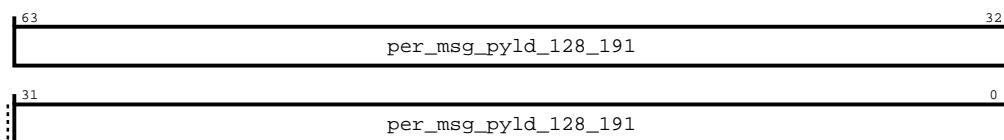


Table 4-85: por_ccla_permmsg_pyld_128_191 attributes

Bits	Name	Description	Type	Reset
[63:0]	per_msg_pyld_128_191	Protocol Error Msg Payload[191:128]	RW	64'b0

4.3.4.12 por_ccla_permmsg_pyld_192_255

Contains bits[255:192] of CCIX Protocol Error (PER) Message payload.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD18

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-70: por_ccla_permmsg_pyld_192_255

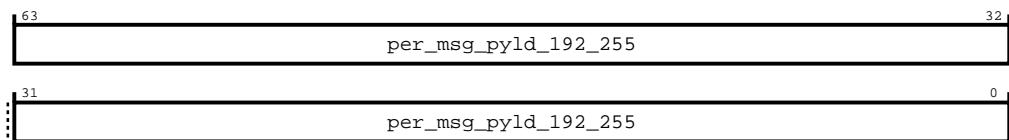


Table 4-86: por_ccla_permmsg_pyld_192_255 attributes

Bits	Name	Description	Type	Reset
[63:0]	per_msg_pyld_192_255	Protocol Error Msg Payload[255:192]	RW	64'b0

4.3.4.13 por_ccla_permmsg_ctl

Contains Control bits to trigger CCIX Protocol Error (PER) Message.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD20

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-71: por_ccla_permmsg_ctl

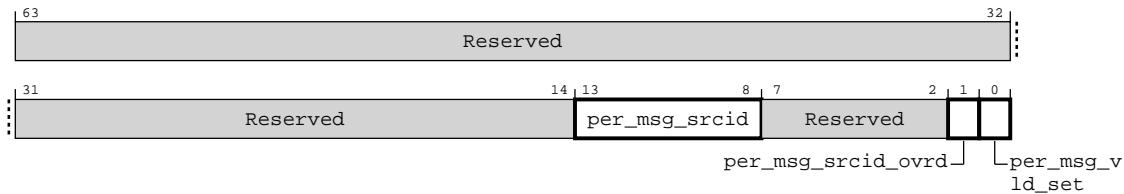


Table 4-87: por_ccla_permmsg_ctl attributes

Bits	Name	Description	Type	Reset
[63:14]	Reserved	Reserved	RO	-
[13:8]	per_msg_srcid	Contains Source ID used on CCIX Protocol Error Msg. Used when per_msg_srcid_ovrd is set.	RW	6'b0
[7:2]	Reserved	Reserved	RO	-
[1]	per_msg_srcid_ovrd	When set, overrides the Source ID on Protocol Error Msg by value specified in this register. Or else the source ID from payload[55:48] is used.	RW	1'b0
[0]	per_msg_vld_set	When set, sends CCIX Protocol Error Msg. Must be cleared after the current error is processed and before a new error message is triggered	RW	1'b0

4.3.4.14 por_ccla_err_agent_id

Contains Error Agent ID. Must be programmed by CCIX discovery s/w. Used as TargetID on CCIX Protocol Error (PER) Message.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD28

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-72: por_ccla_err_agent_id

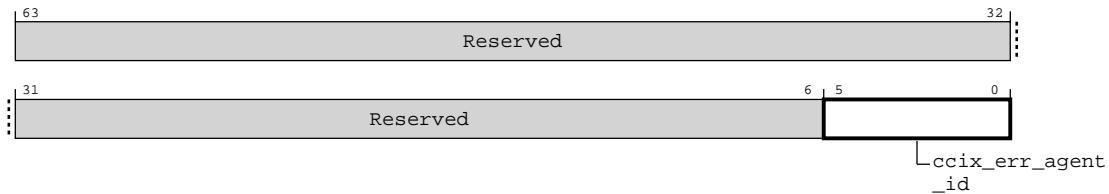


Table 4-88: por_ccla_err_agent_id attributes

Bits	Name	Description	Type	Reset
[63:6]	Reserved	Reserved	RO	-
[5:0]	ccix_err_agent_id	CCIX Error AgentID	RW	6'b0

4.3.4.15 por_ccla_agentid_to_portid_reg0

Specifies the mapping of Agent ID to Port ID for Agent IDs 0 to 7.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD30

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-73: por_ccla_agentid_to_portid_reg0

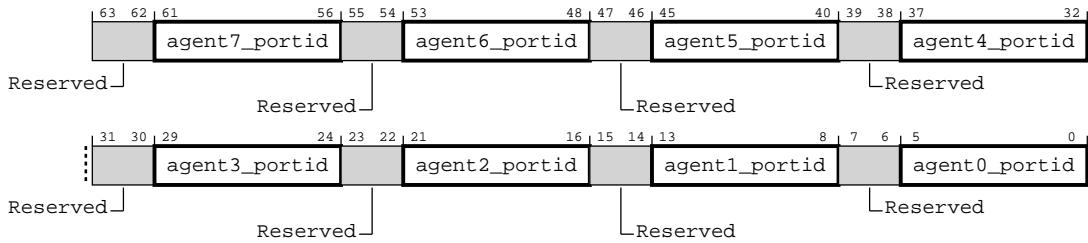


Table 4-89: por_ccla_agentid_to_portid_reg0 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent7_portid	Specifies the Port ID for Agent ID 7	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent6_portid	Specifies the Port ID for Agent ID 6	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent5_portid	Specifies the Port ID for Agent ID 5	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent4_portid	Specifies the Port ID for Agent ID 4	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent3_portid	Specifies the Port ID for Agent ID 3	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent2_portid	Specifies the Port ID for Agent ID 2	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent1_portid	Specifies the Port ID for Agent ID 1	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent0_portid	Specifies the Port ID for Agent ID 0	RW	6'h0

4.3.4.16 por_ccla_agentid_to_portid_reg1

Specifies the mapping of Agent ID to Port ID for Agent IDs 8 to 15.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD38

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-74: por_ccla_agentid_to_portid_reg1

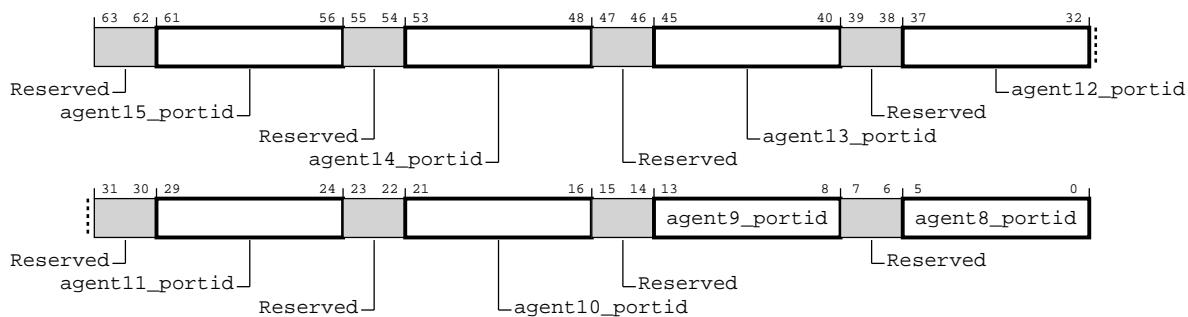


Table 4-90: por_ccla_agentid_to_portid_reg1 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent15_portid	Specifies the Port ID for Agent ID 15	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent14_portid	Specifies the Port ID for Agent ID 14	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent13_portid	Specifies the Port ID for Agent ID 13	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent12_portid	Specifies the Port ID for Agent ID 12	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent11_portid	Specifies the Port ID for Agent ID 11	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent10_portid	Specifies the Port ID for Agent ID 10	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent9_portid	Specifies the Port ID for Agent ID 9	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent8_portid	Specifies the Port ID for Agent ID 8	RW	6'h0

4.3.4.17 por_ccla_agentid_to_portid_reg2

Specifies the mapping of Agent ID to Port ID for Agent IDs 16 to 23.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD40

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-75: por_ccla_agentid_to_portid_reg2

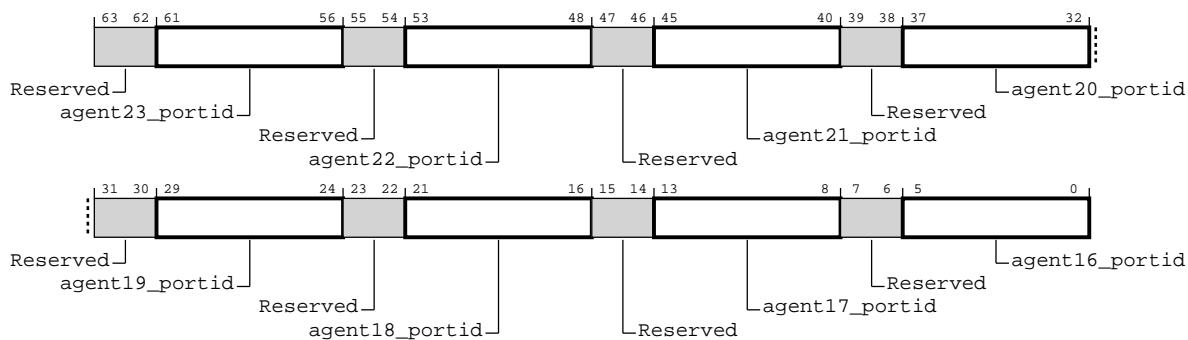


Table 4-91: por_ccla_agentid_to_portid_reg2 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent23_portid	Specifies the Port ID for Agent ID 23	RW	6'h0
[55:54]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[53:48]	agent22_portid	Specifies the Port ID for Agent ID 22	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent21_portid	Specifies the Port ID for Agent ID 21	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent20_portid	Specifies the Port ID for Agent ID 20	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent19_portid	Specifies the Port ID for Agent ID 19	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent18_portid	Specifies the Port ID for Agent ID 18	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent17_portid	Specifies the Port ID for Agent ID 17	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent16_portid	Specifies the Port ID for Agent ID 16	RW	6'h0

4.3.4.18 por_ccla_agentid_to_portid_reg3

Specifies the mapping of Agent ID to Port ID for Agent IDs 24 to 31.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD48

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-76: por_ccla_agentid_to_portid_reg3

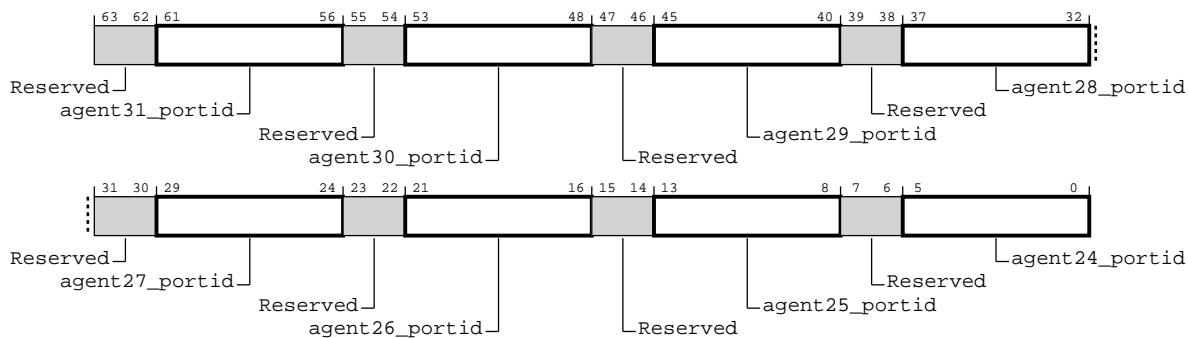


Table 4-92: por_ccla_agentid_to_portid_reg3 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent31_portid	Specifies the Port ID for Agent ID 31	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent30_portid	Specifies the Port ID for Agent ID 30	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent29_portid	Specifies the Port ID for Agent ID 29	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent28_portid	Specifies the Port ID for Agent ID 28	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent27_portid	Specifies the Port ID for Agent ID 27	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent26_portid	Specifies the Port ID for Agent ID 26	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent25_portid	Specifies the Port ID for Agent ID 25	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent24_portid	Specifies the Port ID for Agent ID 24	RW	6'h0

4.3.4.19 por_ccla_agentid_to_portid_reg4

Specifies the mapping of Agent ID to Port ID for Agent IDs 32 to 39.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16 'hD50

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-77: por_ccla_agentid_to_portid_reg4

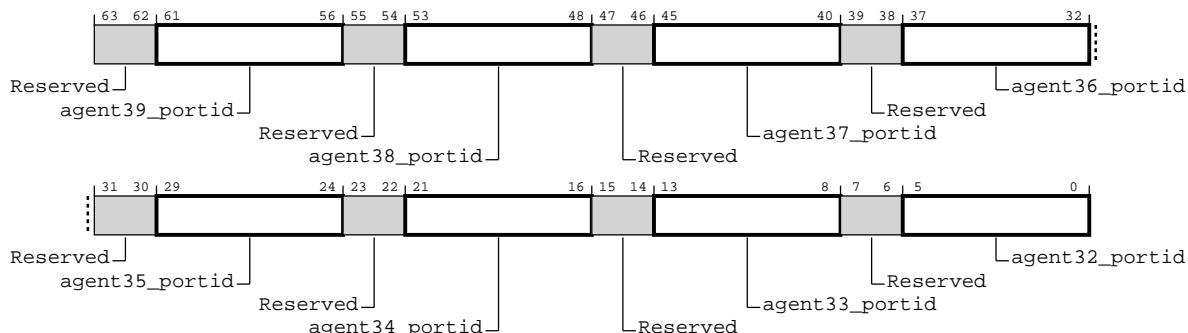


Table 4-93: por_ccla_agentid_to_portid_reg4 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent39_portid	Specifies the Port ID for Agent ID 39	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent38_portid	Specifies the Port ID for Agent ID 38	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent37_portid	Specifies the Port ID for Agent ID 37	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent36_portid	Specifies the Port ID for Agent ID 36	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent35_portid	Specifies the Port ID for Agent ID 35	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent34_portid	Specifies the Port ID for Agent ID 34	RW	6'h0
[15:14]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[13:8]	agent33_portid	Specifies the Port ID for Agent ID 33	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent32_portid	Specifies the Port ID for Agent ID 32	RW	6'h0

4.3.4.20 por_ccla_agentid_to_portid_reg5

Specifies the mapping of Agent ID to Port ID for Agent IDs 40 to 47.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD58

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-78: por_ccla_agentid_to_portid_reg5

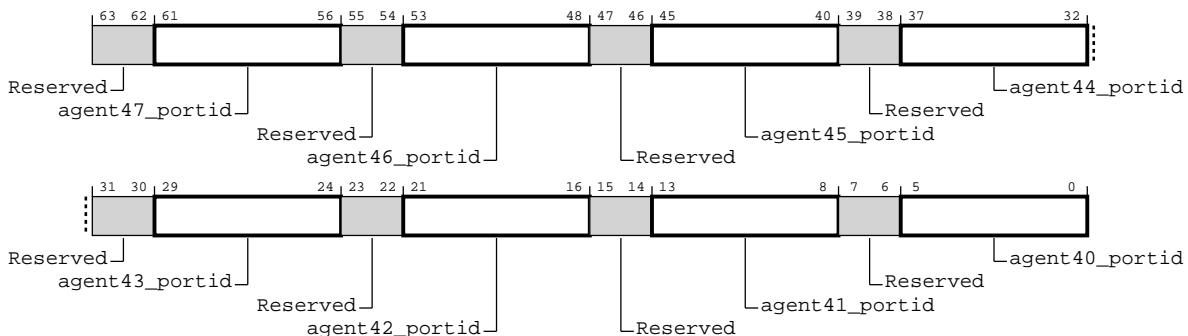


Table 4-94: por_ccla_agentid_to_portid_reg5 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent47_portid	Specifies the Port ID for Agent ID 47	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent46_portid	Specifies the Port ID for Agent ID 46	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent45_portid	Specifies the Port ID for Agent ID 45	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent44_portid	Specifies the Port ID for Agent ID 44	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent43_portid	Specifies the Port ID for Agent ID 43	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent42_portid	Specifies the Port ID for Agent ID 42	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent41_portid	Specifies the Port ID for Agent ID 41	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent40_portid	Specifies the Port ID for Agent ID 40	RW	6'h0

4.3.4.21 por_ccla_agentid_to_portid_reg6

Specifies the mapping of Agent ID to Port ID for Agent IDs 48 to 55.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD60

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-79: por_ccla_agentid_to_portid_reg6

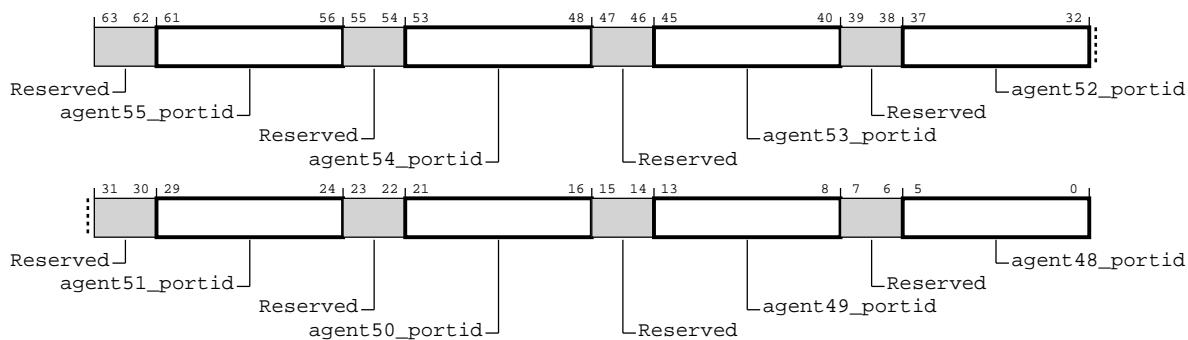


Table 4-95: por_ccla_agentid_to_portid_reg6 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent55_portid	Specifies the Port ID for Agent ID 55	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent54_portid	Specifies the Port ID for Agent ID 54	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent53_portid	Specifies the Port ID for Agent ID 53	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent52_portid	Specifies the Port ID for Agent ID 52	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent51_portid	Specifies the Port ID for Agent ID 51	RW	6'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent50_portid	Specifies the Port ID for Agent ID 50	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent49_portid	Specifies the Port ID for Agent ID 49	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent48_portid	Specifies the Port ID for Agent ID 48	RW	5'h0

4.3.4.22 por_ccla_agentid_to_portid_reg7

Specifies the mapping of Agent ID to Port ID for Agent IDs 56 to 63.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16 'hD68

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.portid_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-80: por_ccla_agentid_to_portid_reg7

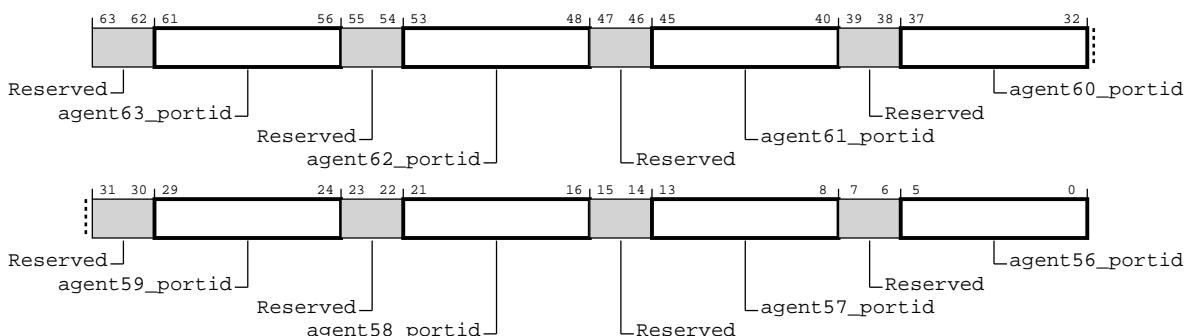


Table 4-96: por_ccla_agentid_to_portid_reg7 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	agent63_portid	Specifies the Port ID for Agent ID 63	RW	6'h0
[55:54]	Reserved	Reserved	RO	-
[53:48]	agent62_portid	Specifies the Port ID for Agent ID 62	RW	6'h0
[47:46]	Reserved	Reserved	RO	-
[45:40]	agent61_portid	Specifies the Port ID for Agent ID 61	RW	6'h0
[39:38]	Reserved	Reserved	RO	-
[37:32]	agent60_portid	Specifies the Port ID for Agent ID 60	RW	6'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	agent59_portid	Specifies the Port ID for Agent ID 59	RW	6'h0

Bits	Name	Description	Type	Reset
[23:22]	Reserved	Reserved	RO	-
[21:16]	agent58_portid	Specifies the Port ID for Agent ID 58	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	agent57_portid	Specifies the Port ID for Agent ID 57	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	agent56_portid	Specifies the Port ID for Agent ID 56	RW	6'h0

4.3.4.23 por_ccla_agentid_to_portid_val

Specifies which Agent ID to Port ID mappings are valid.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD70

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-81: por_ccla_agentid_to_portid_val

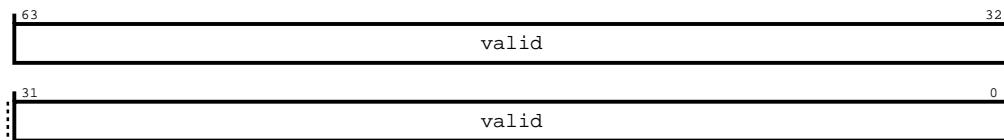


Table 4-97: por_ccla_agentid_to_portid_val attributes

Bits	Name	Description	Type	Reset
[63:0]	valid	Specifies whether the Port ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

4.3.4.24 por_ccla_portfwd_en

Functions as the Port-to-Port forwarding control register. Works with por_ccla_portfwd_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD78

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-82: por_ccla_portfwd_en

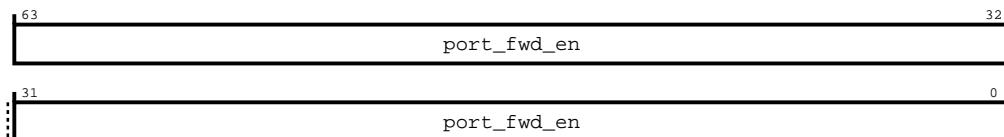


Table 4-98: por_ccla_portfwd_en attributes

Bits	Name	Description	Type	Reset
[63:0]	port_fwd_en	Bit vector, where each bit represents logical PortID of a Port (CCG) present on CMN. Each bit when set, enables Port-to-Port forwarding with the corresponding port. 1'b0 Port-to-Port forwarding is disabled 1'b1 Port-to-Port forwarding is enabled	RW	64'b0

4.3.4.25 por_ccla_portfwd_status

Functions as the Port-to-Port forwarding status register. Works with por_ccla_portfwd_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD80

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-83: por_ccla_portfwd_status

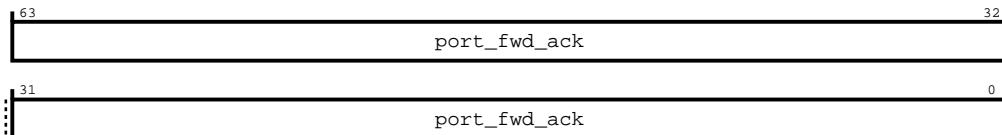


Table 4-99: por_ccla_portfwd_status attributes

Bits	Name	Description	Type	Reset
[63:0]	port_fwd_ack	Bit vector, where each bit represents logical PortID of a Port (CCG) present on CMN. Each bit represents the status of the port-to-port control request sent to the corresponding port. 1'b0 Port-to-Port forwarding channel is de-active. 1'b1 Port-to-Port forwarding channel is active	RO	64'b0

4.3.4.26 por_ccla_portfwd_req

Functions as the Port-to-Port forwarding control register. Works with por_ccla_portfwd_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD88

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-84: por_ccla_portfwd_req

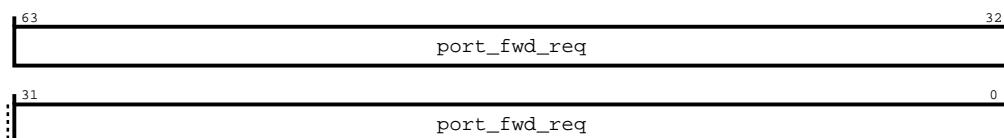


Table 4-100: por_ccla_portfwd_req attributes

Bits	Name	Description	Type	Reset
[63:0]	port_fwd_req	Bit vector, where each bit represents logical PortID of a Port (CCG) present on CMN. Each bit is used to control the communication channel with the corresponding port. 1'b0 Port-to-Port forwarding channel de-activate request 1'b1 Port-to-Port forwarding channel activate request	RW	64'b0

4.3.4.27 por_ccla_linkid_to_hops

Specifies number of portforward hops for the linkid.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16 'hD90

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.portid_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-85: por_ccla_linkid_to_hops

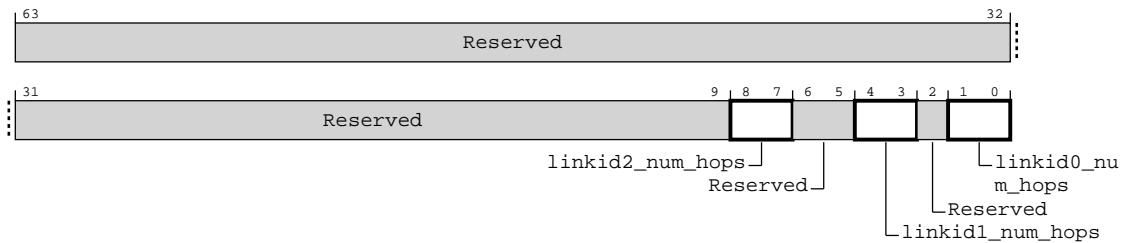


Table 4-101: por_ccla_linkid_to_hops attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8:7]	linkid2_num_hops	Specifies the number of portforward hops for linkid2	RW	2'b00
[6:5]	Reserved	Reserved	RO	-
[4:3]	linkid1_num_hops	Specifies the number of portforward hops for linkid1	RW	2'b00
[2]	Reserved	Reserved	RO	-
[1:0]	linkid0_num_hops	Specifies the number of portforward hops for linkid0	RW	2'b00

4.3.4.28 por_ccla_cxl_link_rx_credit_ctl

CXL Link Rx Credit Control Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE00

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-86: por_ccla_cxl_link_rx_credit_ctl

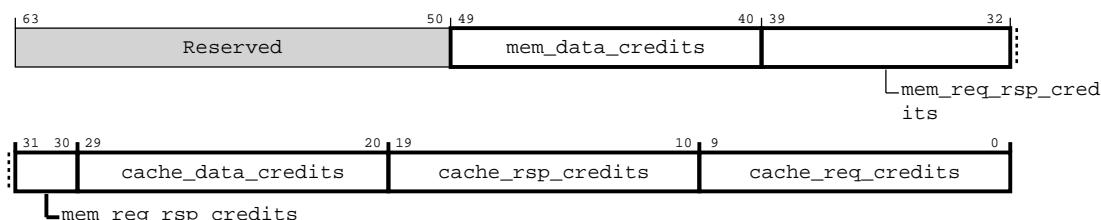


Table 4-102: por_ccla_cxl_link_rx_credit_ctl attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	mem_data_credits	Credits to advertise for Mem Data channel at init	RW	Configuration dependent
[39:30]	mem_req_rsp_credits	Credits to advertise for Mem Request or Response channel at init	RW	Configuration dependent
[29:20]	cache_data_credits	Credits to advertise for Cache Data channel at init	RW	Configuration dependent
[19:10]	cache_rsp_credits	Credits to advertise for Cache Response channel at init	RW	Configuration dependent
[9:0]	cache_req_credits	Credits to advertise for Cache Request channel at init	RW	Configuration dependent

4.3.4.29 por_ccla_cxl_link_rx_credit_return_stat

CXL Link Rx Credit Return Status Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE08

Type

RO

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-87: por_ccla_cxl_link_rx_credit_return_stat

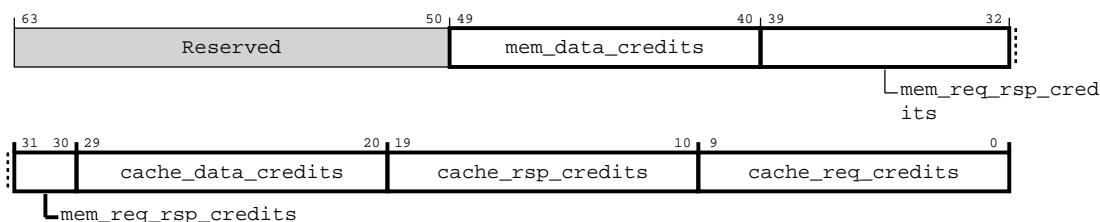


Table 4-103: por_ccla_cxl_link_rx_credit_return_stat attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	mem_data_credits	Running snapshot of accumulated Mem Data credits to be returned	RO	10'b0
[39:30]	mem_req_rsp_credits	Running snapshot of accumulated Mem Request or Response credits to be returned	RO	10'b0
[29:20]	cache_data_credits	Running snapshot of accumulated Cache Data credits to be returned	RO	10'b0
[19:10]	cache_rsp_credits	Running snapshot of accumulated Cache Response credits to be returned	RO	10'b0
[9:0]	cache_req_credits	Running snapshot of accumulated Cache Request credits to be returned	RO	10'b0

4.3.4.30 por_ccla_cxl_link_tx_credit_stat

CXL Link Tx Credit Status Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE10

Type

RO

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-88: por_ccla_cxl_link_tx_credit_stat

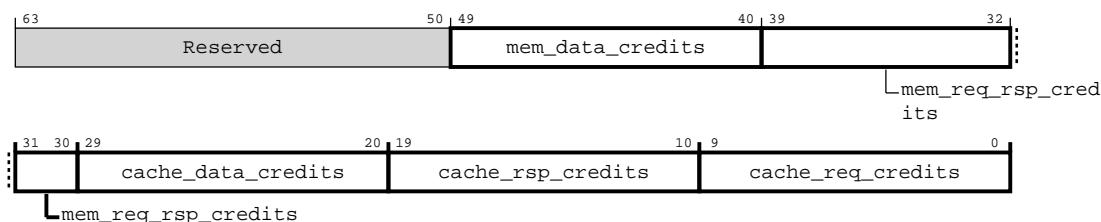


Table 4-104: por_ccla_cxl_link_tx_credit_stat attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	mem_data_credits	Running snapshot of accumulated Mem Data credits for TX	RO	10'b0
[39:30]	mem_req_rsp_credits	Running snapshot of accumulated Mem Request or Response credits for TX	RO	10'b0
[29:20]	cache_data_credits	Running snapshot of accumulated Cache Data credits for TX	RO	10'b0
[19:10]	cache_rsp_credits	Running snapshot of accumulated Cache Response credits for TX	RO	10'b0
[9:0]	cache_req_credits	Running snapshot of accumulated Cache Request credits for TX	RO	10'b0

4.3.4.31 por_ccla_cxl_security_policy

Contains CXL Security Policy

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE50

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-89: por_ccla_cxl_security_policy

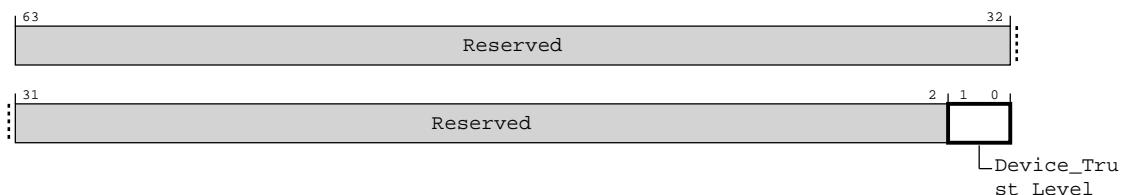


Table 4-105: por_ccla_cxl_security_policy attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	Device_Trust_Level	0 --> Trusted CXL Device. At this setting a CXL Device will be able to get access on CXL.cache for both host-attached and device attached memory ranges. The Host can still protect security sensitive memory regions. '1 --> Trusted for Device Attached Memory Range Only. At this setting a CXL Device will be able to get access on CXL.cache for device attached memory ranges only. Requests on CXL.cache for host-attached memory ranges will be aborted by the Host. '2 --> Untrusted CXL Device. At this setting all requests on CXL.cache will be aborted by the Host. Please note that these settings only apply to requests on CXL.cache. The device can still source requests on CXL.io regardless of these settings. Protection on CXL.io will be implemented using IOMMU based page tables. Default value of this field is 2.	RW	2'h2

4.3.4.32 por_ccla_cxl_hdm_decoder_capability

Contains CXL_HDM_Decoder_Capability_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE78

Type

RO

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-90: por_ccla_cxl_hdm_decoder_capability

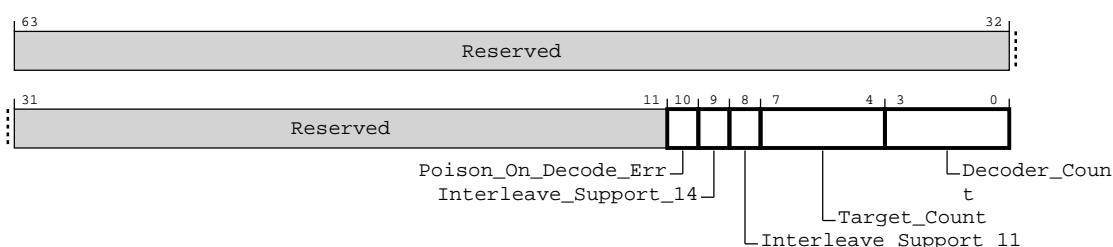


Table 4-106: por_ccla_cxl_hdm_decoder_capability attributes

Bits	Name	Description	Type	Reset
[63:11]	Reserved	Reserved	RO	-
[10]	Poison_On_Decode_Err	If set the component is capable of returning poison on read access to addresses that are not positively decoded by any HDM Decoders in this component. If clear the component is not capable of returning poison under such scenarios.	RO	1'h0

Bits	Name	Description	Type	Reset
[9]	Interleave_Support_14	If set the component supports interleaving based on Address bit 14 Address bit 13 and Address bit 12. Root ports and switches shall always set this bit indicating support for interleaving based on Address bits 14-12.	RO	1'h0
[8]	Interleave_Support_11	If set the component supports interleaving based on Address bit 11 Address bit 10 Address bit 9 and Address bit 8. Root Ports and Upstream Switch Ports shall always set this bit indicating support for interleaving based on Address bit 11-8.	RO	1'h0
[7:4]	Target_Count	The number of target ports each decoder supports (applicable to Upstream Switch Port and Root Port only). Maximum of 8. 1 1 target port 2 2 target ports 8 8 target ports Other Reserved	RO	4'h1
[3:0]	Decoder_Count	Reports the number of memory address decoders implemented by the component. 0 1 Decoder 1 2 Decoders 2 4 Decoders 3 6 Decoders 4 8 Decoders 5 10 Decoders Others Reserved	RO	4'h0

4.3.4.33 por_ccla_cxl_hdm_decoder_global_control

Contains CXL_HDM_Decoder_Global_Control_Register . Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE80

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-91: por_ccla_cxl_hdm_decoder_global_control

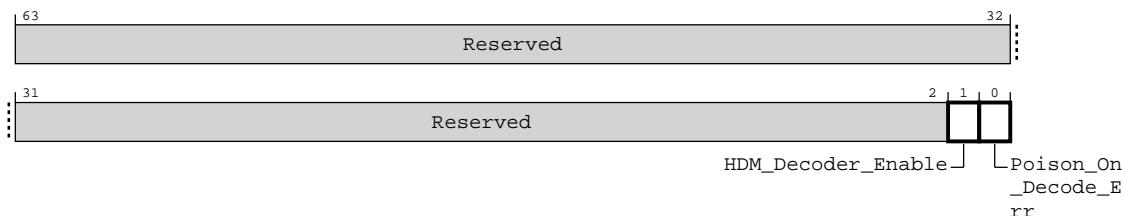


Table 4-107: por_ccla_cxl_hdm_decoder_global_control attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	HDM_Decoder_Enable	This bit is only applicable to CXL.mem devices and shall return 0 on Root Ports and Upstream Switch Ports. When this bit is set device shall use HDM decoders to decode CXL.mem transactions and not use HDM Base registers in DVSEC ID 0. Root Ports and Upstream Switch Ports always use HDM Decoders to decode CXL.mem transactions.	RW	1'h0
[0]	Poison_On_Decode_Error	This bit is RO and is hard-wired to 0 if Poison On Decode Error Capability=0. If set the component returns poison on read access to addresses that are not positively decoded by the component. If clear the component returns all 1s data without a poison under such scenarios.	RW	1'h0

4.3.4.34 por_ccla_cxl_hdm_decoder_0_base_low

Contains CXL_HDM_Decoder_0_Base_High_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE88

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-92: por_ccla_cxl_hdm_decoder_0_base_low

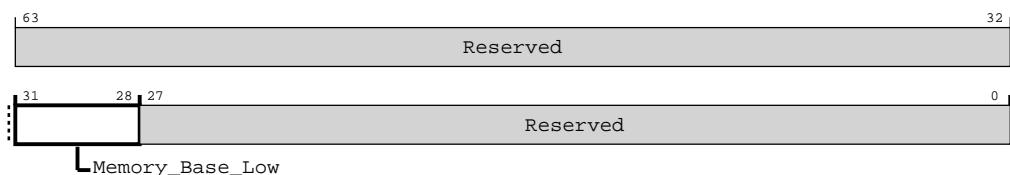


Table 4-108: por_ccla_cxl_hdm_decoder_0_base_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Base_Low	Corresponds to bits 31:28 of the base of the address range managed by decoder 0	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.4.35 por_ccla_cxl_hdm_decoder_0_base_high

Contains CXL_HDM_Decoder_0_Base_Low_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hE90`

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-93: por_ccla_cxl_hdm_decoder_0_base_high

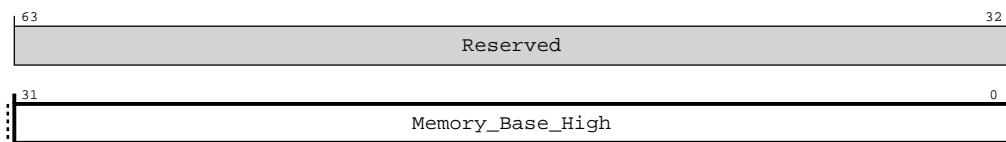


Table 4-109: por_ccla_cxl_hdm_decoder_0_base_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Base_High	Corresponds to bits 63:32 of the base of the address range managed by decoder 0.	RWL	32'h0

4.3.4.36 por_ccla_cxl_hdm_decoder_0_size_low

Contains CXL_HDM_Decoder_0_Size_Low_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE98

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-94: por_ccla_cxl_hdm_decoder_0_size_low

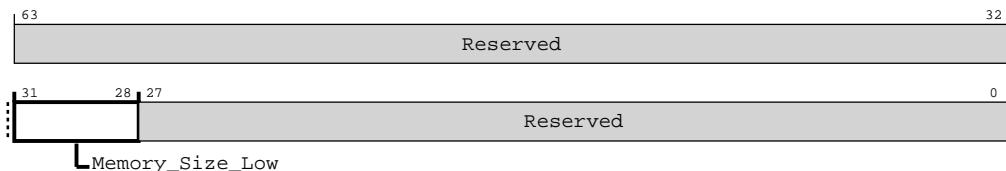


Table 4-110: por_ccla_cxl_hdm_decoder_0_size_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Size_Low	Corresponds to bits 31:28 of the size of the address range managed by decoder 0	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.4.37 por_ccla_cxl_hdm_decoder_0_size_high

Contains CXL_HDM_Decoder_0_Size_High_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEA0

Type

RWL

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-95: por_ccla_cxl_hdm_decoder_0_size_high

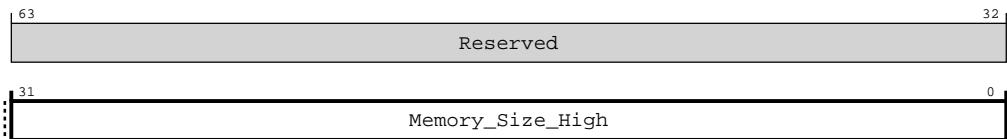


Table 4-111: por_ccla_cxl_hdm_decoder_0_size_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Size_High	Corresponds to bits 63:32 of the size of address range managed by decoder 0.	RWL	32'h0

4.3.4.38 por_ccla_cxl_hdm_decoder_0_control

Contains CXL_HDM_Decoder_0_Control_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEA8

Type

RWL

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-96: por_ccla_cxl_hdm_decoder_0_control

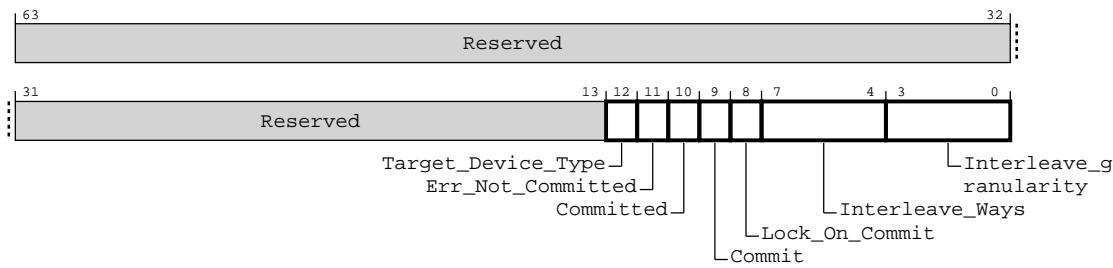


Table 4-112: por_ccla_cxl_hdm_decoder_0_control attributes

Bits	Name	Description	Type	Reset
[63:13]	Reserved	Reserved	RO	-
[12]	Target_Device_Type	0 Target is a CXL Type 2 Device 1 Target is a CXL Type 3 Device	RWL	1'h0
[11]	Err_Not_Committed	Indicates the decode programming had an error and decoder is not active.	RWL	1'h0
[10]	Committed	Indicates the decoder is active	RWL	1'h0
[9]	Commit	Software sets this to 1 to commit this decoder	RWL	1'h0
[8]	Lock_On_Commit	If set all RWL fields in Decoder 0 registers will become read only when Committed changes to 1.	RWL	1'h0
[7:4]	Interleave_Ways	The number of targets across which this memory range is interleaved. 0 - 1 way 1 - 2 way 2 - 4 way 3 - 8 way All other reserved	RWL	4'h0
[3:0]	Interleave_granularity	The number of consecutive bytes that are assigned to each target in the Target List. 0 256 Bytes 1 512 Bytes 2 1024 Bytes (1KB) 3 2048 Bytes (2KB) 4 4096 Bytes (4KB) 5 8192 Bytes (8 KB) 6 16384 Bytes (16 KB)	RWL	4'h0

4.3.4.39 por_ccla_cxl_hdm_decoder_0_dpa_skip_low

Contains CXL_HDM_Decoder_0_DPA_Skip_Low_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16 'hEC0

Type

RWL

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-97: por_ccla_cxl_hdm_decoder_0_dpa_skip_low

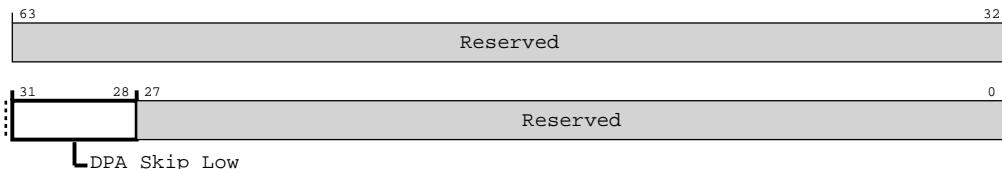


Table 4-113: por_ccla_cxl_hdm_decoder_0_dpa_skip_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	DPA_Skip_Low	Corresponds to bits 31:28 of the DPA Skip length which when non-zero specifies a length of DPA space that is skipped unmapped by any decoder prior to the HPA to DPA mapping provided by this decoder.	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.4.40 por_ccla_cxl_hdm_decoder_0_dpa_skip_high

Contains CXL_HDM_Decoder_0_DPA_Skip_High_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEC8

Type

RWL

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-98: por_ccla_cxl_hdm_decoder_0_dpa_skip_high

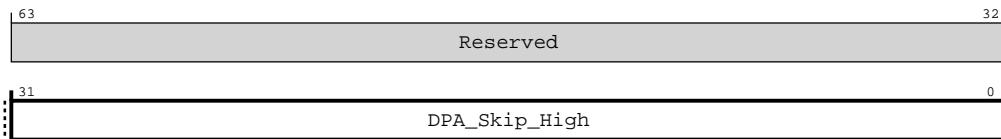


Table 4-114: por_ccla_cxl_hdm_decoder_0_dpa_skip_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	DPA_Skip_High	Corresponds to bits 63:32 of the DPA Skip length which when non-zero specifies a length of DPA space that is skipped unmapped by any decoder prior to the HPA to DPA mapping provided by this decoder.	RWL	32'h0

4.3.4.41 por_ccla_snoop_filter_group_id

Contains Snoop_Filter_Group_ID

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hED0

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-99: por_ccla_snoop_filter_group_id

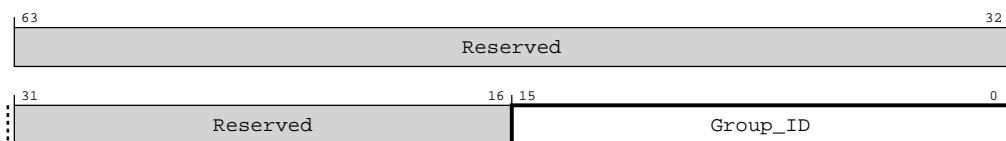


Table 4-115: por_ccla_snoop_filter_group_id attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	Group_ID	Uniquely identifies a snoop filter instance that is used to track CXL.cache devices below this Port. All Ports that share a single Snoop Filter instance shall set this field to the same value.	RW	16'h0

4.3.4.42 por_ccla_snoop_filter_effective_size

Contains Snoop_Filter_Effective_Size

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hED8

Type

RW

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-100: por_ccla_snoop_filter_effective_size

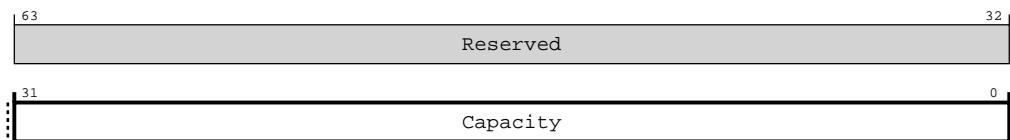


Table 4-116: por_ccla_snoop_filter_effective_size attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Capacity	Effective Snoop Filter Capacity representing the size of cache that can be effectively tracked by the Snoop Filter with this Group ID in multiples of 64K.	RW	32'h0

4.3.4.43 por_ccla_dvsec_cxl_range_1_base_high

Contains DVSEC_CXL_Range_1_Base_High. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEE0

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-101: por_ccla_dvsec_cxl_range_1_base_high

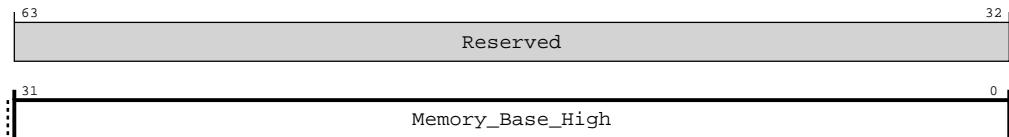


Table 4-117: por_ccla_dvsec_cxl_range_1_base_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Base_High	Corresponds to bits 63:32 of CXL Range 1 base in the host address space. Locked by CONFIG_LOCK. If a device implements CXL HDM Decoder Capability registers and software has enabled HDM Decoder by setting HDM Decoder Enable bit in CXL HDM Decoder Global Control register the value of this field is not used during address decode. It is recommended that software program this to match CXL HDM Decoder 0 Base High Register for backward compatibility reasons.	RWL	32'h0

4.3.4.44 por_ccla_dvsec_cxl_range_1_base_low

Contains DVSEC_CXL_Range_1_Base_Low. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEE8

Type

RWL

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-102: por_ccla_dvsec_cxl_range_1_base_low

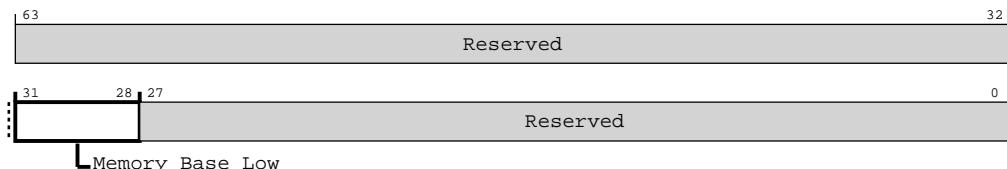


Table 4-118: por_ccla_dvsec_cxl_range_1_base_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Base_Low	Corresponds to bits 31:28 of CXL Range 1 base in the host address space. Locked by CONFIG_LOCK. If a device implements CXL HDM Decoder Capability registers and software has enabled HDM Decoder by setting HDM Decoder Enable bit in CXL HDM Decoder Global Control register the value of this field is not used during address decode. It is recommended that software program this to match CXL HDM Decoder 0 Base Low Register for backward compatibility reasons.	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.4.45 por_ccla_dvsec_cxl_range_2_base_high

Contains DVSEC_CXL_Range_2_Base_High. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEF0

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-103: por_ccla_dvsec_cxl_range_2_base_high

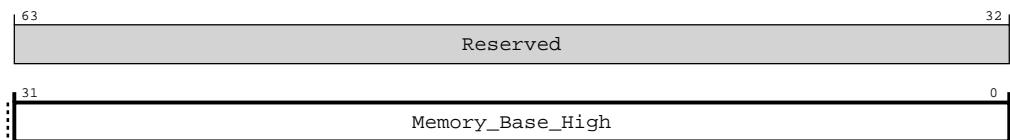


Table 4-119: por_ccla_dvsec_cxl_range_2_base_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Base_High	Corresponds to bits 63:32 of CXL Range 2 base in the host address space. Locked by CONFIG_LOCK. If a device implements CXL HDM Decoder Capability registers and software has enabled HDM Decoder by setting HDM Decoder Enable bit in CXL HDM Decoder Global Control register the value of this field is not used during address decode. It is recommended that software program this to match the corresponding CXL HDM Decoder Base High Register for backward compatibility reasons.	RWL	32'h0

4.3.4.46 por_ccla_dvsec_cxl_range_2_base_low

Contains DVSEC_CXL_Range_2_Base_Low. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hEF8`

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-104: por_ccla_dvsec_cxl_range_2_base_low

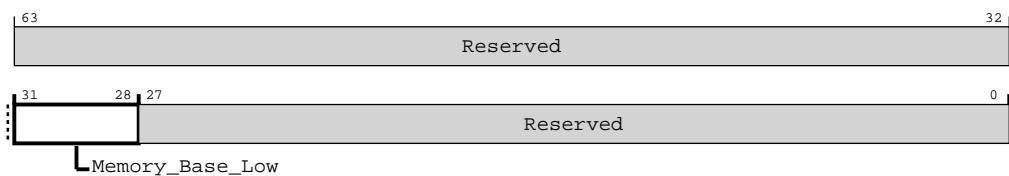


Table 4-120: por_ccla_dvsec_cxl_range_2_base_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Base_Low	Corresponds to bits 31:28 of CXL Range 2 base in the host address space. Locked by CONFIG_LOCK	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.4.47 por_ccla_dvsec_cxl_control

Contains DVSEC_CXL_Control. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF00

Type

RWL

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxllink_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-105: por_ccla_dvsec_cxl_control

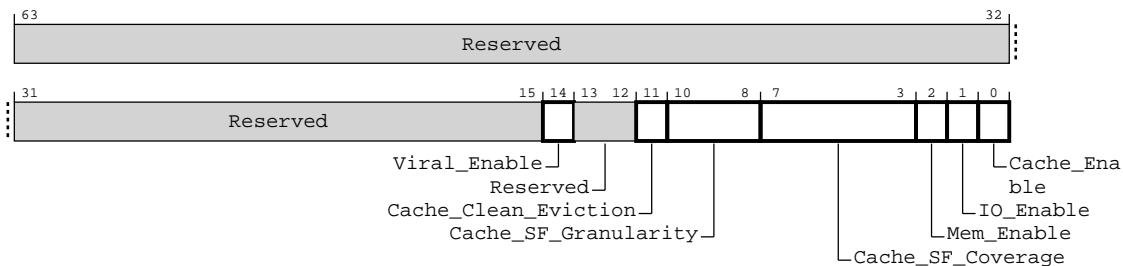


Table 4-121: por_ccla_dvsec_cxl_control attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14]	Viral_Enable	When set enables Viral handling in the CXL device. Locked by CONFIG_LOCK. If 0 the CXL device may ignore the viral that it receives	RWL	1'h0
[13:12]	Reserved	Reserved	RO	-
[11]	Cache_Clean_Eviction	Performance hint to the device. Locked by CONFIG_LOCK. 0 Indicates clean evictions from device caches are needed for best performance 1 Indicates clean evictions from device caches are NOT needed for best performance	RWL	1'h0
[10:8]	Cache_SF_Granularity	Performance hint to the device. Locked by CONFIG_LOCK. 000 Indicates 64B granular tracking on the Host 001 Indicates 128B granular tracking on the Host 010 Indicates 256B granular tracking on the Host 011 Indicates 512B granular tracking on the Host 100 Indicates 1KB granular tracking on the Host 101 Indicates 2KB granular tracking on the Host 110 Indicates 4KB granular tracking on the Host 111 Reserved	RWL	3'h0
[7:3]	Cache_SF_Coverage	Performance hint to the device. Locked by CONFIG_LOCK. 0x00: Indicates no Snoop Filter coverage on the Host For all other values of N: Indicates Snoop Filter coverage on the Host of 2^{N+15d} Bytes.	RWL	5'h0
[2]	Mem_Enable	When set enables CXL.mem protocol operation when in Flex Bus.CXL mode. Locked by CONFIG_LOCK.	RWL	1'h0
[1]	IO_Enable	When set enables CXL.io protocol operation when in Flex Bus.CXL mode.	RWL	1'h1
[0]	Cache_Enable	When set enables CXL.cache protocol operation when in Flex Bus.CXL mode. Locked by CONFIG_LOCK.	RWL	1'h0

4.3.4.48 por_ccla_dvsec_cxl_control2

Contains DVSEC_CXL_Control2. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF08

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-106: por_ccla_dvsec_cxl_control2

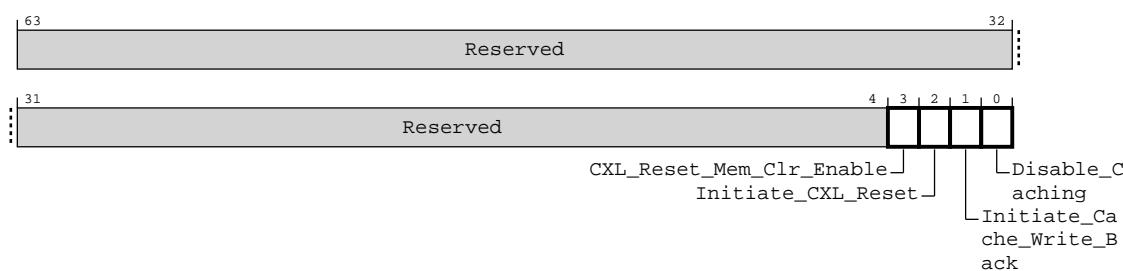


Table 4-122: por_ccla_dvsec_cxl_control2 attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	CXL_Reset_Mem_Clr_Enable	When set and CXL Reset Mem Clr Capable returns 1 Device shall clear or randomize volatile HDM ranges as part of the CXL Reset operation. When CXL Reset Mem Clr Capable is clear this bit is ignored and volatile HDM ranges may or may not be cleared or randomized during CXL Reset.	RW	1'h0
[2]	Initiate_CXL_Reset	When set to 1 device shall initiate CXL Reset as defined in Section 9.7. This bit always returns the value of 0 when read by the software. A write of 0 is ignored.	RW	1'h0

Bits	Name	Description	Type	Reset
[1]	Initiate_Cache_Write_Back	When set to 1 device shall write back all modified lines in the local cache and invalidate all lines. The device shall send CacheFlushed message to host as required by CXL.Cache protocol to indicate it does not hold any modified lines.	RW	1'h0
[0]	Disable_Caching	When set to 1 device shall no longer cache new modified lines in its local cache. Device shall continue to correctly respond to CXL.cache transactions.	RW	1'h0

4.3.4.49 por_ccla_dvsec_cxl_lock

Contains DVSEC_CXL_Lock. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF10

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-107: por_ccla_dvsec_cxl_lock

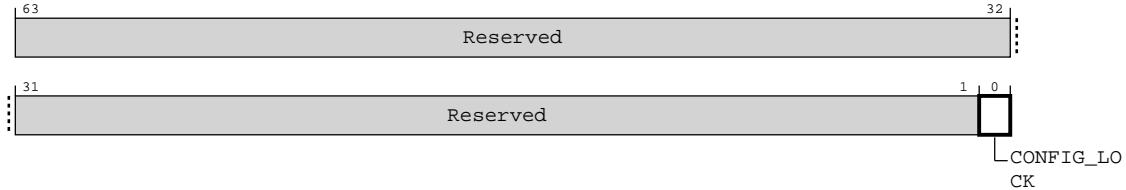


Table 4-123: por_ccla_dvsec_cxl_lock attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	CONFIG_LOCK	When set all register fields in the PCIe DVSEC for CXL Devices Capability with RWL attribute become read only. Consult individual register fields for details. This bit is cleared upon device Conventional Reset. This bit and all the fields that are locked by this bit are not affected by CXL Reset.	RW	1'h0

4.3.4.50 por_ccla_dvsec_flex_bus_port_control

Contains DVSEC_Flex_Bus_Port_Control

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF18

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-108: por_ccla_dvsec_flex_bus_port_control

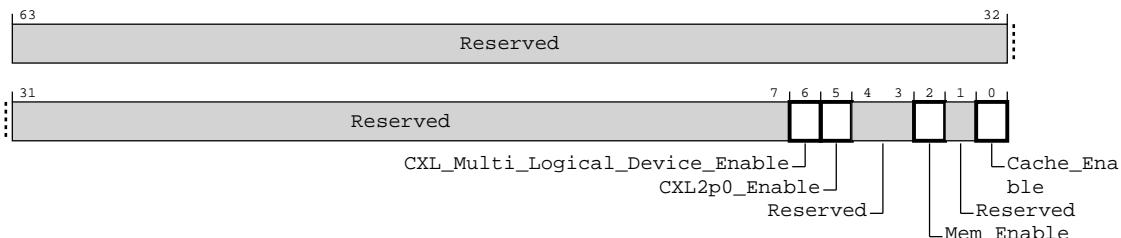


Table 4-124: por_ccla_dvsec_flex_bus_port_control attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6]	CXL_Multi_Logical_Device_Enable	When set enable Multi-Logical Device operation when in Flex Bus.CXL mode	RW	1'h0
[5]	CXL2p0_Enable	When set enable CXL2.0 protocol operation when in Flex Bus.CXL mode.	RW	1'h0
[4:3]	Reserved	Reserved	RO	-
[2]	Mem_Enable	When set enables CXL.mem protocol operation when in Flex Bus.CXL mode.	RW	1'h0
[1]	Reserved	Reserved	RO	-
[0]	Cache_Enable	When set enables CXL.cache protocol operation when in Flex Bus.CXL mode.	RW	1'h0

4.3.4.51 por_ccla_err_capabilities_control

Contains err_capabilities_control. Only applicable to device. Host doesn't use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF40

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-109: por_ccla_err_capabilities_control

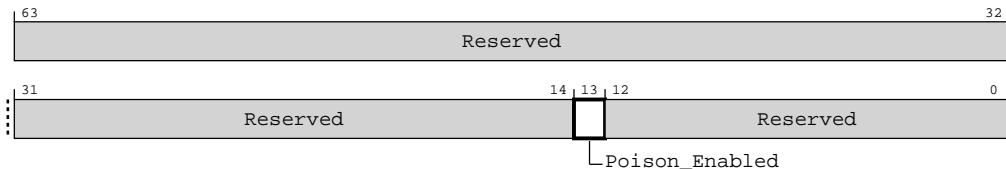


Table 4-125: por_ccla_err_capabilities_control attributes

Bits	Name	Description	Type	Reset
[63:14]	Reserved	Reserved	RO	-
[13]	Poison_Enabled	If this bit is 0 CXL 1.1 Upstream Ports CXL 1.1 Downstream Ports and CXL 2.0 Root Port shall treat poison received on CXL.cache or CXL.mem as uncorrectable error and log the error in Uncorrectable Error Status Register. If this bit is 1 these ports shall treat poison received on CXL.cache or CXL.mem as correctable error and log the error in Correctable Error Status Register. This bit defaults to 1. This bit is hardwired to 1 in CXL 2.0 Upstream Switch Port CXL 2.0 Downstream Switch Port and CXL 2.0 device.	RW	1'h0
[12:0]	Reserved	Reserved	RO	-

4.3.4.52 por_ccla_IDE_key_refresh_time_control

Contains IDE_key_refresh_time_control. Not applicable to CMN 700

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF58

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-110: por_ccla_IDE_key_refresh_time_control

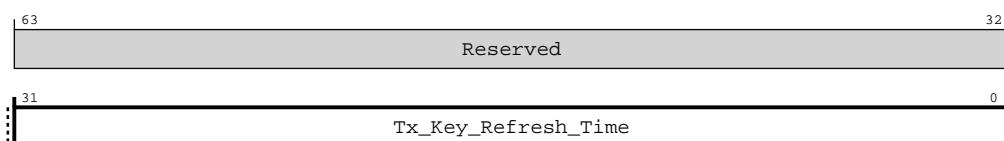


Table 4-126: por_ccla_IDE_key_refresh_time_control attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Tx_Key_Refresh_Time	Minimum number of flits transmitter needs to block transmission of protocol flits after IDE.Start has sent. Used when switching keys.	RW	32'h0

4.3.4.53 por_ccla_IDE_truncation_transmit_delay_control

Contains IDE_truncation_transmit_delay_control. Not applicable to CMN 700

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF60

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-111: por_ccla_IDE_truncation_transmit_delay_control

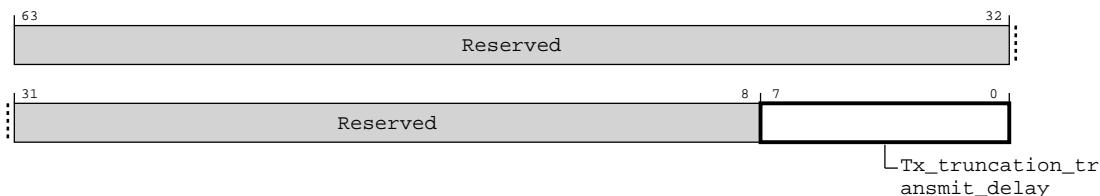


Table 4-127: por_ccla_IDE_truncation_transmit_delay_control attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[7:0]	Tx_truncation_transmit_delay	This parameter feeds into the computation of minimum number of IDE idle flits Transmitter needs send after sending a truncated MAC flit.	RW	8'h0

4.3.4.54 por_ccla_ll_to ull msg

Contains III_to_ull_message

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF70

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-112: por_ccla_ll_to ull msg

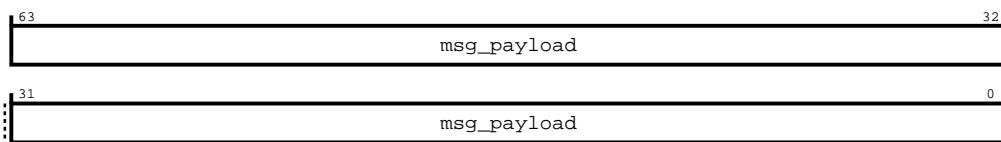


Table 4-128: por_ccla_ll_to ull msg attributes

Bits	Name	Description	Type	Reset
[63:0]	msg_payload	Contains 64 bits of message sent from ll to ull	RW	64'h0

4.3.4.55 por_ccla_cxl_timeout_isolation_control

Contains cxl_timeout_isolation_control. Not applicable to CMN 700

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF80

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-113: por_ccla_cxl_timeout_isolation_control

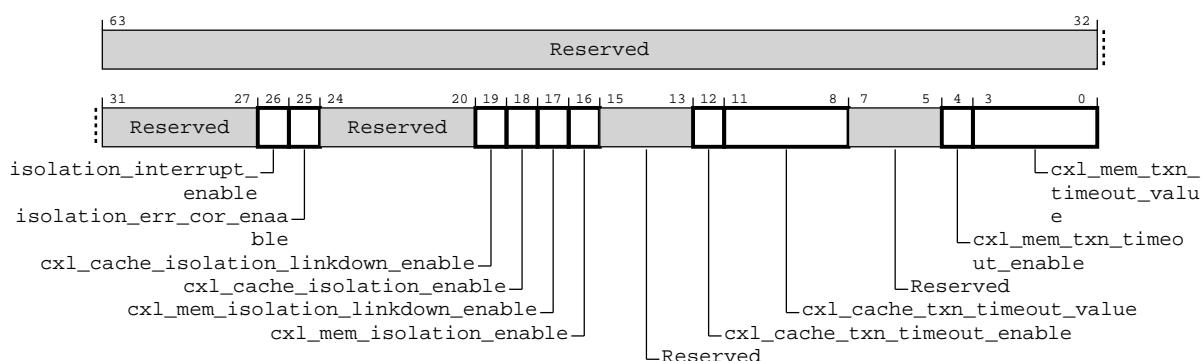


Table 4-129: por_ccla_cxl_timeout_isolation_control attributes

Bits	Name	Description	Type	Reset
[63:27]	Reserved	Reserved	RO	-
[26]	isolation_interrupt_enable	When Set this bit enables the generation of an interrupt to indicate that Isolation has been triggered.	RW	1'h0

Bits	Name	Description	Type	Reset
[25]	isolation_err_cor_enable	When Set this bit enables the sending of an ERR_COR Message to indicate Isolation has been triggered.	RW	1'h0
[24:20]	Reserved	Reserved	RO	-
[19]	cxl_cache_isolation_linkdown_enable	This field allows System Software to trigger link down on the CXL Root Port if CXL.cache enters Isolation mode.	RW	1'h0
[18]	cxl_cache_isolation_enable	This field allows System Software to enable CXL.cache Isolation actions.	RW	1'h0
[17]	cxl_mem_isolation_linkdown_enable	This field allows System Software to trigger link down on the CXL Root Port if CXL.mem enters Isolation mode.	RW	1'h0
[16]	cxl_mem_isolation_enable	This field allows System Software to enable CXL.mem Isolation actions. If this field is set Isolation actions will be triggered if either a CXL.mem Transaction Timeout is detected or if the CXL link went down.	RW	1'h0
[15:13]	Reserved	Reserved	RO	-
[12]	cxl_cache_txn_timeout_enable	-	RW	1'h0
[11:8]	cxl_cache_txn_timeout_value	In CXL Root Port Functions that support Transaction Timeout programmability this field allows system software to modify the Transaction Timeout Value for CXL.cache.	RW	4'h0
[7:5]	Reserved	Reserved	RO	-
[4]	cxl_mem_txn_timeout_enable	When Set this bit enables CXL.mem Transaction Timeout mechanism.	RW	1'h0
[3:0]	cxl_mem_txn_timeout_value	In CXL Root Port Functions that support Transaction Timeout programmability this field allows system software to modify the Transaction Timeout Value for CXL.mem.	RW	4'h0

4.3.4.56 por_ccla_root_port_n_security_policy

Contains Root_Port_n_Security_Policy_Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF28

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-114: por_ccla_root_port_n_security_policy

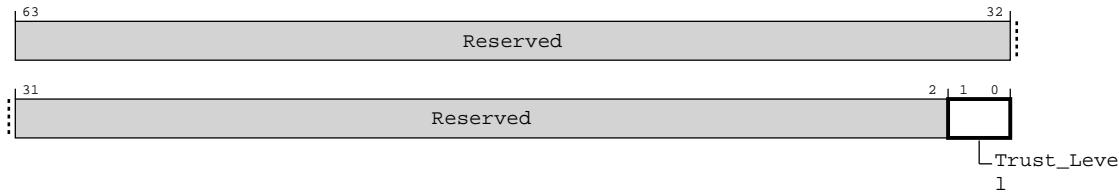


Table 4-130: por_ccla_root_port_n_security_policy attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	Trust_Level	Trust Level for the CXL.cache Device below Root Port n	RW	2'h2

4.3.4.57 por_ccla_root_port_n_id

Contains Root_Port_n_ID_Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF30

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-115: por_ccla_root_port_n_id

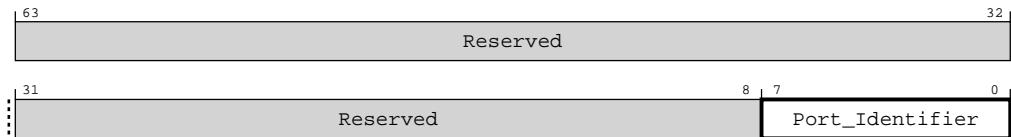


Table 4-131: por_ccla_root_port_n_id attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7:0]	Port_Identifier	Port Identifier of the Root Port n	RW	8'h0

4.3.4.58 por_ccla_cxl_link_layer_defeature

CXL Link Layer Defeature Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE18

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxllink_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-116: por_ccla_cxl_link_layer_defeature

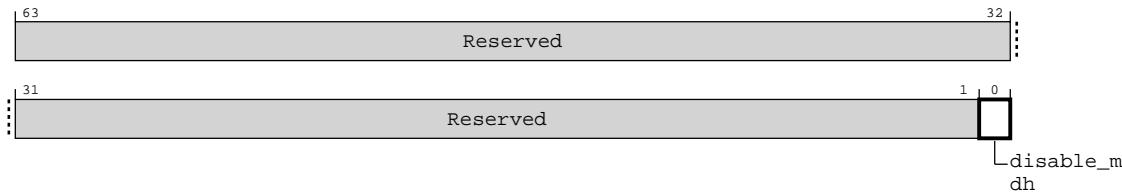


Table 4-132: por_ccla_cxl_link_layer_defeature attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	disable_mdh	Write 1 to disable MDH. Software needs to ensure it programs this value consistently on the UP & DP. After programming, a warm reset is required for the disable to take effect.	RW	1'b0

4.3.4.59 por_ccla_ull_ctl

Upper Link Layer Control Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE20

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ull_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-117: por_ccla_ull_ctl

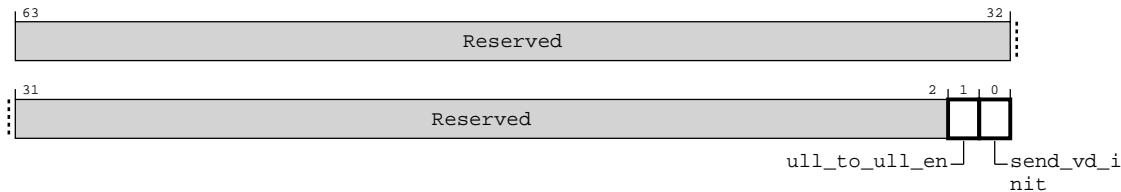


Table 4-133: por_ccla_ull_ctl attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	ull_to_ull_en	Used to enable ULL-to_ULL mode. Must be set on both sides of the link before 'send_vd_init' is set on either side 1'b0 When clear, ull-to-ull mode is disabled. 1'b1 When set, ull-to-ull mode is enabled.	RW	1'b0
[0]	send_vd_init	Used to send VD Init message. Must only be used for direct ULL to ULL connection. Must be used along with Tx ULL state (tx_ull_state) status bit 1'b0 When clear and tx_ull_state is in run_state, sends VD.De-activate flit. 1'b1 When set and tx_ull_state is in stop state, sends VD.Activate flit.	RW	1'b0

4.3.4.60 por_ccla_ull_status

Upper Link Layer Status Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE28

Type

RO

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ull_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-118: por_ccla_ull_status

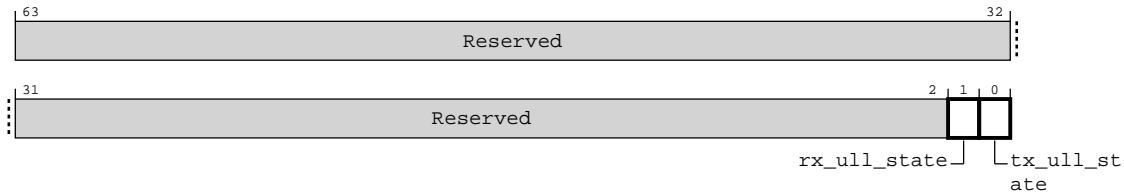


Table 4-134: por_ccla_ull_status attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	rx_ull_state	Reflects the Rx ULL state . 1'b0 Rx ULL is in Stop state 1'b1 Rx ULL is in Run state	RO	1'b0
[0]	tx_ull_state	Reflects the Tx ULL state . 1'b0 Tx ULL is in Stop state 1'b1 Tx ULL is in Run state	RO	1'b0

4.3.4.61 por_ccla_cxl_ll_errinject_ctl

CXL .cache .mem Link Layer Error Injection Control Register. Not used in Host mode

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE30

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.cxlerrinj_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-119: por_ccla_cxl_ll_errinject_ctl

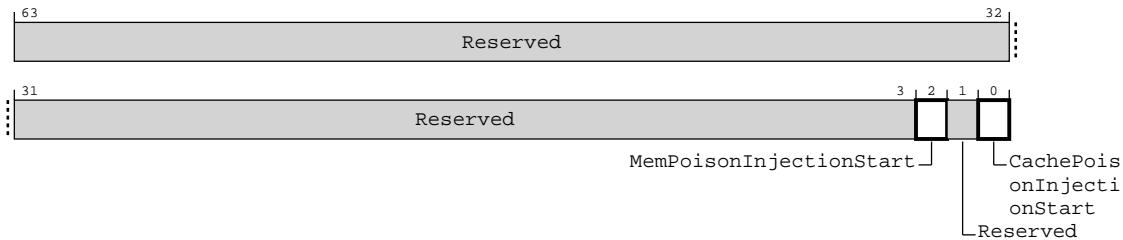


Table 4-135: por_ccla_cxl_ll_errinject_ctl attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	MemPoisonInjectionStart	Software writes 0x1 to this bit to trigger a single poison injection on a CXL.mem message in the Tx direction. Hardware must override the poison field in the data header slot of the corresponding message (DRS if device, RWD if Host). This bit is required only if CXL.mem protocol is supported.	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	CachePoisonInjectionStart	Software writes 0x1 to this bit to trigger a single poison injection on a CXL.cache message in the Tx direction. Hardware must override the poison field in the data header slot of the corresponding message (D2H if device, H2D if Host). This bit is required only if CXL.cache protocol is supported.	RW	1'b0

4.3.4.62 por_ccla_cxl_ll_errinject_stat

CXL .cache .mem Link Layer Error Injection Status Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE38

Type

RO

Reset value

See individual bit resets

Secure group override

`por_ccla_secure_register_groups_override.cxlerrinj_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-120: por_ccla_cxl_ll_errinject_stat

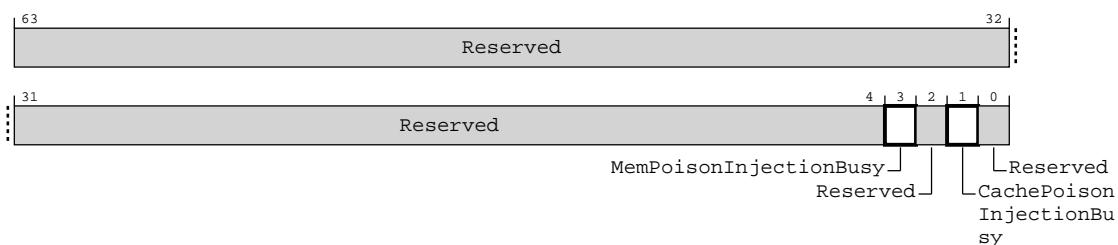


Table 4-136: por_ccla_cxl_ll_errinject_stat attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	MemPoisonInjectionBusy	Hardware loads 1 to this bit when the Start bit is written. Hardware must clear this bit to indicate that it has indeed finished poisoning a packet. Software is permitted to poll on this bit to find out when hardware has finished poison injection. This bit is required only if CXL.mem protocol is supported.	RO	1'b0
[2]	Reserved	Reserved	RO	-
[1]	CachePoisonInjectionBusy	Hardware loads 1 to this bit when the Start bit is written. Hardware must clear this bit to indicate that it has indeed finished poisoning a packet. Software is permitted to poll on this bit to find out when hardware has finished poison injection. This bit is required only if CXL.cache protocol is supported.	RO	1'b0
[0]	Reserved	Reserved	RO	-

4.3.4.63 por_ccla_cxl_viral_prop_en

Bit Vector which controls viral propagation. Each bit represents the logical ID of corresponding CML gateway block.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE40

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-121: por_ccla_cxl_viral_prop_en

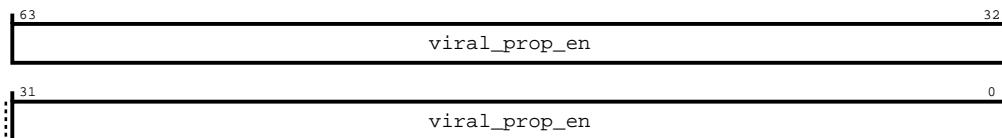


Table 4-137: por_ccla_cxl_viral_prop_en attributes

Bits	Name	Description	Type	Reset
[63:0]	viral_prop_en	Bit vector, where each bit represents logical ID of a CML gateway block present on CMN. Each bit when set, enables propagation of CXL Viral to that gateway block. 1'b0 Viral propagation is disabled 1'b1 Viral propagation is enabled	RW	64'b0

4.3.4.64 por_ccla_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2008

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-122: por_ccla_pmu_event_sel

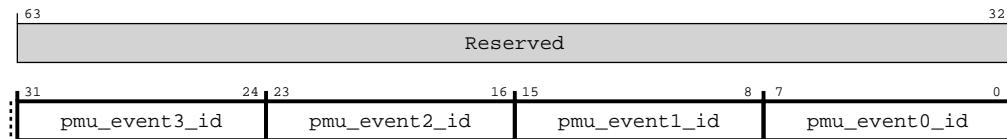


Table 4-138: por_ccla_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:24]	pmu_event3_id	CCLA PMU Event 3 ID; see pmu_event0_id for encodings	RW	8'b0
[23:16]	pmu_event2_id	CCLA PMU Event 2 ID; see pmu_event0_id for encodings	RW	8'b0
[15:8]	pmu_event1_id	CCLA PMU Event 1 ID; see pmu_event0_id for encodings	RW	8'b0
[7:0]	pmu_event0_id	CCLA PMU Event 0 ID 8'h00 No event 8'h21 LA_RX_CXS : number of RX CXS beats 8'h22 LA_TX_CXS : number of TX CXS beats 8'h23 LA_RX_CXS_AVG_SIZE : average size of RX CXS beats 8'h24 LA_TX_CXS_AVG_SIZE : average size of TX CXS beats 8'h25 LA_TX_CXS_LCRD_BACKPRESSURE : CXS backpressure due to lack of CXS credits 8'h26 LA_LINK_CRDBUF_OCC : CCLA RX RAM buffer occupancy 8'h27 LA_LINK_CRDBUF_ALLOC: CCLA RX RAM buffer allocation 8'h28 PFWD RCVR CXS beats 8'h29 PFWD SNDR NUM FLITS 8'h2A PFWD SNDR Number of message stalls due to static credits 8'h2B PFWD SNDR Number of message stalls due to dynamic credits	RW	8'b0

4.3.4.65 por_ccla_errfr

Functions as the error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3000

Type

RO

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-123: por_ccla_errfr

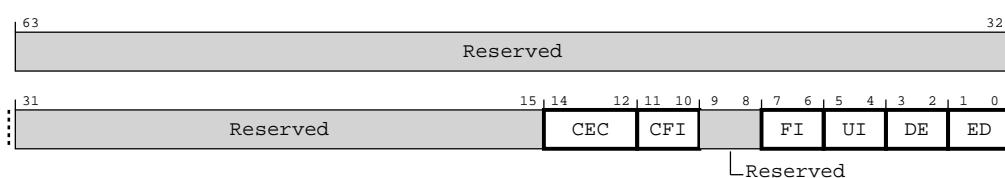


Table 4-139: por_ccla_errfr attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000 Does not implement standardized error counter model 3'b010 Implements 8-bit error counter in por_ccla_errmisc[39:32] 3'b100 Implements 16-bit error counter in por_ccla_errmisc[47:32]	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10

Bits	Name	Description	Type	Reset
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors for data poison	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.4.66 por_ccla_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferral are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3008

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-124: por_ccla_errctlr

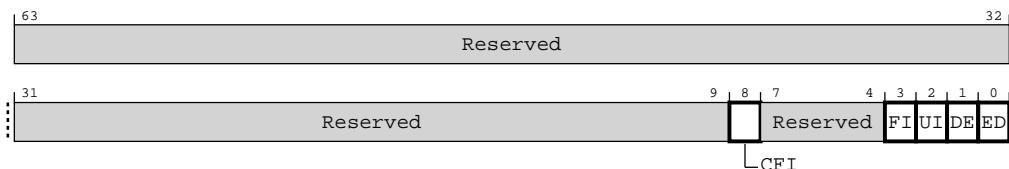


Table 4-140: por_ccla_errctlr attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[8]	CFI	Enables corrected error interrupt as specified in por_ccla_errfr.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_ccla_errfr.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_ccla_errfr.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_ccla_errfr.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_ccla_errfr.ED	RW	1'b0

4.3.4.67 por_ccla_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3010

Type

W1C

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-125: por_ccla_errstatus

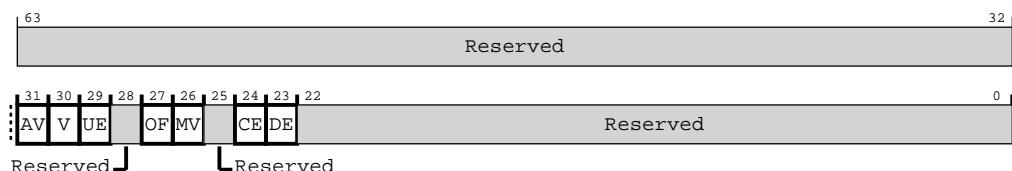


Table 4-141: por_ccla_errstatus attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; por_ccla_erraddr contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	por_ccla_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0

Bits	Name	Description	Type	Reset
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.4.68 por_ccla_erraddr

Contains the error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3018

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-126: por_ccla_erraddr

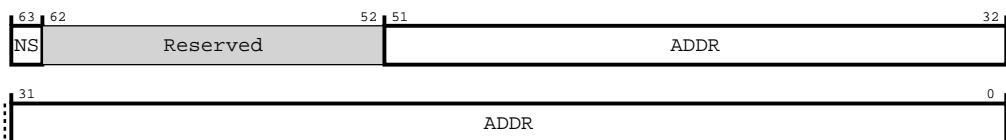


Table 4-142: por_ccla_erraddr attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: por_ccla_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.4.69 por_ccla_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3020

Type

RW

Reset value

See individual bit resets

Secure group override

por_ccla_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-127: por_ccla_errmisc

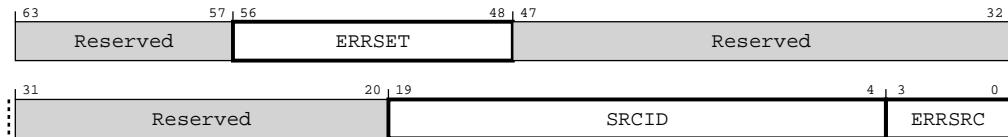


Table 4-143: por_ccla_errmisc attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:48]	ERRSET	RAM entry set address for parity error	RW	9'b0
[47:20]	Reserved	Reserved	RO	-
[19:4]	SRCID	CCIX RAID of the requestor or the snoop target	RW	16'b0
[3:0]	ERRSRC	Source of the parity error	RW	4'b0000
	4'b0000	Read data buffer 0		
	4'b0001	Read data buffer 1		
	4'b0010	Write data buffer 0		
	4'b0011	Write data buffer 1		
	4'b0100	Passive Buffer		
	4'b0101	CCLA Data RAM		
	4'b0110:	PortFwd Data RAM		
	4'b0111	CXL Viral		
	4'b1000	CXL.Mem Poison		
	4'b1001	CXL.Cache Poison		

4.3.4.70 por_ccla_errfr_NS

Functions as the Non-secure error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3100

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-128: por_ccla_errfr_NS

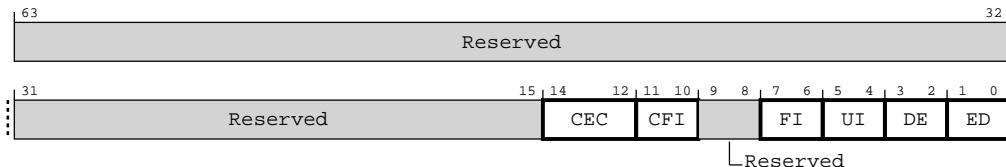


Table 4-144: por_ccla_errfr_NS attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000 Does not implement standardized error counter model 3'b010 Implements 8-bit error counter in por_ccla_errmisc[39:32] 3'b100 Implements 16-bit error counter in por_ccla_errmisc[47:32]	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors for data poison	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.4.71 por_ccla_errctlr_NS

Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferral are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3108

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-129: por_ccla_errctlr_NS

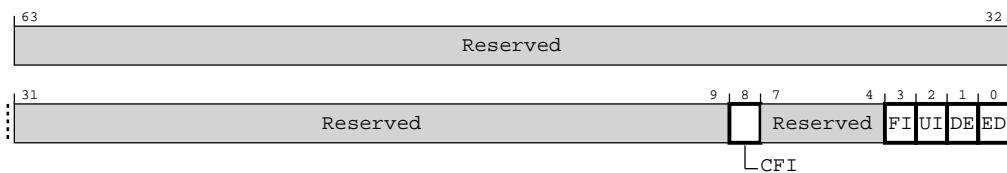


Table 4-145: por_ccla_errctlr_NS attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_ccla_errfr.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_ccla_errfr.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_ccla_errfr.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_ccla_errfr.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_ccla_errfr.ED	RW	1'b0

4.3.4.72 por_ccla_errstatus_NS

Functions as the Non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3110

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-130: por_ccla_errstatus_NS

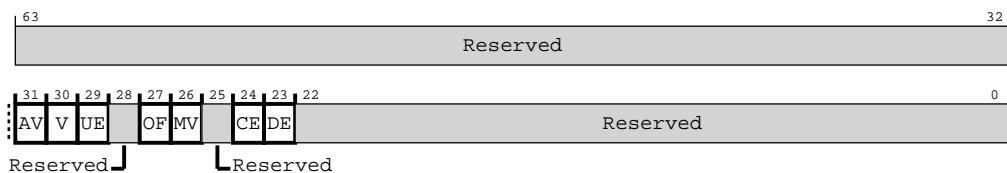


Table 4-146: por_ccla_errstatus_NS attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; por_ccla_erraddr contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	por_ccla_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.4.73 por_ccla_erraddr_NS

Contains the Non-secure error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3118

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-131: por_ccla_erraddr_NS

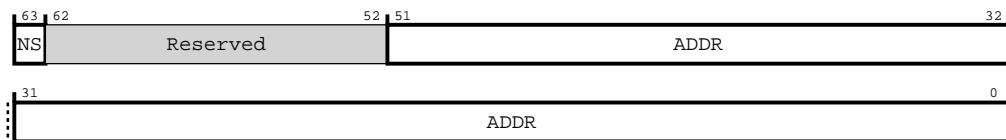


Table 4-147: por_ccla_erraddr_NS attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: por_ccla_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.4.74 por_ccla_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3120

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-132: por_ccla_errmisc_NS

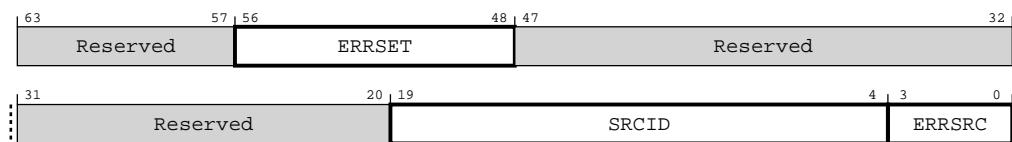


Table 4-148: por_ccla_errmisc_NS attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:48]	ERRSET	RAM entry set address for parity error	RW	9'b0
[47:20]	Reserved	Reserved	RO	-
[19:4]	SRCID	CCIX RAID of the requestor or the snoop target	RW	16'b0
[3:0]	ERRSRC	Source of the parity error	RW	4'b0000
		4'b0000 Read data buffer 0		
		4'b0001 Read data buffer 1		
		4'b0010 Write data buffer 0		
		4'b0011 Write data buffer 1		
		4'b0100 Passive Buffer		
		4'b0101 CCLA Data RAM		
		4'b0110: PortFwd Data RAM		
		4'b0111 CXL Viral		
		4'b1000 CXL.Mem Poison		
		4'b1001 CXL.Cache Poison		

4.3.5 Configuration manager register descriptions

This section lists the configuration registers.

4.3.5.1 por_cfgm_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-133: por_cfgm_node_info

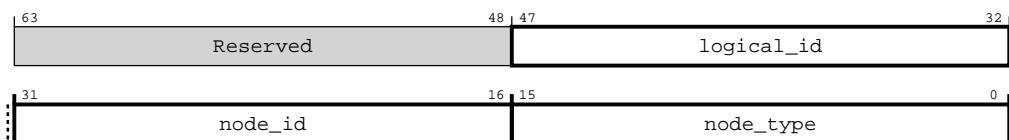


Table 4-149: por_cfgm_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0002

4.3.5.2 por_cfgm_periph_id_0_periph_id_1

Functions as the peripheral ID 0 and peripheral ID 1 register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h8`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-134: por_cfgm_periph_id_0_periph_id_1

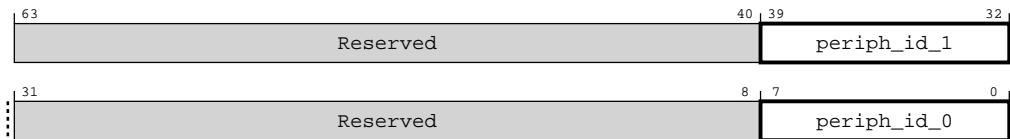


Table 4-150: por_cfgm_periph_id_0_periph_id_1 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	periph_id_1	Peripheral ID 1	RO	8'b10110100
[31:8]	Reserved	Reserved	RO	-
[7:0]	periph_id_0	Peripheral ID 0	RO	Configuration dependent

4.3.5.3 por_cfgm_periph_id_2_periph_id_3

Functions as the peripheral ID 2 and peripheral ID 3 register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h10`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-135: por_cfgm_periph_id_2_periph_id_3

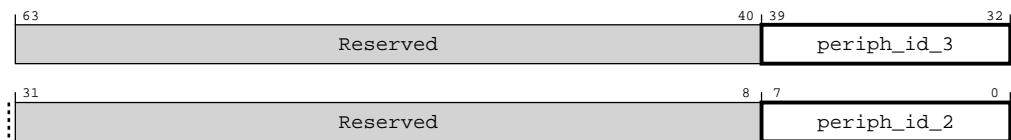


Table 4-151: por_cfgm_periph_id_2_periph_id_3 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	periph_id_3	Peripheral ID 3	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	periph_id_2	Peripheral ID 2 [7:4] indicates revision: 0x0 r0p0 0x1 r1p0 0x2 r2p0 0x3 r3p0 [3] JEDEC JEP106 identity code, 1'b1 [2:0] JEP106 identity code [6:4], 0'b011	RO	Configuration dependent

4.3.5.4 por_cfgm_periph_id_4_periph_id_5

Functions as the peripheral ID 4 and peripheral ID 5 register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h18

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-136: por_cfgm_periph_id_4_periph_id_5

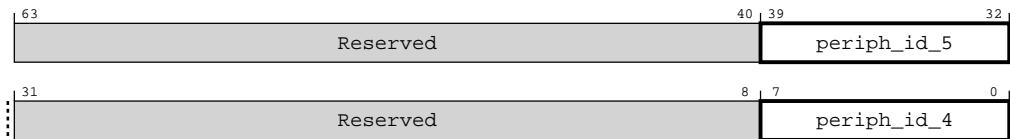


Table 4-152: por_cfgm_periph_id_4_periph_id_5 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	periph_id_5	Peripheral ID 5	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	periph_id_4	Peripheral ID 4	RO	8'b11000100

4.3.5.5 por_cfgm_periph_id_6_periph_id_7

Functions as the peripheral ID 6 and peripheral ID 7 register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h20

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-137: por_cfgm_periph_id_6_periph_id_7

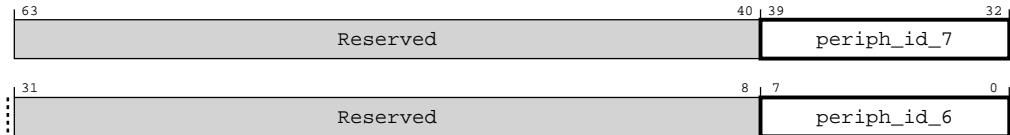


Table 4-153: por_cfgm_periph_id_6_periph_id_7 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	periph_id_7	Peripheral ID 7	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	periph_id_6	Peripheral ID 6	RO	8'b0

4.3.5.6 por_cfgm_component_id_0_component_id_1

Functions as the component ID 0 and component ID 1 register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h28

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-138: por_cfgm_component_id_0_component_id_1

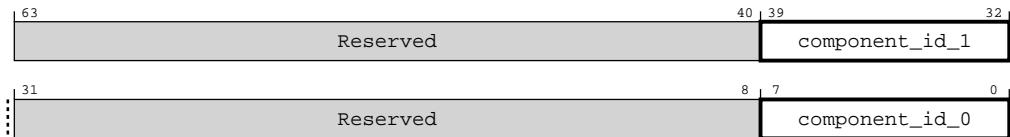


Table 4-154: por_cfgm_component_id_0_component_id_1 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	component_id_1	Component ID 1	RO	8'b11110000
[31:8]	Reserved	Reserved	RO	-
[7:0]	component_id_0	Component ID 0	RO	8'b00001101

4.3.5.7 por_cfgm_component_id_2_component_id_3

Functions as the component ID 2 and component ID 3 register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h30

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-139: por_cfgm_component_id_2_component_id_3

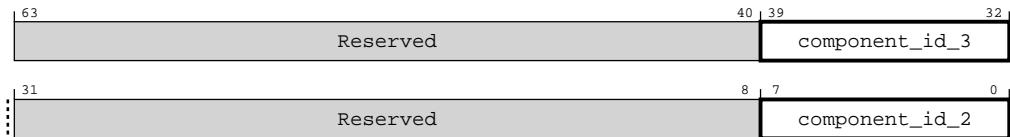


Table 4-155: por_cfgm_component_id_2_component_id_3 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	component_id_3	Component ID 3	RO	8'b10110001
[31:8]	Reserved	Reserved	RO	-
[7:0]	component_id_2	Component ID 2	RO	8'b00000101

4.3.5.8 por_cfgm_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-140: por_cfgm_child_info

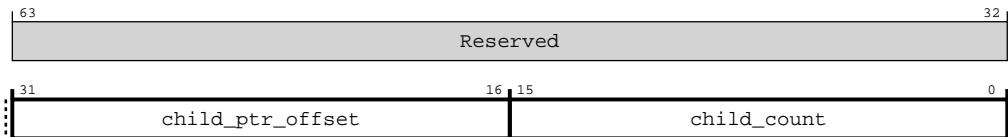


Table 4-156: por_cfgm_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
[15:0]	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

4.3.5.9 por_cfgm_secure_access

Functions as the Secure access control register. This register must be set up at boot time. Before initiating a write to this register, software must ensure that no other configuration accesses are in flight. Once this write is initiated, no other configuration accesses are initiated until complete.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-141: por_cfgm_secure_access

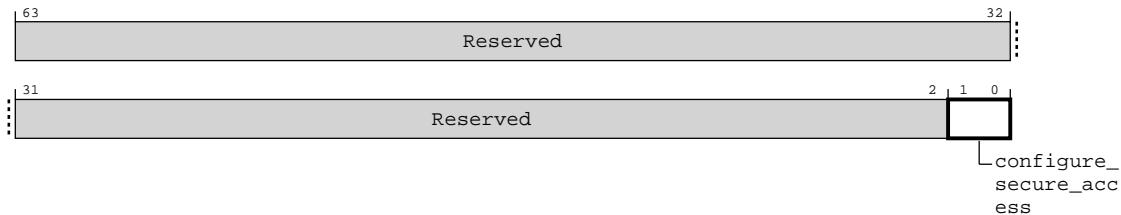


Table 4-157: por_cfgm_secure_access attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	configure_secure_access	Secure access mode 2'b00: Default operation 2'b01: Allows Non-secure access to Secure registers 2'b10: Allows Secure access only to any configuration register regardless of its security status 2'b11: Undefined behavior	RW	2'b0

4.3.5.10 por_cfgm_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h988

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-142: por_cfgm_secure_register_groups_override

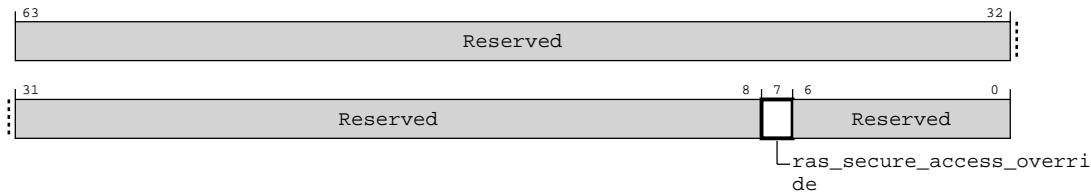


Table 4-158: por_cfgm_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7]	ras_secure_access_override	Allow Non-secure access to Secure RAS registers	RW	1'b0
[6:0]	Reserved	Reserved	RO	-

4.3.5.11 por_cfgm_errgsr_mxp_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the XP <n> Secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3000 + # { 8 * index }

Type

RO

Reset value

See individual bit resets

Secure group override

por_cfgm_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-143: por_cfgm_errgsr_mxp_0-7

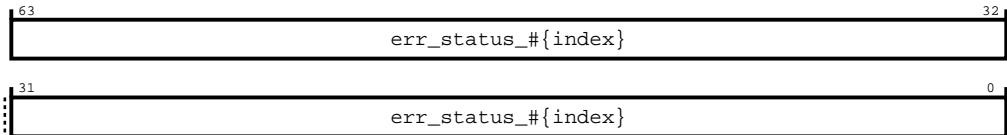


Table 4-159: por_cfgm_errgsr_mxp_0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}	Read-only copy of MXP [Error/Fault] <n> status	RO	64'h0

4.3.5.12 por_cfgm_errgsr_mxp_0-7_NS

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the XP <n> Non-secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3040 + #{8*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-144: por_cfgm_errgsr_mxp_0-7_NS

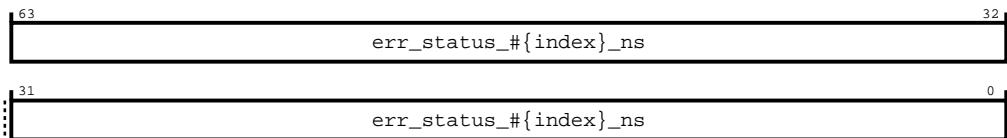


Table 4-160: por_cfgm_errgsr_mxp_0-7_NS attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}	Read-only copy of MXP [Error/Fault] <n> status	RO	64'h0

4.3.5.13 por_cfgm_errgsr_hni_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the HNI <n> Secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3080 + # {8 * index}

Type

RO

Reset value

See individual bit resets

Secure group override

por_cfgm_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-145: por_cfgm_errgsr_hni_0-7

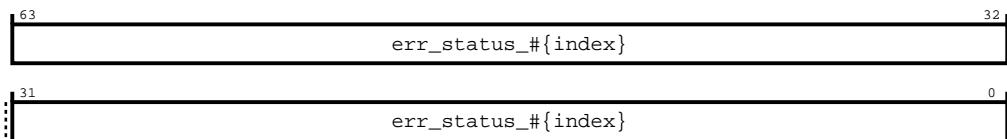


Table 4-161: por_cfgm_errgsr_hni_0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}	Read-only copy of HNI [Error/Fault] <n> status	RO	64'h0

4.3.5.14 por_cfgm_errgsr_hni_0-7_NS

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the HNI <n> Non-secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h30C0 + #{8*index}`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-146: por_cfgm_errgsr_hni_0-7_NS

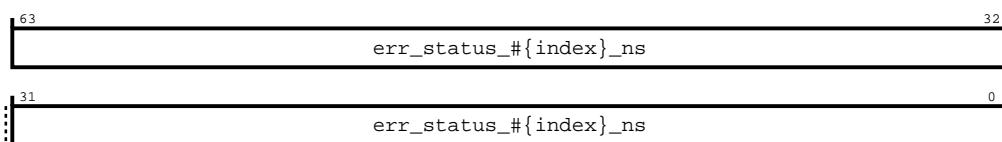


Table 4-162: por_cfgm_errgsr_hni_0-7_NS attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}_ns	Read-only copy of HNI [Error/Fault] <n> status	RO	64'h0

4.3.5.15 por_cfgm_errgsr_hnf_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the HNF <n> Secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h3100 + #{8*index}`

Type

RO

Reset value

See individual bit resets

Secure group override

`por_cfgm_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-147: por_cfgm_errgsr_hnf_0-7

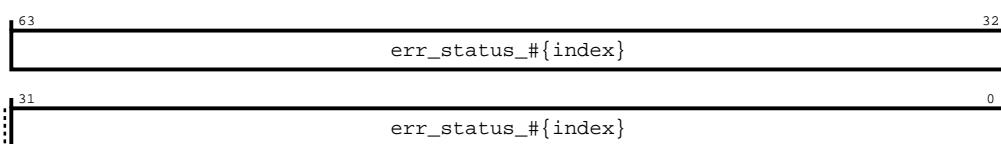


Table 4-163: por_cfgm_errgsr_hnf_0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_#{index}	Read-only copy of HNF [Error/Fault] <n> status	RO	64'h0

4.3.5.16 por_cfgm_errgsr_hnf_0-7_NS

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the HNF <n> Non-secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3140 + # {8 * index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-148: por_cfgm_errgsr_hnf_0-7_NS

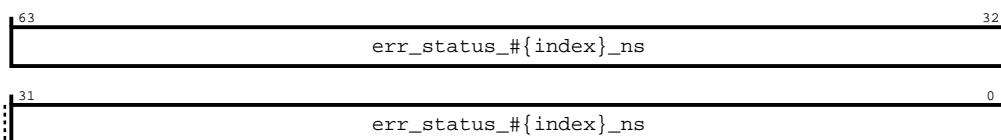


Table 4-164: por_cfgm_errgsr_hnf_0-7_NS attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}_ns	Read-only copy of HNF [Error/Fault] <n> status	RO	64'h0

4.3.5.17 por_cfgm_errgsr_sbsx_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the SBSX <n> Secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h3180 + #{8*index}`

Type

RO

Reset value

See individual bit resets

Secure group override

`por_cfgm_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-149: por_cfgm_errgsr_sbsx_0-7

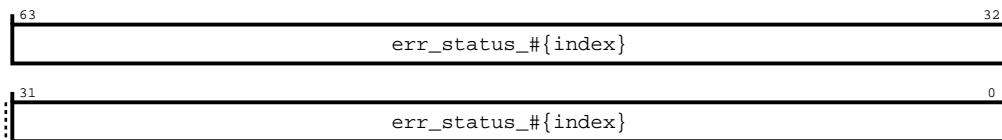


Table 4-165: por_cfgm_errgsr_sbsx_0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_#{index}	Read-only copy of SBSX [Error/Fault] <n> status	RO	64'h0

4.3.5.18 por_cfgm_errgsr_sbsx_0-7_NS

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the SBSX <n> Non-secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h31C0 + # {8 * index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-150: por_cfgm_errgsr_sbsx_0-7_NS

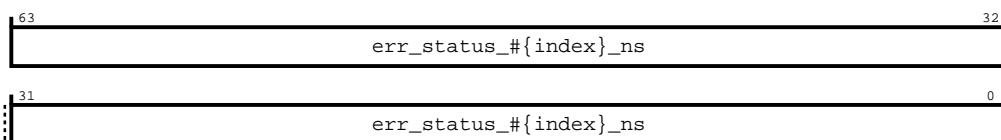


Table 4-166: por_cfgm_errgsr_sbsx_0-7_NS attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}_ns	Read-only copy of SBSX [Error/Fault] <n> status	RO	64'h0

4.3.5.19 por_cfgm_errgsr_cxg_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the CXG <n> Secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h3200 + #{8*index}`

Type

RO

Reset value

See individual bit resets

Secure group override

`por_cfgm_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-151: por_cfgm_errgsr_cxg_0-7

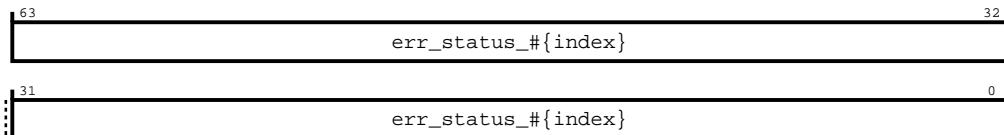


Table 4-167: por_cfgm_errgsr_cxg_0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_#{index}	Read-only copy of CXG [Error/Fault] <n> status	RO	64'h0

4.3.5.20 por_cfgm_errgsr_cxg_0-7_NS

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the CXG <n> Non-secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3240 + # {8 * index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-152: por_cfgm_errgsr_cxg_0-7_NS

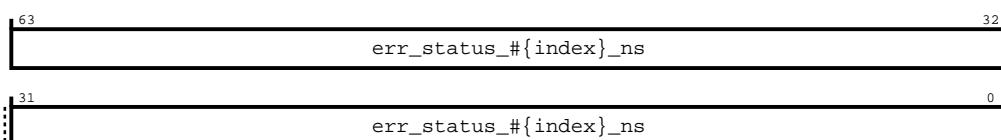


Table 4-168: por_cfgm_errgsr_cxg_0-7_NS attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}_ns	Read-only copy of CXG [Error/Fault] <n> status	RO	64'h0

4.3.5.21 por_cfgm_errgsr_mtsx_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the MTSX <n> Secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h3280 + # {8 * index}`

Type

RO

Reset value

See individual bit resets

Secure group override

`por_cfgm_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-153: por_cfgm_errgsr_mtsx_0-7

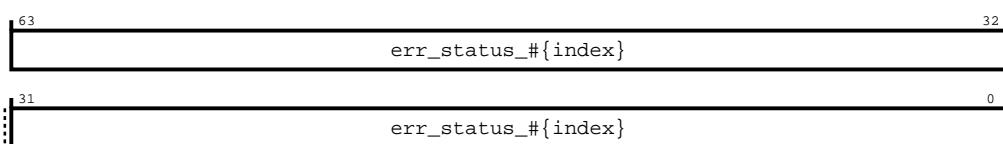


Table 4-169: por_cfgm_errgsr_mtsx_0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_#{index}	Read-only copy of MTSX [Error/Fault] <n> status	RO	64'h0

4.3.5.22 por_cfgm_errgsr_mtsx_0-7_NS

There are 8 iterations of this register. The index ranges from 0 to 7. Provides the MTSX <n> Non-secure [Error/Fault] status. Where, Error occurs when the index is even and Fault occurs when the index is odd

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h32C0 + # {8 * index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-154: por_cfgm_errgsr_mtsx_0-7_NS

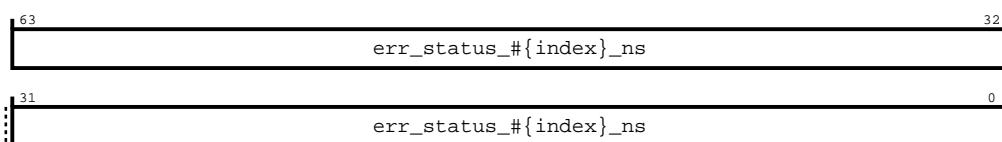


Table 4-170: por_cfgm_errgsr_mtsx_0-7_NS attributes

Bits	Name	Description	Type	Reset
[63:0]	err_status_{index}_ns	Read-only copy of MTSX [Error/Fault] <n> status	RO	64'h0

4.3.5.23 por_cfgm_errdevaff

Functions as the device affinity register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FA8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-155: por_cfgm_errdevaff

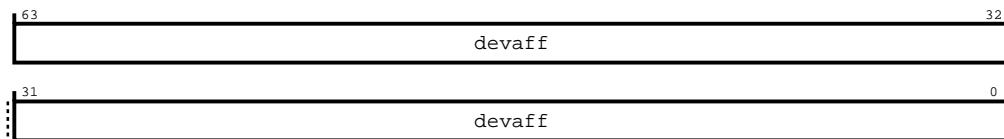


Table 4-171: por_cfgm_errdevaff attributes

Bits	Name	Description	Type	Reset
[63:0]	devaff	Device affinity register	RO	64'b0

4.3.5.24 por_cfgm_errdevarch

Functions as the device architecture register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FB8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-156: por_cfgm_errdevarch

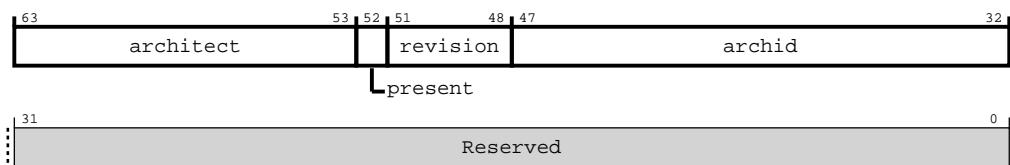


Table 4-172: por_cfgm_errdevarch attributes

Bits	Name	Description	Type	Reset
[63:53]	architect	Architect	RO	11'h23B
[52]	present	Present	RO	1'b1
[51:48]	revision	Architecture revision	RO	4'b0
[47:32]	archid	Architecture ID	RO	16'h0A00
[31:0]	Reserved	Reserved	RO	-

4.3.5.25 por_cfgm_erridr

Contains the number of error records.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FC8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-157: por_cfgm_erridr

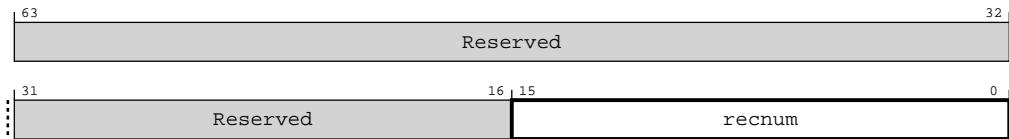


Table 4-173: por_cfgm_erridr attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	recnum	Number of error records; equal to 2*(number of logical devices)	RO	Configuration dependent

4.3.5.26 por_cfgm_errpidr45

Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FD0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-158: por_cfgm_errpidr45

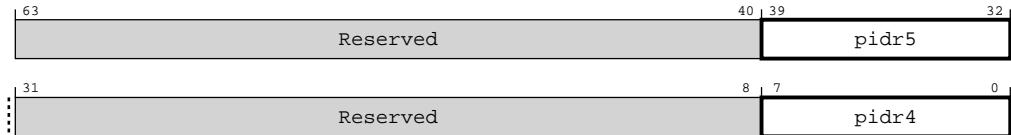


Table 4-174: por_cfgm_errpidr45 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr5	Peripheral ID 5	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr4	Peripheral ID 4	RO	8'h4

4.3.5.27 por_cfgm_errpidr67

Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FD8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-159: por_cfgm_errpidr67

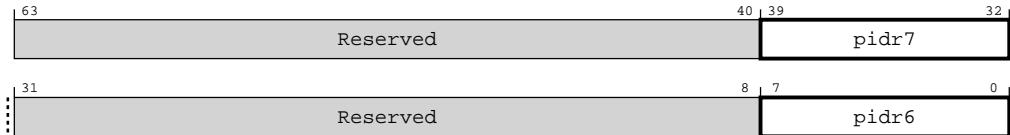


Table 4-175: por_cfgm_errpidr67 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr7	Peripheral ID 7	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr6	Peripheral ID 6	RO	8'b0

4.3.5.28 por_cfgm_errpidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FE0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-160: por_cfgm_errpidr01

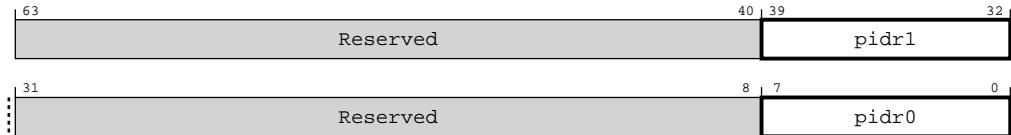


Table 4-176: por_cfgm_errpidr01 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr1	Peripheral ID 1	RO	8'hb4
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr0	Peripheral ID 0	RO	8'h34

4.3.5.29 por_cfgm_errpidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FE8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-161: por_cfgm_errpidr23

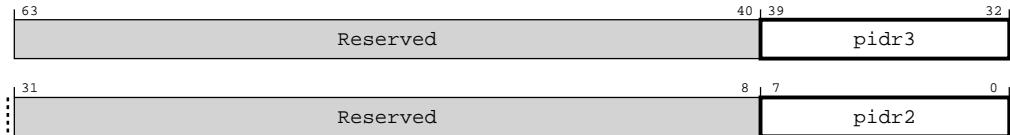


Table 4-177: por_cfgm_errpidr23 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr3	Peripheral ID 3	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr2	Peripheral ID 2	RO	8'h7

4.3.5.30 por_cfgm_errcidr01

Functions as the identification register for component ID 0 and component ID 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FF0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-162: por_cfgm_errcidr01

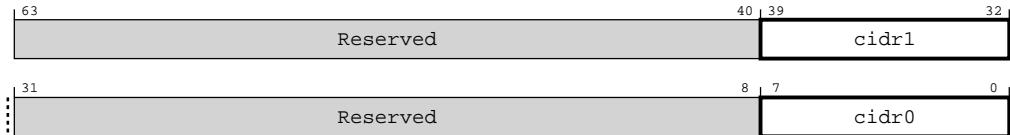


Table 4-178: por_cfgm_errcidr01 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	cidr1	Component ID 1	RO	8'hff
[31:8]	Reserved	Reserved	RO	-
[7:0]	cidr0	Component ID 0	RO	8'hd

4.3.5.31 por_cfgm_errcidr23

Functions as the identification register for component ID 2 and component ID 3.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3FF8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-163: por_cfgm_errcidr23

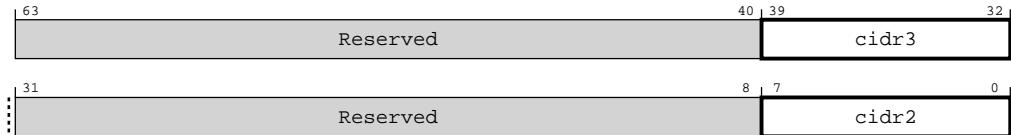


Table 4-179: por_cfgm_errcidr23 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	cidr3	Component ID 3	RO	8'hb1
[31:8]	Reserved	Reserved	RO	-
[7:0]	cidr2	Component ID 2	RO	8'h5

4.3.5.32 por_info_global

Contains user-specified values of build-time global configuration parameters.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-164: por_info_global

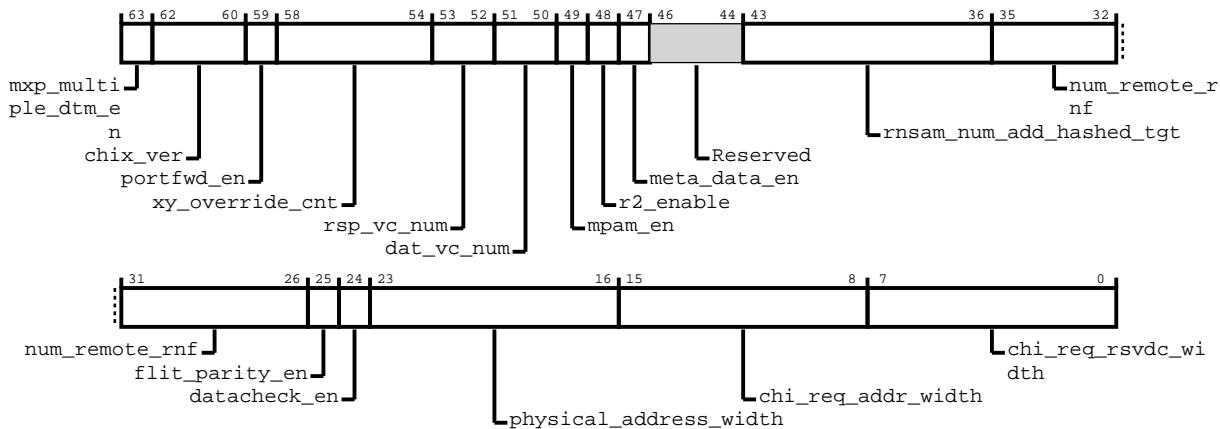


Table 4-180: por_info_global attributes

Bits	Name	Description	Type	Reset
[63]	mpx_multiple_dtm_en	Multiple DTM's feature enable. This is used if number of device ports on the XP is > 2	RO	Configuration dependent
[62:60]	chix_ver	CHIX Version Parameter: 2 -> CHIB, 3 -> CHIC, 4 -> CHID, 5 -> CHIE	RO	Configuration dependent
[59]	portfwd_en	CCIX Port to Port Forwarding feature enable	RO	Configuration dependent
[58:54]	xy_override_cnt	Number of Src-Tgt pairs whose XY route path can be overridden	RO	Configuration dependent
[53:52]	rsp_vc_num	Number of additional RSP channels internal to MXP. For increased bandwidth, this parameter need to be set to 2	RO	Configuration dependent
[51:50]	dat_vc_num	Number of additional DAT channels internal to MXP. For increased bandwidth, this parameter need to be set to 2	RO	Configuration dependent
[49]	mpam_en	MPAM enable	RO	Configuration dependent
[48]	r2_enable	CMN R2 feature enable	RO	Configuration dependent
[47]	meta_data_en	Meta Data Preservation mode enable	RO	Configuration dependent
[46:44]	Reserved	Reserved	RO	-
[43:36]	rnsam_num_add_hashed_tgt	Number of additional hashed target ID's supported by the RN SAM, beyond the local HNF count	RO	Configuration dependent
[35:26]	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent
[25]	flit_parity_en	Indicates whether parity checking is enabled in the transport layer on all flits sent on the interconnect	RO	Configuration dependent
[24]	datacheck_en	Indicates whether datacheck feature is enabled for CHI DAT flit	RO	Configuration dependent
[23:16]	physical_address_width	Physical address width	RO	Configuration dependent

Bits	Name	Description	Type	Reset
[15:8]	chi_req_addr_width	REQ address width	RO	Configuration dependent
[7:0]	chi_req_rsvdc_width	RSVDC field width in CHI REQ flit	RO	Configuration dependent

4.3.5.33 por_info_global_1

Contains user-specified values of build-time global configuration parameters.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-165: por_info_global_1

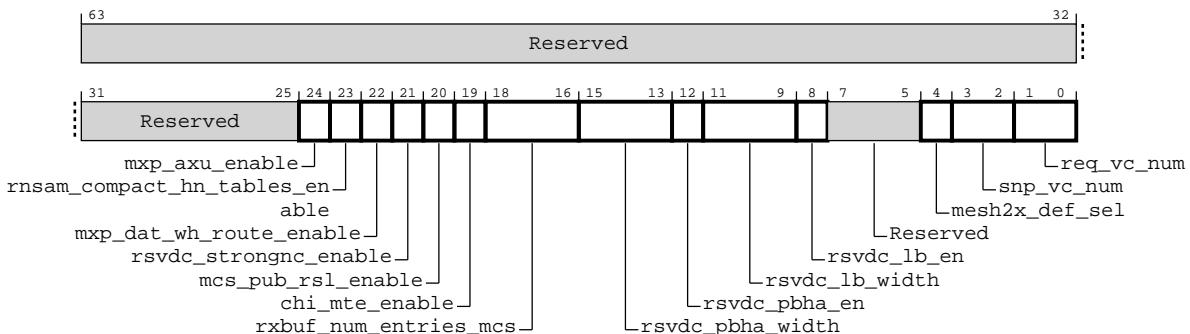


Table 4-181: por_info_global_1 attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	mxp_axu_enable	MXP AXU interface Enable	RO	Configuration dependent
[23]	rnsam_compact_hn_tables_enable	RNSAM Compact HN Tables Enable	RO	Configuration dependent
[22]	mxp_dat_wh_route_enable	Worm Hole Routing Enable for MXP DAT channel	RO	Configuration dependent
[21]	rsvdc_strongnc_enable	RSVDC StrongNC Mode Enable	RO	Configuration dependent
[20]	mcs_pub_rsl_enable	Register Slice enable for MCS PUB outputs	RO	Configuration dependent
[19]	chi_mte_enable	CHI MTE Feature Enable	RO	Configuration dependent
[18:16]	rxbuf_num_entries_mcs	RX Buffer Entries at upload interface of MCSX/MCSY	RO	Configuration dependent
[15:13]	rsvdc_pbha_width	RSVDC PBHA Field Width	RO	Configuration dependent
[12]	rsvdc_pbha_en	RSVDC PBHA Mode Enable	RO	Configuration dependent
[11:9]	rsvdc_lb_width	RSVDC Loop Back Field Width	RO	Configuration dependent
[8]	rsvdc_lb_en	RSVDC Loop Back Mode Enable	RO	Configuration dependent
[7:5]	Reserved	Reserved	RO	-
[4]	mesh2x_def_sel	Default ping-pong scheme selection for TGTID Lookup in 2xMESH	RO	Configuration dependent
[3:2]	snp_vc_num	Number of additional SNP channels internal to MXP. For increased bandwidth, this parameter need to be set to 2	RO	Configuration dependent
[1:0]	req_vc_num	Number of additional REQ channels internal to MXP. For increased bandwidth, this parameter need to be set to 2	RO	Configuration dependent

4.3.5.34 por_ppu_int_enable

Configures the HN-F PPU event interrupt. Contains the interrupt mask.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C00

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-166: por_ppu_int_enable

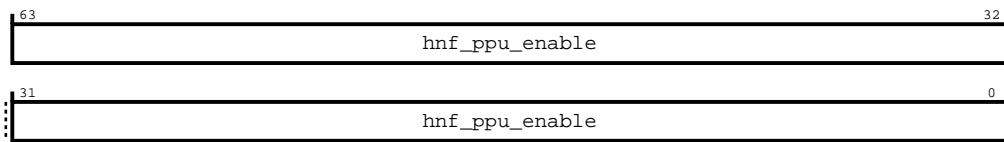


Table 4-182: por_ppu_int_enable attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_ppu_enable	Interrupt mask	RW	64'b0

4.3.5.35 por_ppu_int_enable_1

Configures the HN-F PPU event interrupt. Contains the interrupt mask.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-167: por_ppu_int_enable_1

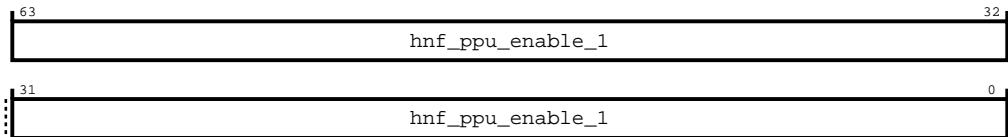


Table 4-183: por_ppu_int_enable_1 attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_ppu_enable_1	Interrupt mask	RW	64'b0

4.3.5.36 por_ppu_int_status

Provides HN-F PPU event interrupt status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C10

Type

W1C

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-168: por_ppu_int_status

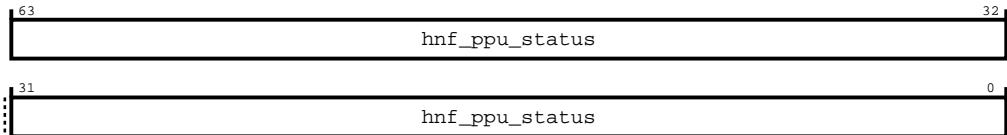


Table 4-184: por_ppu_int_status attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_ppu_status	Interrupt status	W1C	64'b0

4.3.5.37 por_ppu_int_status_1

Provides HN-F PPU event interrupt status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C18

Type

W1C

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-169: por_ppu_int_status_1

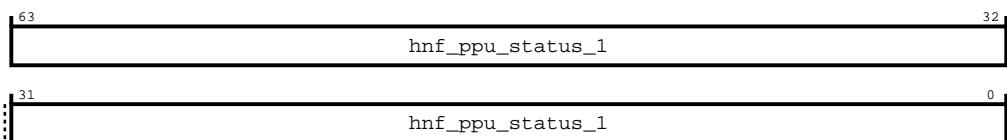


Table 4-185: por_ppu_int_status_1 attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_ppu_status_1	Interrupt status	W1C	64'b0

4.3.5.38 por_ppu_qactive_hyst

Number of hysteresis clock cycles to retain QACTIVE assertion

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C20

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-170: por_ppu_qactive_hyst

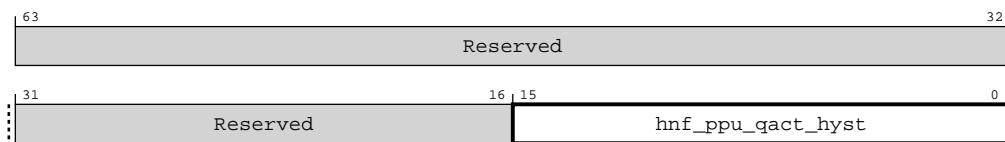


Table 4-186: por_ppu_qactive_hyst attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hnf_ppu_qact_hyst	QACTIVE hysteresis	RW	16'h10

4.3.5.39 por_mpam_s_err_int_status

Provides HN-F MPAM Secure Error interrupt status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C28

Type

W1C

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-171: por_mpam_s_err_int_status

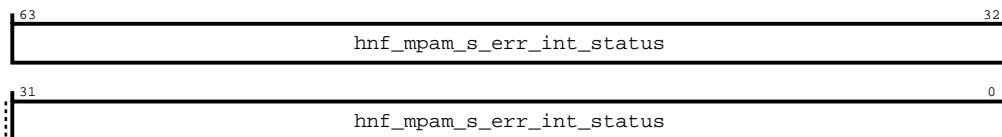


Table 4-187: por_mpam_s_err_int_status attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_mpam_s_err_int_status	MPAM S Interrupt status	W1C	64'b0

4.3.5.40 por_mpam_s_err_int_status_1

Provides HN-F MPAM Secure Error interrupt status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C30

Type

W1C

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-172: por_mpam_s_err_int_status_1

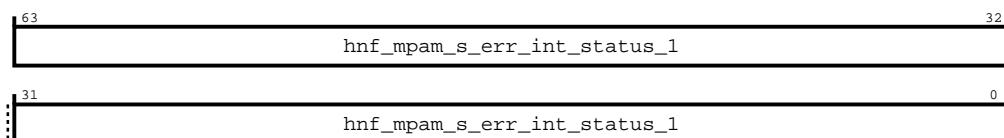


Table 4-188: por_mpam_s_err_int_status_1 attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_mpam_s_err_int_status_1	MPAM S Interrupt status	W1C	64'b0

4.3.5.41 por_mpam_ns_err_int_status

Provides HN-F MPAM Non-secure Error interrupt status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C38

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-173: por_mpam_ns_err_int_status

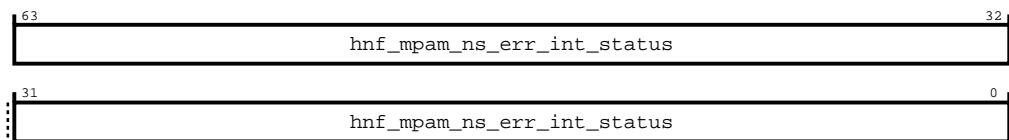


Table 4-189: por_mpam_ns_err_int_status attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_mpam_ns_err_int_status	MPAM NS Interrupt status	W1C	64'b0

4.3.5.42 por_mpam_ns_err_int_status_1

Provides HN-F MPAM Non-secure Error interrupt status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C40

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-174: por_mpam_ns_err_int_status_1

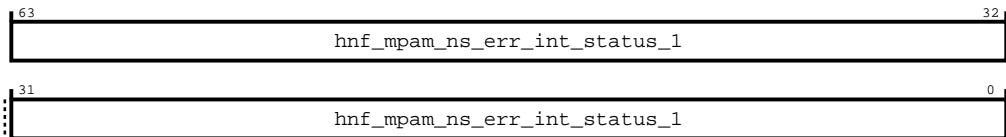


Table 4-190: por_mpam_ns_err_int_status_1 attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_mpam_ns_err_int_status_1	MPAM NS Interrupt status	W1C	64'b0

4.3.5.43 por_cfgm_child_pointer_0-255

There are 256 iterations of this register. The index ranges from 0 to 255. Contains base address of child configuration node. NOTE: There will be as many child pointer registers in the Global Config Unit as the number of XP's on the chip. Each successive child pointer register will be at the next 8 byte address boundary. Each successive child pointer register will be named with the suffix corresponding to the register number. For example `por_cfgm_child_pointer_<0:255>`

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h100 + #{8 * index}`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-175: por_cfgm_child_pointer_0-255

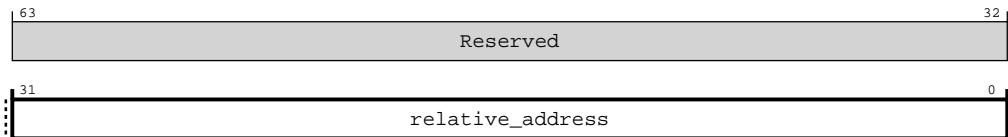


Table 4-191: por_cfgm_child_pointer_0-255 attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	relative_address	Bits: [31] External or internal child node [30] Set to 1'b0 Bits [29:0] Child node address offset relative to PERIPHBASE 1'b1 Indicates child pointer points to a configuration node that is external to CMN-700 1'b0 Indicates child pointer points to a configuration node that is internal to CMN-700	RO	32'b0

4.3.6 CXLAPB register descriptions

This section lists the CXLAPB registers.

4.3.6.1 por_cxlapb_link_rx_credit_ctl

CXL Link Rx Credit Control Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1110

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-176: por_cxlapb_link_rx_credit_ctl

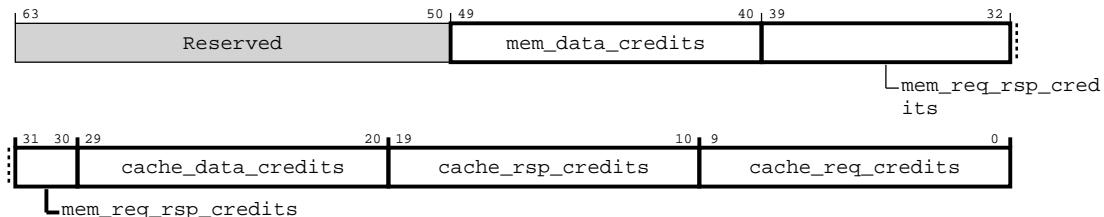


Table 4-192: por_cxlapb_link_rx_credit_ctl attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	mem_data_credits	Credits to advertise for Mem Data channel at init	RW	Configuration dependent
[39:30]	mem_req_rsp_credits	Credits to advertise for Mem Request or Response channel at init	RW	Configuration dependent
[29:20]	cache_data_credits	Credits to advertise for Cache Data channel at init	RW	Configuration dependent
[19:10]	cache_rsp_credits	Credits to advertise for Cache Response channel at init	RW	Configuration dependent
[9:0]	cache_req_credits	Credits to advertise for Cache Request channel at init	RW	Configuration dependent

4.3.6.2 por_cxlapb_link_rx_credit_return_stat

CXL Link Rx Credit Return Status Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1118

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-177: por_cxlapb_link_rx_credit_return_stat

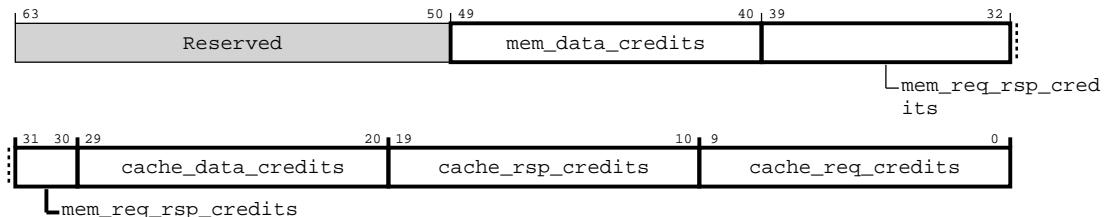


Table 4-193: por_cxlapb_link_rx_credit_return_stat attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	mem_data_credits	Running snapshot of accumulated Mem Data credits to be returned	RO	10'b0
[39:30]	mem_req_rsp_credits	Running snapshot of accumulated Mem Request or Response credits to be returned	RO	10'b0
[29:20]	cache_data_credits	Running snapshot of accumulated Cache Data credits to be returned	RO	10'b0
[19:10]	cache_rsp_credits	Running snapshot of accumulated Cache Response credits to be returned	RO	10'b0
[9:0]	cache_req_credits	Running snapshot of accumulated Cache Request credits to be returned	RO	10'b0

4.3.6.3 por_cxlapb_link_tx_credit_stat

CXL Link Tx Credit Status Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1120

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-178: por_cxlapb_link_tx_credit_stat

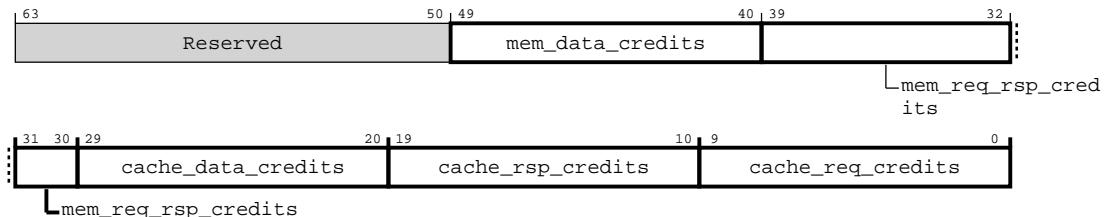


Table 4-194: por_cxlapb_link_tx_credit_stat attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	mem_data_credits	Running snapshot of accumulated Mem Data credits for TX	RO	10'b0
[39:30]	mem_req_rsp_credits	Running snapshot of accumulated Mem Request or Response credits for TX	RO	10'b0
[29:20]	cache_data_credits	Running snapshot of accumulated Cache Data credits for TX	RO	10'b0
[19:10]	cache_rsp_credits	Running snapshot of accumulated Cache Response credits for TX	RO	10'b0
[9:0]	cache_req_credits	Running snapshot of accumulated Cache Request credits for TX	RO	10'b0

4.3.6.4 por_cxlapb_cxl_security_policy

Contains CXL Security Policy

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1060

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-179: por_cxlapb_cxl_security_policy

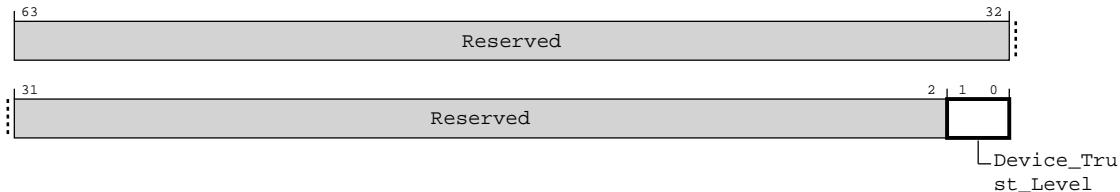


Table 4-195: por_cxlapb_cxl_security_policy attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	Device_Trust_Level	0 --> Trusted CXL Device. At this setting a CXL Device will be able to get access on CXL.cache for both host-attached and device attached memory ranges. The Host can still protect security sensitive memory regions. '1 --> Trusted for Device Attached Memory Range Only. At this setting a CXL Device will be able to get access on CXL.cache for device attached memory ranges only. Requests on CXL.cache for host-attached memory ranges will be aborted by the Host. '2 --> Untrusted CXL Device. At this setting all requests on CXL.cache will be aborted by the Host. Please note that these settings only apply to requests on CXL.cache. The device can still source requests on CXL.io regardless of these settings. Protection on CXL.io will be implemented using IOMMU based page tables. Default value of this field is 2.	RW	2'h2

4.3.6.5 por_cxlapb_cxl_hdm_decoder_capability

Contains CXL_HDM_Decoder_Capability_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1200

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-180: por_cxlapb_cxl_hdm_decoder_capability

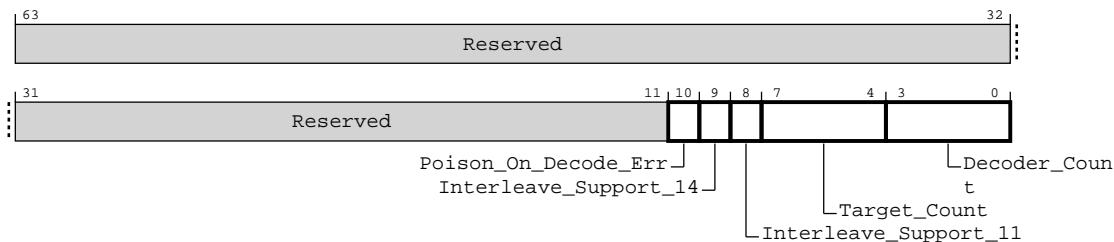


Table 4-196: por_cxlapb_cxl_hdm_decoder_capability attributes

Bits	Name	Description	Type	Reset
[63:11]	Reserved	Reserved	RO	-
[10]	Poison_On_Decode_Err	If set the component is capable of returning poison on read access to addresses that are not positively decoded by any HDM Decoders in this component. If clear the component is not capable of returning poison under such scenarios.	RO	1'h0
[9]	Interleave_Support_14	If set the component supports interleaving based on Address bit 14 Address bit 13 and Address bit 12. Root ports and switches shall always set this bit indicating support for interleaving based on Address bits 14-12.	RO	1'h0
[8]	Interleave_Support_11	If set the component supports interleaving based on Address bit 11 Address bit 10 Address bit 9 and Address bit 8. Root Ports and Upstream Switch Ports shall always set this bit indicating support for interleaving based on Address bit 11-8.	RO	1'h0
[7:4]	Target_Count	The number of target ports each decoder supports (applicable to Upstream Switch Port and Root Port only). Maximum of 8. 1 2 8 Other Reserved	RO	4'h1
[3:0]	Decoder_Count	Reports the number of memory address decoders implemented by the component. 0 1 2 3 4 5 Others 1 Decoder 2 Decoders 4 Decoders 6 Decoders 8 Decoders 10 Decoders Reserved	RO	4'h0

4.3.6.6 por_cxlapb_cxl_hdm_decoder_global_control

Contains CXL_HDM_Decoder_Global_Control_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1204

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-181: por_cxlapb_cxl_hdm_decoder_global_control

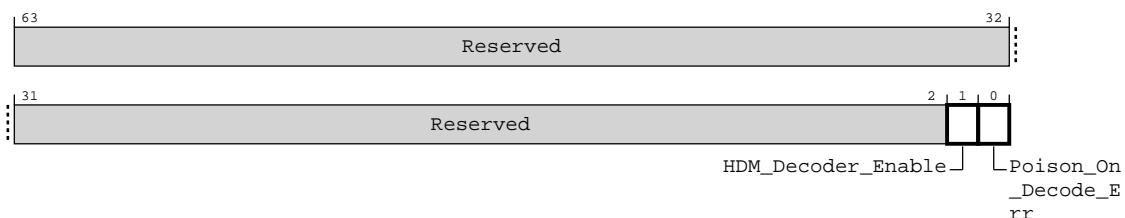


Table 4-197: por_cxlapb_cxl_hdm_decoder_global_control attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	HDM_Decoder_Enable	This bit is only applicable to CXL.mem devices and shall return 0 on Root Ports and Upstream Switch Ports. When this bit is set device shall use HDM decoders to decode CXL.mem transactions and not use HDM Base registers in DVSEC ID 0. Root Ports and Upstream Switch Ports always use HDM Decoders to decode CXL.mem transactions.	RW	1'h0
[0]	Poison_On_Decode_Error	This bit is RO and is hard-wired to 0 if Poison On Decode Error Capability=0. If set the component returns poison on read access to addresses that are not positively decoded by the component. If clear the component returns all 1s data without a poison under such scenarios.	RW	1'h0

4.3.6.7 por_cxlapb_cxl_hdm_decoder_0_base_low

Contains CXL_HDM_Decoder_0_Base_High_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1210

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-182: por_cxlapb_cxl_hdm_decoder_0_base_low

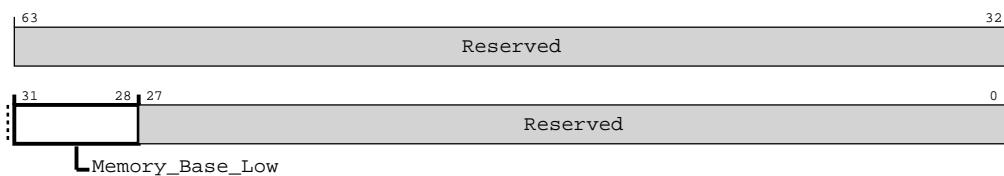


Table 4-198: por_cxlapb_cxl_hdm_decoder_0_base_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Base_Low	Corresponds to bits 31:28 of the base of the address range managed by decoder 0	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.6.8 por_cxlapb_cxl_hdm_decoder_0_base_high

Contains CXL_HDM_Decoder_0_Base_Low_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1214

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-183: por_cxlapb_cxl_hdm_decoder_0_base_high

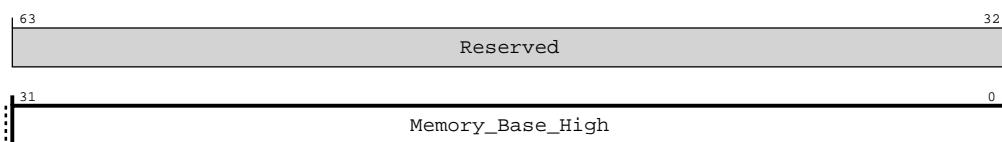


Table 4-199: por_cxlapb_cxl_hdm_decoder_0_base_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Base_High	Corresponds to bits 63:32 of the base of the address range managed by decoder 0.	RWL	32'h0

4.3.6.9 por_cxlapb_cxl_hdm_decoder_0_size_low

Contains CXL_HDM_Decoder_0_Size_Low_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1218

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-184: por_cxlapb_cxl_hdm_decoder_0_size_low

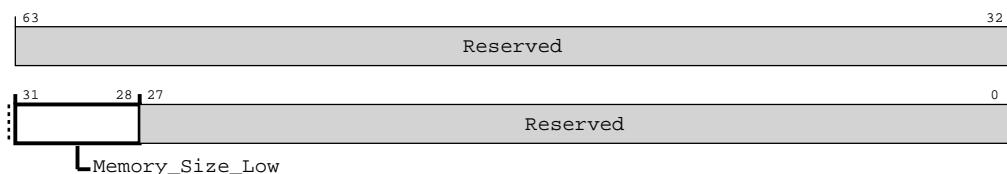


Table 4-200: por_cxlapb_cxl_hdm_decoder_0_size_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Size_Low	Corresponds to bits 31:28 of the size of the address range managed by decoder 0	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.6.10 por_cxlapb_cxl_hdm_decoder_0_size_high

Contains CXL_HDM_Decoder_0_Size_High_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h121C

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-185: por_cxlapb_cxl_hdm_decoder_0_size_high

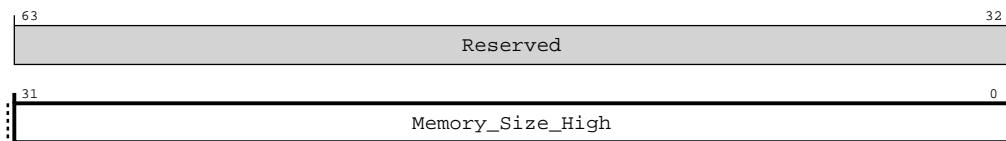


Table 4-201: por_cxlapb_cxl_hdm_decoder_0_size_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Size_High	Corresponds to bits 63:32 of the size of address range managed by decoder 0.	RWL	32'h0

4.3.6.11 por_cxlapb_cxl_hdm_decoder_0_control

Contains CXL_HDM_Decoder_0_Control_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1220

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-186: por_cxlapb_cxl_hdm_decoder_0_control

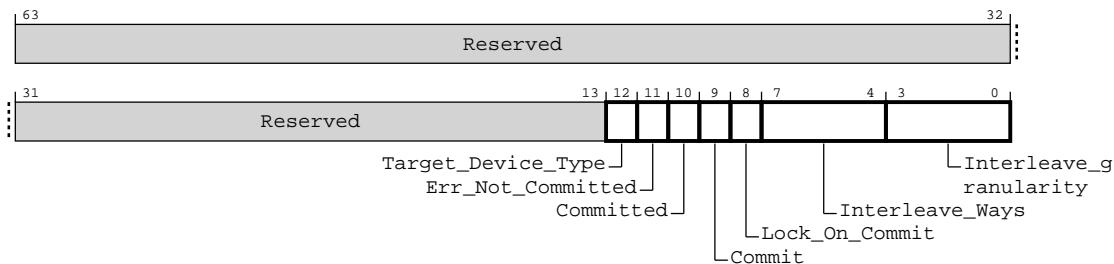


Table 4-202: por_cxlapb_cxl_hdm_decoder_0_control attributes

Bits	Name	Description	Type	Reset
[63:13]	Reserved	Reserved	RO	-
[12]	Target_Device_Type	<p>0 Target is a CXL Type 2 Device</p> <p>1 Target is a CXL Type 3 Device</p>	RWL	1'h0
[11]	Err_Not_Committed	Indicates the decode programming had an error and decoder is not active.	RWL	1'h0
[10]	Committed	Indicates the decoder is active	RWL	1'h0
[9]	Commit	Software sets this to 1 to commit this decoder	RWL	1'h0
[8]	Lock_On_Commit	If set all RWL fields in Decoder 0 registers will become read only when Committed changes to 1.	RWL	1'h0
[7:4]	Interleave_Ways	The number of targets across which this memory range is interleaved. 0 - 1 way 1 - 2 way 2 4 way 3 8 way All other reserved	RWL	4'h0
[3:0]	Interleave_granularity	<p>The number of consecutive bytes that are assigned to each target in the Target List.</p> <p>0 256 Bytes</p> <p>1 512 Bytes</p> <p>2 1024 Bytes (1KB)</p> <p>3 2048 Bytes (2KB)</p> <p>4 4096 Bytes (4KB)</p> <p>5 8192 Bytes (8 KB)</p> <p>6 16384 Bytes (16 KB)</p>	RWL	4'h0

4.3.6.12 por_cxlapb_cxl_hdm_decoder_0_dpa_skip_low

Contains CXL_HDM_Decoder_0_DPA_Skip_Low_Register. Only applicable for device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1224

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-187: por_cxlapb_cxl_hdm_decoder_0_dpa_skip_low

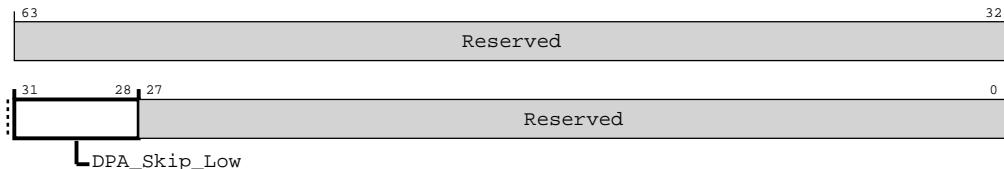


Table 4-203: por_cxlapb_cxl_hdm_decoder_0_dpa_skip_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	DPA_Skip_Low	Corresponds to bits 31:28 of the DPA Skip length which when non-zero specifies a length of DPA space that is skipped unmapped by any decoder prior to the HPA to DPA mapping provided by this decoder.	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.6.13 por_cxlapb_cxl_hdm_decoder_0_dpa_skip_high

Contains CXL_HDM_Decoder_0_DPA_Skip_High_Register. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1228

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-188: por_cxlapb_cxl_hdm_decoder_0_dpa_skip_high

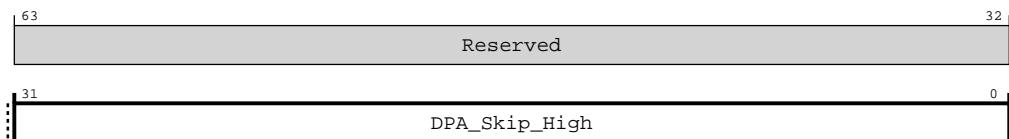


Table 4-204: por_cxlapb_cxl_hdm_decoder_0_dpa_skip_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	DPA_Skip_High	Corresponds to bits 63:32 of the DPA Skip length which when non-zero specifies a length of DPA space that is skipped unmapped by any decoder prior to the HPA to DPA mapping provided by this decoder.	RWL	32'h0

4.3.6.14 por_cxlapb_snoop_filter_group_id

Contains Snoop_Filter_Group_ID

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1800

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-189: por_cxlapb_snoop_filter_group_id

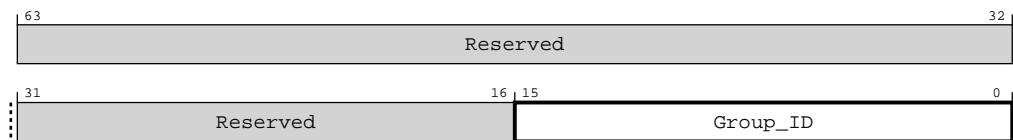


Table 4-205: por_cxlapb_snoop_filter_group_id attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	Group_ID	Uniquely identifies a snoop filter instance that is used to track CXL.cache devices below this Port. All Ports that share a single Snoop Filter instance shall set this field to the same value.	RO	16'h0

4.3.6.15 por_cxlapb_snoop_filter_effective_size

Contains Snoop_Filter_Effective_Size

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1804

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-190: por_cxlapb_snoop_filter_effective_size

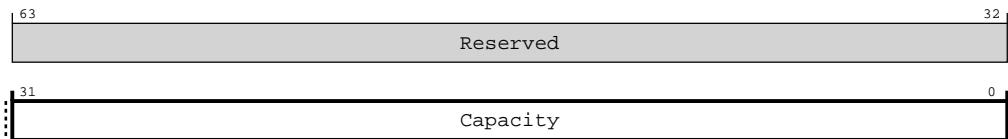


Table 4-206: por_cxlapb_snoop_filter_effective_size attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Capacity	Effective Snoop Filter Capacity representing the size of cache that can be effectively tracked by the Snoop Filter with this Group ID in multiples of 64K.	RO	32'h0

4.3.6.16 por_cxlapb_dvsec_cxl_range_1_base_high

Contains DVSEC_CXL_Range_1_Base_High. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h120

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-191: por_cxlapb_dvsec_cxl_range_1_base_high

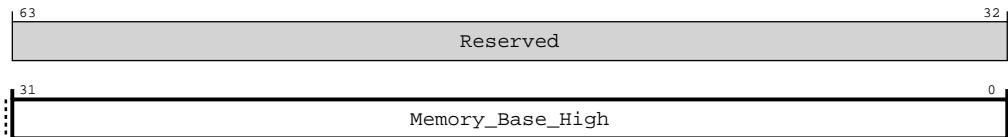


Table 4-207: por_cxlapb_dvsec_cxl_range_1_base_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Base_High	Corresponds to bits 63:32 of CXL Range 1 base in the host address space. Locked by CONFIG_LOCK. If a device implements CXL HDM Decoder Capability registers and software has enabled HDM Decoder by setting HDM Decoder Enable bit in CXL HDM Decoder Global Control register the value of this field is not used during address decode. It is recommended that software program this to match CXL HDM Decoder 0 Base High Register for backward compatibility reasons.	RWL	32'h0

4.3.6.17 por_cxlapb_dvsec_cxl_range_1_base_low

Contains DVSEC_CXL_Range_1_Base_Low. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h124

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-192: por_cxlapb_dvsec_cxl_range_1_base_low

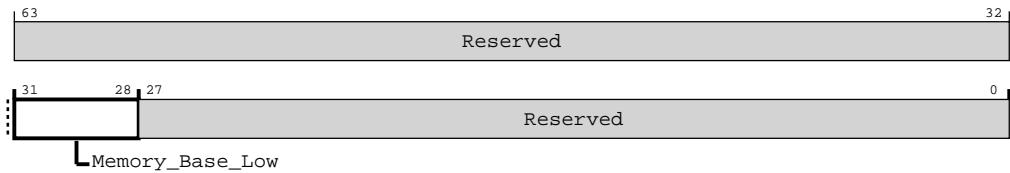


Table 4-208: por_cxlapb_dvsec_cxl_range_1_base_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Base_Low	Corresponds to bits 31:28 of CXL Range 1 base in the host address space. Locked by CONFIG_LOCK. If a device implements CXL HDM Decoder Capability registers and software has enabled HDM Decoder by setting HDM Decoder Enable bit in CXL HDM Decoder Global Control register the value of this field is not used during address decode. It is recommended that software program this to match CXL HDM Decoder 0 Base Low Register for backward compatibility reasons.	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.6.18 por_cxlapb_dvsec_cxl_range_2_base_high

Contains DVSEC_CXL_Range_2_Base_High. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h130

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-193: por_cxlapb_dvsec_cxl_range_2_base_high

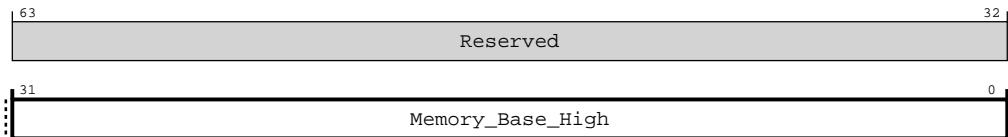


Table 4-209: por_cxlapb_dvsec_cxl_range_2_base_high attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Memory_Base_High	Corresponds to bits 63:32 of CXL Range 2 base in the host address space. Locked by CONFIG_LOCK. If a device implements CXL HDM Decoder Capability registers and software has enabled HDM Decoder by setting HDM Decoder Enable bit in CXL HDM Decoder Global Control register the value of this field is not used during address decode. It is recommended that software program this to match the corresponding CXL HDM Decoder Base High Register for backward compatibility reasons.	RWL	32'h0

4.3.6.19 por_cxlapb_dvsec_cxl_range_2_base_low

Contains DVSEC_CXL_Range_2_Base_Low. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h134

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-194: por_cxlapb_dvsec_cxl_range_2_base_low

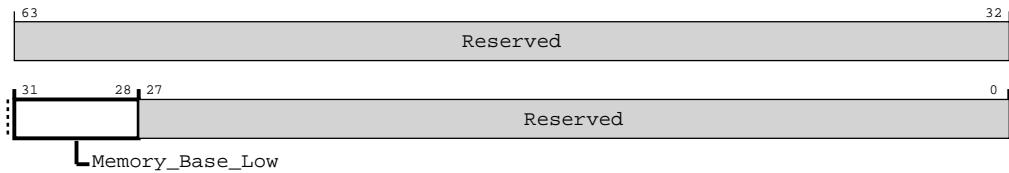


Table 4-210: por_cxlapb_dvsec_cxl_range_2_base_low attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	Memory_Base_Low	Corresponds to bits 31:28 of CXL Range 2 base in the host address space. Locked by CONFIG_LOCK	RWL	4'h0
[27:0]	Reserved	Reserved	RO	-

4.3.6.20 por_cxlapb_dvsec_cxl_control

Contains DVSEC_CXL_Control. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h10C

Type

RWL

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-195: por_cxlapb_dvsec_cxl_control

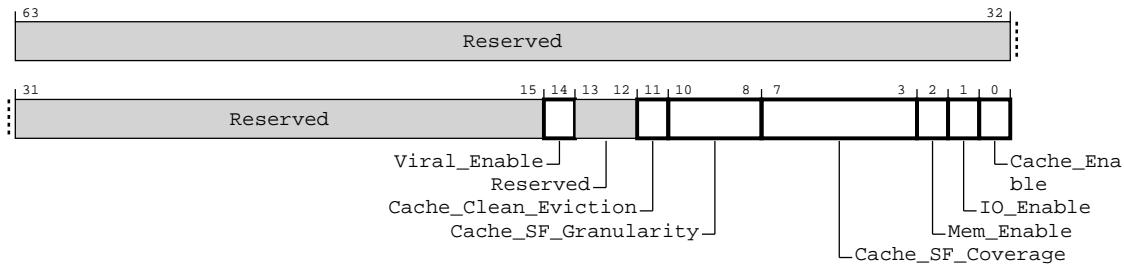


Table 4-211: por_cxlapb_dvsec_cxl_control attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14]	Viral_Enable	When set enables Viral handling in the CXL device. Locked by CONFIG_LOCK. If 0 the CXL device may ignore the viral that it receives	RWL	1'h0
[13:12]	Reserved	Reserved	RO	-
[11]	Cache_Clean_Eviction	Performance hint to the device. Locked by CONFIG_LOCK. 0 Indicates clean evictions from device caches are needed for best performance 1 Indicates clean evictions from device caches are NOT needed for best performance	RWL	1'h0
[10:8]	Cache_SF_Granularity	Performance hint to the device. Locked by CONFIG_LOCK. 000 Indicates 64B granular tracking on the Host 001 Indicates 128B granular tracking on the Host 010 Indicates 256B granular tracking on the Host 011 Indicates 512B granular tracking on the Host 100 Indicates 1KB granular tracking on the Host 101 Indicates 2KB granular tracking on the Host 110 Indicates 4KB granular tracking on the Host 111 Reserved	RWL	3'h0
[7:3]	Cache_SF_Coverage	Performance hint to the device. Locked by CONFIG_LOCK. 0x00: Indicates no Snoop Filter coverage on the Host For all other values of N: Indicates Snoop Filter coverage on the Host of $2^{(N+15d)}$ Bytes.	RWL	5'h0
[2]	Mem_Enable	When set enables CXL.mem protocol operation when in Flex Bus.CXL mode. Locked by CONFIG_LOCK.	RWL	1'h0
[1]	IO_Enable	When set enables CXL.io protocol operation when in Flex Bus.CXL mode.	RWL	1'h1
[0]	Cache_Enable	When set enables CXL.cache protocol operation when in Flex Bus.CXL mode. Locked by CONFIG_LOCK.	RWL	1'h0

4.3.6.21 por_cxlapb_dvsec_cxl_control2

Contains DVSEC_CXL_Control2. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h110

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-196: por_cxlapb_dvsec_cxl_control2

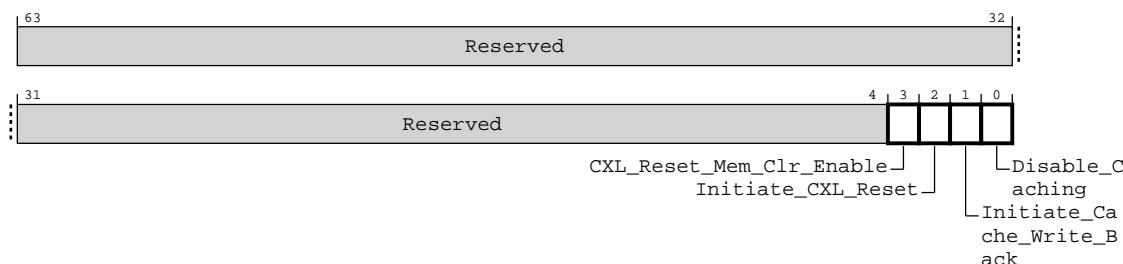


Table 4-212: por_cxlapb_dvsec_cxl_control2 attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	CXL_Reset_Mem_Clr_Enable	When set and CXL Reset Mem Clr Capable returns 1 Device shall clear or randomize volatile HDM ranges as part of the CXL Reset operation. When CXL Reset Mem Clr Capable is clear this bit is ignored and volatile HDM ranges may or may not be cleared or randomized during CXL Reset.	RW	1'h0
[2]	Initiate_CXL_Reset	When set to 1 device shall initiate CXL Reset as defined in Section 9.7. This bit always returns the value of 0 when read by the software. A write of 0 is ignored.	RW	1'h0
[1]	Initiate_Cache_Write_Back	When set to 1 device shall write back all modified lines in the local cache and invalidate all lines. The device shall send CacheFlushed message to host as required by CXL.Cache protocol to indicate it does not hold any modified lines.	RW	1'h0
[0]	Disable_Caching	When set to 1 device shall no longer cache new modified lines in its local cache. Device shall continue to correctly respond to CXL.cache transactions.	RW	1'h0

4.3.6.22 por_cxlapp_dvsec_cxl_lock

Contains DVSEC_CXL_Lock. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h114

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-197: por_cxlapp_dvsec_cxl_lock

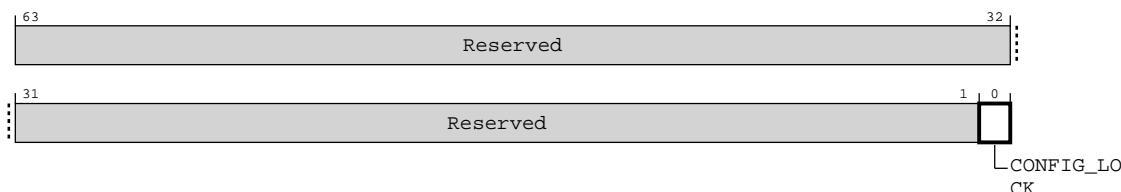


Table 4-213: por_cxlapp_dvsec_cxl_lock attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	CONFIG_LOCK	When set all register fields in the PCIe DVSEC for CXL Devices Capability with RWL attribute become read only. Consult individual register fields for details. This bit is cleared upon device Conventional Reset. This bit and all the fields that are locked by this bit are not affected by CXL Reset.	RW	1'h0

4.3.6.23 por_cxlapb_dvsec_flex_bus_port_control

Contains DVSEC_Flex_Bus_Port_Control

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h20C

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-198: por_cxlapb_dvsec_flex_bus_port_control

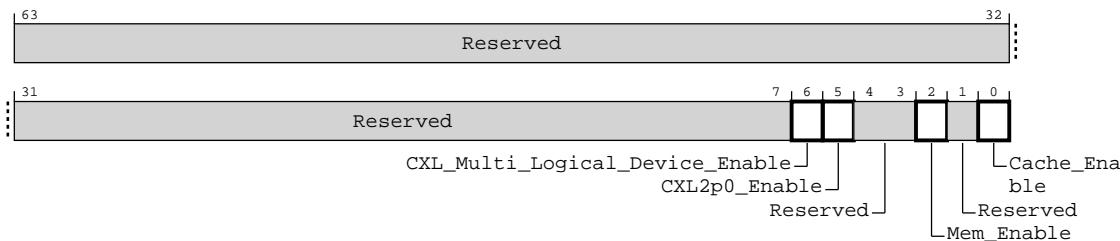


Table 4-214: por_cxlapb_dvsec_flex_bus_port_control attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6]	CXL_Multi_Logical_Device_Enable	When set enable Multi-Logical Device operation when in Flex Bus.CXL mode	RW	1'h0
[5]	CXL2p0_Enable	When set enable CXL2.0 protocol operation when in Flex Bus.CXL mode.	RW	1'h0
[4:3]	Reserved	Reserved	RO	-
[2]	Mem_Enable	When set enables CXL.mem protocol operation when in Flex Bus.CXL mode.	RW	1'h0
[1]	Reserved	Reserved	RO	-
[0]	Cache_Enable	When set enables CXL.cache protocol operation when in Flex Bus.CXL mode.	RW	1'h0

4.3.6.24 por_cxlapp_err_capabilities_control

Contains err_capabilities_control. Only applicable for Device. Host does not use this register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1014

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-199: por_cxlapp_err_capabilities_control

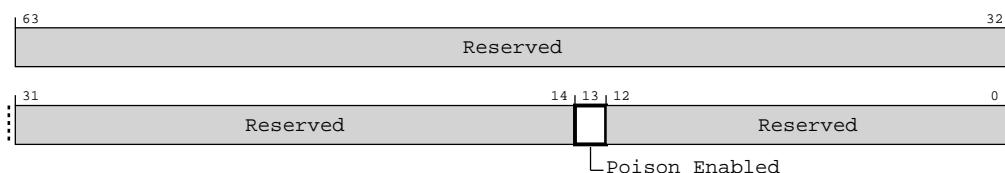


Table 4-215: por_cxlapp_err_capabilities_control attributes

Bits	Name	Description	Type	Reset
[63:14]	Reserved	Reserved	RO	-
[13]	Poison_Enabled	If this bit is 0 CXL 1.1 Upstream Ports CXL 1.1 Downstream Ports and CXL 2.0 Root Port shall treat poison received on CXL.cache or CXL.mem as uncorrectable error and log the error in Uncorrectable Error Status Register. If this bit is 1 these ports shall treat poison received on CXL.cache or CXL.mem as correctable error and log the error in Correctable Error Status Register. This bit defaults to 1. This bit is hardwired to 1 in CXL 2.0 Upstream Switch Port CXL 2.0 Downstream Switch Port and CXL 2.0 device.	RW	1'h0
[12:0]	Reserved	Reserved	RO	-

4.3.6.25 por_cxlapp_IDE_key_refresh_time_control

Contains IDE_key_refresh_time_control. Not applicable to CMN 700

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h18

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-200: por_cxlapp_IDE_key_refresh_time_control

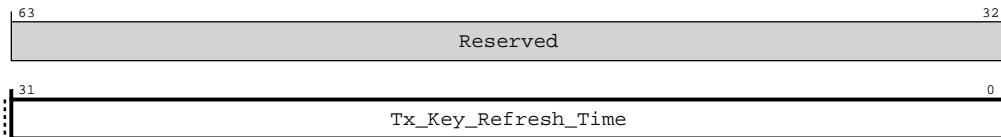


Table 4-216: por_cxlapp_IDE_key_refresh_time_control attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	Tx_Key_Refresh_Time	Minimum number of flits transmitter needs to block transmission of protocol flits after IDE.Start has sent. Used when switching keys.	RW	32'h0

4.3.6.26 por_cxlapp_IDE_truncation_transmit_delay_control

Contains IDE_truncation_transmit_delay_control. Not applicable to CMN 700

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h24

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-201: por_cxlapb_IDE_truncation_transmit_delay_control

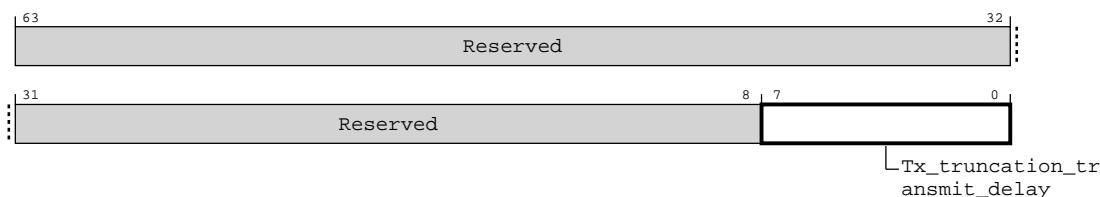


Table 4-217: por_cxlapb_IDE_truncation_transmit_delay_control attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7:0]	Tx_truncation_transmit_delay	This parameter feeds into the computation of minimum number of IDE idle flits Transmitter needs send after sending a truncated MAC flit.	RW	8'h0

4.3.6.27 por_cxlapb_ll_to_ull_msg

Contains ll_to_ull_message

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-202: por_cxlapb_ll_to_ull_msg

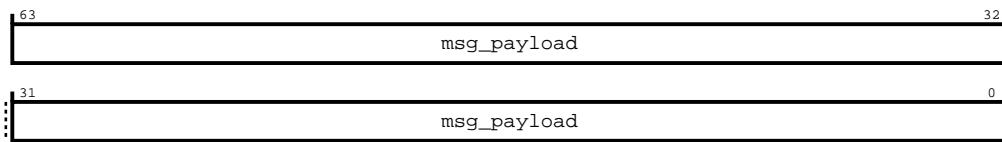


Table 4-218: por_cxlapb_ll_to_ull_msg attributes

Bits	Name	Description	Type	Reset
[63:0]	msg_payload	Contains 64 bits of message sent from ll to ull	RW	64'h0

4.3.6.28 por_cxlapb_cxl_timeout_isolation_control

Contains `cxl_timeout_isolation_control`. Not applicable to CMN 700

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h8`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-203: por_cxlapb_cxl_timeout_isolation_control

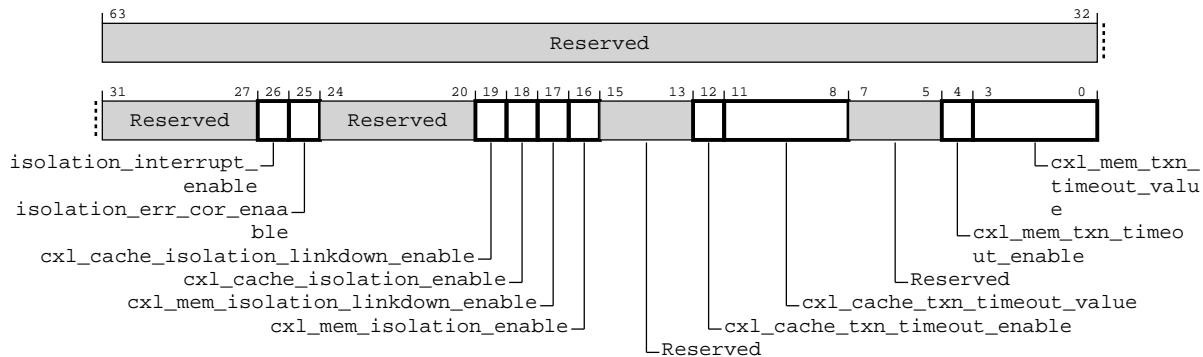


Table 4-219: por_cxlapb_cxl_timeout_isolation_control attributes

Bits	Name	Description	Type	Reset
[63:27]	Reserved	Reserved	RO	-
[26]	isolation_interrupt_enable	When Set this bit enables the generation of an interrupt to indicate that Isolation has been triggered.	RW	1'h0
[25]	isolation_err_cor_enaa	When Set this bit enables the sending of an ERR_COR Message to indicate Isolation has been triggered.	RW	1'h0
[24:20]	Reserved	Reserved	RO	-
[19]	cxl_cache_isolation_linkdown_enable	This field allows System Software to trigger link down on the CXL Root Port if CXL.cache enters Isolation mode.	RW	1'h0
[18]	cxl_cache_isolation_enable	This field allows System Software to enable CXL.cache Isolation actions.	RW	1'h0
[17]	cxl_mem_isolation_linkdown_enable	This field allows System Software to trigger link down on the CXL Root Port if CXL.mem enters Isolation mode.	RW	1'h0
[16]	cxl_mem_isolation_enable	This field allows System Software to enable CXL.mem Isolation actions. If this field is set Isolation actions will be triggered if either a CXL.mem Transaction Timeout is detected or if the CXL link went down.	RW	1'h0
[15:13]	Reserved	Reserved	RO	-
[12]	cxl_cache_txn_timeout_enable	-	RW	1'h0
[11:8]	cxl_cache_txn_timeout_value	In CXL Root Port Functions that support Transaction Timeout programmability this field allows system software to modify the Transaction Timeout Value for CXL.cache.	RW	4'h0
[7:5]	Reserved	Reserved	RO	-
[4]	cxl_mem_txn_timeout_enable	When Set this bit enables CXL.mem Transaction Timeout mechanism.	RW	1'h0
[3:0]	cxl_mem_txn_timeout_value	In CXL Root Port Functions that support Transaction Timeout programmability this field allows system software to modify the Transaction Timeout Value for CXL.mem.	RW	4'h0

4.3.6.29 por_cxlapb_link_layer_defeature

CXL Link Layer Defeature Register

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1130

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-204: por_cxlapb_link_layer_defeature

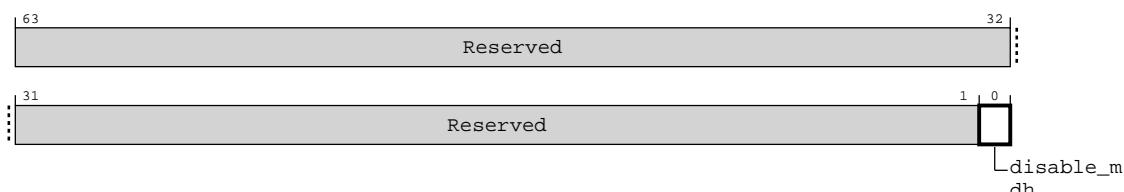


Table 4-220: por_cxlapb_link_layer_defeature attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	disable_mdh	Write 1 to disable MDH. Software needs to ensure it programs this value consistently on the UP & DP. After programming, a warm reset is required for the disable to take effect.	RW	1'b0

4.3.7 Debug and trace register descriptions

This section lists the debug and trace registers.

4.3.7.1 por_dt_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-205: por_dt_node_info

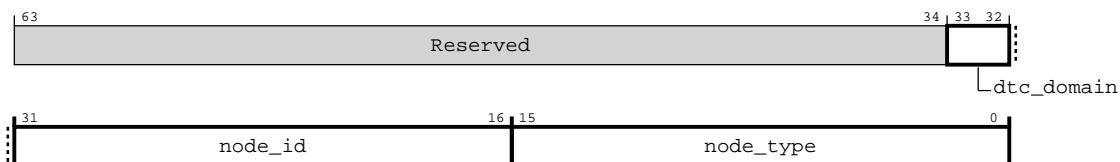


Table 4-221: por_dt_node_info attributes

Bits	Name	Description	Type	Reset
[63:34]	Reserved	Reserved	RO	-
[33:32]	dtc_domain	DTC domain number	RO	Configuration dependent
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h3

4.3.7.2 por_dt_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-206: por_dt_child_info

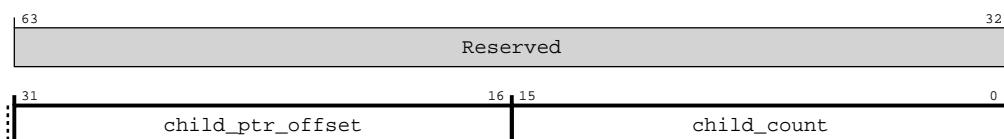


Table 4-222: por_dt_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0000
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.7.3 por_dt_secure_access

Functions as the Secure access control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-207: por_dt_secure_access

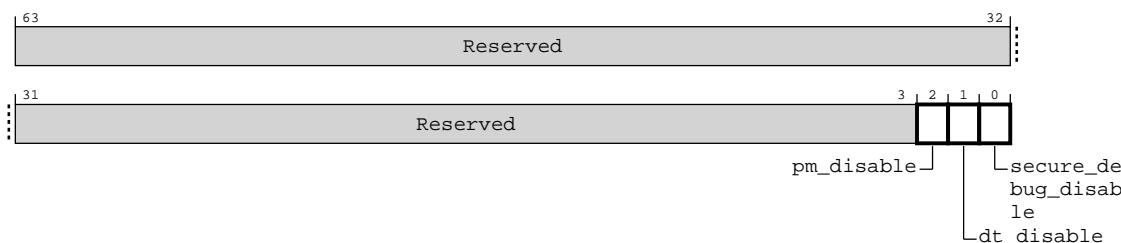


Table 4-223: por_dt_secure_access attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	pm_disable	PMU disable 1'b0 PMU function is not affected 1'b1 PMU function is disabled.	RW	1'b0
[1]	dt_disable	Debug disable 1'b0 DT function is not affected 1'b1 DT function is disabled.	RW	1'b0
[0]	secure_debug_disable	Secure debug disable 1'b0 Secure events are monitored by the PMU 1'b1 Secure events are only monitored by the PMU if SPNIDEN is set to 1	RW	1'b0

4.3.7.4 por_dt_dtc_ctl

Functions as the debug trace control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-208: por dt dtc ctl

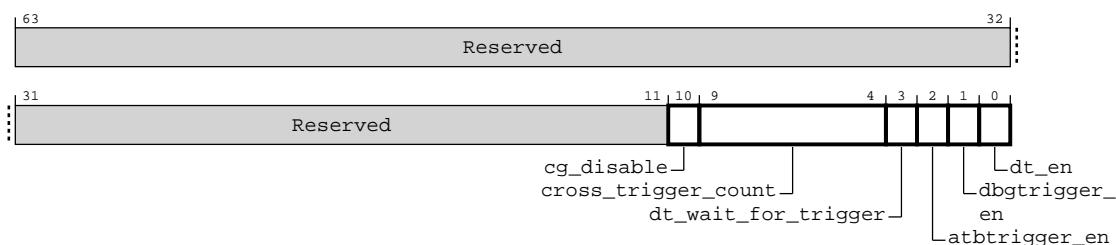


Table 4-224: por_dt_dtc_ctl attributes

Bits	Name	Description	Type	Reset
[63:11]	Reserved	Reserved	RO	-
[10]	cg_disable	Disables DT architectural clock gates	RW	1'b0
[9:4]	cross_trigger_count	Number of cross triggers received before trace enable NOTE: Only applicable if dt_wait_for_trigger is set to 1.	RW	6'b0
[3]	dt_wait_for_trigger	Enables waiting for cross trigger before trace enable	RW	1'b0
[2]	atbtrigger_en	ATB trigger enable	RW	1'b0
[1]	dbgtrigger_en	DBGWATCHTRIG enable	RW	1'b0
[0]	dt_en	Enables debug, trace, and PMU features	RW	1'b0

4.3.7.5 por_dt_trigger_status

Provides the trigger status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA10

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-209: por_dt_trigger_status

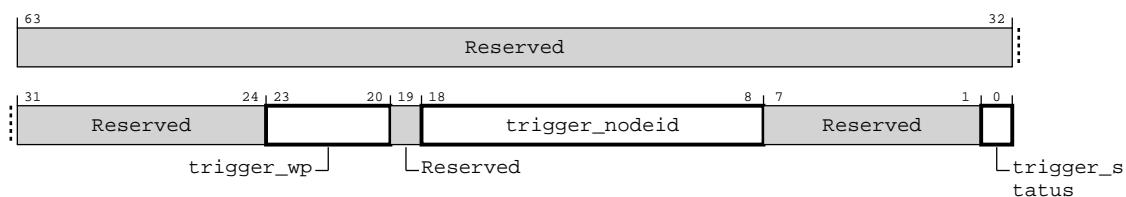


Table 4-225: por_dt_trigger_status attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:20]	trigger_wp	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by watchpoint	RO	1'h0
[19]	Reserved	Reserved	RO	-
[18:8]	trigger_nodeid	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by node ID	RO	11'h0
[7:1]	Reserved	Reserved	RO	-
[0]	trigger_status	Indicates DBGWATCHTRIGREQ assertion and/or ATB trigger	RO	1'h0

4.3.7.6 por_dt_trigger_status_clr

Clears the trigger status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA20

Type

WO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-210: por_dt_trigger_status_clr

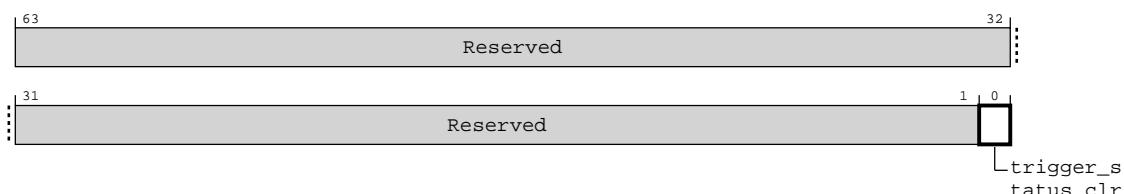


Table 4-226: por_dt_trigger_status_clr attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	trigger_status_clr	Write a 1 to clear por_dt_trigger_status.trigger_status	WO	1'b0

4.3.7.7 por_dt_trace_control

Functions as the trace control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA30

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-211: por_dt_trace_control

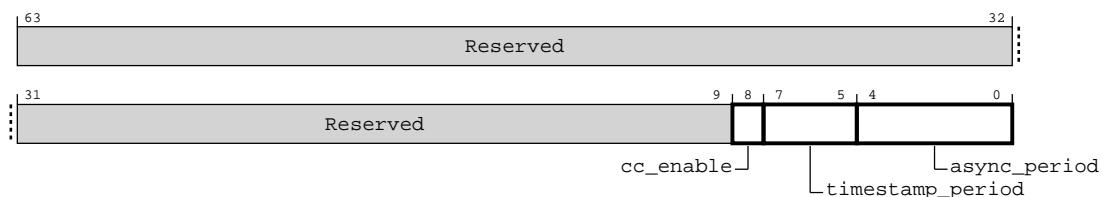


Table 4-227: por_dt_trace_control attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	cc_enable	Cycle count enable	RW	1'b0
[7:5]	timestamp_period	Time stamp packet insertion period 3'b000: Time stamp disabled 3'b011: Time stamp every 8K clock cycles 3'b100: Time stamp every 16K clock cycles 3'b101: Time stamp every 32K clock cycles 3'b110: Time stamp every 64K clock cycles	RW	3'b0
[4:0]	async_period	Alignment sync packet insertion period 5'h00: Alignment sync disabled 5'h08: Alignment sync inserted after 256B of trace 5'h09: Alignment sync inserted after 512B of trace 5'h14: Alignment sync inserted after 1048576B of trace NOTE: All other values are reserved.	RW	5'b0

4.3.7.8 por_dt_traceid

Contains the ATB ID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA48

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-212: por_dt_traceid

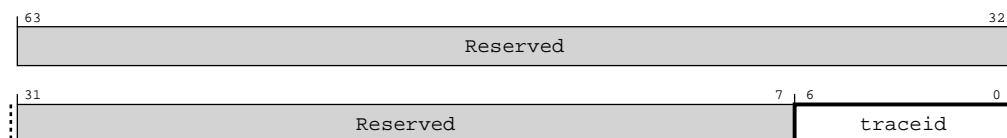


Table 4-228: por_dt_traceid attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6:0]	traceid	ATB ID	RW	7'h0

4.3.7.9 por_dt_pmevcntAB

Contains the PMU event counters A and B.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-213: por_dt_pmevcntAB

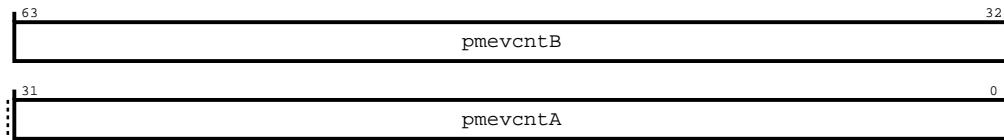


Table 4-229: por_dt_pmevcntAB attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntB	PMU counter B	RW	32'h0000
[31:0]	pmevcntA	PMU counter A	RW	32'h0000

4.3.7.10 por_dt_pmevcntCD

Contains the PMU event counters C and D.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2010

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-214: por_dt_pmevcntCD

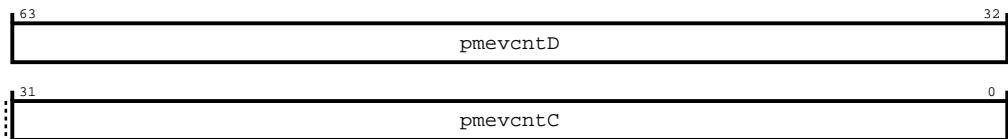


Table 4-230: por_dt_pmevcntCD attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntD	PMU counter D	RW	32'h0000
[31:0]	pmevcntC	PMU counter C	RW	32'h0000

4.3.7.11 por_dt_pmevcntEF

Contains the PMU event counters E and F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2020

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-215: por_dt_pmevcntEF

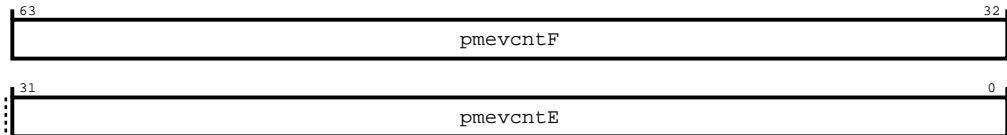


Table 4-231: por_dt_pmevcntEF attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntF	PMU counter F	RW	32'h0000
[31:0]	pmevcntE	PMU counter E	RW	32'h0000

4.3.7.12 por_dt_pmevcntGH

Contains the PMU event counters G and H.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2030

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-216: por_dt_pmevcntGH

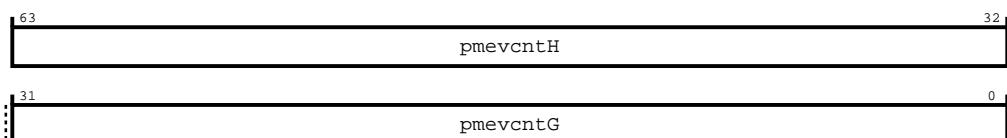


Table 4-232: por_dt_pmevcntGH attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntH	PMU counter H	RW	32'h0000
[31:0]	pmevcntG	PMU counter G	RW	32'h0000

4.3.7.13 por_dt_pmccntr

Contains the PMU cycle counter.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2040

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-217: por_dt_pmccntr

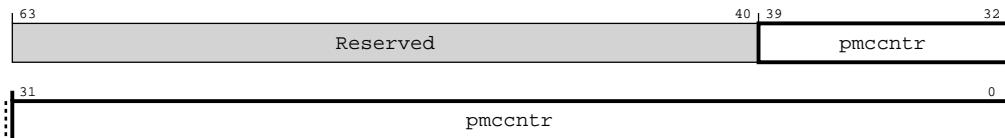


Table 4-233: por_dt_pmccntr attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:0]	pmccntr	PMU cycle counter	RW	40'h0

4.3.7.14 por_dt_pmevcntsrAB

Contains the PMU event counter shadow registers A and B.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2050

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-218: por_dt_pmevcntsrAB

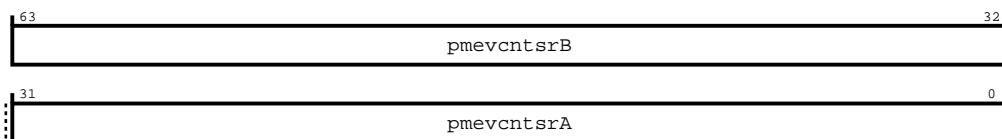


Table 4-234: por_dt_pmevcntsrAB attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntsrB	PMU counter B shadow register	RW	32'h0000
[31:0]	pmevcntsrA	PMU counter A shadow register	RW	32'h0000

4.3.7.15 por_dt_pmevcntsrCD

Contains the PMU event counter shadow registers C and D.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2060

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-219: por_dt_pmevcntsrCD

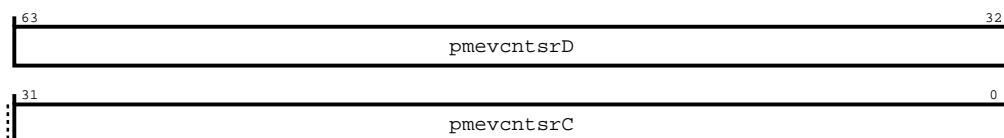


Table 4-235: por_dt_pmevcntsrCD attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntsrD	PMU counter D shadow register	RW	32'h0000
[31:0]	pmevcntsrC	PMU counter C shadow register	RW	32'h0000

4.3.7.16 por_dt_pmevcntsrEF

Contains the PMU event counter shadow registers E and F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2070

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-220: por_dt_pmevcntsrEF

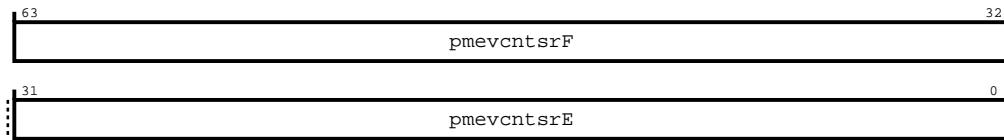


Table 4-236: por_dt_pmevcntsrEF attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntsrF	PMU counter F shadow register	RW	32'h0000
[31:0]	pmevcntsrE	PMU counter E shadow register	RW	32'h0000

4.3.7.17 por_dt_pmevcntsrGH

Contains the PMU event counter shadow registers G and H.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2080

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-221: por_dt_pmevcntsrGH

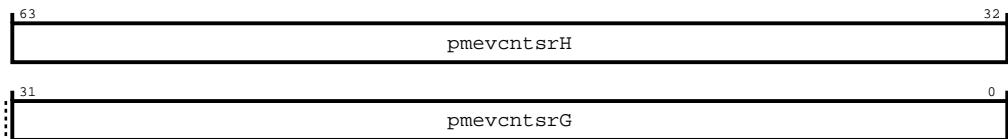


Table 4-237: por_dt_pmevcntsrGH attributes

Bits	Name	Description	Type	Reset
[63:32]	pmevcntsrH	PMU counter H shadow register	RW	32'h0000
[31:0]	pmevcntsrG	PMU counter G shadow register	RW	32'h0000

4.3.7.18 por_dt_pmccntrs

Contains the PMU cycle counter shadow register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2090

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-222: por_dt_pmccntrs

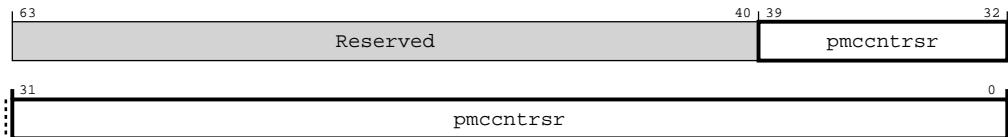


Table 4-238: por_dt_pmccntrs attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:0]	pmccntrs	PMU cycle counter shadow register	RW	40'h0

4.3.7.19 por_dt_pmc

Functions as the PMU control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2100

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-223: por_dt_pmcr

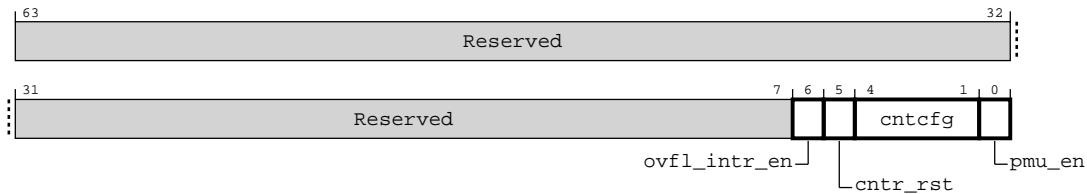


Table 4-239: por_dt_pmcr attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6]	ovfl_intr_en	Enables INTREQPMU assertion on PMU counter overflow	RW	1'h0
[5]	cntr_rst	Enables clearing of live counters upon assertion of por_dt_pmsrr.ss_req or PMUSNAPSHOTREQ	RW	1'h0
[4:1]	cntcfg	Groups adjacent 32-bit registers into a 64-bit register	RW	4'h0
[0]	pmu_en	Enables PMU features	RW	1'b0

4.3.7.20 por_dt_pmovsr

Provides the PMU overflow status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2118

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-224: por_dt_pmovsr

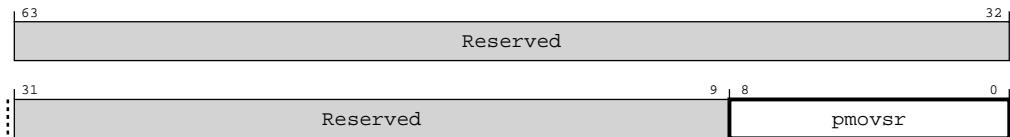


Table 4-240: por_dt_pmovsr attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8:0]	pmovsr	PMU overflow status Bit 8: Indicates overflow from cycle counter Bits [7:0]: Indicates overflow from counters 7 to 0	RO	9'h0

4.3.7.21 por_dt_pmovsr_clr

Clears the PMU overflow status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2120

Type

WO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-225: por_dt_pmovsr_clr

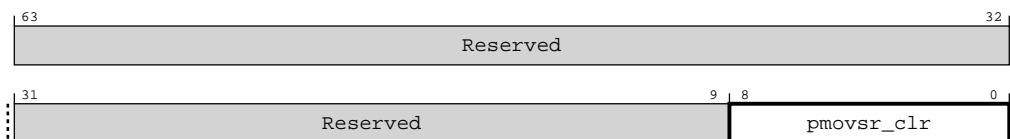


Table 4-241: por_dt_pmovsr_clr attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8:0]	pmovsr_clr	Write a 1 to clear the corresponding bit in por_dt_pmovsr.pmovsr	WO	9'b0

4.3.7.22 por_dt_pmssr

Provides the PMU snapshot status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2128

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-226: por_dt_pmssr

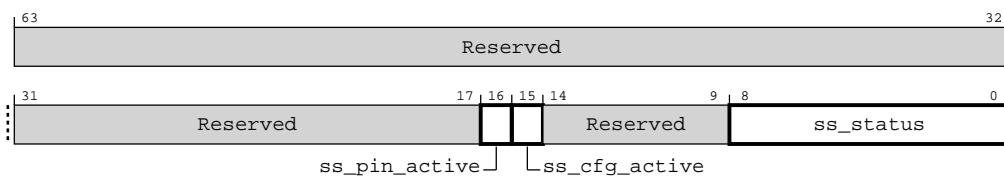


Table 4-242: por_dt_pmssr attributes

Bits	Name	Description	Type	Reset
[63:17]	Reserved	Reserved	RO	-
[16]	ss_pin_active	Activates PMU snapshot from PMUSNAPSHOTREQ	RO	1'b0
[15]	ss_cfg_active	PMU snapshot activated from configuration write	RO	1'b0
[14:9]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[8:0]	ss_status	PMU snapshot status Bit 8: Indicates snapshot status for cycle counter Bits [7:0]: Indicates snapshot status for counters 7 to 0	RO	9'b0

4.3.7.23 por_dt_pmsrr

Sends PMU snapshot requests.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2130

Type

WO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-227: por_dt_pmsrr

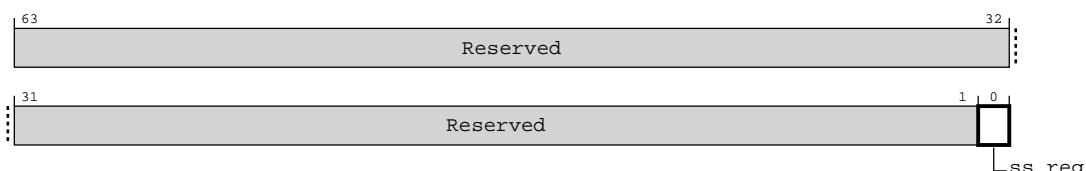


Table 4-243: por_dt_pmsrr attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	ss_req	Write a 1 to request PMU snapshot	WO	1'b0

4.3.7.24 por_dt_claim

Functions as the claim tag set register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFA0

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-228: por_dt_claim

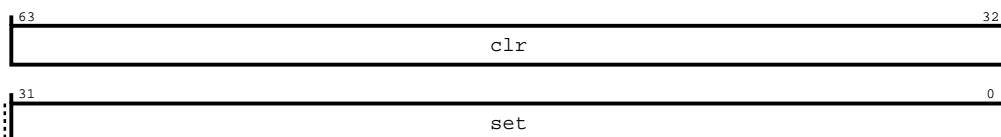


Table 4-244: por_dt_claim attributes

Bits	Name	Description	Type	Reset
[63:32]	clr	Upper half of the claim tag value; enables individual bits to be cleared (write) and returns the current claim tag value (read)	RW	32'b0
[31:0]	set	Lower half of the claim tag value; allows individual bits to be set (write) and returns the number of bits that can be set (read)	RW	32'hfffffff

4.3.7.25 por_dt_devaff

Functions as the device affinity register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFA8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-229: por_dt_devaff

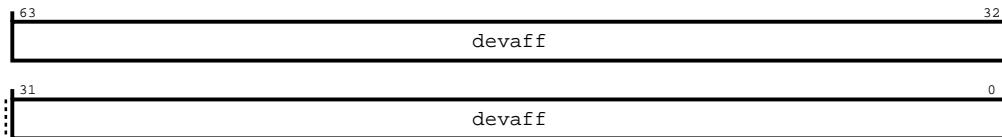


Table 4-245: por_dt_devaff attributes

Bits	Name	Description	Type	Reset
[63:0]	devaff	Device affinity register	RO	64'b0

4.3.7.26 por_dt_lsr

Functions as the lock status register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFB0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-230: por_dt_lsr

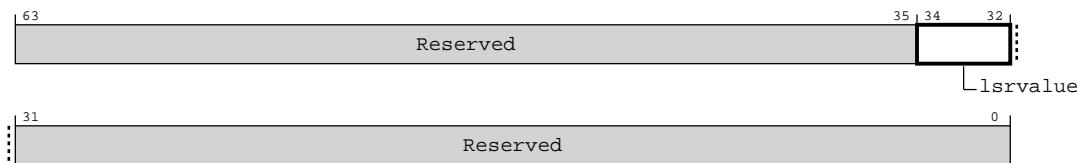


Table 4-246: por_dt_lsr attributes

Bits	Name	Description	Type	Reset
[63:35]	Reserved	Reserved	RO	-
[34:32]	lsrvvalue	Lock status value	RO	3'b0
[31:0]	Reserved	Reserved	RO	-

4.3.7.27 por_dt_authstatus_devarch

Functions as the authentication status register and the device architecture register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFB8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-231: por_dt_authstatus_devarch

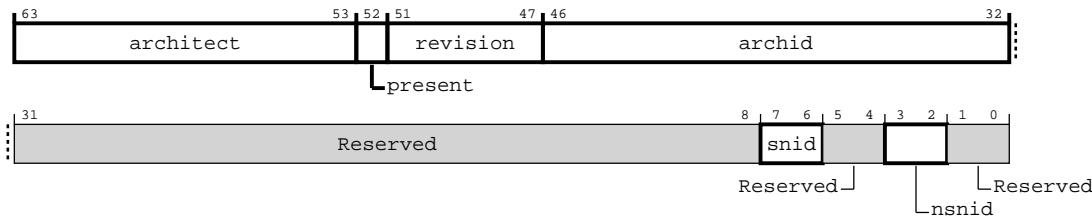


Table 4-247: por_dt_authstatus_devarch attributes

Bits	Name	Description	Type	Reset
[63:53]	architect	Architect	RO	11'b0
[52]	present	Present	RO	1'b1
[51:47]	revision	Architecture revision	RO	6'b0
[46:32]	archid	Architecture ID	RO	16'b0
[31:8]	Reserved	Reserved	RO	-
[7:6]	snid	Secure non-invasive debug	RO	2'b10
[5:4]	Reserved	Reserved	RO	-
[3:2]	nsnid	Non-secure non-invasive debug	RO	2'b10
[1:0]	Reserved	Reserved	RO	-

4.3.7.28 por_dt_devid

Functions as the device configuration register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFC0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-232: por_dt_devid

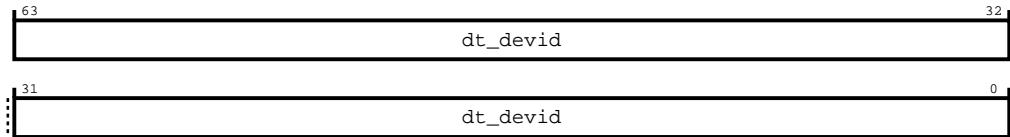


Table 4-248: por_dt_devid attributes

Bits	Name	Description	Type	Reset
[63:0]	dt_devid	Device ID	RO	64'b0

4.3.7.29 por_dt_devtype

Functions as the device type identifier register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFC8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-233: por_dt_devtype

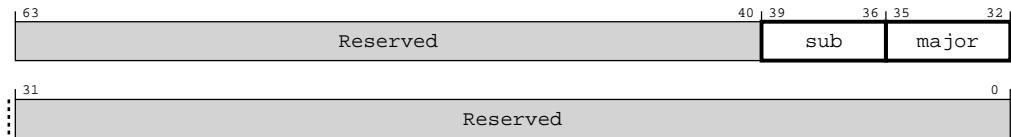


Table 4-249: por_dt_devtype attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:36]	sub	Sub type	RO	4'h4
[35:32]	major	Major type	RO	4'h3
[31:0]	Reserved	Reserved	RO	-

4.3.7.30 por_dt_pidr45

Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFD0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-234: por_dt_pidr45

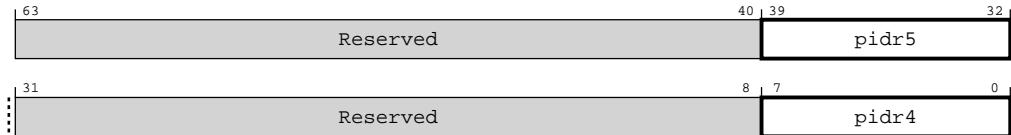


Table 4-250: por_dt_pidr45 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr5	Peripheral ID 5	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr4	Peripheral ID 4	RO	8'h4

4.3.7.31 por_dt_pidr67

Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFD8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-235: por_dt_pidr67

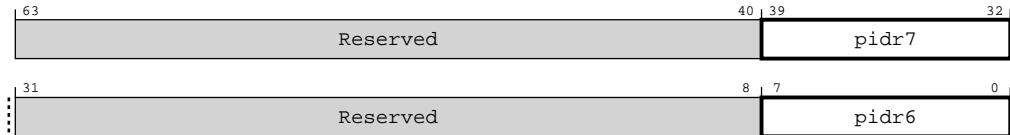


Table 4-251: por_dt_pidr67 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr7	Peripheral ID 7	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr6	Peripheral ID 6	RO	8'b0

4.3.7.32 por_dt_pidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFE0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-236: por_dt_pidr01

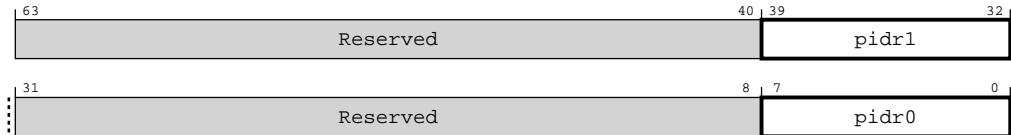


Table 4-252: por_dt_pidr01 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr1	Peripheral ID 1	RO	8'hb4
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr0	Peripheral ID 0	RO	8'h34

4.3.7.33 por_dt_pidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFE8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-237: por_dt_pidr23

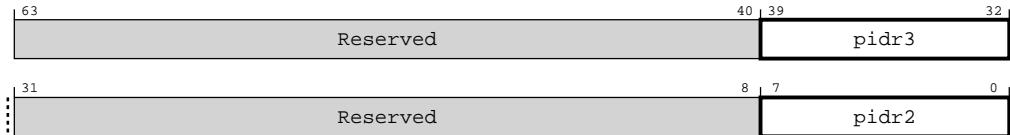


Table 4-253: por_dt_pidr23 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pidr3	Peripheral ID 3	RO	8'b0
[31:8]	Reserved	Reserved	RO	-
[7:0]	pidr2	Peripheral ID 2	RO	8'h7

4.3.7.34 por_dt_cidr01

Functions as the identification register for component ID 0 and component ID 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFF0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-238: por_dt_cidr01

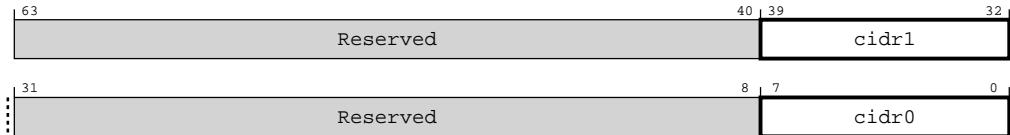


Table 4-254: por_dt_cidr01 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	cidr1	Component ID 1	RO	8'h9f
[31:8]	Reserved	Reserved	RO	-
[7:0]	cidr0	Component ID 0	RO	8'hd

4.3.7.35 por_dt_cidr23

Functions as the identification register for component ID 2 and component ID 3.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFF8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-239: por_dt_cidr23

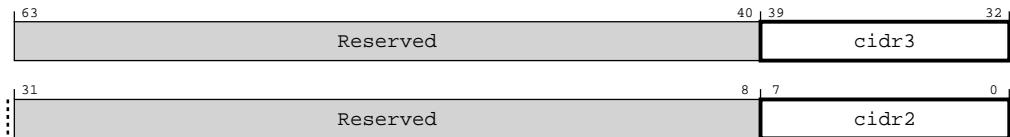


Table 4-255: por_dt_cidr23 attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	cidr3	Component ID 3	RO	8'h1
[31:8]	Reserved	Reserved	RO	-
[7:0]	cidr2	Component ID 2	RO	8'h5

4.3.8 DN register descriptions

This section lists the DN registers.

4.3.8.1 por_dn_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-240: por_dn_node_info

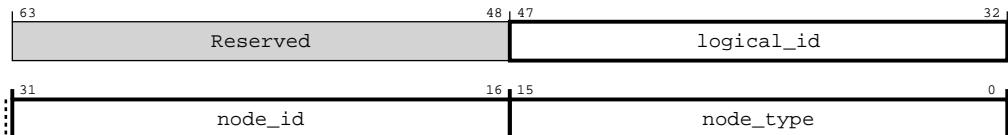


Table 4-256: por_dn_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component CHI node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0001

4.3.8.2 por_dn_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-241: por_dn_child_info

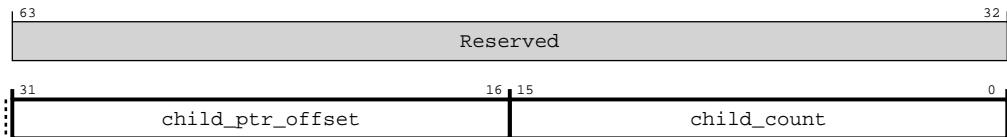


Table 4-257: por_dn_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'h0

4.3.8.3 por_dn_build_info

Contains the configuration parameter values. Indicates the specific DN configuration.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-242: por_dn_build_info

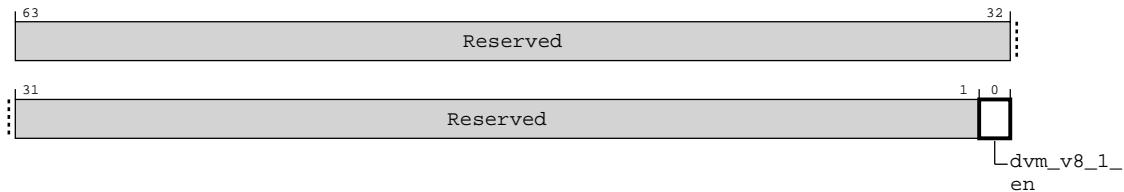


Table 4-258: por_dn_build_info attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	dvm_v8_1_en	Indicates that all nodes receiving DVM snoops support DVM v8/v8.1 operations.	RO	1'b1

4.3.8.4 por_dn_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-243: por_dn_secure_register_groups_override

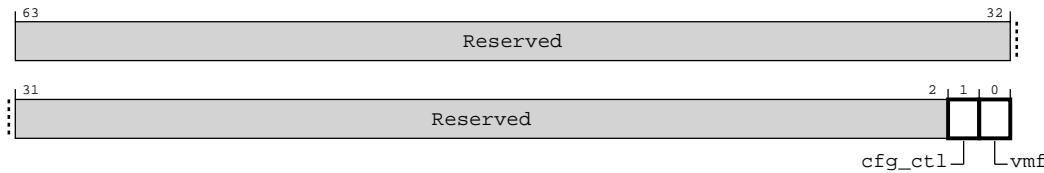


Table 4-259: por_dn_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	cfg_ctl	Allows Non-secure access to Secure configuration control register (por_dn_cfg_ctl)	RW	1'b0
[0]	vmf	Allows Non-secure access to Secure VMF registers	RW	1'b0

4.3.8.5 por_dn_cfg_ctl

Functions as the configuration control register for DVM Node.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

por_dn_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-244: por_dn_cfg_ctl

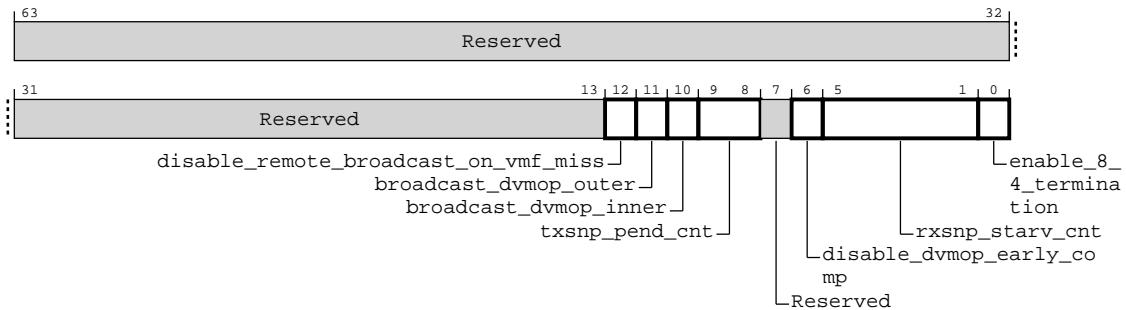


Table 4-260: por_dn_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:13]	Reserved	Reserved	RO	-
[12]	disable_remote_broadcast_on_vmf_miss	Disables broadcast of VMID Filterable DVMOps to remote on VMF miss.	RW	1'h0
[11]	broadcast_dvmop_outer	Used to filter DVMOps marked as outershareable (OS) from being sent off-chip.	RW	1'h1
[10]	broadcast_dvmop_inner	Used to filter DVMOps marked as innershareable (IS) from being sent off-chip.	RW	1'h1
[9:8]	txsnp_pend_cnt	Maximum number of (Non-Sync + Sync) SnpDVMOps issued on TXSNP. 2'b00: Max of 4 SnpDVMOps in progress (default) 2'b01: Max of 8 SnpDVMOps in progress 2'b10: Max of 16 SnpDVMOps in progress 2'b11: Reserved	RW	2'h0
[7]	Reserved	Reserved	RO	-
[6]	disable_dvmop_early_comp	Disables Early Comp (CompDBID) for DVMOps	RW	1'b0
[5:1]	rxsnp_starv_cnt	Number of cycles RXSNP lost to RXREQ for RCB alloc.	RW	5'h8
[0]	enable_8_4_termination	Enables termination of 8.4 DVMOps in DN.	RW	1'b0

4.3.8.6 por_dn_aux_ctl

Functions as the auxiliary control register for DN.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-245: por_dn_aux_ctl

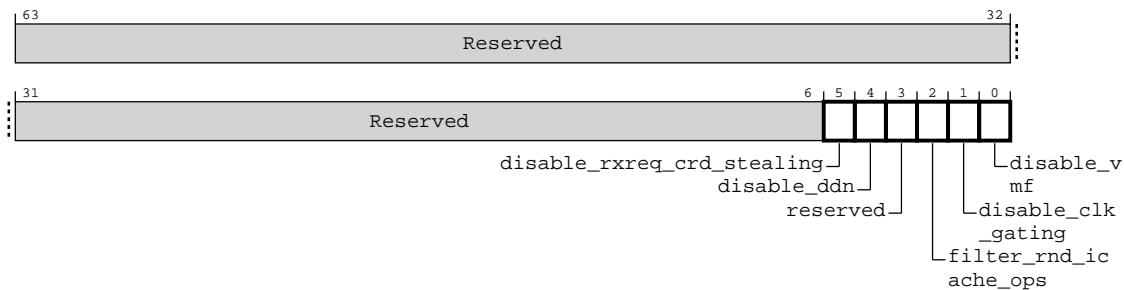


Table 4-261: por_dn_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:6]	Reserved	Reserved	RO	-
[5]	disable_rxreq_crd_stealing	Disables credit stealing from RXREQ LinkLayer when RXSNP is starved for RCB alloc.	RW	1'b0
[4]	disable_ddn	Disables Distributed DN functionality- Snoops all RNs and CML nodes in the mesh and disables snooping other DNs. Must program all RNSAMs to target HND for DVMs and then set this to 1 in HND.	RW	1'b0
[3]	reserved	Reserved field	RW	1'b0
[2]	filter_rnd_icache_ops	Filters out BPI and VICI/PICI SnpS to RNDs when set	RW	Configuration dependent
[1]	disable_clk_gating	Disables autonomous clock gating when set	RW	1'b0
[0]	disable_vmf	Disables VMID-based DVM snoop filtering when set	RW	Configuration dependent

4.3.8.7 por_dn_vmf0-15_ctrl

There are 16 iterations of this register. The index ranges from 0 to 15. Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hC00 + # {56*index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_dn_secure_register_groups_override.vmf`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-246: por_dn_vmf0-15_ctrl

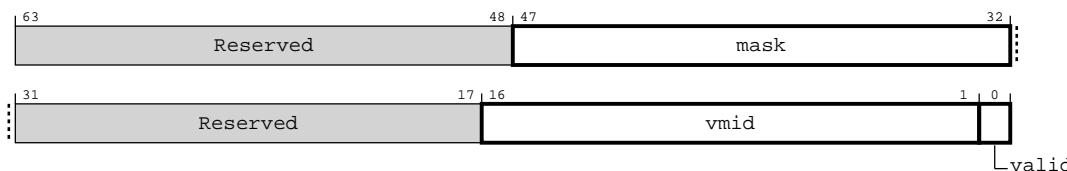


Table 4-262: por_dn_vmf0-15_ctrl attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf#:{index}_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff
[31:17]	Reserved	Reserved	RO	-
[16:1]	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
[0]	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

4.3.8.8 por_dn_vmf0-15_rnf0

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hC00 + #{56*index+8}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_dn_secure_register_groups_override.vmf`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-247: por_dn_vmf0-15_rnf0

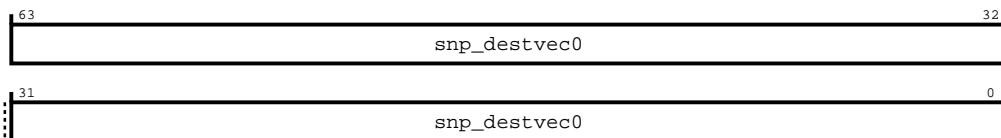


Table 4-263: por_dn_vmf0-15_rnf0 attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf#{index}_ctrl.vmid	RW	64'b0

4.3.8.9 por_dn_vmf0-15_rnf1

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical RN-F bit vector 127:64 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC00 + #{56*index+16}

Type

RW

Reset value

See individual bit resets

Secure group override

por_dn_secure_register_groups_override.vmf

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-248: por_dn_vmf0-15_rnf1

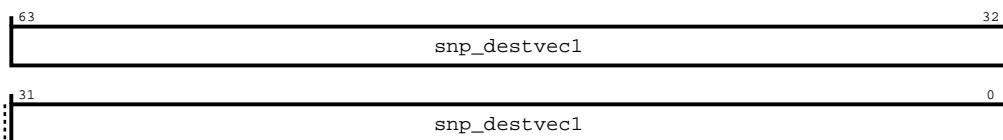


Table 4-264: por_dn_vmf0-15_rnf1 attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec1	RN-F bit vector 127:64 corresponding to por_dn_vmf#{index}_ctrl.vmid	RW	64'b0

4.3.8.10 por_dn_vmf0-15_rnf2

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical RN-F bit vector 191:128 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hC00 + #{56*index+24}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_dn_secure_register_groups_override.vmf`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-249: por_dn_vmf0-15_rnf2

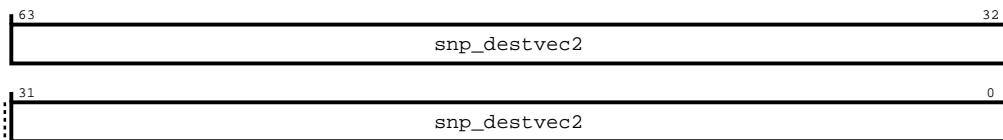


Table 4-265: por_dn_vmf0-15_rnf2 attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec2	RN-F bit vector 191:128 corresponding to por_dn_vmf#{index}_ctrl.vmid	RW	64'b0

4.3.8.11 por_dn_vmf0-15_rnf3

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical RN-F bit vector 255:192 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC00 + # {56*index+32}

Type

RW

Reset value

See individual bit resets

Secure group override

por_dn_secure_register_groups_override.vmf

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-250: por_dn_vmf0-15_rnf3

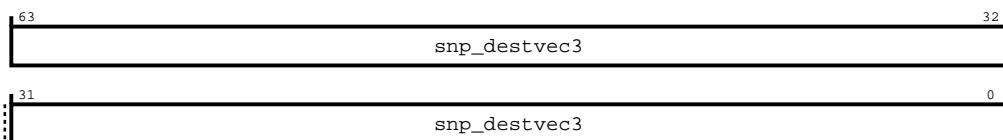


Table 4-266: por_dn_vmf0-15_rnf3 attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec3	RN-F bit vector 255:192 corresponding to por_dn_vmf#{index}_ctrl.vmid	RW	64'b0

4.3.8.12 por_dn_vmf0-15_rnd0

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hC00 + #{56*index+40}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_dn_secure_register_groups_override.vmf`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-251: por_dn_vmf0-15_rnd0

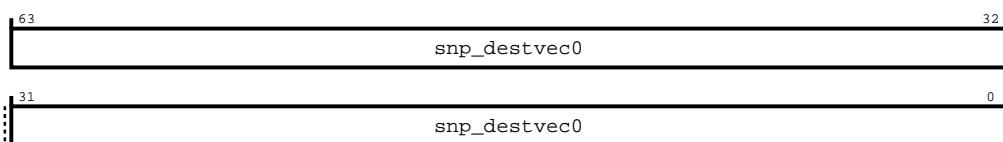


Table 4-267: por_dn_vmf0-15_rnd0 attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec0	RN-D bit vector 63:0 corresponding to por_dn_vmf#{index}_ctrl.vmid	RW	64'b0

4.3.8.13 por_dn_vmf0-15_cxra

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-700 system. Does not have any effect.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hC00 + # {56*index+48}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_dn_secure_register_groups_override.vmf`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-252: por_dn_vmf0-15_cxra

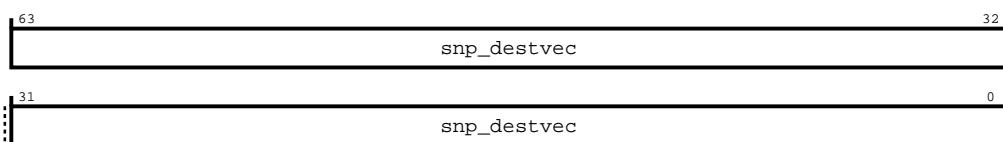


Table 4-268: por_dn_vmf0-15_cxra attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf#{index}_ctrl.vmid	RW	64'b0

4.3.8.14 por_dn_domain_rnf0-3

There are 4 iterations of this register. The index ranges from 0 to 3. RNF logical list for DDN

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16'hF80 + \{8 * \text{index}\}$

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-253: por_dn_domain_rnf0-3

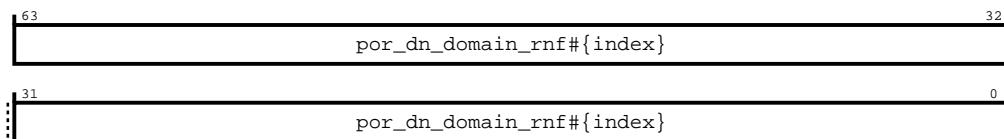


Table 4-269: por_dn_domain_rnf0-3 attributes

Bits	Name	Description	Type	Reset
[63:0]	por_dn_domain_rnf#{index}	RNF logical list corresponding to RNF #{{((index +1)*64)-1};#{{index}*64}}	RW	Configuration dependent

4.3.8.15 por_dn_domain_rnd0

RND logical list for DDN

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFA0

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-254: por_dn_domain_rnd0

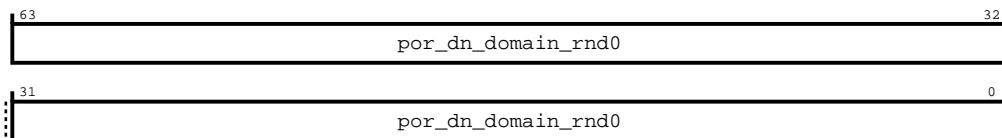


Table 4-270: por_dn_domain_rnd0 attributes

Bits	Name	Description	Type	Reset
[63:0]	por_dn_domain_rnd0	RND logical list for DDN corresponding to RND 63:0	RW	Configuration dependent

4.3.8.16 por_dn_domain_cxra

CXRA logical list for DDN

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFA8

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-255: por_dn_domain_cxra

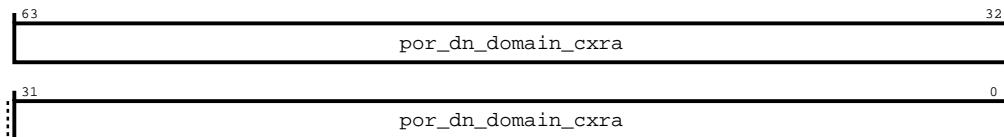


Table 4-271: por_dn_domain_cxra attributes

Bits	Name	Description	Type	Reset
[63:0]	por_dn_domain_cxra	CXRA logical list for DDN	RW	Configuration dependent

4.3.8.17 por_dn_vmf0-15_rnd1

There are 16 iterations of this register. The index ranges from 0 to 15. Contains the logical RN-D bit vector 127:64 corresponding to por_dn_vmf#{index}_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16^{\prime}hFB0 + \#(8 * \text{index})$

Type

RW

Reset value

See individual bit resets

Secure group override

`por_dn_secure_register_groups_override.vmf`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-256: por_dn_vmf0-15_rnd1

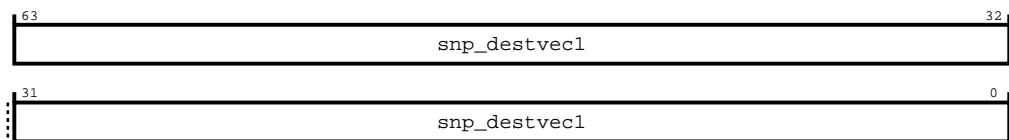


Table 4-272: por_dn_vmf0-15_rnd1 attributes

Bits	Name	Description	Type	Reset
[63:0]	snp_destvec1	RN-D bit vector 127:64 corresponding to por_dn_vmf#[index].ctrl.vmid	RW	64'b0

4.3.8.18 por_dn_domain_rnd1

RND logical list for DDN

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h1030`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-257: por_dn_domain_rnd1

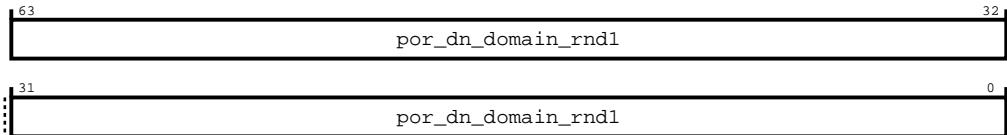


Table 4-273: por_dn_domain_rnd1 attributes

Bits	Name	Description	Type	Reset
[63:0]	por_dn_domain_rnd1	RND logical list for DDN corresponding to RND 127:64	RW	Configuration dependent

4.3.8.19 por_dn_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-258: por_dn_pmu_event_sel

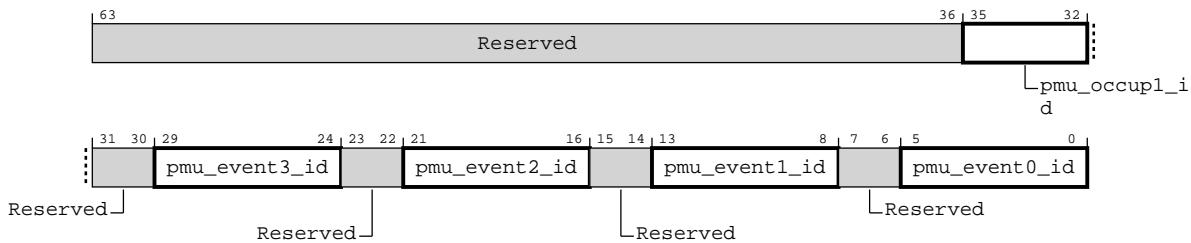


Table 4-274: por_dn_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:36]	Reserved	Reserved	RO	-
[35:32]	pmu_occup1_id	PMU occupancy event selector ID 4'b0000 All 4'b0001 DVM ops 4'b0010 DVM syncs	RW	4'b0
[31:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0
[7:6]	Reserved	Reserved	RO	-
[5:0]	pmu_event0_id	PMU Event 0 ID 6'h00 No event 6'h01 Number of TLBI DVM op requests 6'h02 Number of BPI DVM op requests 6'h03 Number of PICI DVM op requests 6'h04 Number of VICI DVM op requests 6'h05 Number of DVM sync requests 6'h06 Number of DVM op requests that were filtered using VMID filtering 6'h07 Number of DVM op requests to RNDs, BPI or PICI/VICI, that were filtered 6'h08 Number of retried REQ 6'h09 Number of SNPs sent to RNs 6'h0a Number of SNPs stalled to RNs due to lack of Crds 6'h0b DVM tracker full counter 6'h0c DVM RNF tracker occupancy counter 6'h0d DVM CXHA tracker occupancy counter 6'h0e DVM Peer DN tracker occupancy counter 6'h0f DVM RNF tracker Alloc 6'h10 DVM CXHA tracker Alloc 6'h11 DVM Peer DN tracker Alloc 6'h12 TXSNP stall due to number outstanding limit 6'h13 RXSNP stall starvation threshold hit 6'h14 TXSNP SYNC stall due to outstanding early completed Op	RW	5'b0

4.3.9 HN-I register descriptions

This section lists the HN-I registers.

4.3.9.1 por_hni_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-259: por_hni_node_info

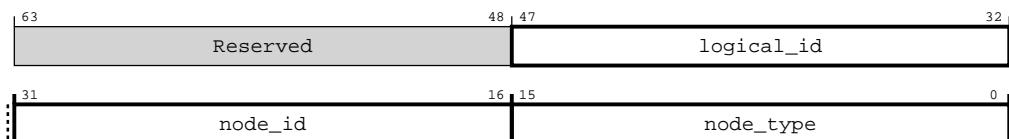


Table 4-275: por_hni_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	Configuration dependent

4.3.9.2 por_hni_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-260: por_hni_child_info

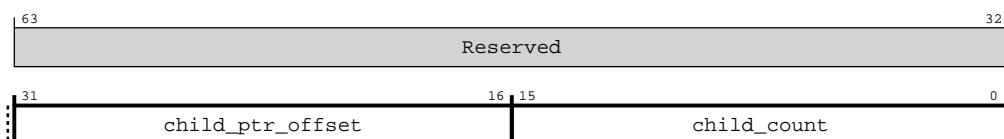


Table 4-276: por_hni_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.9.3 por_hni_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-261: por_hni_secure_register_groups_override

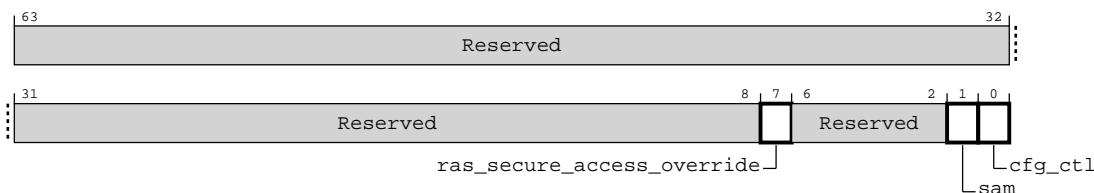


Table 4-277: por_hni_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7]	ras_secure_access_override	Allow Non-secure access to Secure RAS registers	RW	1'b0
[6:2]	Reserved	Reserved	RO	-
[1]	sam	Allows Non-secure access to Secure SAM registers	RW	1'b0
[0]	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

4.3.9.4 por_hni_unit_info

Provides component identification information for HN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-262: por_hni_unit_info

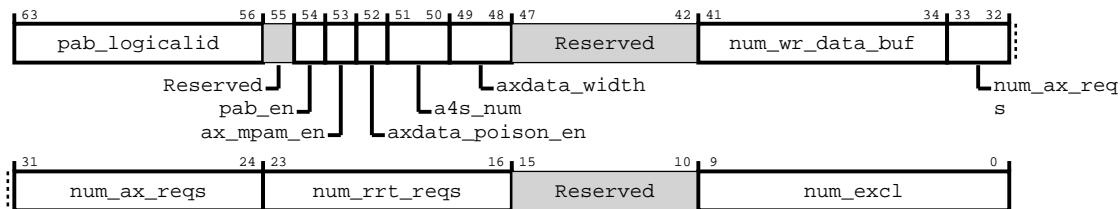


Table 4-278: por_hni_unit_info attributes

Bits	Name	Description	Type	Reset
[63:56]	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
[55]	Reserved	Reserved	RO	-
[54]	pab_en	PUB AUB bridge enable	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[53]	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[52]	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b0 Not supported 1'b1 Supported		
[51:50]	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent

Bits	Name	Description	Type	Reset
[49:48]	axdata_width	Data width on ACE-Lite/AXI4 interface 2'b00 128 bits 2'b01 256 bits 2'b10 512 bits	RO	Configuration dependent
[47:42]	Reserved	Reserved	RO	-
[41:34]	num_wr_data_buf	Number of write data buffers in HN-I	RO	Configuration dependent
[33:24]	num_ax_reqs	Maximum number of outstanding ACE-Lite/AXI4 requests	RO	Configuration dependent
[23:16]	num_rrt_reqs	Number of CHI RRT request tracker entries in HN-I.	RO	Configuration dependent
[15:10]	Reserved	Reserved	RO	-
[9:0]	num_excl	Number of exclusive monitors in HN-I	RO	Configuration dependent

4.3.9.5 por_hni_unit_info_1

Provides component identification information for HN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-263: por_hni_unit_info_1

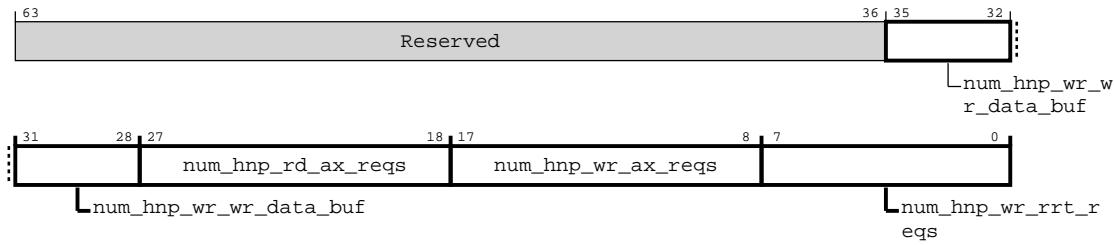


Table 4-279: por_hni_unit_info_1 attributes

Bits	Name	Description	Type	Reset
[63:36]	Reserved	Reserved	RO	-
[35:28]	num_hnp_wr_wr_data_buf	Number of P2P write data buffers in HN-I. HN-P only.	RO	Configuration dependent
[27:18]	num_hnp_rd_ax_reqs	Maximum number of outstanding P2P Read ACE-Lite/AXI4 requests. HN-P only.	RO	Configuration dependent
[17:8]	num_hnp_wr_ax_reqs	Maximum number of outstanding P2P Write ACE-Lite/AXI4 requests. HN-P only.	RO	Configuration dependent
[7:0]	num_hnp_wr_rrt_reqs	Number of P2P Write CHI RRT request tracker entries. HN-P only.	RO	Configuration dependent

4.3.9.6 por_hni_sam_addrregion0_cfg

Configures Address Region 0.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC00

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.sam

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-264: por_hni_sam_addrregion0_cfg

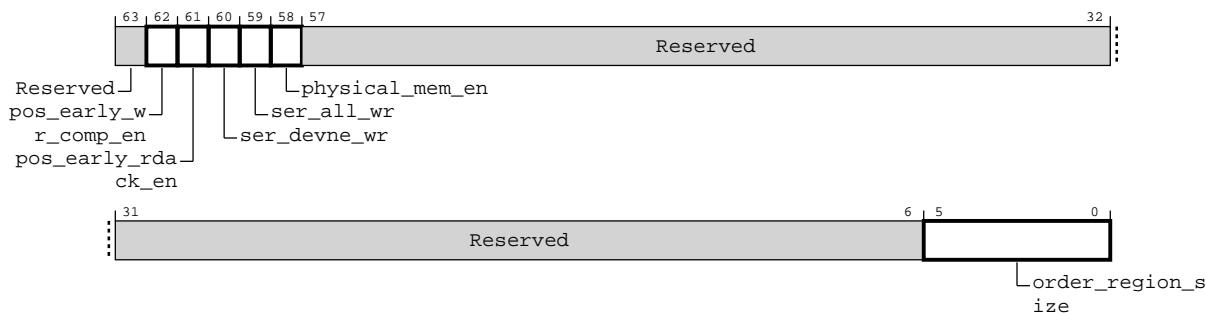


Table 4-280: por_hni_sam_addrregion0_cfg attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62]	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 0; used to improve write performance	RW	1'b1
[61]	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 0; used to improve ordered read performance	RW	1'b1
[60]	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 0	RW	1'b0
[59]	ser_all_wr	Used to serialize all writes within Address Region 0	RW	1'b0
[58]	physical_mem_en	Address Region 0 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
[57:6]	Reserved	Reserved	RO	-
[5:0]	order_region_size	<n>; used to calculate Order Region 0 size within Address Region 0 ($2^n \times 4\text{KB}$)	RW	6'b111111

4.3.9.7 por_hni_sam_addrregion1_cfg

Configures Address Region 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC08

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.sam

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-265: por_hni_sam_addrregion1_cfg

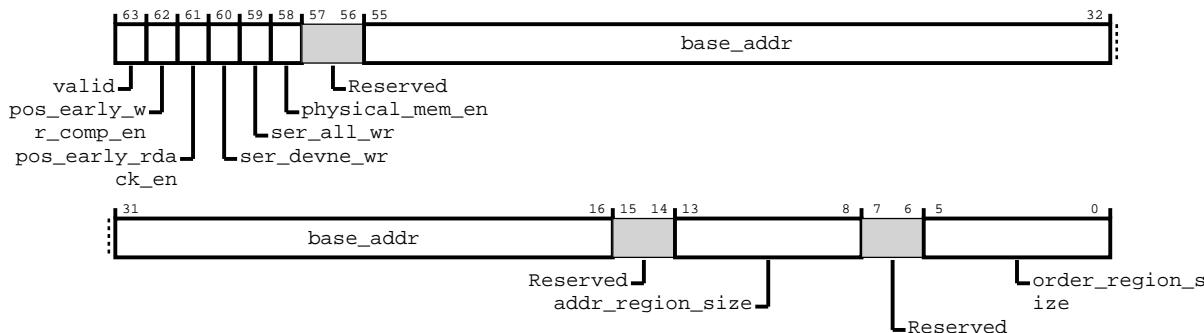


Table 4-281: por_hni_sam_addrregion1_cfg attributes

Bits	Name	Description	Type	Reset
[63]	valid	Address Region 1 fields are programmed and valid	RW	1'h0
[62]	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 1; used to improve write performance	RW	1'b1
[61]	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 1; used to improve ordered read performance	RW	1'b1
[60]	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 1	RW	1'b0
[59]	ser_all_wr	Used to serialize all writes within Address Region 1	RW	1'b0
[58]	physical_mem_en	Address Region 1 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
[57:56]	Reserved	Reserved	RO	-
[55:16]	base_addr	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	40'h0
[15:14]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[13:8]	addr_region_size	<n>; used to calculate Address Region 1 size ($2^n \times 4KB$) CONSTRAINT: <n> must be configured so that the Address Region 1 size is less than or equal to $2^{(address\ width)}$.	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	order_region_size	<n>; used to calculate Order Region 1 size within Address Region 1 ($2^n \times 4KB$)	RW	6'h0

4.3.9.8 por_hni_sam_addrregion2_cfg

Configures Address Region 2.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC10

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.sam

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-266: por_hni_sam_addrregion2_cfg

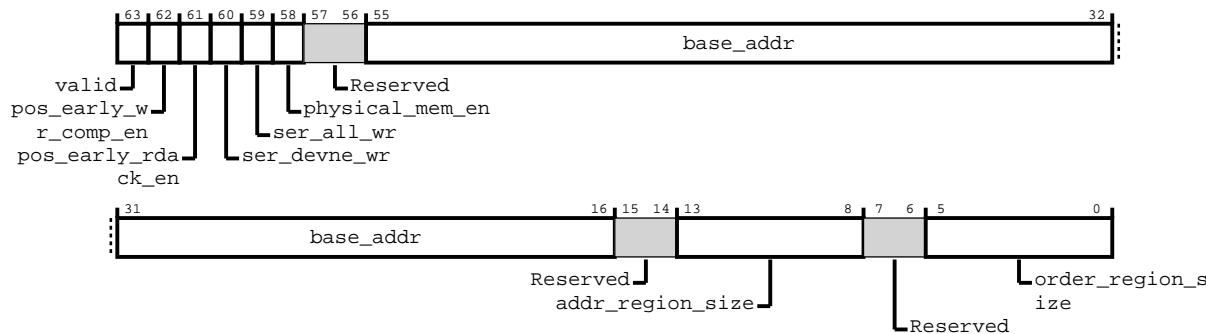


Table 4-282: por_hni_sam_addrregion2_cfg attributes

Bits	Name	Description	Type	Reset
[63]	valid	Address Region 2 fields are programmed and valid	RW	1'h0
[62]	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 2; used to improve write performance	RW	1'b1
[61]	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 2; used to improve ordered read performance	RW	1'b1
[60]	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 2	RW	1'b0
[59]	ser_all_wr	Used to serialize all writes within Address Region 2	RW	1'b0
[58]	physical_mem_en	Address Region 2 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
[57:56]	Reserved	Reserved	RO	-
[55:16]	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	40'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	addr_region_size	<n>; used to calculate Address Region 2 size ($2^n \times 4KB$) CONSTRAINT: <n> must be configured so that the Address Region 2 size is less than or equal to $2^{(address\ width)}$.	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	order_region_size	<n>; used to calculate Order Region 2 size within Address Region 2 ($2^n \times 4KB$)	RW	6'h0

4.3.9.9 por_hni_sam_addrregion3_cfg

Configures Address Region 3.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC18

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.sam

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-267: por_hni_sam_addrregion3_cfg

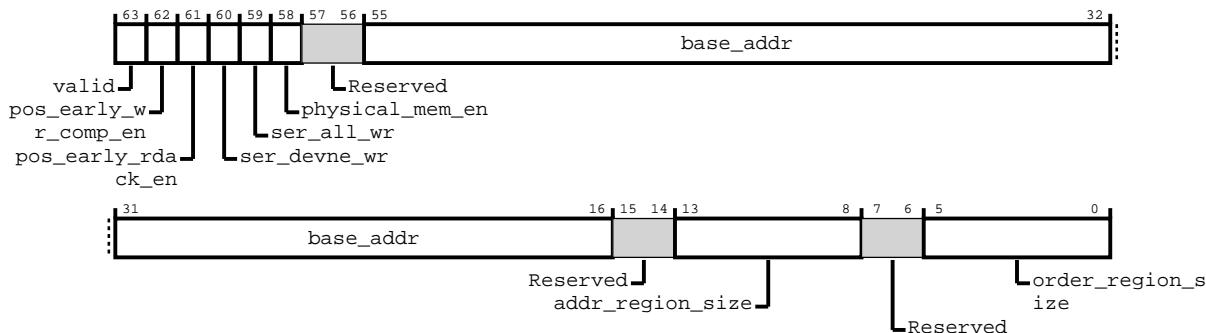


Table 4-283: por_hni_sam_addrregion3_cfg attributes

Bits	Name	Description	Type	Reset
[63]	valid	Fields of Address Region 3 are programmed and valid	RW	1'h0
[62]	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 3; used to improve write performance	RW	1'b1
[61]	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 3; used to improve ordered read performance	RW	1'b1
[60]	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 3	RW	1'b0
[59]	ser_all_wr	Used to serialize all writes within Address Region 3	RW	1'b0
[58]	physical_mem_en	Address Region 3 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
[57:56]	Reserved	Reserved	RO	-
[55:16]	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	40'h0
[15:14]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[13:8]	addr_region_size	<n>; used to calculate Address Region 3 size ($2^n \times 4KB$) CONSTRAINT: <n> must be configured so that the Address Region 3 size is less than or equal to $2^{(address\ width)}$.	RW	6'h0
[7:6]	Reserved	Reserved	RO	-
[5:0]	order_region_size	<n>; used to calculate Order Region 3 size within Address Region 3 ($2^n \times 4KB$)	RW	6'h0

4.3.9.10 por_hni_cfg_ctl

Functions as the configuration control register for HN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-268: por_hni_cfg_ctl

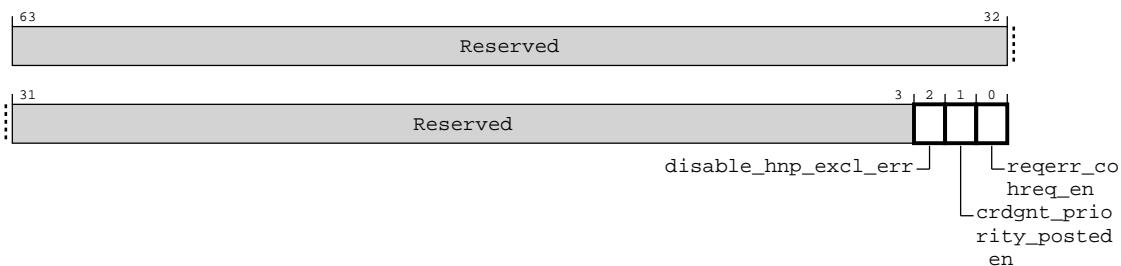


Table 4-284: por_hni_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	disable_hnp_excl_err	Disables sending NDE and Error logging on ReadNoSnp and WriteNoSnp Exclusives	RW	1'b0
[1]	crdgnt_priority_posted_en	Enables High priority Credit Grant responses to Posted requests	RW	1'b0
[0]	reqerr_cohreq_en	Enables sending of NDE response error to RN and logging of error information for the following requests: <ol style="list-style-type: none">1. Coherent Read2. CleanUnique/MakeUnique3. Coherent/CopyBack Write	RW	1'b1

4.3.9.11 por_hni_aux_ctl

Functions as the auxiliary control register for HN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-269: por_hni_aux_ctl

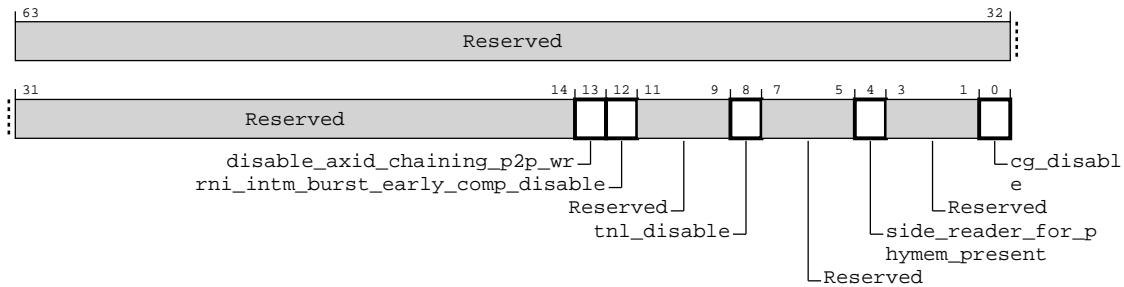


Table 4-285: por_hni_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:14]	Reserved	Reserved	RO	-
[13]	disable_axid_chaining_p2p_wr	Disables AXID based chaining of PCIe writes in P2P Write slice. HNP only	RW	1'b0
[12]	rni_intm_burst_early_comp_disable	Disables Early COMP to RNI for non-last burst writes	RW	1'b0
[11:9]	Reserved	Reserved	RO	-
[8]	tnl_disable	Disables RNI-HNI Tunneling in HNI. por_rni_aux_ctl.dis_hni_wr_stream must be set before setting this bit	RW	1'b0
[7:5]	Reserved	Reserved	RO	-
[4]	side_reader_for_phymem_present	Enables side reader in physical memory range	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	cg_disable	Disables HN-I architectural clock gates	RW	1'b0

4.3.9.12 por_hni_errfr

Functions as the error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3000

Type

RO

Reset value

See individual bit resets

Secure group override

`por_hni_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-270: por_hni_errfr

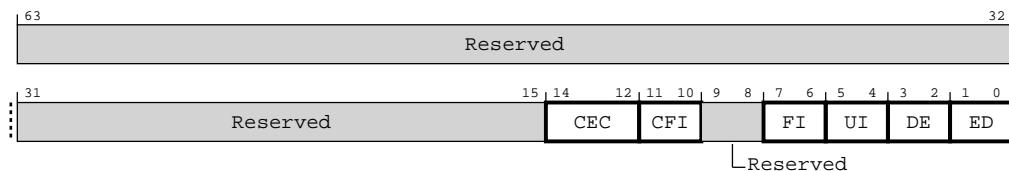


Table 4-286: por_hni_errfr attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.9.13 por_hni_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h3008`

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-271: por_hni_errctlr

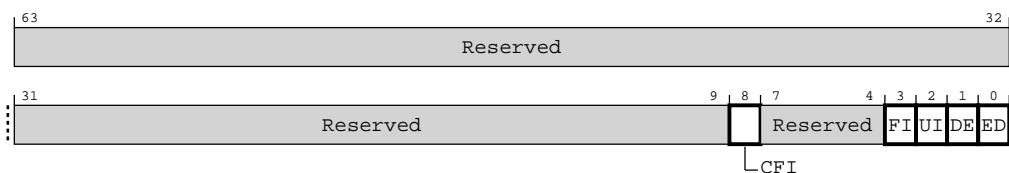


Table 4-287: por_hni_errctlr attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_hni_errfr.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_hni_errfr.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_hni_errfr.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_hni_errfr.ED	RW	1'b0

4.3.9.14 por_hni_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3010

Type

W1C

Reset value

See individual bit resets

Secure group override

`por_hni_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-272: por_hni_errstatus

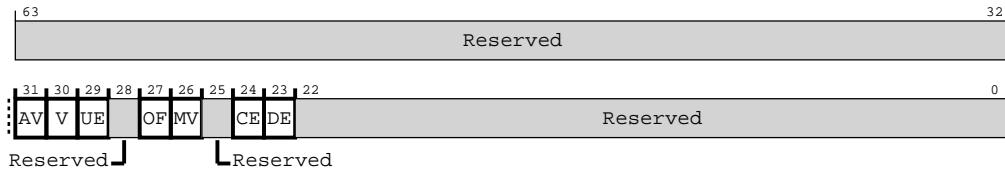


Table 4-288: por_hni_errstatus attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; por_hni_erraddr contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	por_hni_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.9.15 por_hni_erraddr

Contains the error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3018

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-273: por_hni_erraddr

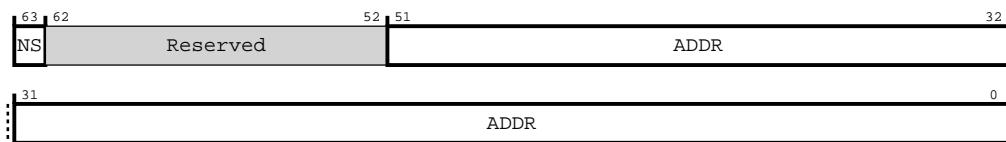


Table 4-289: por_hni_erraddr attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: por_hni_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.9.16 por_hni_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3020

Type

RW

Reset value

See individual bit resets

Secure group override

por_hni_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-274: por_hni_errmisc

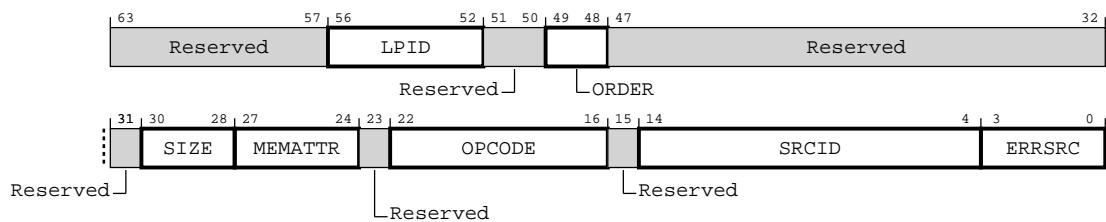


Table 4-290: por_hni_errmisc attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:52]	LPID	Error logic processor ID	RW	5'b0
[51:50]	Reserved	Reserved	RO	-
[49:48]	ORDER	Error order	RW	4'b0
[47:31]	Reserved	Reserved	RO	-
[30:28]	SIZE	Error transaction size	RW	3'b0
[27:24]	MEMATTR	Error memory attributes	RW	4'b0
[23]	Reserved	Reserved	RO	-
[22:16]	OPCODE	Error opcode	RW	7'b0
[15]	Reserved	Reserved	RO	-
[14:4]	SRCID	Error source ID	RW	11'b0

Bits	Name	Description	Type	Reset
[3:0]	ERRSRC	<p>Error source</p> <p>4'b0000 Coherent read 4'b0001 Coherent write 4'b0010 CleanUnique/MakeUnique 4'b0011 Atomic 4'b0100 Illegal configuration read 4'b0101 Illegal configuration write 4'b0110 Configuration write data partial byte enable error 4'b0111 Configuration write data parity error or poison error 4'b1000 BRESP error 4'b1001 Poison error 4'b1010 BRESP error and poison error 4'b1011 Unsupported Exclusive access (HN-P only)</p> <p>NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc.SRCID is the only valid field. For other error types, all fields are valid.</p>	RW	4'b0

4.3.9.17 por_hni_errfr_NS

Functions as the Non-secure error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3100

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-275: por_hni_errfr_NS

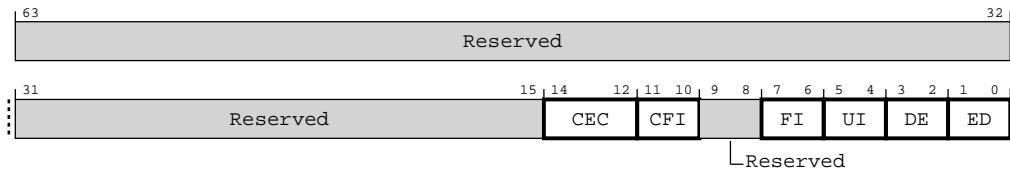


Table 4-291: por_hni_errfr_NS attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.9.18 por_hni_errctlr_NS

Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3108

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-276: por_hni_errctlr_NS

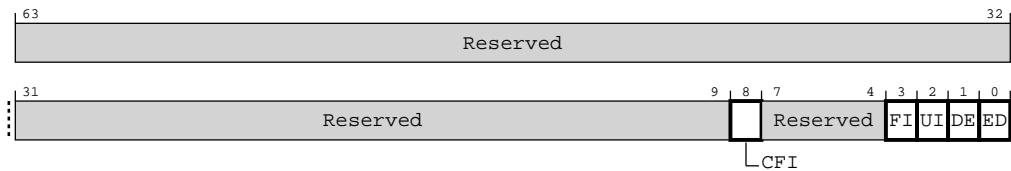


Table 4-292: por_hni_errctlr_NS attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_hni_errfr_NS.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr_NS.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_hni_errfr_NS.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_hni_errfr_NS.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_hni_errfr_NS.ED	RW	1'b0

4.3.9.19 por_hni_errstatus_NS

Functions as the Non-secure error status register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3110

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-277: por_hni_errstatus_NS

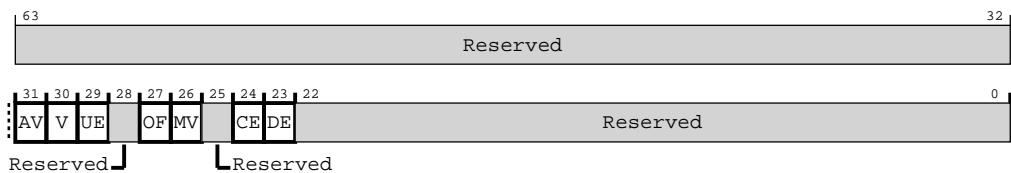


Table 4-293: por_hni_errstatus_NS attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; por_hni_erraddr_NS contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	por_hni_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.9.20 por_hni_erraddr_NS

Contains the Non-secure error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3118

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-278: por_hni_erraddr_NS

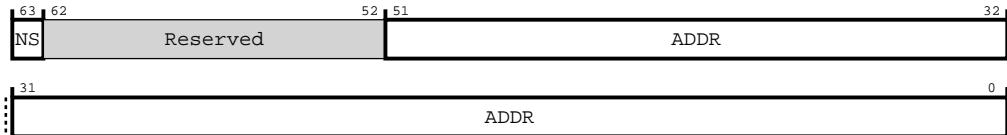


Table 4-294: por_hni_erraddr_NS attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: por_hni_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.9.21 por_hni_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3120

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-279: por_hni_errmisc_NS

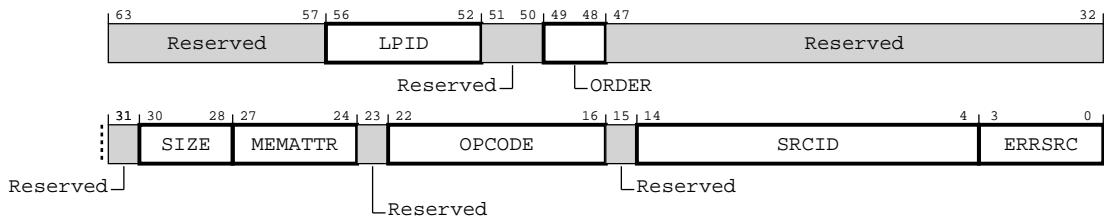


Table 4-295: por_hni_errmisc_NS attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:52]	LPID	Error logic processor ID	RW	5'b0
[51:50]	Reserved	Reserved	RO	-
[49:48]	ORDER	Error order	RW	4'b0
[47:31]	Reserved	Reserved	RO	-
[30:28]	SIZE	Error transaction size	RW	3'b0
[27:24]	MEMATTR	Error memory attributes	RW	4'b0
[23]	Reserved	Reserved	RO	-
[22:16]	OPCODE	Error opcode	RW	7'b0
[15]	Reserved	Reserved	RO	-
[14:4]	SRCID	Error source ID	RW	11'b0
[3:0]	ERRSRC	Error source 4'b0000 Coherent read 4'b0001 Coherent write 4'b0010 CleanUnique/MakeUnique 4'b0011 Atomic 4'b0100 Illegal configuration read 4'b0101 Illegal configuration write 4'b0110 Configuration write data partial byte enable error 4'b0111 Configuration write data parity error or poison error 4'b1000 BRESP error 4'b1001 Poison error 4'b1010 BRESP error and poison error 4'b1011 Unsupported Exclusive access (HN-P only)	RW	4'b0
		NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc_NS.SRCID is the only valid field. For other error types, all fields are valid.		

4.3.9.22 por_hni_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-280: por_hni_pmu_event_sel

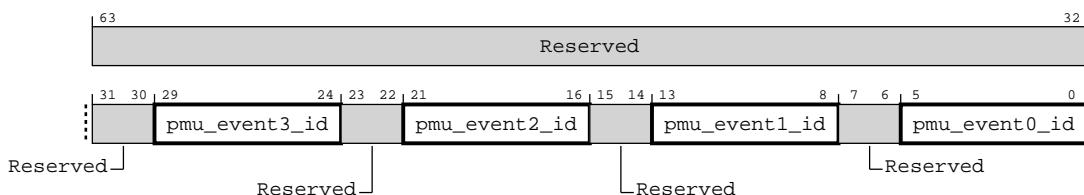


Table 4-296: por_hni_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	HN-I PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	HN-I PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	HN-I PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0
[7:6]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[5:0]	pmu_event0_id	<p>HN-I PMU Event 0 select</p> <p>6'h00 No event 6'h20 RRT read occupancy count overflow 6'h21 RRT write occupancy count overflow 6'h22 RDT read occupancy count overflow 6'h23 RDT write occupancy count overflow 6'h24 WDB occupancy count overflow 6'h25 RRT read allocation 6'h26 RRT write allocation 6'h27 RDT read allocation 6'h28 RDT write allocation 6'h29 WDB allocation 6'h2A RETRYACK TXRSP flit sent 6'h2B ARVALID set without ARREADY event 6'h2C ARREADY set without ARVALID event 6'h2D AWVALID set without AWREADY event 6'h2E AWREADY set without AWVALID event 6'h2F WVALID set without WREADY event 6'h30 TXDAT stall (TXDAT valid but no link credit available) 6'h31 Non-PCIe serialization event 6'h32 PCIe serialization event</p> <p>NOTE: All other encodings are reserved.</p>	RW	6'b0

4.3.9.23 por_hnp_pmu_event_sel

Specifies the PMU event to be counted. HNP only

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2008

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-281: por_hnp_pmu_event_sel

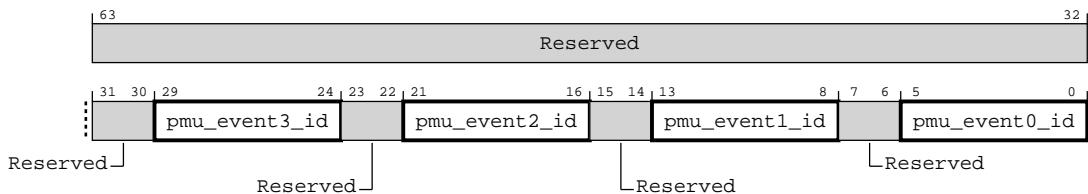


Table 4-297: por_hnp_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	P2P Slice PMU Event 3 select; see pmu_event0_id for encodings"	RW	6'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	P2P Slice PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	P2P Slice PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0
[7:6]	Reserved	Reserved	RO	-
[5:0]	pmu_event0_id	P2P Slice PMU Event 0 select 6'h00 No event 6'h01 RRT write occupancy count overflow 6'h02 RDT write occupancy count overflow 6'h03 WDB occupancy count overflow 6'h04 RRT write allocation 6'h05 RDT write allocation 6'h06 WDB allocation 6'h07 without AWREADY event 6'h08 AWREADY set without AWVALID event 6'h09 WVALID set without WREADY event 6'h11 RRT read occupancy count overflow 6'h12 RDT read occupancy count overflow 6'h13 RRT read allocation 6'h14 RDT read allocation 6'h15 ARVALID set without ARREADY event 6'h16 ARREADY set without ARVALID event NOTE: All other encodings are reserved.	RW	6'b0

4.3.10 HN-F register descriptions

This section lists the HN-F registers.

4.3.10.1 cmn_hns_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-282: cmn_hns_node_info

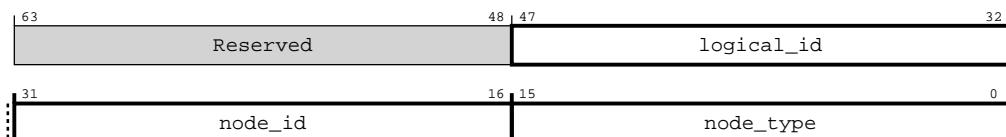


Table 4-298: cmn_hns_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	\$logical_id_description	RO	Configuration dependent
[31:16]	node_id	\$node_id_description	RO	Configuration dependent
[15:0]	node_type	\$node_type_description	RO	Configuration dependent

4.3.10.2 cmn_hns_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-283: cmn_hns_child_info

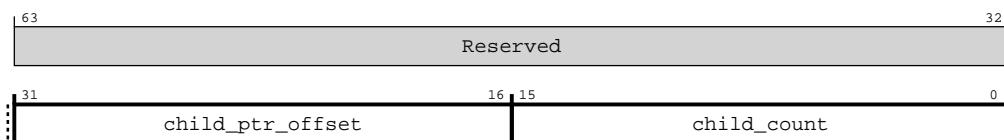


Table 4-299: cmn_hns_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.10.3 cmn_hns_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-284: cmn_hns_secure_register_groups_override

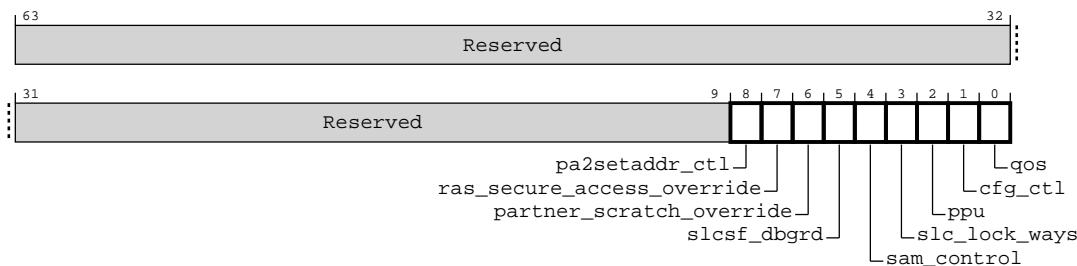


Table 4-300: cmn_hns_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	pa2setaddr_ctl	Allow Non-secure access to Secure PA2SETADDR registers	RW	1'b0
[7]	ras_secure_access_override	Allow Non-secure access to Secure RAS registers	RW	1'b0
[6]	partner_scratch_override	Allows Non-secure access to Secure Partner scratch registers	RW	1'b0
[5]	slcsf_dbgrd	Allows Non-secure access to Secure SLC/SF debug read registers	RW	1'b0
[4]	sam_control	Allows Non-secure access to Secure HN-F SAM control registers	RW	1'b0
[3]	slc_lock_ways	Allows Non-secure access to Secure cache way locking registers	RW	1'b0
[2]	ppu	Allows Non-secure access to Secure power policy registers	RW	1'b0
[1]	cfg_ctl	Allows Non-secure access to Secure configuration control register (cmn_hns_cfg_ctl)	RW	1'b0
[0]	qos	Allows Non-secure access to Secure QoS registers	RW	1'b0

4.3.10.4 cmn_hns_unit_info

Provides component identification information for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-285: cmn_hns_unit_info

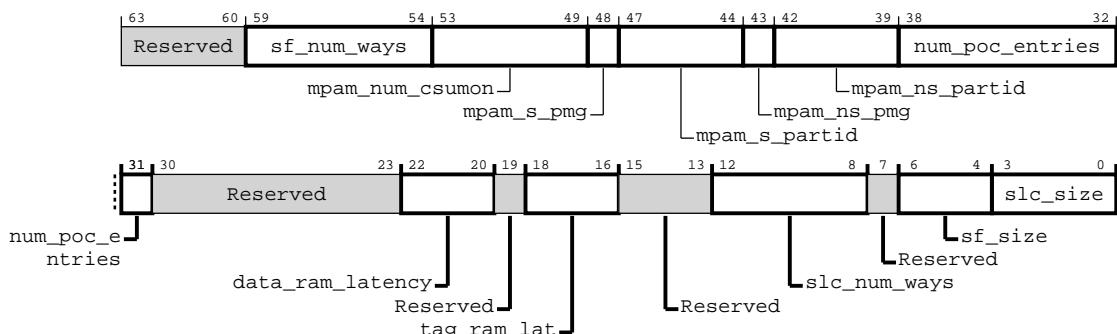


Table 4-301: cmn_hns_unit_info attributes

Bits	Name	Description	Type	Reset
[63:60]	Reserved	Reserved	RO	-
[59:54]	sf_num_ways	Number of cache ways in the SF	RO	-
[53:49]	mpam_num_csumon	Number of Cache Storage Usage Monitors for MPAM	RO	Configuration dependent
[48]	mpam_s_pmg	MPAM Secure supported PMGs	RO	-
	1'b0	1 PMG		
	1'b1	2 S PMG		

Bits	Name	Description	Type	Reset
[47:44]	mpam_s_partid	MPAM Secure supported PARTIDs 4'b0000 1 S PARTID 4'b0001 2 S PARTID 4'b0010 4 S PARTID 4'b0011 8 S PARTID 4'b0100 16 S PARTID 4'b0101 32 S PARTID 4'b0110 64 S PARTID 4'b0111 128 S PARTID 4'b1000 256 S PARTID 4'b1001 512 S PARTID	RO	-
[43]	mpam_ns_pmg	MPAM Non-secure supported PMGs 1'b0 1 NS PMG 1'b1 2 NS PMG	RO	-
[42:39]	mpam_ns_partid	MPAM Non-secure supported PARTIDs 4'b0000 1 NS PARTID 4'b0001 2 NS PARTID 4'b0010 4 NS PARTID 4'b0011 8 NS PARTID 4'b0100 16 NS PARTID 4'b0101 32 NS PARTID 4'b0110 64 NS PARTID 4'b0111 128 NS PARTID 4'b1000 256 NS PARTID 4'b1001 512 NS PARTID	RO	-
[38:31]	num_poc_entries	Number of POCQ entries	RO	Configuration dependent
[30:23]	Reserved	Reserved	RO	-
[22:20]	data_ram_latency	SLC data RAM latency (in cycles)	RO	-
[19]	Reserved	Reserved	RO	-
[18:16]	tag_ram_lat	SLC tag RAM latency (in cycles)	RO	-
[15:13]	Reserved	Reserved	RO	-
[12:8]	slc_num_ways	Number of cache ways in the SLC	RO	-
[7]	Reserved	Reserved	RO	-
[6:4]	sf_size	SF size 3'b000 (32KB * sf_num_ways) 3'b001 (64KB * sf_num_ways) 3'b010 (128KB * sf_num_ways) 3'b011 (256KB * sf_num_ways) 3'b101 (512KB * sf_num_ways)	RO	-

Bits	Name	Description	Type	Reset
[3:0]	slc_size	SLC size	RO	-
		4'b0000 No SLC		
		4'b0001 128KB		
		4'b0010 256KB		
		4'b0011 512KB		
		4'b0100 1MB		
		4'b0101 1.5MB		
		4'b0110 2MB		
		4'b0111 3MB		
		4'b1000 4MB		
		4'b1001 384KB		

4.3.10.5 cmn_hns_unit_info_1

Provides component identification information for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-286: cmn_hns_unit_info_1

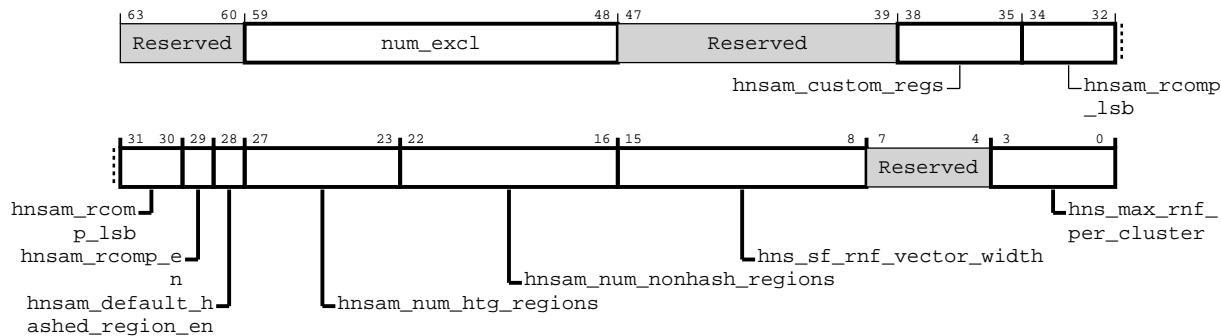


Table 4-302: cmn_hns_unit_info_1 attributes

Bits	Name	Description	Type	Reset
[63:60]	Reserved	Reserved	RO	-
[59:48]	num_excl	Number of exclusive monitors	RO	-
[47:39]	Reserved	Reserved	RO	-
[38:35]	hnsam_custom_regs	Number of customer specific registers for customer implemented logic	RO	Configuration dependent
[34:30]	hnsam_rcomp_lsb	Defines the minimum size of HTG when POR_HNSAM_RCOMP_EN_PARAM = 1, 20 value defines minimum size as 1MB and 26 value defines minimum size as 64MB	RO	Configuration dependent
[29]	hnsam_rcomp_en	Enable Range based address comparison for HNSAM HTG/Nonhashed groups. Program start address and end address	RO	Configuration dependent
[28]	hnsam_default_hashed_region_en	Enable default hashed group for HNSAM. To support backward compatible, set this parameter	RO	Configuration dependent
[27:23]	hnsam_num_htg_regions	Number of HTG regions supported by the HNSAM	RO	Configuration dependent
[22:16]	hnsam_num_nonhash_regions	Number of non-hashed regions supported by the HNSAM	RO	Configuration dependent
[15:8]	hns_sf_rnf_vector_width	Total Number of bits in RNF tracking vector in the Snoop Filter (Total SF_VEC_WIDTH = (TOTAL_RNF/HNS_MAX_CLUSTER_PARAM)+HNS_SF_ADD_VECTOR_WIDTH)	RO	Configuration dependent
[7:4]	Reserved	Reserved	RO	-
[3:0]	hns_max_rnf_per_cluster	Describes the maximum number of RN-F's in a single cluster	RO	Configuration dependent

4.3.10.6 cmn_hns_cfg_ctl

Functions as the configuration control register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-287: cmn_hns_cfg_ctl

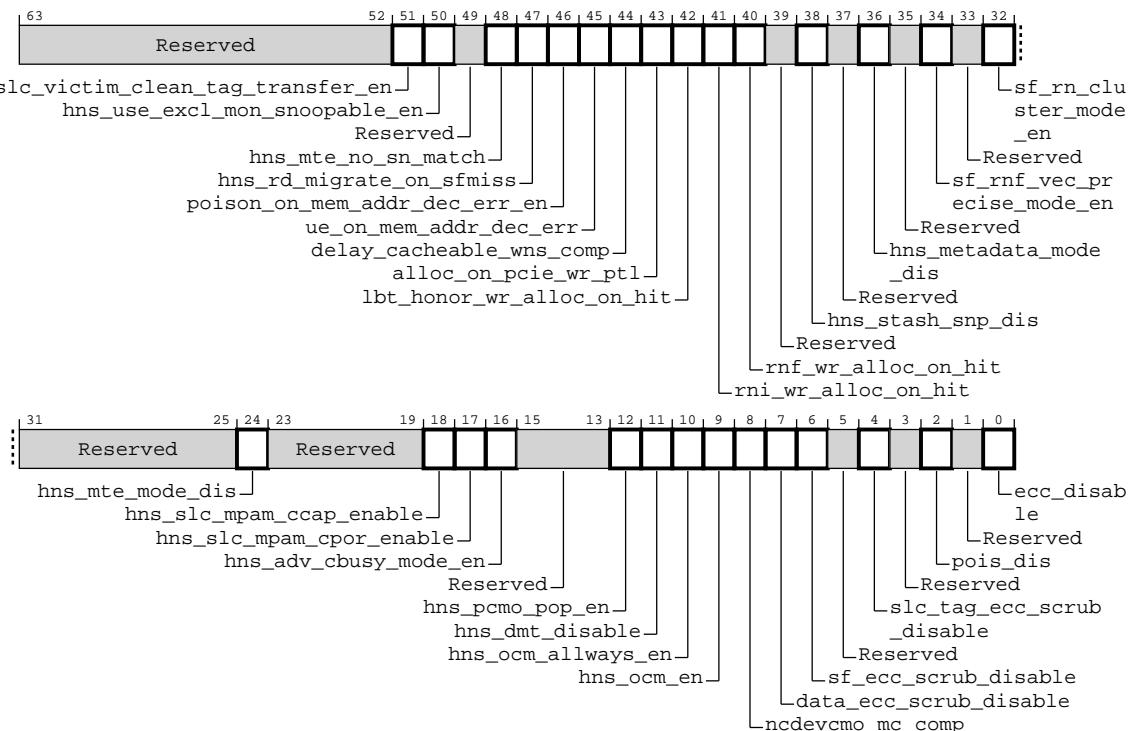


Table 4-303: cmn_hns_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51]	slc_victim_clean_tag_transfer_en	When set, HNS propagates clean tag to SN when SLC victim has clean tag	RW	1'b0
[50]	hns_use_excl_mon_snoopable_en	When set, HNS uses exclusive monitor for snoopable traffic in imprecise SF modes	RW	1'b0
[49]	Reserved	Reserved	RO	-
[48]	hns_mte_no_sn_match	When set, HNS does MTE match locally without propagating to SN	RW	1'b0
[47]	hns_rd_migrate_on_sfmiss	Migrates a read from LCC/SLC if sf miss	RW	1'b1
[46]	poison_on_mem_addr_dec_err_en	When set, set poison in read data for CXL address decode error	RW	1'b1
[45]	ue_on_mem_addr_dec_err	Log CXL address decode error as UE in error register	RW	1'b0
[44]	delay_cacheable_wns_comp	Sends late completion for cacheable WriteNoSnoop	RW	1'b0
[43]	alloc_on_pcie_wr_ptl	Forces HBT PCIE partial writes to allocate in SLC	RW	1'b0
[42]	lbt_honor_wr_alloc_on_hit	Forces LBT Write requests to honor wlu_alloc_on_hit, rnf_wr_alloc_on_hit, and rni_wr_alloc_on_hit	RW	1'b0
[41]	rni_wr_alloc_on_hit	Forces RNI Write requests to allocate if the line hit in SLC	RW	1'b0
[40]	rnf_wr_alloc_on_hit	Forces RNF Write requests to allocate if the line hit in SLC	RW	1'b0
[39]	Reserved	Reserved	RO	-
[38]	hns_stash_snp_dis	Disables stashing snoop in HNS when set to 1'b1	RW	1'b0
[37]	Reserved	Reserved	RO	-
[36]	hns_metadata_mode_dis	Disables the METADATA features in HNS when set to 1'b1	RW	1'b0
[35]	Reserved	Reserved	RO	-
[34]	sf_rnf_vec_precise_mode_en	Enables the snoop filter's precise RNF vector in clustered mode when set to 1'b1	RW	1'b1
[33]	Reserved	Reserved	RO	-
[32]	sf_rn_cluster_mode_en	Enables the snoop filter clustering of the RN-F ID's using programmable registers	RW	1'b1
[31:25]	Reserved	Reserved	RO	-
[24]	hns_mte_mode_dis	Disables the MTE features in HNS when set to 1'b1	RW	1'b0
[23:19]	Reserved	Reserved	RO	-
[18]	hns_slc_mpam_ccap_enable	Enable MPAM Cache Capacity Partitioning for SLC 1'b1 Cache Capacity Partitioning is enabled if supported in Hardware. 1'b0 Cache Capacity Partitioning is disabled for SLC. NOTE: If MPAM is disabled at build time, this bit has no meaning.	RW	1'b0

Bits	Name	Description	Type	Reset
[17]	hns_slc_mpam_cpor_enable	Enable MPAM Cache Portion Partitioning for SLC 1'b1 Cache Portion Partitioning is enabled if supported in Hardware. 1'b0 Cache Portion Partitioning is disabled for SLC. . NOTE: If MPAM is disabled at build time, this bit has no meaning.	RW	1'b0
[16]	hns_adv_cbusy_mode_en	Enables the advanced features of HNS CBusy handling	RW	1'b0
[15:13]	Reserved	Reserved	RO	-
[12]	hns_pcmo_pop_en	Terminates PCMO in HNS when this bit is set to 1'b1	RW	1'b0
[11]	hns_dmt_disable	Disables DMT when set	RW	1'b0
[10]	hns_ocm_allways_en	Enables all SLC ways with OCM	RW	1'b0
[9]	hns_ocm_en	Enables region locking with OCM support	RW	1'b0
[8]	ncdevcmo_mc_comp	Disables HN-F completion when set NOTE: When set, HN-F sends completion for the following transactions received after completion from SN: 1. Non-Cacheable WriteNoSnp 2. Device WriteNoSnp 3. CMO (cache maintenance operations) CONSTRAINT: When this bit is set, por_rni_cfg_ctl.dis_ncwr_stream and por_rnd_cfg_ctl.dis_ncwr_stream must also be set.	RW	1'b0
[7]	data_ecc_scrub_disable	Disables data single-bit ECC error scrubbing for non-migrating reads when set	RW	1'b1
[6]	sf_ecc_scrub_disable	Disables SF tag single-bit ECC error scrubbing when set	RW	1'b0
[5]	Reserved	Reserved	RO	-
[4]	slc_tag_ecc_scrub_disable	Disables SLC tag single-bit ECC error scrubbing when set	RW	1'b0
[3]	Reserved	Reserved	RO	-
[2]	pois_dis	Disables parity error data poison when set	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	ecc_disable	Disables SLC and SF ECC generation/detection when set	RW	1'b0

4.3.10.7 cmn_hns_aux_ctl

Functions as the auxiliary control register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-288: cmn_hns_aux_ctl

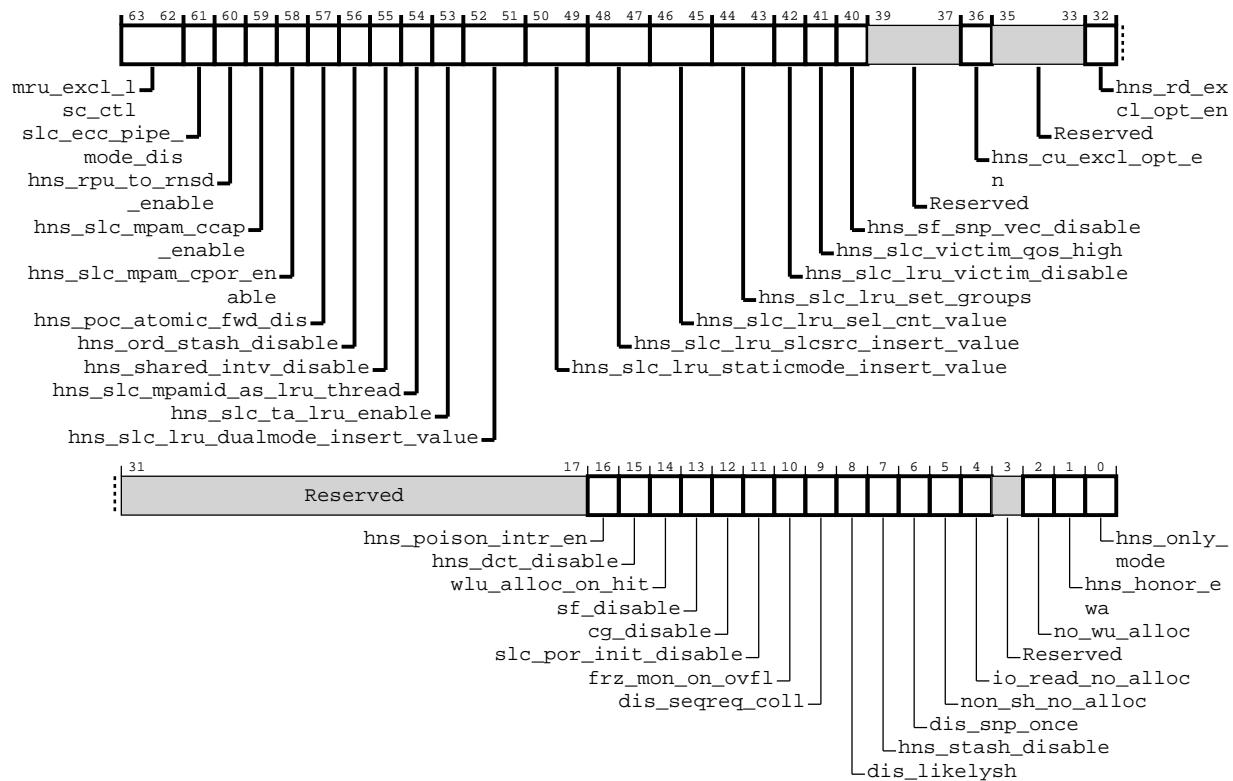


Table 4-304: cmn_hns_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:62]	mru_excl_lsc_ctl	MRU Exclusive control for LSC.	RW	2'b00
[61]	slc_ecc_pipe_mode_dis	Disables inline ECC pipe mode in SLC. CONSTRAINT: Must be programmed at boot time.	RW	1'b1
[60]	hns_rpu_to_rnsd_enable	Enables HN-F to treat ReadPrefUnique ops as ReadNotSharedDirty	RW	1'b0

Bits	Name	Description	Type	Reset
[59]	hns_slc_mpam_ccap_enable	<p>Enable MPAM Cache Capacity Partitioning for SLC</p> <p>1'b1 Cache Capacity Partitioning is enabled if supported in Hardware.</p> <p>1'b0 Cache Capacity Partitioning is disabled for SLC.</p> <p>NOTE: This bit moved to cfg_ctl and will be removed in future version of ICN. NOTE: If MPAM is disabled at build time, this bit has no meaning.</p>	RW	1'b0
[58]	hns_slc_mpam_cpor_enable	<p>Enable MPAM Cache Portion Partitioning for SLC</p> <p>1'b1 Cache Portion Partitioning is enabled if supported in Hardware.</p> <p>1'b0 Cache Portion Partitioning is disabled for SLC.</p> <p>. NOTE: This bit moved to cfg_ctl and will be removed in future version of ICN. NOTE: If MPAM is disabled at build time, this bit has no meaning.</p>	RW	1'b0
[57]	hns_poc_atomic_fwd_dis	Disable the atomic data forwarding in POCQ	RW	1'b0
[56]	hns_ord_stash_disable	Disables stash operation for ordered write stash requests	RW	1'b0
[55]	hns_shared_intv_disable	Disables snoop requests to CHIB RN-F with shared copy	RW	Configuration dependent
[54]	hns_slc_mpamid_as_lru_thread	<p>Use MPAM PARTID as ThreadID for Thread Aware eLRU</p> <p>1'b1 ThreadID is based on MPAM PARTID+NS for Thread Aware eLRU.</p> <p>1'b0 ThreadID is based on LPID+LID for Thread Aware eLRU.</p> <p>Note: MPAM PARTID is used only if MPAM is enabled.</p>	RW	1'b0
[53]	hns_slc_ta_lru_enable	<p>Thread Aware eLRU enable</p> <p>1'b0 ThreadID used for eLRU is zero.</p> <p>1'b1 ThreadID used for eLRU is based on MPAMID or LPID+LID.</p> <p>Note: If SLC size is less than 256KB, this bit is ignore.</p>	RW	1'b0
[52:51]	hns_slc_lru_dualmode_insert_value	Insertion value for Dual mode eLRU NOTE: Default is 2'b11.	RW	2'b11
[50:49]	hns_slc_lru_staticmode_insert_value	Insertion value for Static mode eLRU NOTE: Default is 2'b10.	RW	2'b10
[48:47]	hns_slc_lru_slcsrc_insert_value	Insertion value if SLC source bit is set NOTE: Default is 2'b00.	RW	2'b00

Bits	Name	Description	Type	Reset
[46:45]	hns_slc_lru_sel_cnt_value	<p>Selection counter value for eLRU to determine which group policy is more effective</p> <p>2'b00 Sel counter is like an 8-bit range; upper limit is 255; middle point is 128</p> <p>2'b01 Sel counter is like a 9-bit range; upper limit is 511; middle point is 256</p> <p>2'b10 Sel counter is like a 10-bit range; upper limit is 1023; middle point is 512</p> <p>2'b11 Sel counter is like an 11-bit range; upper limit is 2047; middle point is 1024</p>	RW	2'b10
[44:43]	hns_slc_lru_set_groups	<p>Number of sets in monitor group for enhance LRU</p> <p>2'b00 16</p> <p>2'b01 32</p> <p>2'b10 64</p> <p>2'b11 128</p> <p>NOTE: Default is 32 sets per monitor group. If cache size is small (128KB or less), there would be only one set per group.</p>	RW	2'b01
[42]	hns_slc_lru_victim_disable	<p>Disable enhanced LRU based victim selection for SLC</p> <p>1'b0 SLC victim selection is based on eLRU.</p> <p>1'b1 SLC victim selection is based on LFSR.</p> <p>NOTE: Victim selection for SF is always LFSR-based.</p>	RW	1'b1
[41]	hns_slc_victim_qos_high	<p>SLC victim QoS behavior for SN write request</p> <p>1'b0 Each victim inherits the QoS value of the request which caused it</p> <p>1'b1 All victims use high QoS class (14)</p>	RW	1'b0
[40]	hns_sf_snp_vec_disable	Disables SF snoop vector when set	RW	1'b0
[39:37]	Reserved	Reserved	RO	-
[36]	hns_cu_excl_opt_en	CleanUnique exclusive optimization enable	RW	1'b1
[35:33]	Reserved	Reserved	RO	-
[32]	hns_rd_excl_opt_en	ReadNotSharedDirty exclusive optimization enable	RW	1'b0
[31:17]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[16]	hns_poison_intr_en	Enables reporting an interrupt by HN-F when poison is detected at SLC	RW	Configuration dependent
[15]	hns_dct_disable	Disables DCT when set	RW	Configuration dependent
[14]	wlu_alloc_on_hit	Forces WLU requests to allocate if the line hit in SLC	RW	1'b0
[13]	sf_disable	Disables SF	RW	1'b0
[12]	cg_disable	Disables HN-F architectural clock gates	RW	1'b0
[11]	slc_por_init_disable	Disables SLC and SF initialization on Reset	RW	1'b0
[10]	frz_mon_on_ovfl	Freezes the exclusive monitors	RW	1'b0
[9]	dis_seqreq_coll	-	RW	1'b0
[8]	dis_likelysh	Disables Likely Shared based allocations	RW	1'b0
[7]	hns_stash_disable	Disables HN-F stash support	RW	Configuration dependent
[6]	dis_snp_once	When set, disables SnpOnce and converts to SnpShared	RW	Configuration dependent
[5]	non_sh_no_alloc	Disables SLC allocation for non-shareable cacheable transactions when set	RW	1'b0
[4]	io_read_no_alloc	When set, disables ReadOnce and ReadNoSnp allocation in SLC from RN-Is	RW	1'b0
[3]	Reserved	Reserved	RO	-
[2]	no_wu_alloc	Disables WriteUnique/WriteLineUnique allocations in SLC when set	RW	1'b0
[1]	hns_honor_ewa	When set, postpones completion for writes where EWA=0 in the request until HN-F receives completion from MC or SBSX	RW	1'b1
[0]	hns_only_mode	Enables HN-F only mode; disables SLC and SF when set	RW	1'b0

4.3.10.8 cmn_hns_aux_ctl_1

Functions as the auxiliary control register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA10

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-289: cmn_hns_aux_ctl_1

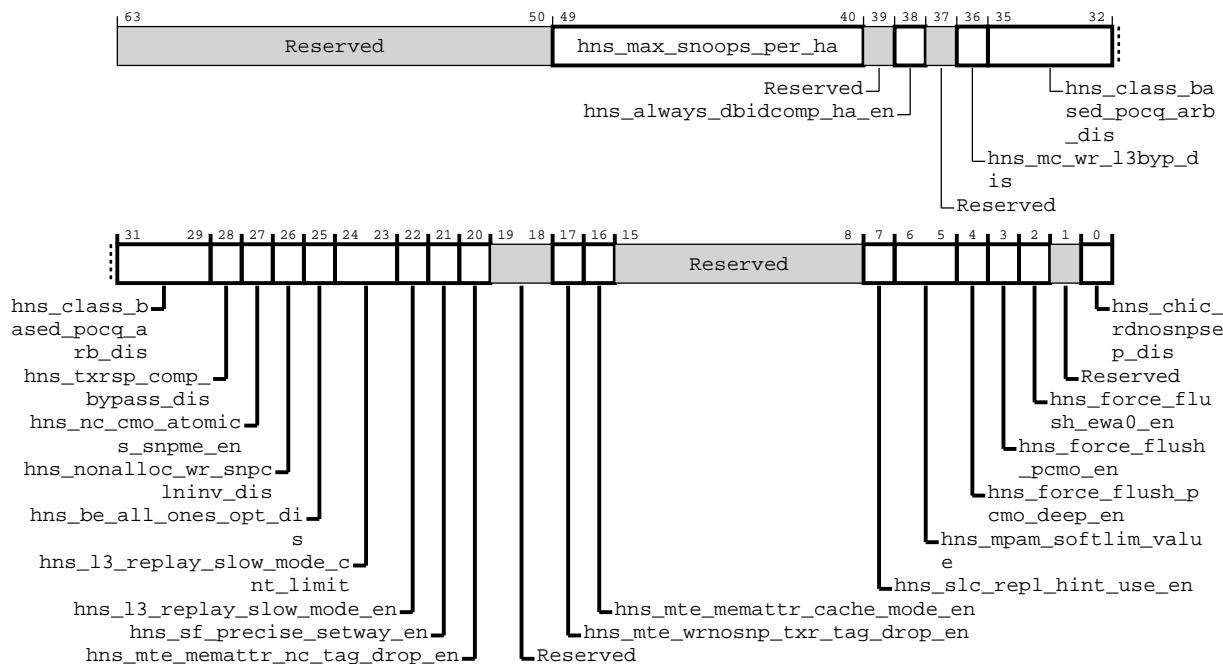


Table 4-305: cmn_hns_aux_ctl_1 attributes

Bits	Name	Description	Type	Reset
[63:50]	Reserved	Reserved	RO	-
[49:40]	hns_max_snoops_per_ha	HNS will use the register value instead of the parameter to control Max snoops per HA	RW	Configuration dependent
[39]	Reserved	Reserved	RO	-
[38]	hns_always_dbidcomp_ha_en	When set, HNS will combine DBID and Comp response for all writeunique requests from CXHA to post SLC/SF lookup and snoops	RW	1'b0
[37]	Reserved	Reserved	RO	-
[36]	hns_mc_wr_l3byp_dis	When set, disables I3 bypass path to mc request for writes	RW	1'b0

Bits	Name	Description	Type	Reset
[35:29]	hns_class_based_pocq_arb_dis	<p>Disables Class based arbitration for various POCQ arbiters. For each bit:</p> <p>1'b0 Use Class based arbitration</p> <p>1'b1 Use QoS based arbitration</p> <p>Legacy mode.</p> <p>[35] POCQ entry selection for SN Static Credit Grant return.</p> <p>[34] POCQ entry selection for SLC/SF pipeline request</p> <p>[33] POCQ entry selection for TXRSP.</p> <p>[32] POCQ entry selection for TXDAT.</p> <p>[31] POCQ entry selection for ADQ</p> <p>[29] Reserved for future use</p>	RW	7'b00000000
[28]	hns_txrsp_comp_bypass_dis	When set, TXRSP COMP bypass gets disabled for WEOE/EVICT	RW	1'b1
[27]	hns_nc_cmo_atomics_snpme_en	When set to 1, all incoming non-cachable atomics and cmo's from RNF will be back-snoped	RW	1'b0
[26]	hns_nonalloc_wr_snpclninv_dis	Disable the.snp type of.snp_cln_inv on non-allocating writes. Send.snp_uniq instead	RW	1'b0
[25]	hns_be_all_ones_opt_dis	Disable the optimizations related to BE=1's hint on WR_PTL from RNI	RW	1'b0
[24:23]	hns_l3_replay_slow_mode_cnt_limit	<p>L3 arbitration throttle count limit, when enabled.</p> <p>00 L3 Throttle is enabled after 512 setway haz replays</p> <p>01 L3 Throttle is enabled after 1024 setway haz replays</p> <p>10 L3 Throttle is enabled after 2048 setway haz replays</p> <p>11 L3 Throttle is enabled after 4096 setway haz replays</p>	RW	2'b00
[22]	hns_l3_replay_slow_mode_en	Enables L3 arbitration slow mode in case of constant replays, when set to 1'b1	RW	1'b0
[21]	hns_sf_precise_setway_en	Enables Precise setway hazard, when set to 1'b1	RW	1'b0
[20]	hns_mte_memattr_nc_tag_drop_en	Enables HNS to drop any dirty tags for Non-Cacheable memory, when set to 1'b1	RW	1'b0
[19:18]	Reserved	Reserved	RO	-
[17]	hns_mte_wrnosnp_txr_tag_drop_en	When set to 1'b1, HNS will drop clean tags from a WriteNoSnp with tagop Transfer	RW	1'b0

Bits	Name	Description	Type	Reset
[16]	hns_mte_memattr_cache_mode_en	When set to 1'b1, it enables HNS to convert Non-cacheable requests to cacheable if MTE tags are required	RW	1'b1
[15:8]	Reserved	Reserved	RO	-
[7]	hns_slc_repl_hint_use_en	<p>1'b0 Interconnect generated SLC Replacement hints are used for eLRU.</p> <p>1'b1 RN-F provided SLC Replacement hints are used for eLRU.</p>	RW	1'b1
[6:5]	hns_mpam_softlim_value	<p>2'b00 Soft limit is 0% below hardlimit</p> <p>2'b01 Soft limit is 3.13% (1/32) below hardlimit</p> <p>2'b10 Soft limit is 6.25% (1/16) below hardlimit</p> <p>2'b11 Soft limit is 9.38% (3/32) below hardlimit</p> <p>NOTE: Default is 3.13% below hardlimit. If CMAX value set is at or below 12.5%, soft limit is ignored.</p>	RW	2'b01
[4]	hns_force_flush_pcmo_deep_en	Make PCMO request for SLC and SF flush generated SN writes as Deep PCMO. CONSTRAINT: hns_force_flush_pcmo_deep_en is valid only if hns_force_flush_pcmo_en bit is set. CONSTRAINT: This bit can be set only if ALL SNS in the system support deep attribute.	RW	1'b0
[3]	hns_force_flush_pcmo_en	Generate PCMO request for SLC and SF flush generated SN writes	RW	1'b0
[2]	hns_force_flush_ewa0_en	Force SLC and SF flush to use EWA 0 for SN writes	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	hns_chic_rdnosnsep_dis	Disables separation of Data and Comp in CHIC mode	RW	1'b0

4.3.10.9 cmn_hns_cbusy_limit_ctl

Cbusy threshold limits for POCQ entries.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA18

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-290: cmn_hns_cbusy_limit_ctl

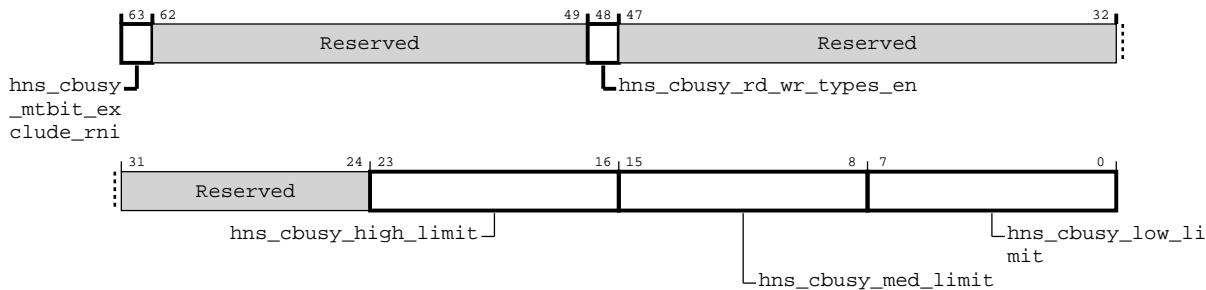


Table 4-306: cmn_hns_cbusy_limit_ctl attributes

Bits	Name	Description	Type	Reset
[63]	hns_cbusy_mtbit_exclude_rni	Exclude RNI sources in multi-source mode	RW	1'b0
[62:49]	Reserved	Reserved	RO	-
[48]	hns_cbusy_rd_wr_types_en	When set, CBusy for Reads and Writes are handled independently. The thresholds specified in this register are used for Read request types in POCQ	RW	1'b0
[47:24]	Reserved	Reserved	RO	-
[23:16]	hns_cbusy_high_limit	POCQ limit for CBusy High	RW	Configuration dependent
[15:8]	hns_cbusy_med_limit	POCQ limit for CBusy Med	RW	Configuration dependent
[7:0]	hns_cbusy_low_limit	POCQ limit for CBusy Low	RW	Configuration dependent

4.3.10.10 cmn_hns_txrsp_arb_weight_ctl

TXRSP arbitration weight controls.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA20

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-291: cmn_hns_txrsp_arb_weight_ctl

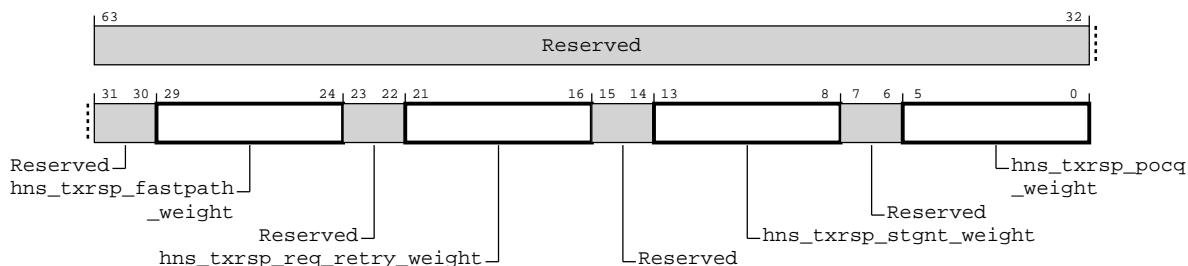


Table 4-307: cmn_hns_txrsp_arb_weight_ctl attributes

Bits	Name	Description	Type	Reset
[63:30]	Reserved	Reserved	RO	-
[29:24]	hns_txrsp_fastpath_weight	Fastpath response weights for TXRSP channel	RW	6'b111111
[23:22]	Reserved	Reserved	RO	-
[21:16]	hns_txrsp_req_retry_weight	Request retry response weights for TXRSP channel	RW	6'b000001
[15:14]	Reserved	Reserved	RO	-
[13:8]	hns_txrsp_stgnt_weight	Static Credit Grant response weights for TXRSP channel	RW	6'b000001
[7:6]	Reserved	Reserved	RO	-
[5:0]	hns_txrsp_pocq_weight	POCQ response weights for TXRSP channel	RW	6'b000001

4.3.10.11 cmn_hns_cbusy_mode_ctl

Control register for additional CBusy controls

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA28

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-292: cmn_hns_cbusy_mode_ctl

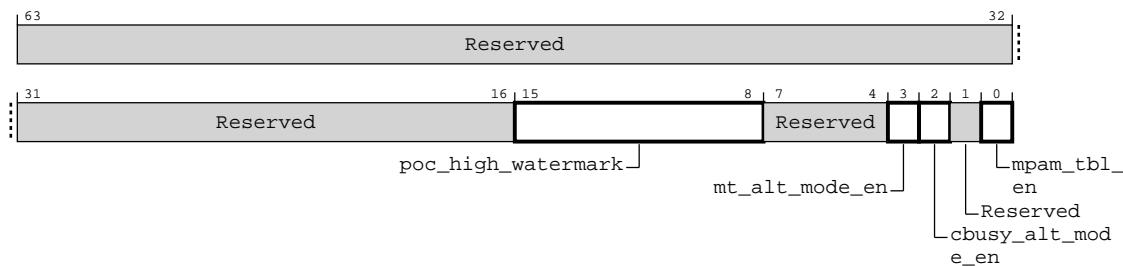


Table 4-308: cmn_hns_cbusy_mode_ctl attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:8]	poc_high_watermark	Number of POCQ entries when it is considered high occupancy	RW	Configuration dependent
[7:4]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[3]	mt_alt_mode_en	Enable CBusy[2] alternate reporting mode: 1'b0 POCQ has requests from more than one source 1'b1 POCQ Occupancy is higher than the poc_high_watermark	RW	1'b0
[2]	cbusy_alt_mode_en	Enables an alternate mode of SN CBusy[1:0] capture for mpam_tbl_en=1 mode: 1'b0 For each MPAM partID, CBusy[1:0] = SN_CBusy[1:0] 1'b1 For each MPAM partID, CBusy[1] = SN's CBusy[2], CBusy[0] = (SN_CBusy[1] & SN_CBusy[0])	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	mpam_tbl_en	Enables cbusy reporting based on MPAM part ID	RW	1'b0

4.3.10.12 cmn_hns_lbt_cfg_ctl

Functions as the configuration control register for HN-F. Only applicable to LBT transactions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA30

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-293: cmn_hns_lbt_cfg_ctl

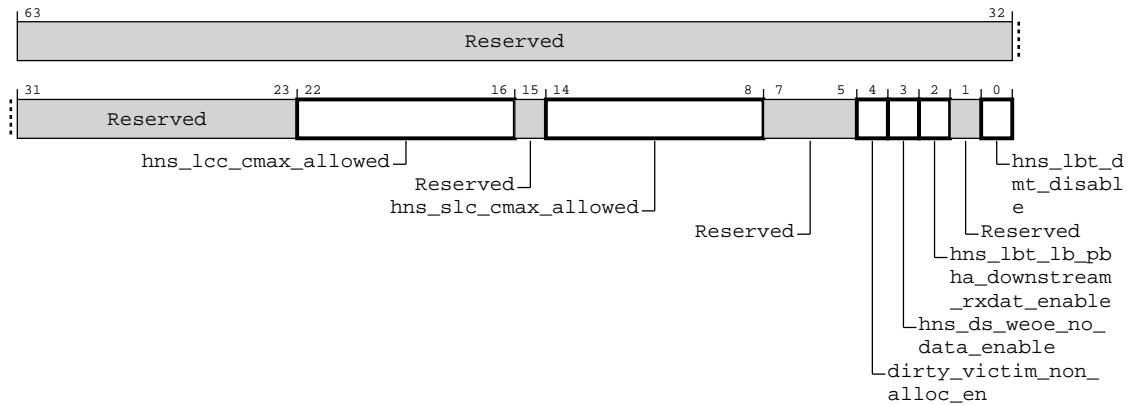


Table 4-309: cmn_hns_lbt_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:23]	Reserved	Reserved	RO	-
[22:16]	hns_lcc_cmax_allowed	Maximum cache capacity usage in fixed-point fraction of the cache capacity by LBT lines	RW	7'b1111111
[15]	Reserved	Reserved	RO	-
[14:8]	hns_slc_cmax_allowed	Maximum cache capacity usage in fixed-point fraction of the cache capacity by HBT lines	RW	7'b1111111
[7:5]	Reserved	Reserved	RO	-
[4]	dirty_victim_non_alloc_en	When HNS issues dirty CopyBack writes for LCC victim or SFBI, set non-allocating type	RW	1'b0
[3]	hns_ds_weoe_no_data_enable	When HNS issues WriteEvictOrEvict downstream, force no data transfer if config bit is set	RW	1'b0
[2]	hns_lbt_lb_pbha_downstream_rxdat_enable	Takes LB/PBHA values from downstream RXDAT for LBT lines	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	hns_lbt_dmt_disable	Disables DMT when set	RW	1'b0

4.3.10.13 cmn_hns_lbt_aux_ctl

Functions as the auxiliary control register for HN-F. Only applicable to LBT transactions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA38

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-294: cmn_hns_lbt_aux_ctl

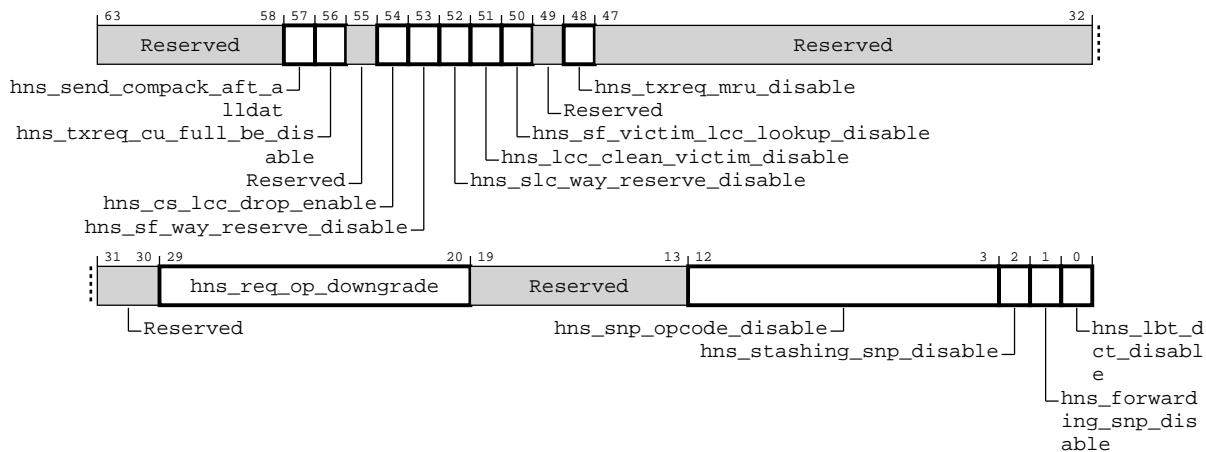


Table 4-310: cmn_hns_lbt_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57]	hns_send_compack_aft_alldat	Enables sending CompAck after all data beats are received	RW	1'b0
[56]	hns_txreq_cu_full_be_disable	Disables LCC always getting ownership by CleanUnique for streaming writes with full BE.	RW	1'b0
[55]	Reserved	Reserved	RO	-
[54]	hns_cs_lcc_drop_enable	Enables LCC to drop clean copy after writing dirty data for CleanShared.	RW	1'b1
[53]	hns_sf_way_reserve_disable	Disables SF reserved way for HBT lines in HNS mode and allow LBT lines to take all ways in SF.	RW	1'b0
[52]	hns_slc_way_reserve_disable	Disables SLC reserved way for HBT lines in HNS mode and allow LBT lines to take all ways in system cache.	RW	1'b0
[51]	hns_lcc_clean_victim_disable	Disables LCC sending clean eviction to Home Node.	RW	1'b0
[50]	hns_sf_victim_lcc_lookup_disable	Disables LCC lookup for a SF victim.	RW	1'b0
[49]	Reserved	Reserved	RO	-
[48]	hns_txreq_mru_disable	Disables sending MRU opcode downstream. Use RDUNIQ instead	RW	1'b0
[47:30]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[29:20]	hns_req_op_downgrade	<p>Downgrades req opcode when set</p> <p>[20] Change READSHARED to READUNIQ</p> <p>[21] Change READNOTSHAREDDIRTY to READUNIQ</p> <p>[22] Change READPREFERUNIQ to READUNIQ</p> <p>[23] Change READONCEMKINV to READONCE</p> <p>[24] Change READONCECLNINV to READONCE</p> <p>[25] Change MAKEUNIQ to CLNUIQ</p> <p>[26] Change MAKEREADUNIQ to READUNIQ</p> <p>[27] Change WRITEEVICTOREVICT to EVICT</p> <p>[28] Change MAKEINVALID to CLEANINVALID</p> <p>[29] Change WRITEUNIQUEFULL to non-allocating WRITEUNIQUEPTL</p>	RW	10'h000
[19:13]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[12:3]	hns_snp_opcode_disable	<p>Disables support for RXSNP different snoop opcodes and changes to similar snoop opcode when set</p> <p>[3] Change SNPSTASHSHARED to SNPQUERY</p> <p>[4] Change SNPSTASHUNIQUE to SNPQUERY</p> <p>[5] Change SNPMAKEINVALIDSTASH to SNPMAKEINVALID</p> <p>[6] Change SNPCLEANSHARED to SNPCLEANINVALID</p> <p>[7] Change SNPPREFERUNIQUE(FWD) to SNPUNIQUE</p> <p>[8] Change SNPNOTSHAREDDIRTY(FWD) to SNPUNIQUE</p> <p>[9] Change SNPCLEAN(FWD) to SNPUNIQUE</p> <p>[10] Change SNPUNIQUESTASH to SNPUNIQUE</p> <p>[11] Change SNPONCE(FWD) to SNPUNIQUE</p> <p>[12] Change SNPSHARED(FWD) to SNPUNIQUE</p>	RW	10'h000
[2]	hns_stashing_snp_disable	Disables Stashing type of snoops when set for RXSNP	RW	1'b1
[1]	hns_forwarding_snp_disable	Disables Forwarding type of snoops when set for RXSNP	RW	1'b1
[0]	hns_lbt_dct_disable	Disables DCT when set	RW	1'b0

4.3.10.14 cmn_hns_ppu_pwpr

Functions as the power policy register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h1C00

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ppu

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-295: cmn_hns_ppu_pwpr

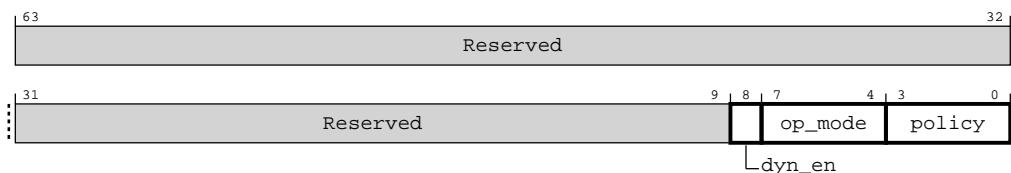


Table 4-311: cmn_hns_ppu_pwpr attributes

Bits	Name	Description	Type	Reset
[32:9]	Reserved	Reserved	RO	-
[8]	dyn_en	Dynamic transition enable	RW	1'b0
[7:4]	op_mode	HN-F operational power mode 4'b0011 FAM 4'b0010 HAM 4'b0001: SFONLY 4'b0000 NOSFSLC	RW	4'b0
[3:0]	policy	HN-F power mode policy 4'b1000 ON 4'b0111 FUNC_RET 4'b0010: MEM_RET 4'b0000 OFF	RW	4'b0

4.3.10.15 cmn_hns_ppu_pwsr

Provides power status information for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h1C08

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-296: cmn_hns_ppu_pwsr

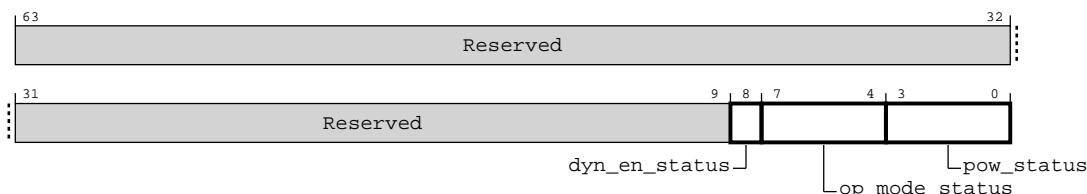


Table 4-312: cmn_hns_ppu_pwsr attributes

Bits	Name	Description	Type	Reset
[32:9]	Reserved	Reserved	RO	-
[8]	dyn_en_status	Dynamic transition status	RO	1'b0

Bits	Name	Description	Type	Reset
[7:4]	op_mode_status	HN-F operational mode status 4'b0011 FAM 4'b0010 HAM 4'b0001: SFONLY 4'b0000 NOSFSLC	RO	4'b0
[3:0]	pow_status	HN-F power mode status 4'b1000 ON 4'b0111 FUNC_RET 4'b0010: MEM_RET 4'b0000 OFF	RO	4'b0

4.3.10.16 cmn_hns_ppu_misr

Functions as the power miscellaneous input current status register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h1C14

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-297: cmn_hns_ppu_misr

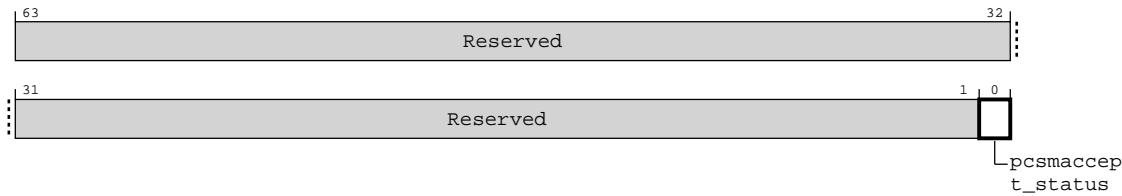


Table 4-313: cmn_hns_ppu_misr attributes

Bits	Name	Description	Type	Reset
[32:1]	Reserved	Reserved	RO	-
[0]	pcsmaccep_t_status	HN-F RAM PCSMACCEPT status	RO	1'b0

4.3.10.17 cmn_hns_ppu_idr0

Provides identification information for the HN-F PPU.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h2BB0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-298: cmn_hns_ppu_idr0

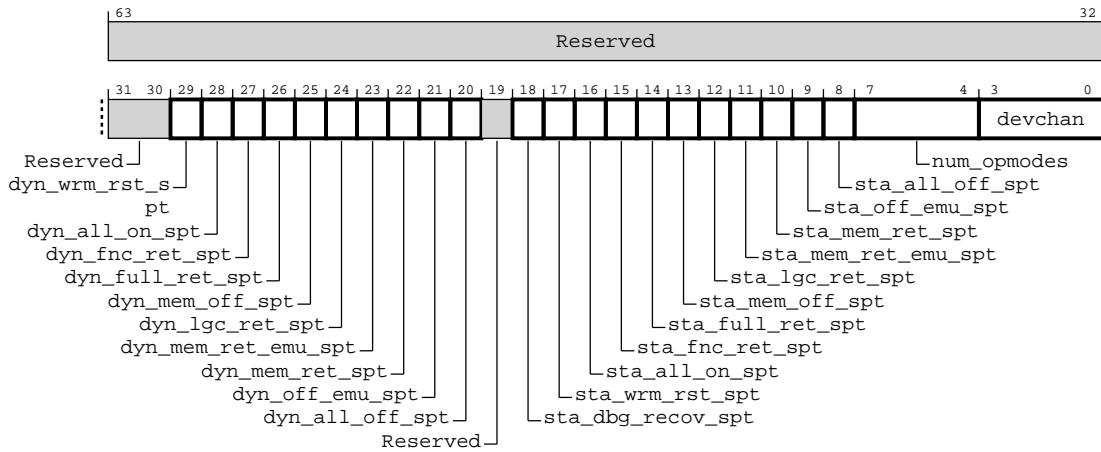


Table 4-314: cmn_hns_ppu_idr0 attributes

Bits	Name	Description	Type	Reset
[32:30]	Reserved	Reserved	RO	-
[29]	dyn_wrm_rst_spt	Dynamic warm_rst support	RO	1'b0
[28]	dyn_all_on_spt	Dynamic on support	RO	1'b0
[27]	dyn_fnc_ret_spt	Dynamic func_ret support	RO	1'b1
[26]	dyn_full_ret_spt	Dynamic full_ret support	RO	1'b0
[25]	dyn_mem_off_spt	Dynamic mem_off support	RO	1'b0
[24]	dyn_lgc_ret_spt	Dynamic logic_ret support	RO	1'b0
[23]	dyn_mem_ret_emu_spt	Dynamic mem_ret_emu support	RO	1'b0
[22]	dyn_mem_ret_spt	Dynamic mem_ret support	RO	1'b0
[21]	dyn_off_emu_spt	Dynamic off_emu support	RO	1'b0
[20]	dyn_all_off_spt	Dynamic off support	RO	1'b0
[19]	Reserved	Reserved	RO	-
[18]	sta_dbg_recov_spt	Static dbg_recov support	RO	1'b0
[17]	sta_wrm_rst_spt	Static warm_rst support	RO	1'b0
[16]	sta_all_on_spt	Static on support	RO	1'b1
[15]	sta_fnc_ret_spt	Static func_ret support	RO	1'b1
[14]	sta_full_ret_spt	Static full_ret support	RO	1'b0
[13]	sta_mem_off_spt	Static mem_off support	RO	1'b1
[12]	sta_lgc_ret_spt	Static logic_ret support	RO	1'b0
[11]	sta_mem_ret_emu_spt	Static mem_ret_emu support	RO	1'b0
[10]	sta_mem_ret_spt	Static mem_ret support	RO	1'b1
[9]	sta_off_emu_spt	Static off_emu support	RO	1'b0
[8]	sta_all_off_spt	Static off support	RO	1'b1
[7:4]	num_opmodes	Number of operational modes	RO	4'b0100
[3:0]	devchan	Number of device interface channels	RO	1'b0

4.3.10.18 cmn_hns_ppu_idr1

Provides identification information for the HN-F PPU.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h2BB4

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-299: cmn_hns_ppu_idr1

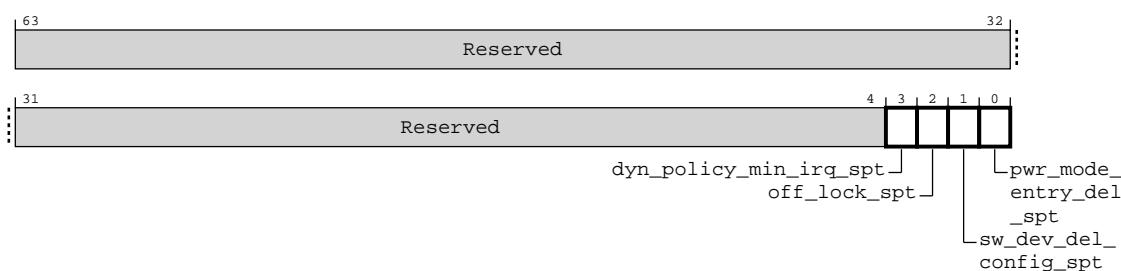


Table 4-315: cmn_hns_ppu_idr1 attributes

Bits	Name	Description	Type	Reset
[32:4]	Reserved	Reserved	RO	-
[3]	dyn_policy_min_irq_spt	Dynamic minimum policy interrupt support	RO	1'b0
[2]	off_lock_spt	Off and mem_ret lock support	RO	1'b0
[1]	sw_dev_del_config_spt	Software device delay control configuration support	RO	1'b0
[0]	pwr_mode_entry_del_spt	Power mode entry delay support	RO	1'b0

4.3.10.19 cmn_hns_ppu_iidr

Functions as the power implementation identification register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h2BC8

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-300: cmn_hns_ppu_iidr

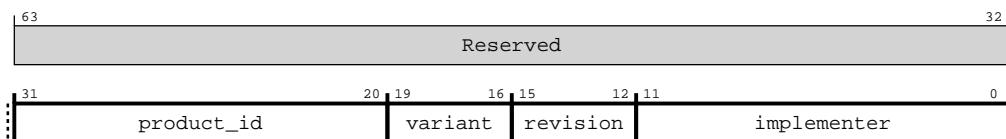


Table 4-316: cmn_hns_ppu_iidr attributes

Bits	Name	Description	Type	Reset
[32]	Reserved	Reserved	RO	-
[31:20]	product_id	Implementation identifier	RO	12'h434
[19:16]	variant	Implementation variant	RO	4'h0
[15:12]	revision	Implementation revision	RO	4'h0
[11:0]	implementer	Arm implementation	RO	12'h43B

4.3.10.20 cmn_hns_ppu_aistr

Functions as the power architecture identification register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

32

Address offset

16'h2BCC

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-301: cmn_hns_ppu_aistr

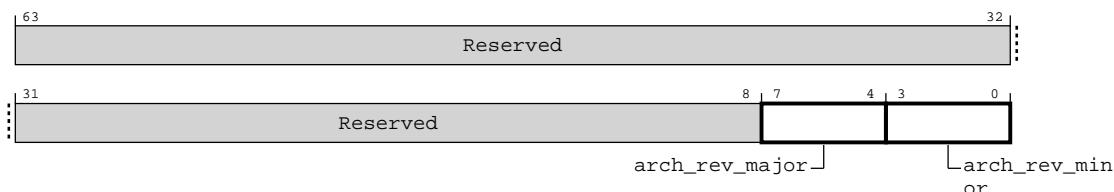


Table 4-317: cmn_hns_ppu_aistr attributes

Bits	Name	Description	Type	Reset
[32:8]	Reserved	Reserved	RO	-
[7:4]	arch_rev_major	PPU architecture major revision	RO	4'h1
[3:0]	arch_rev_minor	PPU architecture minor revision	RO	4'h1

4.3.10.21 cmn_hns_ppu_dyn_ret_threshold

Configures the dynamic retention threshold for SLC and SF RAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1D00

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ppu

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-302: cmn_hns_ppu_dyn_ret_threshold

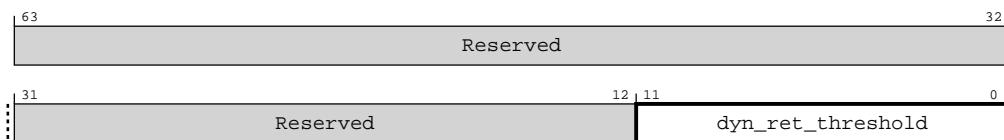


Table 4-318: cmn_hns_ppu_dyn_ret_threshold attributes

Bits	Name	Description	Type	Reset
[63:12]	Reserved	Reserved	RO	-
[11:0]	dyn_ret_threshold	HN-F RAM idle cycle count threshold	RW	32'b0

4.3.10.22 cmn_hns_qos_band

Provides QoS classifications based on the QoS value ranges.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA80

Type

RO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-303: cmn_hns_qos_band

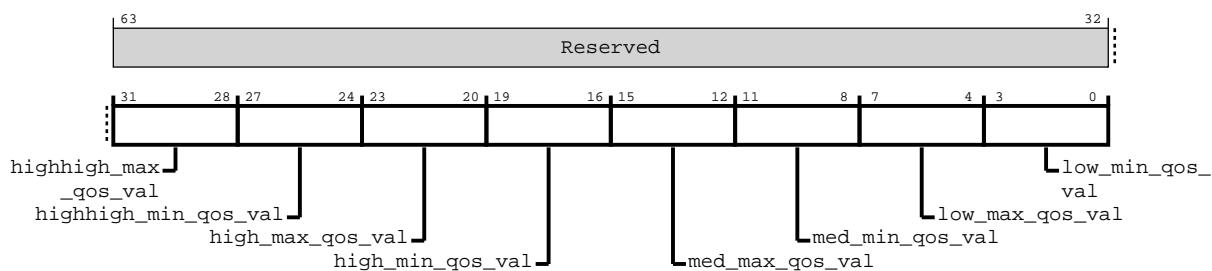


Table 4-319: cmn_hns_qos_band attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	highhigh_max_qos_val	Maximum value for HighHigh QoS class	RO	4'hF
[27:24]	highhigh_min_qos_val	Minimum value for HighHigh QoS class	RO	4'hF
[23:20]	high_max_qos_val	Maximum value for High QoS class	RO	4'hE
[19:16]	high_min_qos_val	Minimum value for High QoS class	RO	4'hC

Bits	Name	Description	Type	Reset
[15:12]	med_max_qos_val	Maximum value for Medium QoS class	RO	4'hB
[11:8]	med_min_qos_val	Minimum value for Medium QoS class	RO	4'h8
[7:4]	low_max_qos_val	Maximum value for Low QoS class	RO	4'h7
[3:0]	low_min_qos_val	Minimum value for Low QoS class	RO	4'h0

4.3.10.23 cmn_hns_errfr

Functions as the error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3000

Type

RO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-304: cmn_hns_errfr

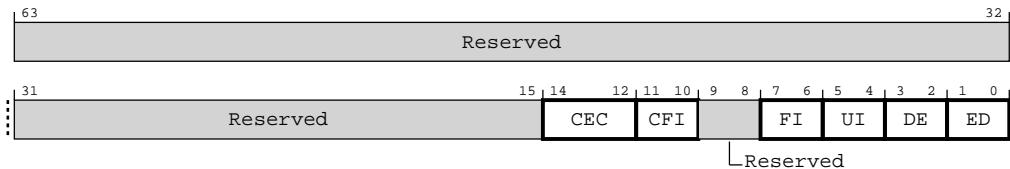


Table 4-320: cmn_hns_errfr attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[14:12]	CEC	Standard corrected error count mechanism 3'b000 Does not implement standardized error counter model 3'b010 Implements 8-bit error counter in cmn_hns_errmisc[39:32] 3'b100 Implements 16-bit error counter in cmn_hns_errmisc[47:32]	RO	3'b100
[11:10]	CFI	Corrected error interrupt	RO	2'b10
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors for data poison	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.10.24 cmn_hns_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3008

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-305: cmn_hns_errctlr

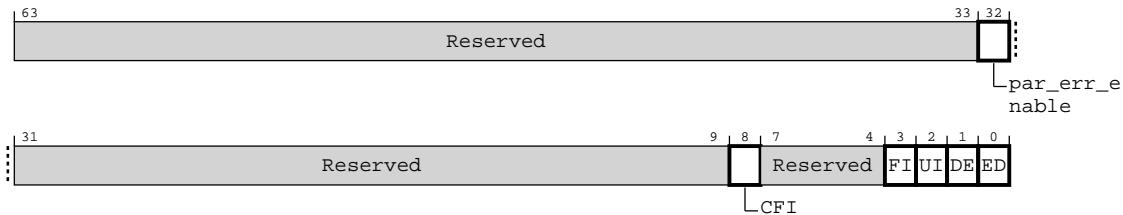


Table 4-321: cmn_hns_errctlr attributes

Bits	Name	Description	Type	Reset
[63:33]	Reserved	Reserved	RO	-
[32]	par_err_enable	Enables external logging parity errors when set to 1'b1	RW	1'b0
[31:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in cmn_hns_errfr.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in cmn_hns_errfr.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in cmn_hns_errfr.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in cmn_hns_errfr.DE	RW	1'b0
[0]	ED	Enables error detection as specified in cmn_hns_errfr.ED	RW	1'b0

4.3.10.25 cmn_hns_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3010

Type

W1C

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-306: cmn_hns_errstatus

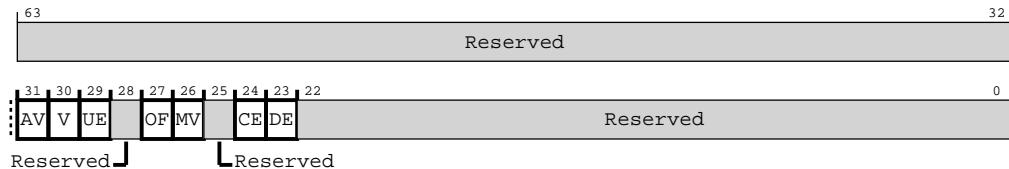


Table 4-322: cmn_hns_errstatus attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; cmn_hns_erraddr contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Bits	Name	Description	Type	Reset
[26]	MV	cmn_hns_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.10.26 cmn_hns_erraddr

Contains the error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3018

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-307: cmn_hns_erraddr

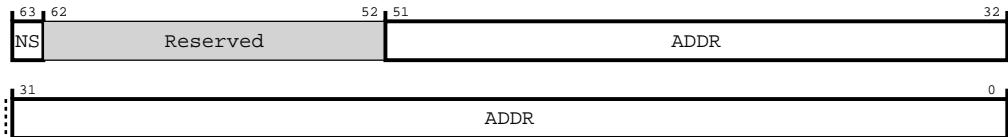


Table 4-323: cmn_hns_erraddr attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: cmn_hns_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.10.27 cmn_hns_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3020

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-308: cmn_hns_errmisc

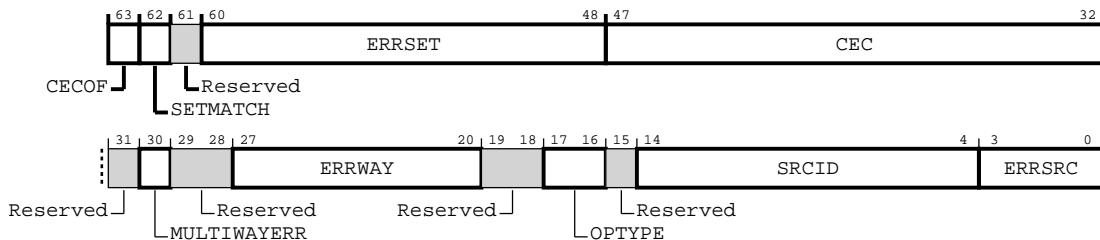


Table 4-324: cmn_hns_errmisc attributes

Bits	Name	Description	Type	Reset
[63]	CECOF	Corrected error counter overflow	RW	1'b0
[62]	SETMATCH	Set address match	RW	1'b0
[61]	Reserved	Reserved	RO	-
[60:48]	ERRSET	SLC/SF set address for ECC error	RW	13'b0
[47:32]	CEC	Corrected ECC error count	RW	16'b0
[31]	Reserved	Reserved	RO	-
[30]	MULTIWAYERR	Indicate multiple ways have ECC error	RW	1'b0
[29:28]	Reserved	Reserved	RO	-
[27:20]	ERRWAY	SLC/SF way ID for ECC error	RW	8'b0
[19:18]	Reserved	Reserved	RO	-
[17:16]	OPTYPE	Error op type	RW	2'b00
		2'b00 Writes, CleanShared, Atomics and stash requests with invalid targets		
		2'b01 WriteBack, Evict, and Stash requests with valid target		
		2'b10 CMO		
		2'b11 Other op types		
[15]	Reserved	Reserved	RO	-
[14:4]	SRCID	Error source ID	RW	11'b0

Bits	Name	Description	Type	Reset
[3:0]	ERRSRC	Error source	RW	4'b0000
		4'b0001 Data single-bit ECC		
		4'b0010 Data double-bit ECC		
		4'b0011 Single-bit ECC overflow		
		4'b0100 Tag single-bit ECC		
		4'b0101 Tag double-bit ECC		
		4'b0111 SF tag single-bit ECC		
		4'b1000 SF tag double-bit ECC		
		4'b1010 Data parity error		
		4'b1011 Data parity and poison		
		4'b1100 NDE		

4.3.10.28 cmn_hns_err_inj

Enables error injection and setup. When enabled for a given source ID and logic processor ID, HN-F returns a subordinate error and reports an error interrupt. This error interrupt emulates a SLC double-bit data ECC error. This feature enables software to test the error handler. The subordinate error is reported for cacheable read access for which SLC hit is the data source. No subordinate error or error interrupt is reported for cacheable read access in which SLC miss is the data source.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3030

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-309: cmn_hns_err_inj

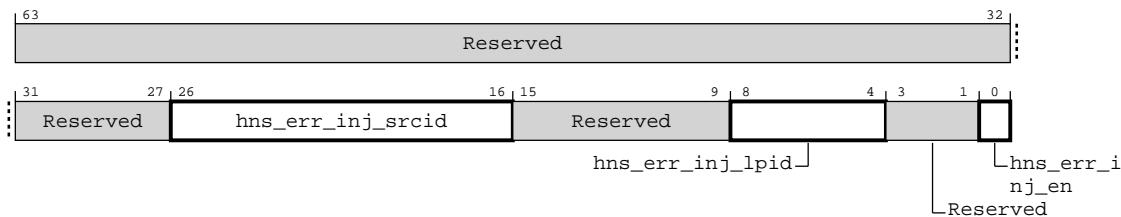


Table 4-325: cmn_hns_err_inj attributes

Bits	Name	Description	Type	Reset
[63:27]	Reserved	Reserved	RO	-
[26:16]	hns_err_inj_srcid	RN source ID for read access which results in a SLC miss; does not report subordinate error or error to match error injection	RW	11'h0
[15:9]	Reserved	Reserved	RO	-
[8:4]	hns_err_inj_lpid	LPID used to match for error injection	RW	5'h0
[3:1]	Reserved	Reserved	RO	-
[0]	hns_err_inj_en	Enables error injection and report	RW	1'b0

4.3.10.29 cmn_hns_byte_par_err_inj

Functions as the byte parity error injection register for HN-F.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3038

Type

WO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-310: cmn_hns_byte_par_err_inj

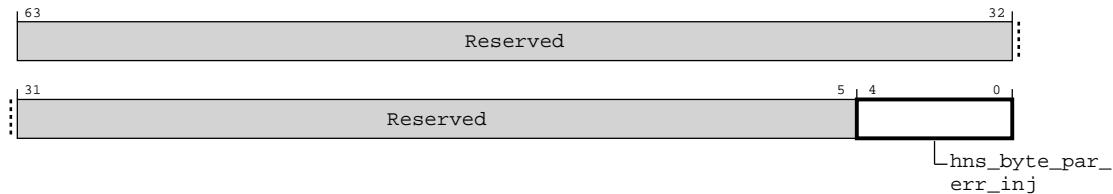


Table 4-326: cmn_hns_byte_par_err_inj attributes

Bits	Name	Description	Type	Reset
[63:5]	Reserved	Reserved	RO	-
[4:0]	hns_byte_par_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next SLC hit; the error will be injected in all data flits on specified byte (0 to 31)	WO	5'h0

4.3.10.30 cmn_hns_errfr_NS

Functions as the Non-secure error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3100

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-311: cmn_hns_errfr_NS

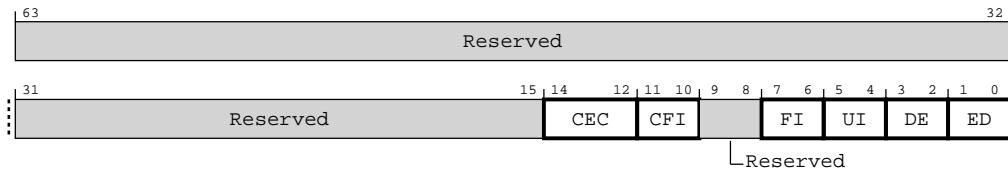


Table 4-327: cmn_hns_errfr_NS attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000 Does not implement standardized error counter model 3'b010 Implements 8-bit error counter in cmn_hns_errmisc[39:32] 3'b100 Implements 16-bit error counter in cmn_hns_errmisc[47:32]	RO	3'b100
[11:10]	CFI	Corrected error interrupt	RO	2'b10
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors for data poison	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.10.31 cmn_hns_errctlr_NS

Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3108

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-312: cmn_hns_errctlr_NS

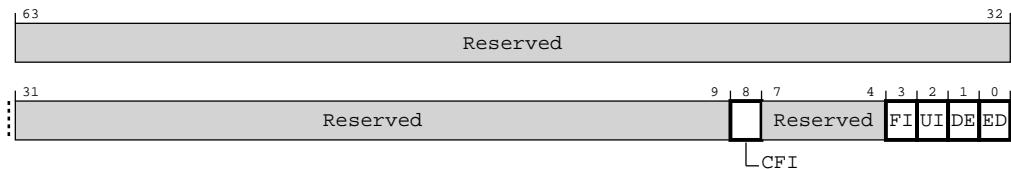


Table 4-328: cmn_hns_errctlr_NS attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in cmn_hns_errfr_NS.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in cmn_hns_errfr_NS.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in cmn_hns_errfr_NS.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in cmn_hns_errfr_NS.DE	RW	1'b0
[0]	ED	Enables error detection as specified in cmn_hns_errfr_NS.ED	RW	1'b0

4.3.10.32 cmn_hns_errstatus_NS

Functions as the Non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3110

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-313: cmn_hns_errstatus_NS

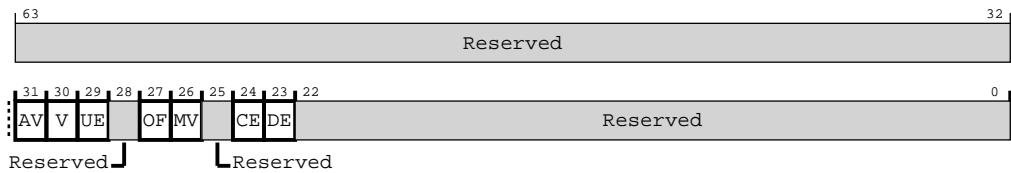


Table 4-329: cmn_hns_errstatus_NS attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; cmn_hns_erraddr_NS contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	cmn_hns_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0

Bits	Name	Description	Type	Reset
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.10.33 cmn_hns_erraddr_NS

Contains the Non-secure error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3118

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-314: cmn_hns_erraddr_NS

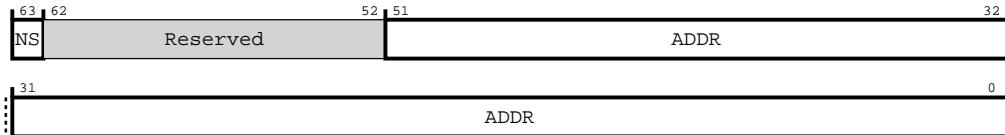


Table 4-330: cmn_hns_erraddr_NS attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: cmn_hns_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.10.34 cmn_hns_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3120

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-315: cmn_hns_errmisc_NS

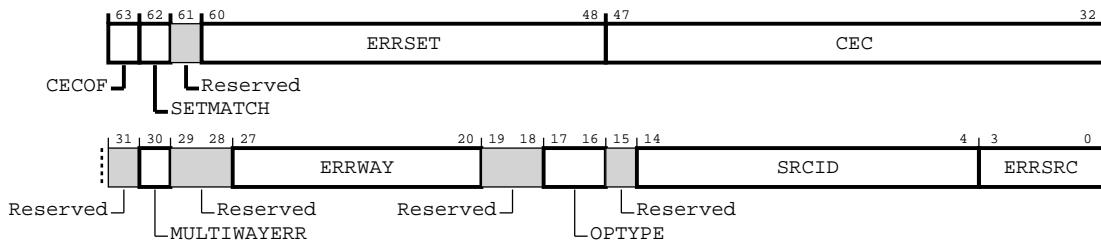


Table 4-331: cmn_hns_errmisc_NS attributes

Bits	Name	Description	Type	Reset
[63]	CECOF	Corrected error counter overflow	RW	1'b0
[62]	SETMATCH	Set address match	RW	1'b0
[61]	Reserved	Reserved	RO	-
[60:48]	ERRSET	SLC/SF set address for ECC error	RW	13'b0
[47:32]	CEC	Corrected ECC error count	RW	16'b0
[31]	Reserved	Reserved	RO	-
[30]	MULTIWAYERR	Indicate multiple ways have ECC error	RW	1'b0
[29:28]	Reserved	Reserved	RO	-
[27:20]	ERRWAY	SLC/SF way ID for ECC error	RW	8'b0
[19:18]	Reserved	Reserved	RO	-
[17:16]	OPTYPE	Error op type	RW	2'b00
		2'b00 Writes, CleanShared, Atomics and stash requests with invalid targets		
		2'b01 WriteBack, Evict, and Stash requests with valid target		
		2'b10 CMO		
		2'b11 Other op types		
[15]	Reserved	Reserved	RO	-
[14:4]	SRCID	Error source ID	RW	11'b0
[3:0]	ERRSRC	Error source	RW	4'b0000
		4'b0001 Data single-bit ECC		
		4'b0010 Data double-bit ECC		
		4'b0011 Single-bit ECC overflow		
		4'b0100 Tag single-bit ECC		
		4'b0101 Tag double-bit ECC		
		4'b0111 SF tag single-bit ECC		
		4'b1000 SF tag double-bit ECC		
		4'b1010 Data parity error		
		4'b1011 Data parity and poison		
		4'b1100 NDE		

4.3.10.35 cmn_hns_slc_lock_ways

Controls SLC way lock settings.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC00

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-316: cmn_hns_slc_lock_ways

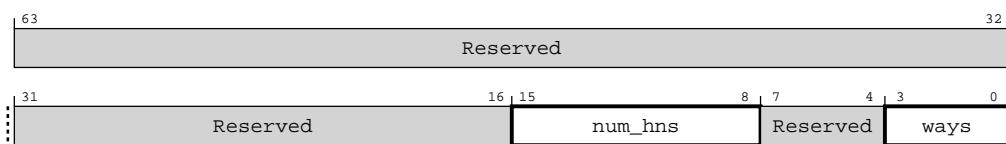


Table 4-332: cmn_hns_slc_lock_ways attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:8]	num_hns	Number of HN-Fs in NUMA (non-uniform memory access) region	RW	Configuration dependent
[7:4]	Reserved	Reserved	RO	-
[3:0]	ways	Number of SLC ways locked (1, 2, 4, 8, 12)	RW	4'b0

4.3.10.36 cmn_hns_slc_lock_base0

Functions as the base register for lock region 0 [47:0].

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16' hC08

Type

RW

Reset value

See individual bit resets

Secure group override

cmm hns secure register groups override.slc lock ways

Usage constraints

Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-317: cmn hns slc lock base0

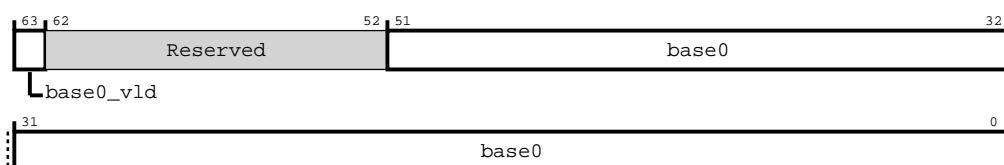


Table 4-333: cmn hns slc lock base0 attributes

Bits	Name	Description	Type	Reset
[63]	base0_vld	Lock region 0 base valid	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	base0	Lock region 0 base address	RW	52'b0

4.3.10.37 cmn_hns_slc_lock_base1

Functions as the base register for lock region 1 [47:0].

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hc10

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-318: cmn_hns_slc_lock_base1

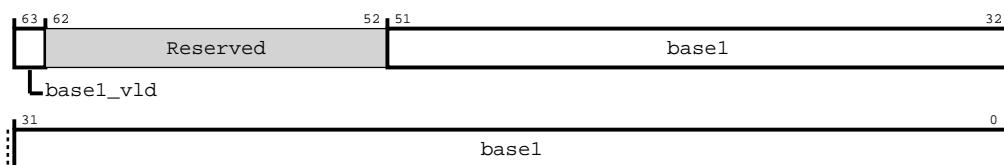


Table 4-334: cmn_hns_slc_lock_base1 attributes

Bits	Name	Description	Type	Reset
[63]	base1_vld	Lock region 1 base valid	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	base1	Lock region 1 base address	RW	52'b0

4.3.10.38 cmn_hns_slc_lock_base2

Functions as the base register for lock region 2 [47:0].

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC18

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-319: cmn_hns_slc_lock_base2

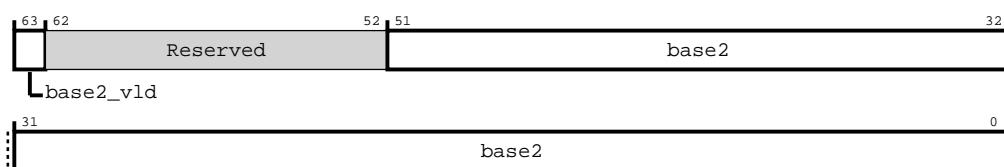


Table 4-335: cmn_hns_slc_lock_base2 attributes

Bits	Name	Description	Type	Reset
[63]	base2_vld	Lock region 2 base valid	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	base2	Lock region 2 base address	RW	52'b0

4.3.10.39 cmn_hns_slc_lock_base3

Functions as the base register for lock region 3 [47:0].

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC20

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-320: cmn_hns_slc_lock_base3

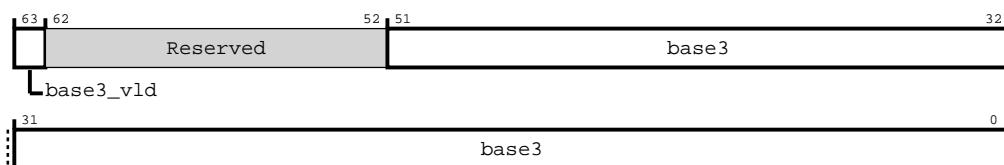


Table 4-336: cmn_hns_slc_lock_base3 attributes

Bits	Name	Description	Type	Reset
[63]	base3_vld	Lock region 3 base valid	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	base3	Lock region 3 base address	RW	52'b0

4.3.10.40 cmn_hns_rni_region_vec

Functions as the control register for RN-I source SLC way allocation.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC28

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-321: cmn_hns_rni_region_vec

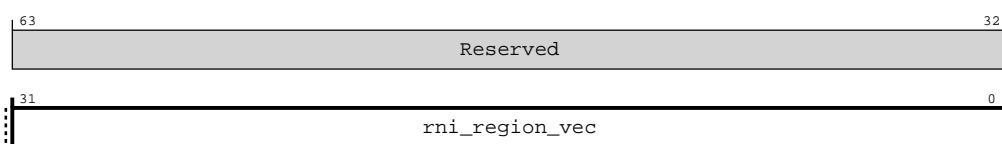


Table 4-337: cmn_hns_rni_region_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rni_region_vec	Bit vector mask; identifies which logical IDs of the RN-Is to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

4.3.10.41 cmn_hns_rnd_region_vec

Functions as the control register for RN-D source SLC way allocation.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC30

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-322: cmn_hns_rnd_region_vec

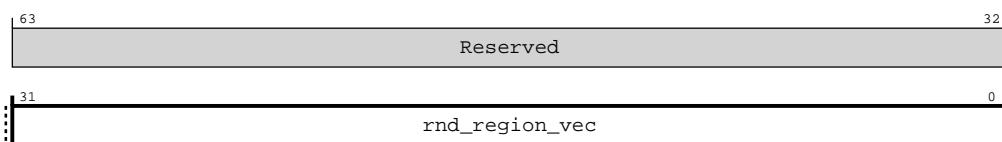


Table 4-338: cmn_hns_rnd_region_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rnd_region_vec	Bit vector mask; identifies which logical IDs of the RN-Ds to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

4.3.10.42 cmn_hns_rnf_region_vec

Functions as the control register for RN-F source SLC way allocation.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC38

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-323: cmn_hns_rnf_region_vec

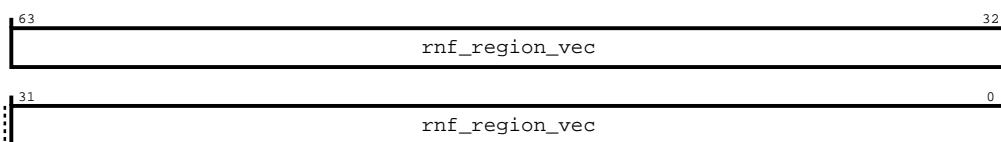


Table 4-339: cmn_hns_rnf_region_vec attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

4.3.10.43 cmn_hns_rnf_region_vec1

Functions as the control register for RN-F source SLC way allocation for logical IDs 64 through 127.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC40

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slc_lock_ways`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-324: cmn_hns_rnf_region_vec1

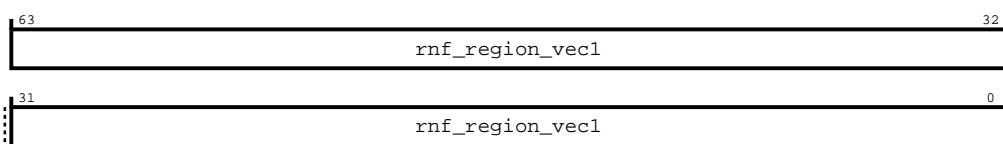


Table 4-340: cmn_hns_rnf_region_vec1 attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

4.3.10.44 cmn_hns_slcway_partition0_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC48

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-325: cmn_hns_slcway_partition0_rnf_vec

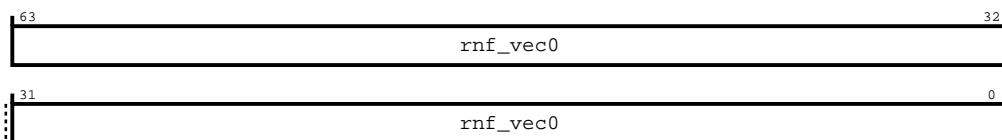


Table 4-341: cmn_hns_slcway_partition0_rnf_vec attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFF

4.3.10.45 cmn_hns_slcway_partition1_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC50

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-326: cmn_hns_slcway_partition1_rnf_vec

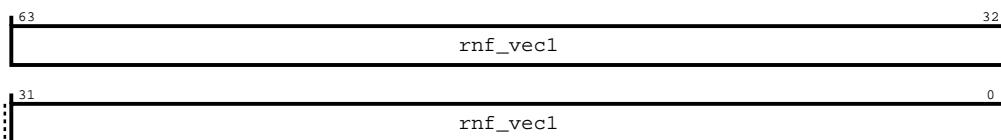


Table 4-342: cmn_hns_slcway_partition1_rnf_vec attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFF

4.3.10.46 cmn_hns_slcway_partition2_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC58

Type

RW

Reset value

See individual bit resets

Secure group override

cmm_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-327: cmm_hns_slcway_partition2_rnf_vec

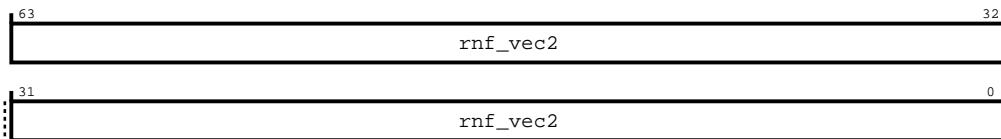


Table 4-343: cmm_hns_slcway_partition2_rnf_vec attributes

Bits	Name	Description	Type	Reset
[63:0]	<code>rnf_vec2</code>	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFF

4.3.10.47 cmm_hns_slcway_partition3_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC60

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slc_lock_ways`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-328: cmn_hns_slcway_partition3_rnf_vec

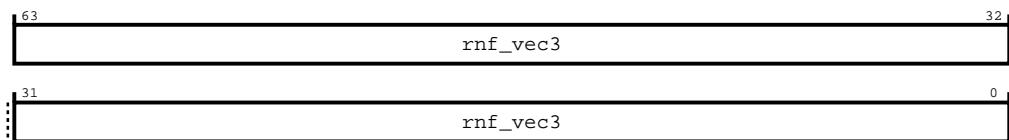


Table 4-344: cmn_hns_slcway_partition3_rnf_vec attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFF

4.3.10.48 cmn_hns_slcway_partition0_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCB0

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slc_lock_ways`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-329: cmn_hns_slcway_partition0_rnf_vec1

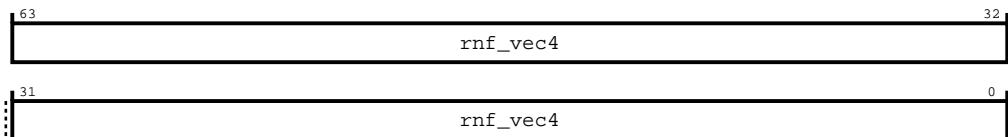


Table 4-345: cmn_hns_slcway_partition0_rnf_vec1 attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFF

4.3.10.49 cmn_hns_slcway_partition1_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7) for Logical RNF IDs 64 to 127.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCB8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-330: cmn_hns_slcway_partition1_rnf_vec1

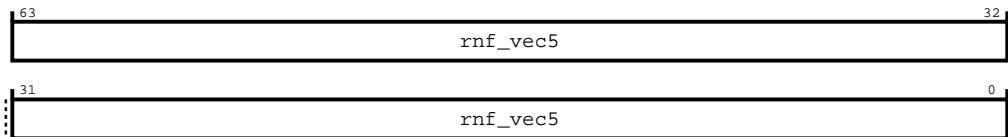


Table 4-346: cmn_hns_slcway_partition1_rnf_vec1 attributes

Bits	Name	Description	Type	Reset
[63:0]	<code>rnf_vec5</code>	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFF

4.3.10.50 cmn_hns_slcway_partition2_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11) for Logical RNF IDs 64 to 127.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCC0

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slc_lock_ways`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-331: cmn_hns_slcway_partition2_rnf_vec1

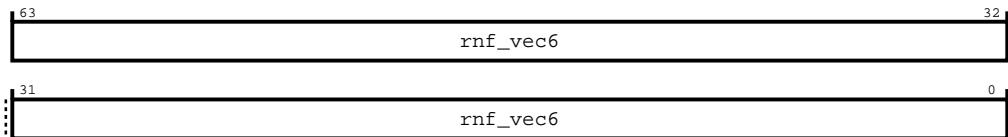


Table 4-347: cmn_hns_slcway_partition2_rnf_vec1 attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFF

4.3.10.51 cmn_hns_slcway_partition3_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15) for Logical RNF IDs 64 to 127.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCC8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-332: cmn_hns_slcway_partition3_rnf_vec1

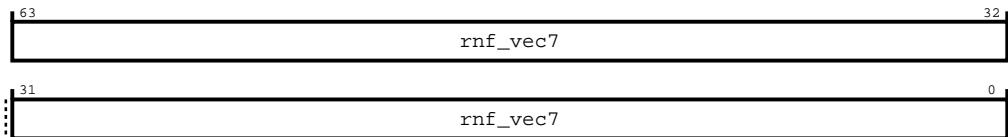


Table 4-348: cmn_hns_slcway_partition3_rnf_vec1 attributes

Bits	Name	Description	Type	Reset
[63:0]	rnf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFF

4.3.10.52 cmn_hns_slcway_partition0_rni_vec

Functions as the control register for RN-Is that can allocate to partition 0 (ways 0, 1, 2, and 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC68

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-333: cmn_hns_slcway_partition0_rni_vec

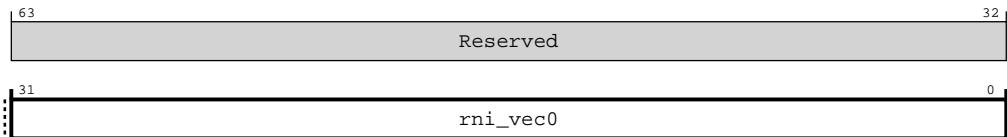


Table 4-349: cmn_hns_slcway_partition0_rni_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rni_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.53 cmn_hns_slcway_partition1_rni_vec

Functions as the control register for RN-Is that can allocate to partition 1 (ways 4, 5, 6, and 7).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC70

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-334: cmn_hns_slcway_partition1_rni_vec

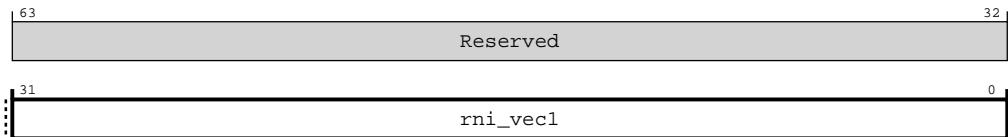


Table 4-350: cmn_hns_slcway_partition1_rni_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rni_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.54 cmn_hns_slcway_partition2_rni_vec

Functions as the control register for RN-Is that can allocate to partition 2 (ways 8, 9, 10, and 11).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC78

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-335: cmn_hns_slcway_partition2_rni_vec

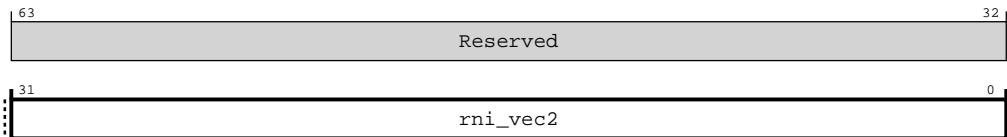


Table 4-351: cmn_hns_slcway_partition2_rni_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rni_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.55 cmn_hns_slcway_partition3_rni_vec

Functions as the control register for RN-Is that can allocate to partition 3 (ways 12, 13, 14, and 15).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC80

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-336: cmn_hns_slcway_partition3_rni_vec

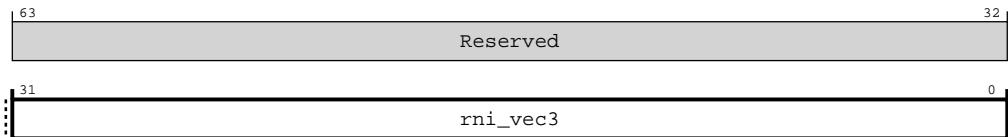


Table 4-352: cmn_hns_slcway_partition3_rni_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rni_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.56 cmn_hns_slcway_partition0_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 0 (ways 0, 1, 2, and 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC88

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-337: cmn_hns_slcway_partition0_rnd_vec

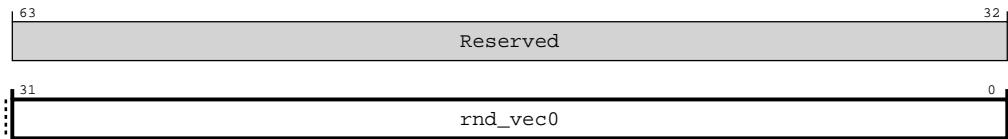


Table 4-353: cmn_hns_slcway_partition0_rnd_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rnd_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.57 cmn_hns_slcway_partition1_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 1 (ways 4, 5, 6, and 7).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC90

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-338: cmn_hns_slcway_partition1_rnd_vec

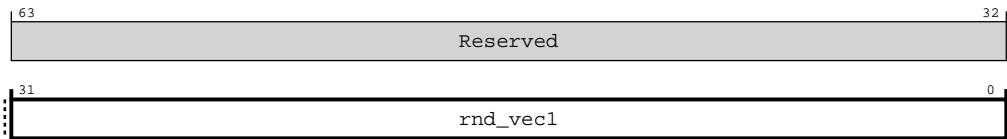


Table 4-354: cmn_hns_slcway_partition1_rnd_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rnd_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.58 cmn_hns_slcway_partition2_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 2 (ways 8, 9, 10, and 11).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC98

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-339: cmn_hns_slcway_partition2_rnd_vec

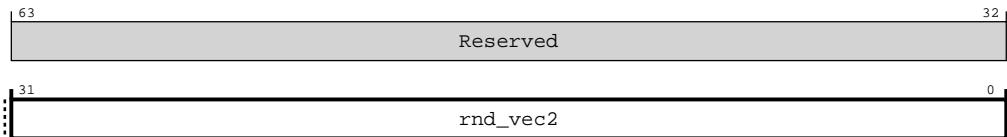


Table 4-355: cmn_hns_slcway_partition2_rnd_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rnd_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.59 cmn_hns_slcway_partition3_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 3 (ways 12, 13, 14, and 15).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCA0

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-340: cmn_hns_slcway_partition3_rnd_vec

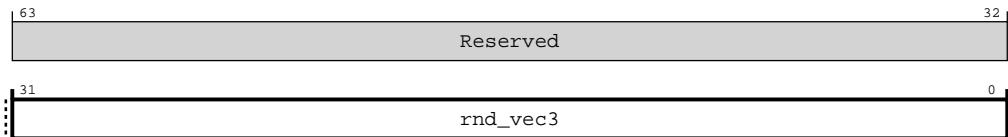


Table 4-356: cmn_hns_slcway_partition3_rnd_vec attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	rnd_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFF

4.3.10.60 cmn_hns_rn_region_lock

Functions as the enable register for source-based SLC way allocation.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCA8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slc_lock_ways

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-341: cmn_hns_rn_region_lock

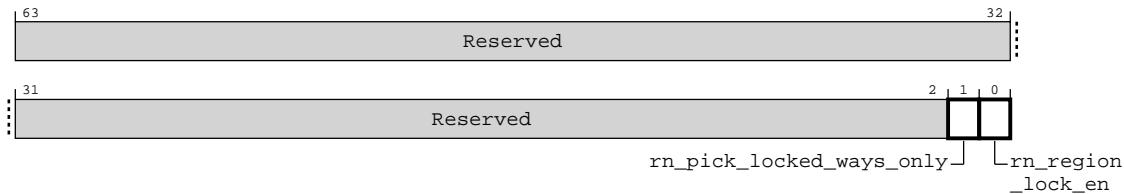


Table 4-357: cmn_hns_rn_region_lock attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	rn_pick_locked_ways_only	Specifies which ways the programmed RNs can allocate new cache lines to 1'b0 Programmed RN will choose all ways including locked 1'b1 Programmed RN will only allocate in locked ways	RW	1'b0
[0]	rn_region_lock_en	Enables SRC-based region locking 1'b0 SRC based way locking is disabled 1'b1 SRC based way locking is enabled	RW	1'b0

4.3.10.61 cmn_hns_sf_cxg_blocked_ways

Specifies the SF ways that are blocked for remote chip to use in CML mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCD0

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-342: cmn_hns_sf_cxg_blocked_ways

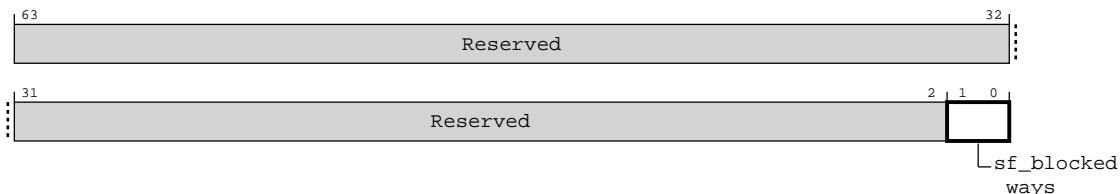


Table 4-358: cmn_hns_sf_cxg_blocked_ways attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	sf_blocked_ways	<p>Number of SF ways blocked from remote chips to be able to use in CML mode.</p> <p>2'b00 No ways are blocked; all SF ways could be used by local or remote RN-Fs</p> <p>2'b01 SF_NUM_WAYS = 16: ways 3:0 for local RN-Fs only; ways 15:4 for local and remote RN-Fs SF_NUM_WAYS > 16: ways 7:0 for local RN-Fs only; ways 31:8 for local and remote RN-Fs</p> <p>2'b10 SF_NUM_WAYS = 16: ways 7:0 for local RN-Fs only; ways 15:8 for local and remote RN-Fs SF_NUM_WAYS > 16: ways 15:0 for local RN-Fs only; ways 31:16 for local and remote RN-Fs</p> <p>2'b11 SF_NUM_WAYS < 26: ways 11:0 for local RN-Fs only; ways 15:12 for local and remote RN-Fs SF_NUM_WAYS >= 26: ways 23:0 for local RN-Fs only; ways 31:24 for local and remote RN-Fs</p>	RW	2'b00

4.3.10.62 cmn_hns_cxg_ha_metadata_exclusion_list

Functions as the control register to identify CXG HA which does not support metadata

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCE0

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-343: cmn_hns_cxg_ha_metadata_exclusion_list

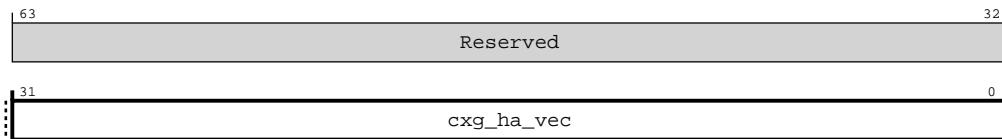


Table 4-359: cmn_hns_cxg_ha_metadata_exclusion_list attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	cxg_ha_vec	Bit vector mask; identifies which logical IDs of the CXG HA does not support metadata	RW	32'h00000000

4.3.10.63 cmn_hns_cxg_ha_smp_exclusion_list

Functions as the control register to identify CXG HA not connected to SMP CCIX link

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCD8

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-344: cmn_hns_cxg_ha_smp_exclusion_list

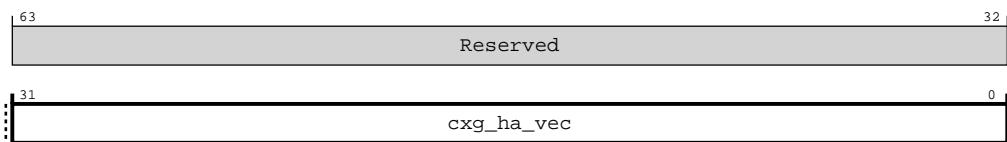


Table 4-360: cmn_hns_cxg_ha_smp_exclusion_list attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	<code>cxg_ha_vec</code>	Bit vector mask; identifies which logical IDs of the CXG HA does not connect to SMP CCIX link	RW	32'h00000000

4.3.10.64 hn_sam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hCF0`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-345: hn_sam_hash_addr_mask_reg

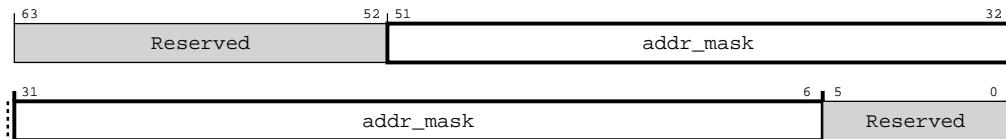


Table 4-361: hn_sam_hash_addr_mask_reg attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:6]	addr_mask	Address mask applied before hashing	RW	46'h3FFFFFFFFF
[5:0]	Reserved	Reserved	RO	-

4.3.10.65 hn_sam_region_cmp_addr_mask_reg

Configures the address mask that is applied before memory region compare.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCF8

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-346: hn_sam_region_cmp_addr_mask_reg

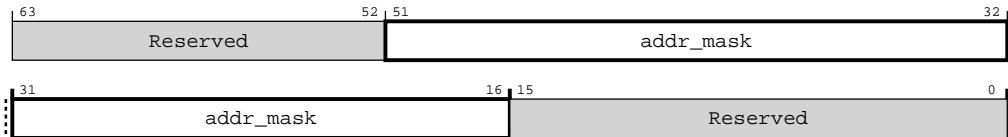


Table 4-362: hn_sam_region_cmp_addr_mask_reg attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	addr_mask	Address mask applied before memory region compare	RW	36'hFFFFFF
[15:0]	Reserved	Reserved	RO	-

4.3.10.66 cmn_hns_sam_cfg1_def_hashed_region

Configures default hashed region in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD48

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-347: cmn_hns_sam_cfg1_def_hashed_region

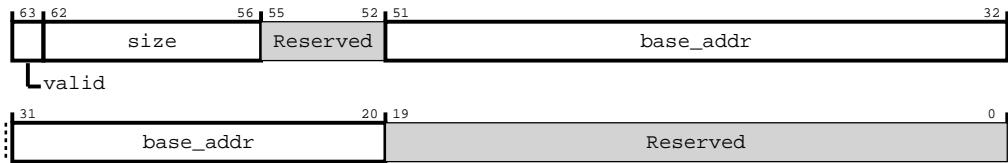


Table 4-363: cmn_hns_sam_cfg1_def_hashed_region attributes

Bits	Name	Description	Type	Reset
[63]	valid	Default hashed region valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'h1
[62:56]	size	Default hashed region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'h7F
[55:52]	Reserved	Reserved	RO	-
[51:20]	base_addr	Bits [51:20] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	32'h0
[19:0]	Reserved	Reserved	RO	-

4.3.10.67 cmn_hns_sam_cfg2_def_hashed_region

Configures default hashed region in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD50

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-348: cmn_hns_sam_cfg2_def_hashed_region

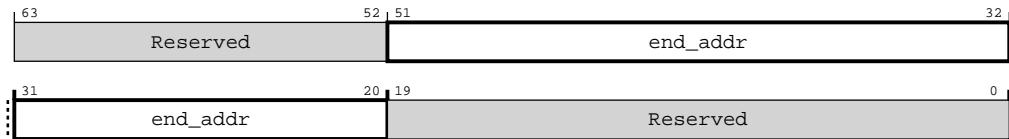


Table 4-364: cmn_hns_sam_cfg2_def_hashed_region attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:20]	end_addr	Bits [51:20] of end address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	32'hFFFFFF
[19:0]	Reserved	Reserved	RO	-

4.3.10.68 cmn_hns_sam_control

Configures HN-F SAM. All top_address_bit fields must be between bits 47 and 28 of the address. top_address_bit2 > top_address_bit1 > top_address_bit0. Must be configured to match corresponding por_rnsam_sys_cache_grp_sn_sam_cfgN register in the RN SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD00

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-349: cmn_hns_sam_control

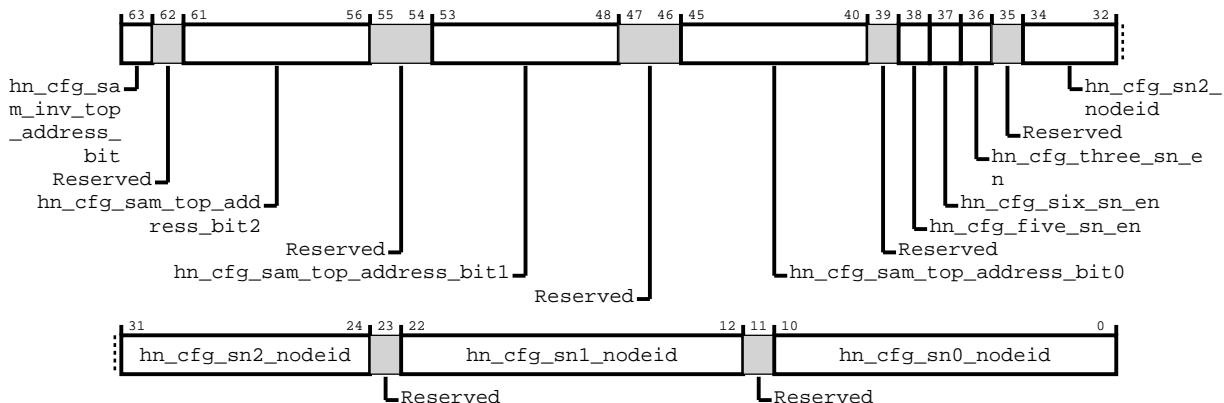


Table 4-365: cmn_hns_sam_control attributes

Bits	Name	Description	Type	Reset
[63]	hn_cfg_sam_inv_top_address_bit	Inverts the top address bit (hn_cfg_sam_top_address_bit1 if 3-SN, hn_cfg_sam_top_address_bit2 if 6-SN) NOTE: Can only be used when the address map does not have unique address bit combinations.	RW	1'h0
[62]	Reserved	Reserved	RO	-
[61:56]	hn_cfg_sam_top_address_bit2	Bit position of top_address_bit2; used for address hashing in 6-SN configuration	RW	6'h00
[55:54]	Reserved	Reserved	RO	-
[53:48]	hn_cfg_sam_top_address_bit1	Bit position of top_address_bit1; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
[47:46]	Reserved	Reserved	RO	-
[45:40]	hn_cfg_sam_top_address_bit0	Bit position of top_address_bit0; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
[39]	Reserved	Reserved	RO	-
[38]	hn_cfg_five_sn_en	Enables 5-SN configuration	RW	1'b0
[37]	hn_cfg_six_sn_en	Enables 6-SN configuration	RW	1'b0
[36]	hn_cfg_three_sn_en	Enables 3-SN configuration	RW	1'b0
[35]	Reserved	Reserved	RO	-
[34:24]	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0
[23]	Reserved	Reserved	RO	-
[22:12]	hn_cfg_sn1_nodeid	SN 1 node ID	RW	11'h0
[11]	Reserved	Reserved	RO	-
[10:0]	hn_cfg_sn0_nodeid	SN 0 node ID	RW	11'h0

4.3.10.69 cmn_hns_sam_control2

Configures HN-F SAM. Must be configured to match corresponding por_rnsam_sys_cache_grp_sn_sam_cfgN register in the RN SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD28

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-350: cmn_hns_sam_control2

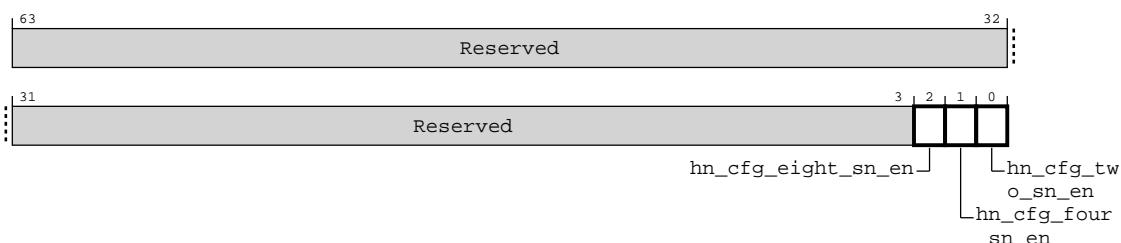


Table 4-366: cmn_hns_sam_control2 attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	hn_cfg_eight_sn_en	Enables 8-SN configuration	RW	1'b0
[1]	hn_cfg_four_sn_en	Enables 4-SN configuration	RW	1'b0
[0]	hn_cfg_two_sn_en	Enables 2-SN configuration	RW	1'b0

4.3.10.70 cmn_hns_sam_memregion0

Configures range-based memory region 0 in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD08

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-351: cmn_hns_sam_memregion0

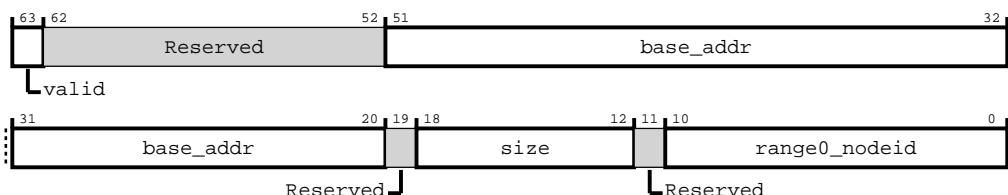


Table 4-367: cmn_hns_sam_memregion0 attributes

Bits	Name	Description	Type	Reset
[63]	valid	Memory region 0 valid 1'b0 Not valid 1'b1 valid for memory region comparison	RW	1'h0
[62:52]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[51:20]	base_addr	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	32'h0
[19]	Reserved	Reserved	RO	-
[18:12]	size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'h0
[11]	Reserved	Reserved	RO	-
[10:0]	range0_nodeid	Memory region 0 target node ID	RW	11'h0

4.3.10.71 cmn_hns_sam_memregion0_end_addr

Configures end address memory region 0 in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD38

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-352: cmn_hns_sam_memregion0_end_addr

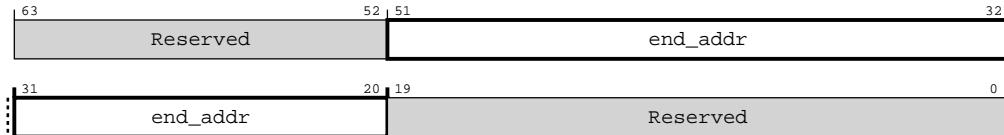


Table 4-368: cmn_hns_sam_memregion0_end_addr attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:20]	end_addr	End address of memory region 0	RW	32'h0
[19:0]	Reserved	Reserved	RO	-

4.3.10.72 cmn_hns_sam_memregion1

Configures range-based memory region 1 in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD10

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-353: cmn_hns_sam_memregion1

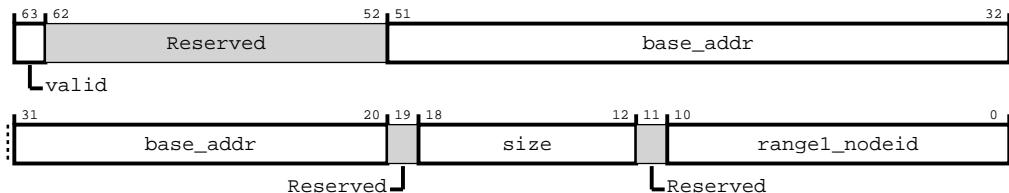


Table 4-369: cmn_hns_sam_memregion1 attributes

Bits	Name	Description	Type	Reset
[63]	valid	Memory region 1 valid 1'b0 Not valid 1'b1 valid for memory region comparison	RW	1'h0
[62:52]	Reserved	Reserved	RO	-
[51:20]	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	32'h0
[19]	Reserved	Reserved	RO	-
[18:12]	size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'h0
[11]	Reserved	Reserved	RO	-
[10:0]	range1_nodeid	Memory region 1 target node ID	RW	11'h0

4.3.10.73 cmn_hns_sam_memregion1_end_addr

Configures end address memory region 1 in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD40

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-354: cmn_hns_sam_memregion1_end_addr

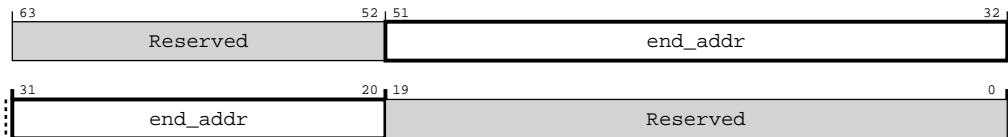


Table 4-370: cmn_hns_sam_memregion1_end_addr attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:20]	end_addr	End address of memory region 1	RW	32'h0
[19:0]	Reserved	Reserved	RO	-

4.3.10.74 cmn_hns_sam_sn_properties

Configures properties for all six SN targets and two range-based SN targets.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD18

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-355: cmn_hns_sam_sn_properties

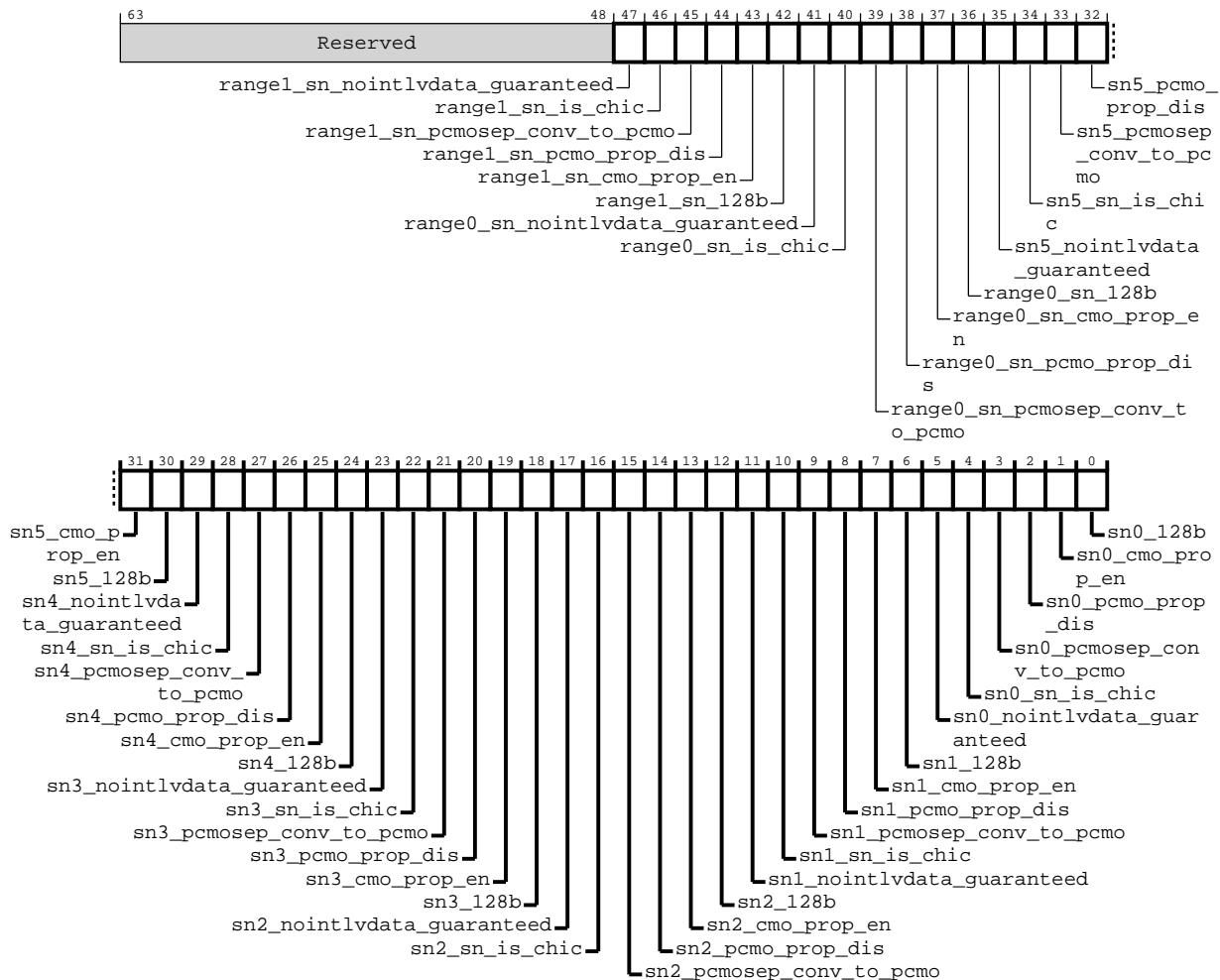


Table 4-371: cmn_hns_sam_sn_properties attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47]	range1_sn_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[46]	range1_sn_is_chic	Indicates that the range 1 SN is a CHI-C SN when set	RW	1'b0
[45]	range1_sn_pcמו_sep_conv_to_pcמו	Convert CleanSharedPersistSep to CleanSharedPersist for range 1 SN when set CONSTRAINT: Should not be enabled when sn_pcמו_prop_dis bit is set to 1	RW	1'b0
[44]	range1_sn_pcמו_prop_dis	Disables PCMO (persistent CMO) propagation for range 1 SN when set	RW	1'b0
[43]	range1_sn_cmo_prop_en	Enables CMO propagation for range 1 SN	RW	1'b0
[42]	range1_sn_128b	Data width of range 1 SN 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[41]	range0_sn_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0

Bits	Name	Description	Type	Reset
[40]	range0_sn_is_chic	Indicates that the range 0 SN is a CHI-C SN when set	RW	1'b0
[39]	range0_sn_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for range 0 SN when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[38]	range0_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 0 SN when set	RW	1'b0
[37]	range0_sn_cmo_prop_en	Enables CMO propagation for range 0 SN	RW	1'b0
[36]	range0_sn_128b	Data width of range 0 SN 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[35]	sn5_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[34]	sn5_sn_is_chic	Indicates that SN5 is a CHI-C SN when set	RW	1'b0
[33]	sn5_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 5 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[32]	sn5_pcmo_prop_dis	Disables PCMO propagation for SN 5 when set	RW	1'b0
[31]	sn5_cmo_prop_en	Enables CMO propagation for SN 5 when set	RW	1'b0
[30]	sn5_128b	Data width of SN 5 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[29]	sn4_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[28]	sn4_sn_is_chic	Indicates that SN4 is a CHI-C SN when set	RW	1'b0
[27]	sn4_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 4 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[26]	sn4_pcmo_prop_dis	Disables PCMO propagation for SN 4 when set	RW	1'b0
[25]	sn4_cmo_prop_en	Enables CMO propagation for SN 4 when set	RW	1'b0
[24]	sn4_128b	Data width of SN 4 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[23]	sn3_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[22]	sn3_sn_is_chic	Indicates that SN3 is a CHI-C SN when set	RW	1'b0
[21]	sn3_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 3 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[20]	sn3_pcmo_prop_dis	Disables PCMO propagation for SN 3 when set	RW	1'b0
[19]	sn3_cmo_prop_en	Enables CMO propagation for SN 3 when set	RW	1'b0
[18]	sn3_128b	Data width of SN 3 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[17]	sn2_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[16]	sn2_sn_is_chic	Indicates that SN2 is a CHI-C SN when set	RW	1'b0
[15]	sn2_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 2 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[14]	sn2_pcmo_prop_dis	Disables PCMO propagation for SN 2 when set	RW	1'b0

Bits	Name	Description	Type	Reset
[13]	sn2_cmo_prop_en	Enables CMO propagation for SN 2 when set	RW	1'b0
[12]	sn2_128b	Data width of SN 2 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[11]	sn1_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[10]	sn1_sn_is_chic	Indicates that SN1 is a CHI-C SN when set	RW	1'b0
[9]	sn1_pcmodsep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 1 when set CONSTRAINT: Should not be enabled when sn_pcmod_prop_dis bit is set to 1	RW	1'b0
[8]	sn1_pcmod_prop_dis	Disables PCMO propagation for SN 1 when set	RW	1'b0
[7]	sn1_cmo_prop_en	Enables CMO propagation for SN 1 when set	RW	1'b0
[6]	sn1_128b	Data width of SN 1 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[5]	sn0_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[4]	sn0_sn_is_chic	Indicates that SNO is a CHI-C SN when set	RW	1'b0
[3]	sn0_pcmodsep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 0 when set CONSTRAINT: Should not be enabled when sn_pcmod_prop_dis bit is set to 1	RW	1'b0
[2]	sn0_pcmod_prop_dis	Disables PCMO propagation for SN 0 when set	RW	1'b0
[1]	sn0_cmo_prop_en	Enables CMO propagation for SN 0 when set	RW	1'b0
[0]	sn0_128b	Data width of SN 0 1'b1 128 bits 1'b0 256 bits	RW	1'b0

4.3.10.75 cmn_hns_sam_6sn_nodeid

Configures node IDs for subordinate nodes 3 to 5 in 6-SN configuration mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hD20

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-356: cmn_hns_sam_6sn_nodeid

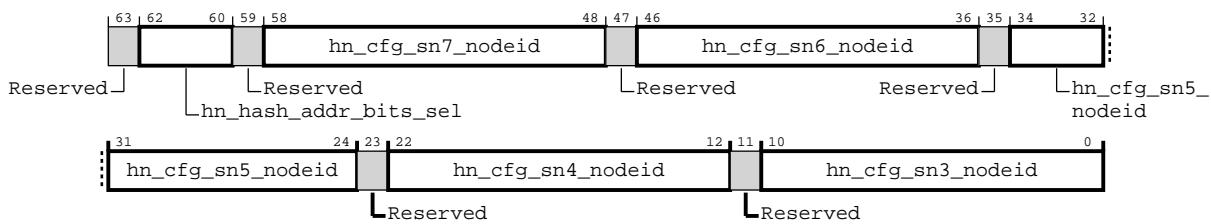


Table 4-372: cmn_hns_sam_6sn_nodeid attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:60]	hn_hash_addr_bits_sel	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[59]	Reserved	Reserved	RO	-
[58:48]	hn_cfg_sn7_nodeid	SN 7 node ID	RW	11'h0
[47]	Reserved	Reserved	RO	-
[46:36]	hn_cfg_sn6_nodeid	SN 6 node ID	RW	11'h0
[35]	Reserved	Reserved	RO	-
[34:24]	hn_cfg_sn5_nodeid	SN 5 node ID	RW	11'h0
[23]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[22:12]	hn_cfg_sn4_nodeid	SN 4 node ID	RW	11'h0
[11]	Reserved	Reserved	RO	-
[10:0]	hn_cfg_sn3_nodeid	SN 3 node ID	RW	11'h0

4.3.10.76 cmn_hns_sam_sn_properties1

Configures additional properties for all six SN targets and two range-based SN targets.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCE8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-357: cmn_hns_sam_sn_properties1

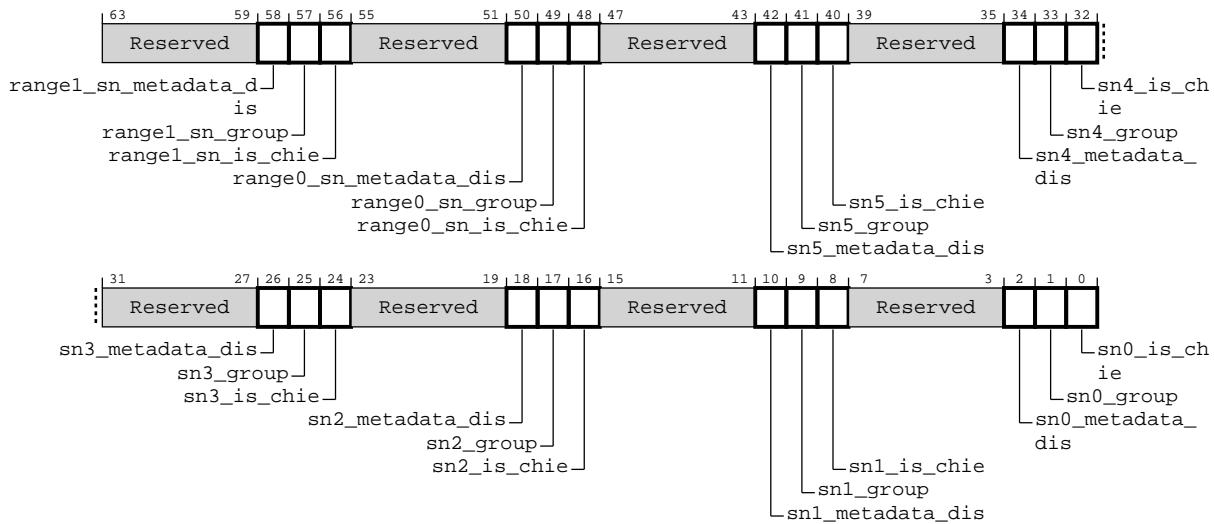


Table 4-373: cmn_hns_sam_sn_properties1 attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58]	<code>range1_sn_metadata_dis</code>	HNS implements metadata termination flow for Range 1 SN when set	RW	1'b0
[57]	<code>range1_sn_group</code>	Specifies the SN-F grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[56]	<code>range1_sn_is_chie</code>	Range 1 SN supports CHI-E	RW	1'b0
[55:51]	Reserved	Reserved	RO	-
[50]	<code>range0_sn_metadata_dis</code>	HNS implements metadata termination flow for Range 0 SN when set	RW	1'b0
[49]	<code>range0_sn_group</code>	Specifies the SN-F grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[48]	<code>range0_sn_is_chie</code>	Range 0 SN supports CHI-E	RW	1'b0
[47:43]	Reserved	Reserved	RO	-
[42]	<code>sn5_metadata_dis</code>	HNS implements metadata termination flow for SN 5 when set	RW	1'b0
[41]	<code>sn5_group</code>	Specifies the SN-F grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[40]	<code>sn5_is_chie</code>	SN 5 supports CHI-E	RW	1'b0
[39:35]	Reserved	Reserved	RO	-
[34]	<code>sn4_metadata_dis</code>	HNS implements metadata termination flow for SN 4 when set	RW	1'b0

Bits	Name	Description	Type	Reset
[33]	sn4_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[32]	sn4_is_chie	SN 4 supports CHI-E	RW	1'b0
[31:27]	Reserved	Reserved	RO	-
[26]	sn3_metadata_dis	HNS implements metadata termination flow for SN 3 when set	RW	1'b0
[25]	sn3_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[24]	sn3_is_chie	SN 3 supports CHI-E	RW	1'b0
[23:19]	Reserved	Reserved	RO	-
[18]	sn2_metadata_dis	HNS implements metadata termination flow for SN 2 when set	RW	1'b0
[17]	sn2_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[16]	sn2_is_chie	SN 2 supports CHI-E	RW	1'b0
[15:11]	Reserved	Reserved	RO	-
[10]	sn1_metadata_dis	HNS implements metadata termination flow for SN 1 when set	RW	1'b0
[9]	sn1_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[8]	sn1_is_chie	SN 1 supports CHI-E	RW	1'b0
[7:3]	Reserved	Reserved	RO	-
[2]	sn0_metadata_dis	HNS implements metadata termination flow for SN 0 when set	RW	1'b0
[1]	sn0_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[0]	sn0_is_chie	SN 0 supports CHI-E	RW	1'b0

4.3.10.77 cmn_hns_sam_sn_properties2

Configures properties for SN-7 & SN-8.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16 'hD30

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-358: cmn_hns_sam_sn_properties2

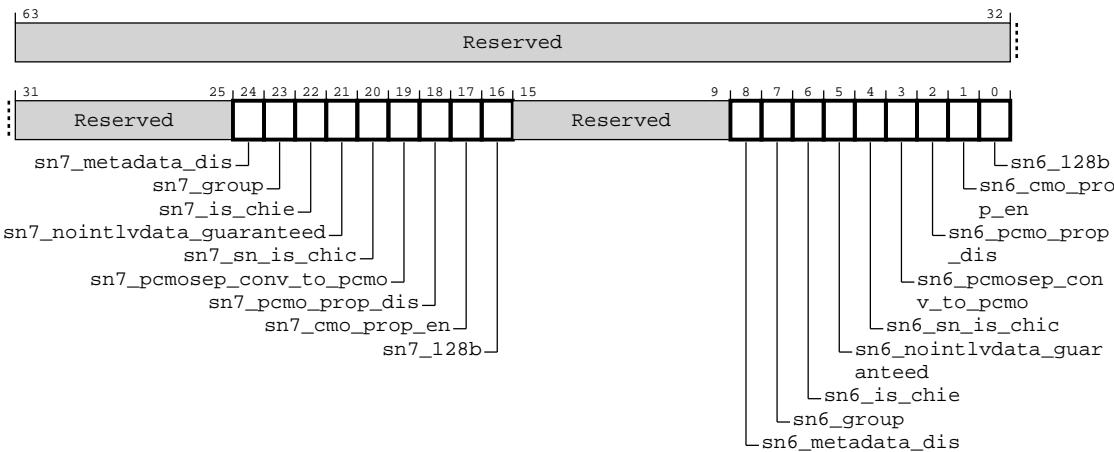


Table 4-374: cmn_hns_sam_sn_properties2 attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	sn7_metadata_dis	HNS implements metadata termination flow for SN 7 when set	RW	1'b0
[23]	sn7_group	Specifies the SN-F grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[22]	sn7_is_chie	SN 7 supports CHI-E	RW	1'b0
[21]	sn7_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[20]	sn7_sn_is_chic	Indicates that SN7 is a CHI-C SN when set	RW	1'b0
[19]	sn7_pcmovep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 7 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0

Bits	Name	Description	Type	Reset
[18]	sn7_pcmo_prop_dis	Disables PCMO propagation for SN 7 when set	RW	1'b0
[17]	sn7_cmo_prop_en	Enables CMO propagation for SN 7 when set	RW	1'b0
[16]	sn7_128b	Data width of SN 7 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[15:9]	Reserved	Reserved	RO	-
[8]	sn6_metadata_dis	HNS implements metadata termination flow for SN 6 when set	RW	1'b0
[7]	sn6_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[6]	sn6_is_chie	SN 6 supports CHI-E	RW	1'b0
[5]	sn6_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[4]	sn6_sn_is_chic	Indicates that SN6 is a CHI-C SN when set	RW	1'b0
[3]	sn6_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 6 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[2]	sn6_pcmo_prop_dis	Disables PCMO propagation for SN 6 when set	RW	1'b0
[1]	sn6_cmo_prop_en	Enables CMO propagation for SN 6 when set	RW	1'b0
[0]	sn6_128b	Data width of SN 6 1'b1 128 bits 1'b0 256 bits	RW	1'b0

4.3.10.78 cmn_hns_cml_port_aggr_grp0-4_add_mask

There are 5 iterations of this register. The index ranges from 0 to 4. Configures the CCIX port aggregation address mask for group 0.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-4) : 16'hF80 + #{8 * index}
index(5-31) : 16'h6000 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-359: cmn_hns_cml_port_aggr_grp0-4_add_mask

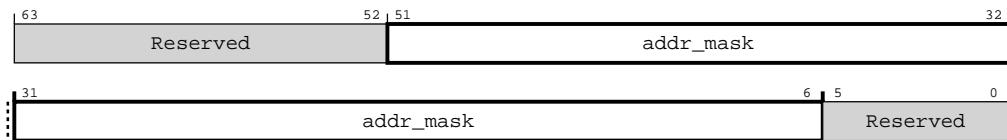


Table 4-375: cmn_hns_cml_port_aggr_grp0-4_add_mask attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:6]	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFF
[5:0]	Reserved	Reserved	RO	-

4.3.10.79 cmn_hns_cml_port_aggr_grp5-31_add_mask

There are 27 iterations of this register. The index ranges from 5 to 31. Configures the CCIX port aggregation address mask for group 0.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-4) : 16'hF80 + #{8 * index}
index(5-31) : 16'h6000 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-360: cmn_hns_cml_port_aggr_grp5-31_add_mask



Table 4-376: cmn_hns_cml_port_aggr_grp5-31_add_mask attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:6]	<code>addr_mask#{index}</code>	Address mask to be applied before hashing	RW	46'h3FFFFFFFFF
[5:0]	Reserved	Reserved	RO	-

4.3.10.80 cmn_hns_cml_port_aggr_grp_reg0-12

There are 13 iterations of this register. The index ranges from 0 to 12. Configures the CCIX port aggregation port Node IDs.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-1) : 16'hFB0 + #{8 * index}
index(2-12) : 16'h6100 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-361: cmn_hns_cml_port_aggr_grp_reg0-12

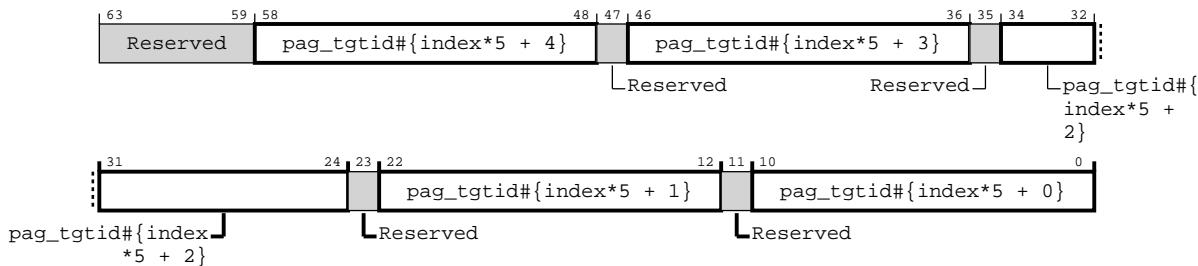


Table 4-377: cmn_hns_cml_port_aggr_grp_reg0-12 attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:48]	pag_tgtid#{index*5 + 4}	Specifies the target ID #{index*5 + 4} for CPAG	RW	11'b0
[47]	Reserved	Reserved	RO	-
[46:36]	pag_tgtid#{index*5 + 3}	Specifies the target ID #{index*5 + 3} for CPAG	RW	11'b0
[35]	Reserved	Reserved	RO	-
[34:24]	pag_tgtid#{index*5 + 2}	Specifies the target ID {index*5 + 2} for CPAG	RW	11'b0
[23]	Reserved	Reserved	RO	-
[22:12]	pag_tgtid#{index*5 + 1}	Specifies the target ID {index*5 + 1} for CPAG	RW	11'b0
[11]	Reserved	Reserved	RO	-
[10:0]	pag_tgtid#{index*5 + 0}	Specifies the target ID {index*5 + 0} for CPAG	RW	11'b0

4.3.10.81 cmn_hns_cml_port_aggr_ctrl_reg

Configures the CCI-X port aggregation port groups

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16 'hFD0

Type

RW

Reset value

See individual bit resets

Secure group override

`cnn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-362: `cnn_hns_cml_port_aggr_ctrl_reg`



Table 4-378: `cnn_hns_cml_port_aggr_ctrl_reg` attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51]	cpag_valid4	Valid programming for CPAG4, Enabled by default (backward compatible)	RW	1'b1
[50:48]	num_cxg_pag4	Specifies the number of CXRAs in CPAG4 Constraint: May use pag_tgtid8 through pag_tgtid9 of <code>cnn_hns_cml_port_aggr_grp_reg1</code> when <code>POR_RNSAM_FLEX_TGTID_EN_PARAM = 0</code>	RW	3'b000
		3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved		
[47:40]	Reserved	Reserved	RO	-
[39]	cpag_valid3	Valid programming for CPAG + 3}, Enabled by default (backward compatible)	RW	1'b1

Bits	Name	Description	Type	Reset
[38:36]	num_cxg_pag3	Specifies the number of CXRAs in CPAG3 Constraint: May use pag_tgtid6 through pag_tgtid7 of cmn_hns_cml_port_aggr_grp_reg1 when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[35:28]	Reserved	Reserved	RO	-
[27]	cpag_valid2	Valid programming for CPAG + 2}, Enabled by default (backward compatible)	RW	1'b1
[26:24]	num_cxg_pag2	Specifies the number of CXRAs in CPAG2 Constraint: May use pag_tgtid4 through pag_tgtid7 of cmn_hns_cml_port_aggr_grp_reg[0,1] when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[23:16]	Reserved	Reserved	RO	-
[15]	cpag_valid1	Valid programming for CPAG + 1}, Enabled by default (backward compatible)	RW	1'b1
[14:12]	num_cxg_pag1	Specifies the number of CXRAs in CPAG1 Constraint: May use pag_tgtid2 through pag_tgtid3 of cmn_hns_cml_port_aggr_grp_reg0 when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[11:4]	Reserved	Reserved	RO	-
[3]	cpag_valid0	Valid programming for CPAG, Enabled by default (backward compatible)	RW	1'b1
[2:0]	num_cxg_pag0	Specifies the number of CXRAs in CPAGO Constraint: May use pag_tgtid0 through pag_tgtid7 of cmn_hns_cml_port_aggr_grp_reg[0,1] when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000

4.3.10.82 cmn_hns_cml_port_aggr_ctrl_reg1-6

There are 6 iterations of this register. The index ranges from 1 to 6. Configures the CCIX port aggregation port groups

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(1-6) : 16'h6200 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-363: cmn_hns_cml_port_aggr_ctrl_reg1-6

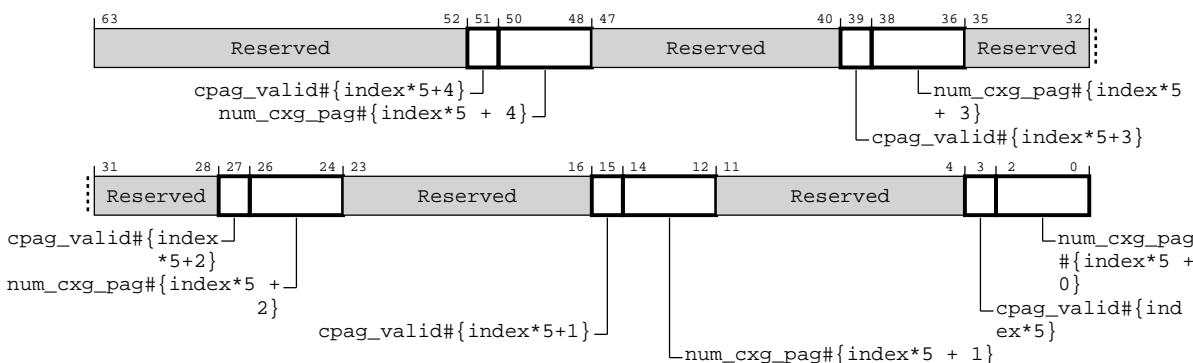


Table 4-379: cmn_hns_cml_port_aggr_ctrl_reg1-6 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[51]	cpag_valid#{index*5+4}	Valid programming for CPAG #{index*5 + 4}, Enabled by default (backward compatible)	RW	1'b1
[50:48]	num_cxg_pag#{index*5 + 4}	Specifies the number of CXRAs in CPAG4#{index*5 + 4} Constraint: May use pag_tgtid8 through pag_tgtid9 of cmn_hns_cml_port_aggr_grp_reg1 when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[47:40]	Reserved	Reserved	RO	-
[39]	cpag_valid#{index*5+3}	Valid programming for CPAG #{index*5 + 3}, Enabled by default (backward compatible)	RW	1'b1
[38:36]	num_cxg_pag#{index*5 + 3}	Specifies the number of CXRAs in CPAG3#{index*5 + 3} Constraint: May use pag_tgtid6 through pag_tgtid7 of cmn_hns_cml_port_aggr_grp_reg1 when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[35:28]	Reserved	Reserved	RO	-
[27]	cpag_valid#{index*5+2}	Valid programming for CPAG #{index*5 + 2}, Enabled by default (backward compatible)	RW	1'b1
[26:24]	num_cxg_pag#{index*5 + 2}	Specifies the number of CXRAs in CPAG2#{index*5 + 2} Constraint: May use pag_tgtid4 through pag_tgtid7 of cmn_hns_cml_port_aggr_grp_reg[0,1] when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[23:16]	Reserved	Reserved	RO	-
[15]	cpag_valid#{index*5+1}	Valid programming for CPAG #{index*5 + 1}, Enabled by default (backward compatible)	RW	1'b1

Bits	Name	Description	Type	Reset
[14:12]	num_cxg_pag#{index*5 + 1}	Specifies the number of CXRAs in CPAG1#{index*5 + 1} Constraint: May use pag_tgtid2 through pag_tgtid3 of cmn_hns_cml_port_aggr_grp_reg0 when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000
[11:4]	Reserved	Reserved	RO	-
[3]	cpag_valid#{index*5}	Valid programming for CPAG #{index*5}, Enabled by default (backward compatible)	RW	1'b1
[2:0]	num_cxg_pag#{index*5 + 0}	Specifies the number of CXRAs in CPAG#{index*5 + 0} Constraint: May use pag_tgtid0 through pag_tgtid7 of cmn_hns_cml_port_aggr_grp_reg[0,1] when POR_RNSAM_FLEX_TGTID_EN_PARAM = 0 3'b000 1 port used 3'b001 2 ports used 3'b010 4 ports used 3'b011 8 ports used 3'b100 16 ports used 3'b101 32 ports used 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b000

4.3.10.83 cmn_hns_abf_lo_addr

Lower address range for Address Based Flush (ABF) [51:0].

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF50

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ppu

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-364: cmn_hns_abf_lo_addr

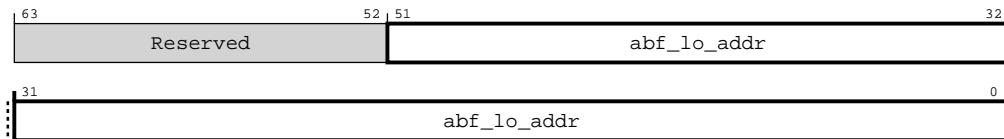


Table 4-380: cmn_hns_abf_lo_addr attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:0]	abf_lo_addr	Lower address range for ABF	RW	52'b0

4.3.10.84 cmn_hns_abf_hi_addr

Upper address range for Address Based Flush (ABF) [51:0].

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF58

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ppu

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-365: cmn_hns_abf_hi_addr

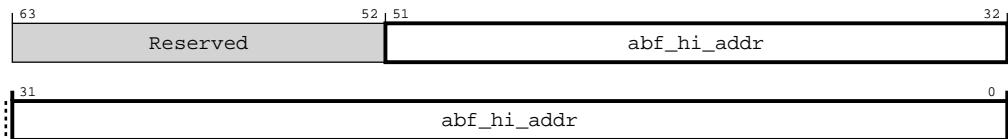


Table 4-381: cmn_hns_abf_hi_addr attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:0]	abf_hi_addr	Upper address range for ABF	RW	52'b0

4.3.10.85 cmn_hns_abf_pr

Functions as the Address Based Flush (ABF) policy register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF60

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.ppu

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-366: cmn_hns_abf_pr

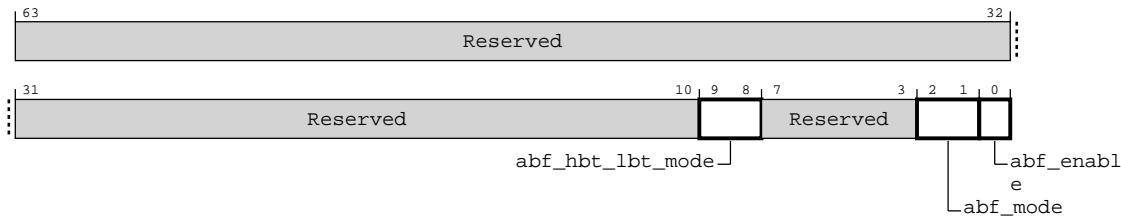


Table 4-382: cmn_hns_abf_pr attributes

Bits	Name	Description	Type	Reset
[63:10]	Reserved	Reserved	RO	-
[9:8]	abf_hbt_lbt_mode	ABF HBT/LBT Flush mode 2'b00 All addresses in ABF range (HBT and LBT) flushed 2'b01 All HBT addresses in ABF range flushed 2'b10 All LBT addresses in ABF range flushed 2'b11 Reserved	RW	2'b00
[7:3]	Reserved	Reserved	RO	-
[2:1]	abf_mode	ABF mode 2'b00 Clean Invalidate; WB dirty data and invalidate local copy 2'b01 Make Invalidate; invalidate without writing back dirty data 2'b10 Clean Shared; WB dirty data and can keep clean copy 2'b11 Reserved	RW	2'b00
[0]	abf_enable	Start Address Based Flushing based on high and low address ranges	RW	1'b0

4.3.10.86 cmn_hns_abf_sr

Functions as the Address Based Flush (ABF) status register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hF68

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-367: cmn_hns_abf_sr

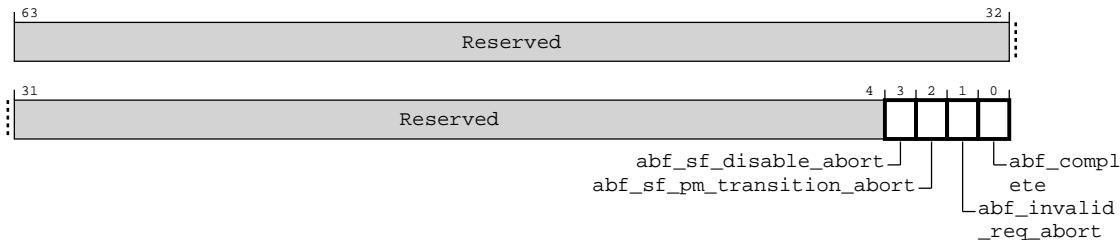


Table 4-383: cmn_hns_abf_sr attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	abf_sf_disable_abort	ABF aborted due to SF not being enabled, either by configuration or double-bit ECC error	RO	1'b0
[2]	abf_sf_pm_transition_abort	ABF aborted due to PM transition while ABF in progress, or both PM and ABF requested at the same time	RO	1'b0
[1]	abf_invalid_req_abort	ABF request made while PM is not in FAM/HAM/SF_ONLY mode; request aborted in this case	RO	1'b0
[0]	abf_complete	ABF completed	RO	1'b0

4.3.10.87 cmn_hns_cbusy_write_limit_ctl

Cbusy threshold limits for POCQ write entries. CONSTRAINT: The hns_adv_cbusy_mode_en must be 1'b1 to use this feature.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1000

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-368: cmn_hns_cbusy_write_limit_ctl

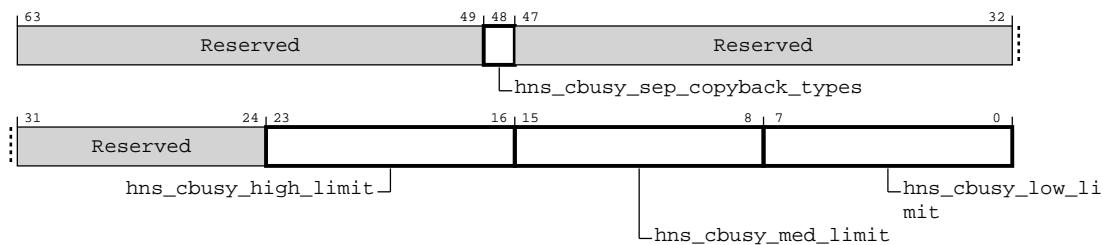


Table 4-384: cmn_hns_cbusy_write_limit_ctl attributes

Bits	Name	Description	Type	Reset
[63:49]	Reserved	Reserved	RO	-
[48]	hns_cbusy_sep_copyback_types	Enables copyback and non-copyback write type separation in cbusy calculation	RW	1'b0
[47:24]	Reserved	Reserved	RO	-
[23:16]	hns_cbusy_high_limit	POCQ limit for Write CBusy High	RW	Configuration dependent
[15:8]	hns_cbusy_med_limit	POCQ limit for Write CBusy Med	RW	Configuration dependent
[7:0]	hns_cbusy_low_limit	POCQ limit for Write CBusy Low	RW	Configuration dependent

4.3.10.88 cmn_hns_cbusy_resp_ctl

Controls the responses sent from HNS to RNF. CONSTRAINT: The `hns_adv_cbusy_mode_en` must be `1'b1` to use this feature.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1008

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-369: cmn_hns_cbusy_resp_ctl

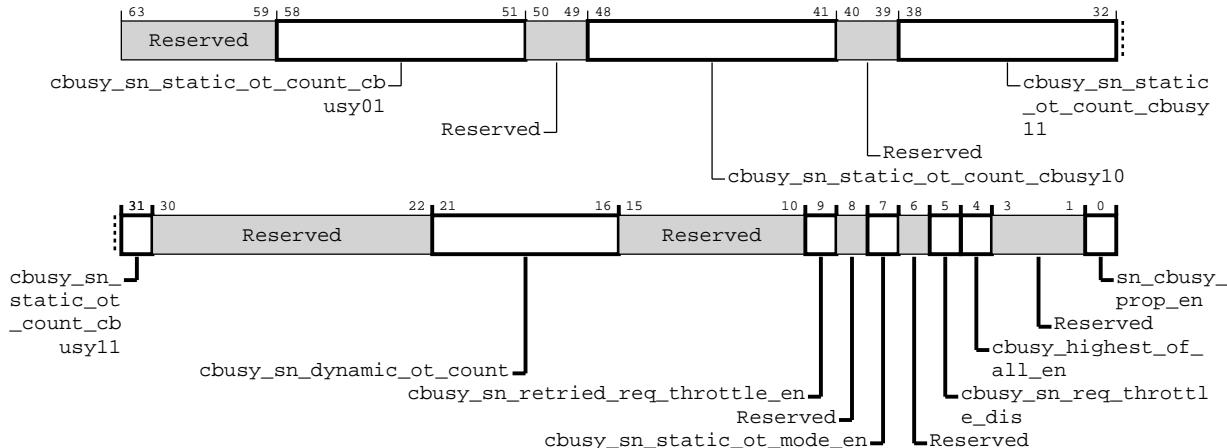


Table 4-385: cmn_hns_cbusy_resp_ctl attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:51]	cbusy_sn_static_ot_count_cbusy01	Specifies the maximum number of transactions to SN-F when SN Cbusy=01 in static throttling mode. CONSTRAINT: Value must be less than HNS_NUM_ENTRIES_POCQ_PARAM-1	RW	Configuration dependent
[50:49]	Reserved	Reserved	RO	-
[48:41]	cbusy_sn_static_ot_count_cbusy10	Specifies the maximum number of transactions to SN-F when SN Cbusy=10 in static throttling mode. CONSTRAINT: Value must be less than HNS_NUM_ENTRIES_POCQ_PARAM-1 and less than cbusy_sn_static_ot_count_cbusy01	RW	Configuration dependent
[40:39]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[38:31]	cbusy_sn_static_ot_count_cbusy11	Specifies the maximum number of transactions to SN-F when SN Cbusy=11 in static throttling mode. CONSTRAINT: Value must be less than HNS_NUM_ENTRIES_POCQ_PARAM-1 and less than cbusy_sn_static_ot_count_cbusy10	RW	Configuration dependent
[30:22]	Reserved	Reserved	RO	-
[21:16]	cbusy_sn_dynamic_ot_count	Specifies the granularity at which HN-F will dynamically throttle transactions to SN-F. CONSTRAINT: 1,2,4,8 are the allowed values	RW	6'b000100
[15:10]	Reserved	Reserved	RO	-
[9]	cbusy_sn_retried_req_throttle_en	Enables throttling retried requests with static grants (from SN) along with dynamic credit requests	RW	1'b0
[8]	Reserved	Reserved	RO	-
[7]	cbusy_sn_static_ot_mode_en	<p>Controls cbusy between HN-F and SN-F</p> <p>1'b0 HN-F will dynamically throttle outstanding requests to SN-F</p> <p>1'b1 HN-F will use fixed transactions count at each CBusy level at 1/4th POCQ granularity</p> <p>CONSTRAINT: For SN request throttling, CBusy aggregation is always based on SN_CBusy[1:0] and cbusy_alt_mode_en is inapplicable</p>	RW	1'b0
[6]	Reserved	Reserved	RO	-
[5]	cbusy_sn_req_throttle_dis	Disables Cbusy based request throttling from HNS to SNF when set to 1'b1	RW	1'b0
[4]	cbusy_highest_of_all_en	<p>Controls cbusy between HN-F and SN-F</p> <p>1'b0 Will send the HN-F or SN-F as configured</p> <p>1'b1 Will select highest CBusy value between the SN-F and HN-F</p>	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	sn_cbusy_prop_en	<p>Controls HN-F and SN-F cbusy on responses to RN-F</p> <p>1'b0 HN-F's POCQ Cbusy is sent</p> <p>1'b1 SN-F's Cbusy is sent</p>	RW	1'b0

4.3.10.89 cmn_hns_cbusy_sn_ctl

Controls the SN-F cbusy thresholds. CONSTRAINT: The hns_adv_cbusy_mode_en must be 1'b1 to use this feature.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1010

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-370: cmn_hns_cbusy_sn_ctl

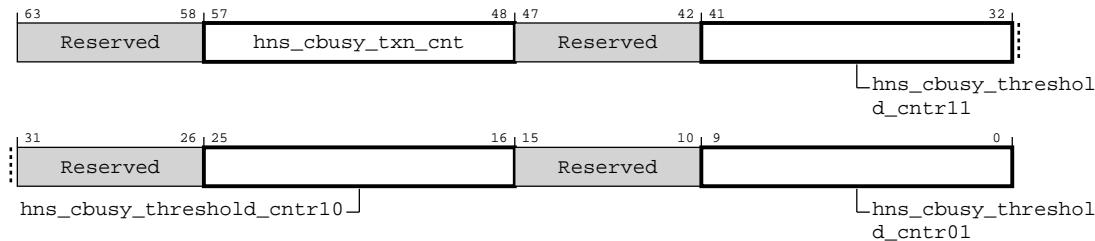


Table 4-386: cmn_hns_cbusy_sn_ctl attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:48]	hns_cbusy_txn_cnt	Number of transactions over which the counters are tracked	RW	10'b0100000000
[47:42]	Reserved	Reserved	RO	-
[41:32]	hns_cbusy_threshold_cntr11	CBusy threshold at which SN-F is considered busy for Counter_11	RW	10'b0000010000
[31:26]	Reserved	Reserved	RO	-
[25:16]	hns_cbusy_threshold_cntr10	CBusy threshold at which SN-F is considered busy for Counter_10	RW	10'b0000100000
[15:10]	Reserved	Reserved	RO	-
[9:0]	hns_cbusy_threshold_cntr01	CBusy threshold at which SN-F is considered busy for Counter_01	RW	10'b0001000000

4.3.10.90 cmn_hns_lbt_cbusy_ctl

Controls the CBusy response for LCN Bound Transactions. CONSTRAINT: The hns_adv_cbusy_mode_en must be 1'b1 to use this feature.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1018

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-371: cmn_hns_lbt_cbusy_ctl

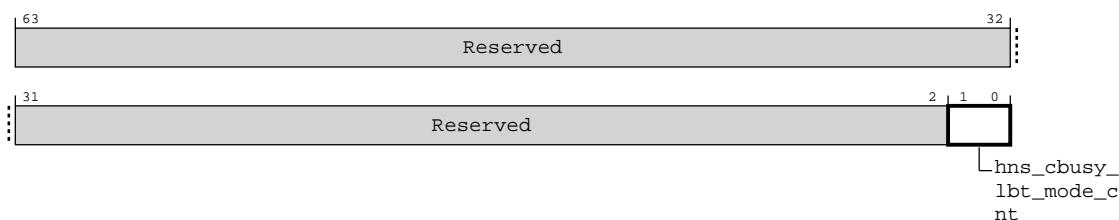


Table 4-387: cmn_hns_lbt_cbusy_ctl attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	hns_cbusy_lbt_mode_cnt	<p>Controls the propagation of Cbusy field for LCN bound transactions.</p> <p>2'b00 Send HNS POCQ Cbusy on all responses based on the limits programmed in cmn_hns_cbusy_limit_ctl</p> <p>2'b01 Pass through HNF CBusy on late completion responses (CompData, Comp)</p> <p>2'b10 Greater of POCQ Cbusy or HNF Cbusy. Applicable to responses where remote Cbusy can be sent</p>	RW	2'b00

4.3.10.91 cmn_hns_pocq_alloc_class_dedicated

Controls Dedicated entries in POCQ for each class.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1020

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-372: cmn_hns_pocq_alloc_class_dedicated

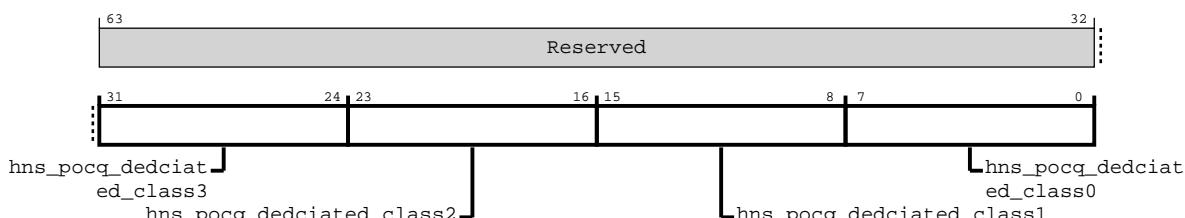


Table 4-388: cmn_hns_pocq_alloc_class_dedicated attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:24]	hns_pocq_dedciated_class3	Dedicated number of entries for Class 3 in POCQ CONSTRAINT: Sum of dedicated entries for classes & SEQ can not exceed HNS_NUM_ENTRIES_POCQ_PARAM. CONSTRAINT: hns_pocq_dedciated_class3 < hns_pocq_max_allowed_class3	RW	8'b00000000

Bits	Name	Description	Type	Reset
[23:16]	hns_pocq_dedicated_class2	Dedicated number of entries for Class 2 in POCQ CONSTRAINT: Sum of dedicated entries for classes & SEQ can not exceed HNS_NUM_ENTRIES_POCQ_PARAM. CONSTRAINT: hns_pocq_dedicated_class2 < hns_pocq_max_allowed_class2	RW	8'b000000000
[15:8]	hns_pocq_dedicated_class1	Dedicated number of entries for Class 1 in POCQ CONSTRAINT: Sum of dedicated entries for classes & SEQ can not exceed HNS_NUM_ENTRIES_POCQ_PARAM. CONSTRAINT: hns_pocq_dedicated_class1 < hns_pocq_max_allowed_class1	RW	8'b000000000
[7:0]	hns_pocq_dedicated_class0	Dedicated number of entries for Class 0 in POCQ CONSTRAINT: Sum of dedicated entries for classes & SEQ can not exceed HNS_NUM_ENTRIES_POCQ_PARAM. CONSTRAINT: hns_pocq_dedicated_class0 < hns_pocq_max_allowed_class0	RW	8'b000000000

4.3.10.92 cmn_hns_pocq_alloc_class_max_allowed

Controls Maximum allowed entries in POCQ for each class.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1028

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-373: cmn_hns_pocq_alloc_class_max_allowed

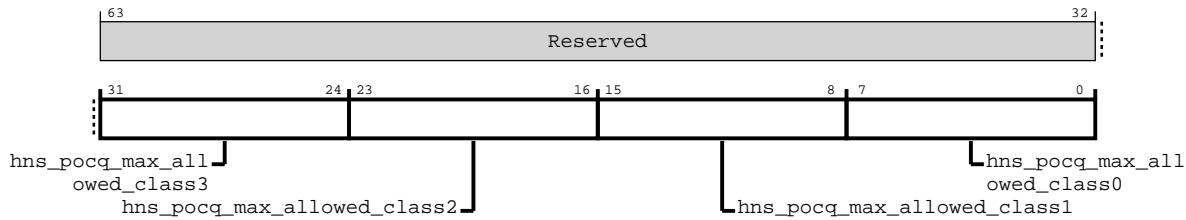


Table 4-389: cmn_hns_pocq_alloc_class_max_allowed attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:24]	hns_pocq_max_allowed_class3	Maximum number of entries for Class 3 in POCQ CONSTRAINT: hns_pocq_dedicated_class3 < hns_pocq_max_allowed_class3	RW	Configuration dependent
[23:16]	hns_pocq_max_allowed_class2	Maximum number of entries for Class 2 in POCQ CONSTRAINT: hns_pocq_dedicated_class2 < hns_pocq_max_allowed_class2	RW	Configuration dependent
[15:8]	hns_pocq_max_allowed_class1	Maximum number of entries for Class 1 in POCQ CONSTRAINT: hns_pocq_dedicated_class1 < hns_pocq_max_allowed_class1	RW	Configuration dependent
[7:0]	hns_pocq_max_allowed_class0	Maximum number of entries for Class 0 in POCQ CONSTRAINT: hns_pocq_dedicated_class0 < hns_pocq_max_allowed_class0	RW	Configuration dependent

4.3.10.93 cmn_hns_pocq_alloc_class_contented_min

Controls Contended minimum entries in POCQ for each class.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1030

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-374: cmn_hns_pocq_alloc_class_contented_min

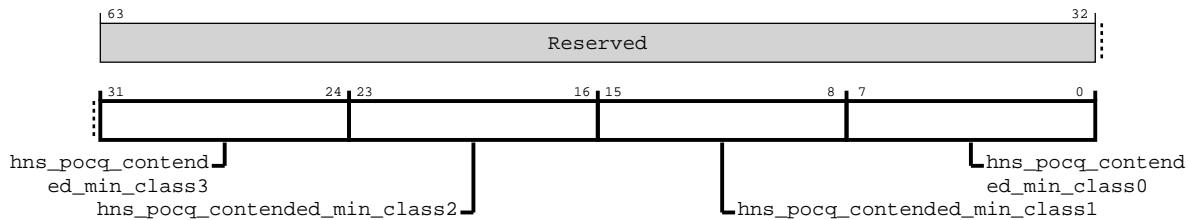


Table 4-390: cmn_hns_pocq_alloc_class_contented_min attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:24]	hns_pocq_contented_min_class3	Contended min entries for Class 3 in POCQ	RW	Configuration dependent
[23:16]	hns_pocq_contented_min_class2	Contended min entries for Class 2 in POCQ	RW	Configuration dependent
[15:8]	hns_pocq_contented_min_class1	Contended min entries for Class 1 in POCQ	RW	Configuration dependent
[7:0]	hns_pocq_contented_min_class0	Contended min entries for Class 0 in POCQ	RW	Configuration dependent

4.3.10.94 cmn_hns_pocq_alloc_misc_max_allowed

Controls Maximum allowed entries in POCQ for SNP, SEQ, and other misc req.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1038

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-375: cmn_hns_pocq_alloc_misc_max_allowed

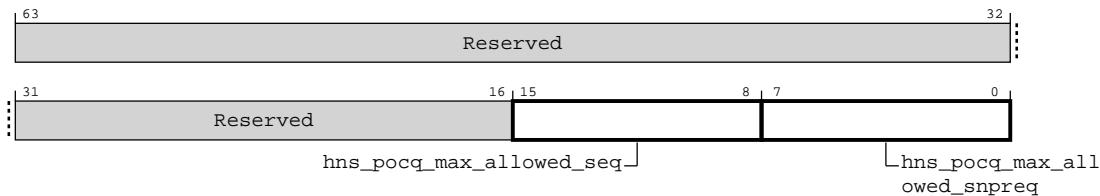


Table 4-391: cmn_hns_pocq_alloc_misc_max_allowed attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:8]	hns_pocq_max_allowed_seq	Maximum number of entries for SEQ in POCQ. Constraint: Only values of 1 or 2 supported.	RW	8'h02
[7:0]	hns_pocq_max_allowed_snreq	Maximum number of entries for RXSNP requests in POCQ	RW	8'h04

4.3.10.95 cmn_hns_class_ctl

Class misc controls.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1040

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-376: cmn_hns_class_ctl

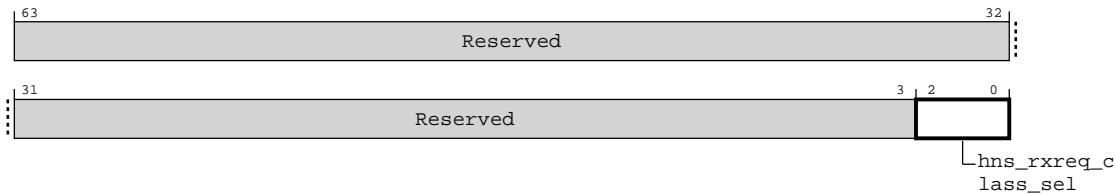


Table 4-392: cmn_hns_class_ctl attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2:0]	hns_rxreq_class_sel	RxReq Class select: 3'b000 QoS based class selection 3'b001 Request Opcode based class selection If un-supported value is programmed, default selection of QoS based is chosen.	RW	3'b000

4.3.10.96 cmn_hns_pocq_qos_class_ctl

QoS bases class identification controls.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1048

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-377: cmn_hns_pocq_qos_class_ctl

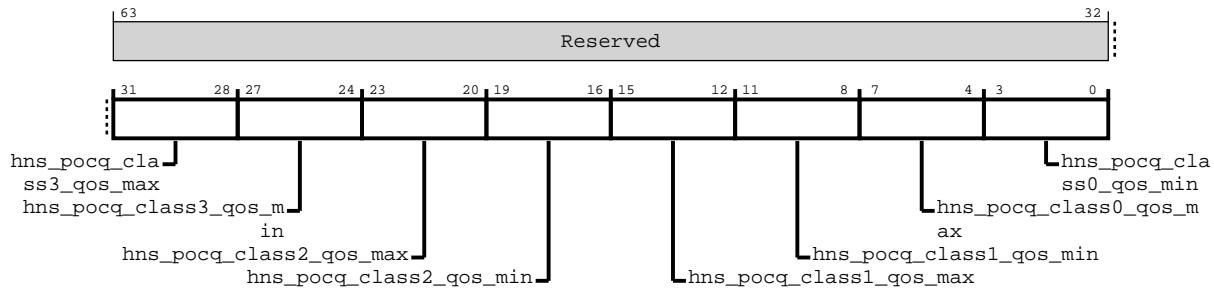


Table 4-393: cmn_hns_pocq_qos_class_ctl attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	hns_pocq_class3_qos_max	QoS maximum value for Class 3	RW	4'b0111
[27:24]	hns_pocq_class3_qos_min	QoS minimum value for Class 3	RW	4'b0000
[23:20]	hns_pocq_class2_qos_max	QoS maximum value for Class 2	RW	4'b1011
[19:16]	hns_pocq_class2_qos_min	QoS minimum value for Class 2	RW	4'b1000
[15:12]	hns_pocq_class1_qos_max	QoS maximum value for Class 1	RW	4'b1110
[11:8]	hns_pocq_class1_qos_min	QoS minimum value for Class 1	RW	4'b1100
[7:4]	hns_pocq_class0_qos_max	QoS maximum value for Class 0	RW	4'b1111
[3:0]	hns_pocq_class0_qos_min	QoS minimum value for Class 0	RW	4'b1111

4.3.10.97 cmn_hns_class_pocq_arb_weight_ctl

Per Class weight controls for scheduling requests from POCQ.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1050

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-378: cmn_hns_class_pocq_arb_weight_ctl

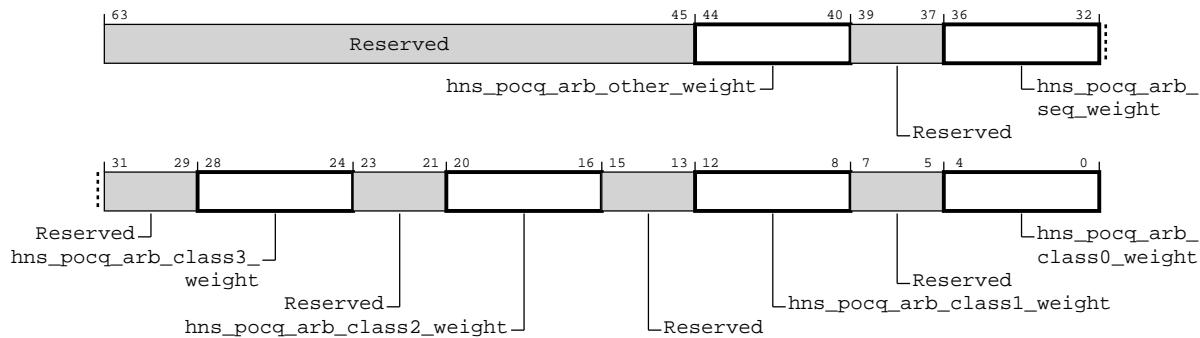


Table 4-394: cmn_hns_class_pocq_arb_weight_ctl attributes

Bits	Name	Description	Type	Reset
[63:45]	Reserved	Reserved	RO	-
[44:40]	hns_pocq_arb_other_weight	Other req weight for scheduling requests from POCQ	RW	5'b00000
[39:37]	Reserved	Reserved	RO	-
[36:32]	hns_pocq_arb_seq_weight	SEQ weight for scheduling requests from POCQ	RW	5'b00000
[31:29]	Reserved	Reserved	RO	-
[28:24]	hns_pocq_arb_class3_weight	Class3 weight for scheduling requests from POCQ	RW	5'b00000
[23:21]	Reserved	Reserved	RO	-
[20:16]	hns_pocq_arb_class2_weight	Class2 weight for scheduling requests from POCQ	RW	5'b00000
[15:13]	Reserved	Reserved	RO	-
[12:8]	hns_pocq_arb_class1_weight	Class1 weight for scheduling requests from POCQ	RW	5'b00000
[7:5]	Reserved	Reserved	RO	-
[4:0]	hns_pocq_arb_class0_weight	Class0 weight for scheduling requests from POCQ	RW	5'b00000

4.3.10.98 cmn_hns_class_retry_weight_ctl

Per Class weight controls for Retry Credit grant.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1058

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-379: cmn_hns_class_retry_weight_ctl

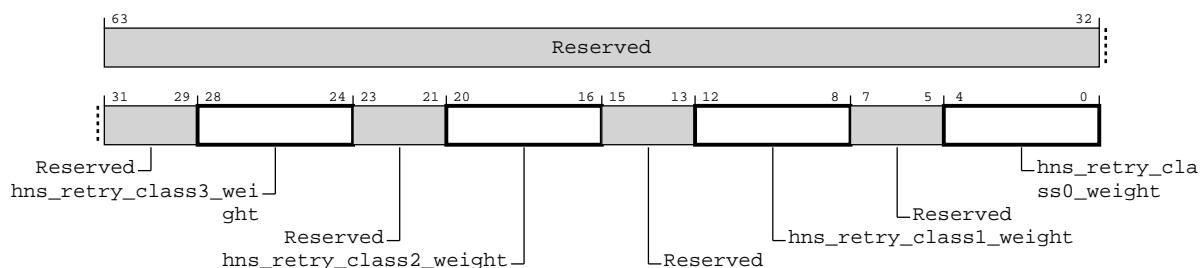


Table 4-395: cmn_hns_class_retry_weight_ctl attributes

Bits	Name	Description	Type	Reset
[63:29]	Reserved	Reserved	RO	-
[28:24]	hns_retry_class3_weight	Overall Class3 weight for credit grant arbitration	RW	5'b00000
[23:21]	Reserved	Reserved	RO	-
[20:16]	hns_retry_class2_weight	Overall Class2 weight for credit grant arbitration	RW	5'b00000
[15:13]	Reserved	Reserved	RO	-
[12:8]	hns_retry_class1_weight	Overall Class1 weight for credit grant arbitration	RW	5'b00000
[7:5]	Reserved	Reserved	RO	-
[4:0]	hns_retry_class0_weight	Overall Class0 weight for credit grant arbitration	RW	5'b00000

4.3.10.99 cmn_hns_pocq_misc_retry_weight_ctl

Weight controls for Snoop, SEQ, Flush and other misc POCQ requests.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1060

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-380: cmn_hns_pocq_misc_retry_weight_ctl

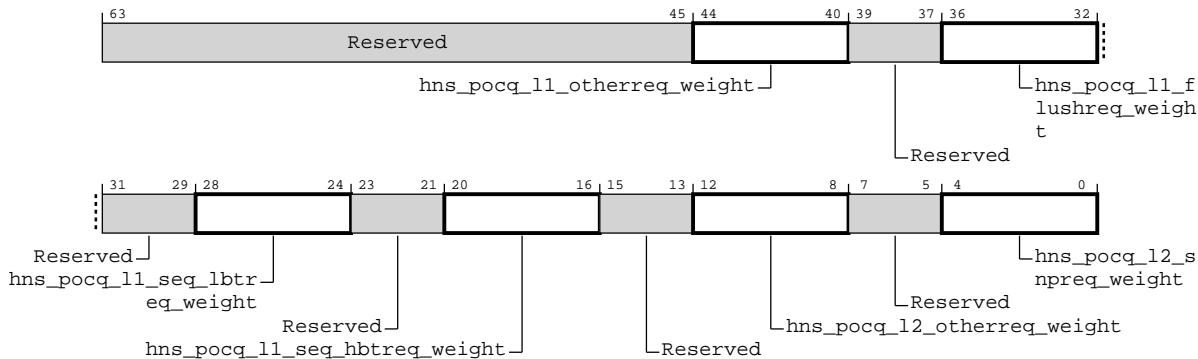


Table 4-396: cmn_hns_pocq_misc_retry_weight_ctl attributes

Bits	Name	Description	Type	Reset
[63:45]	Reserved	Reserved	RO	-
[44:40]	hns_pocq_l1_otherreq_weight	Weight for other requests (Ex: Debug Read) for POCQ allocation arbitration for Level 1. Note: This is first level arb weight control. Second level after this arb is for snpreq.	RW	5'b00000

Bits	Name	Description	Type	Reset
[39:37]	Reserved	Reserved	RO	-
[36:32]	hns_pocq_l1_flushreq_weight	Weight for SLF/SF Flush requests for POCQ allocation arbitration for Level 1. Note: This is first level arb weight control. Second level after this arb is for snpreq.	RW	5'b00000
[31:29]	Reserved	Reserved	RO	-
[28:24]	hns_pocq_l1_seq_lbreq_weight	Weight for SEQ-LBT requests for POCQ allocation arbitration for Level 1. Note: This is first level arb weight control. Second level after this arb is for snpreq.	RW	5'b00000
[23:21]	Reserved	Reserved	RO	-
[20:16]	hns_pocq_l1_seq_hbtreq_weight	Weight for SEQ-HBT requests for POCQ allocation arbitration for Level 1. Note: This is first level arb weight control. Second level after this arb is for snpreq.	RW	5'b00000
[15:13]	Reserved	Reserved	RO	-
[12:8]	hns_pocq_l2_otherreq_weight	Weight for other requests (Ex: Level 1 arb req) for POCQ allocation arbitration for Level 2. Note: This is second level arb weight control. First level is seq, flush, dbgrd, etc.	RW	5'b00000
[7:5]	Reserved	Reserved	RO	-
[4:0]	hns_pocq_l2_snpreq_weight	Weight for external snoop requests for POCQ allocation arbitration for Level 2. Note: This is second level arb weight control. First level is seq, flush, dbgrd, etc	RW	5'b00000

4.3.10.100 cmn_hns_partner_scratch_reg0

Partner scratch register 0

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFE0

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.partner_scratch_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-381: cmn_hns_partner_scratch_reg0

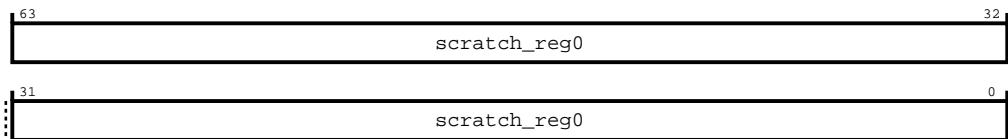


Table 4-397: cmn_hns_partner_scratch_reg0 attributes

Bits	Name	Description	Type	Reset
[63:0]	scratch_reg0	64 bit scratch register 0 with read/write access	RW	64'h00000000

4.3.10.101 cmn_hns_partner_scratch_reg1

Partner scratch register 1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hFE8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.partner_scratch_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-382: cmn_hns_partner_scratch_reg1

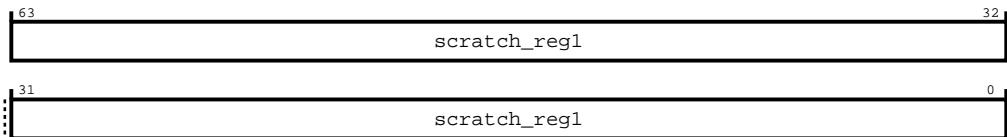


Table 4-398: cmn_hns_partner_scratch_reg1 attributes

Bits	Name	Description	Type	Reset
[63:0]	scratch_reg1	64 bit scratch register 1 with read/write access	RW	64'h00000000

4.3.10.102 cmn_hns_cfg_slcsf_dbgrd

Controls access modes for SLC tags, SLC data, and SF tag debug read.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hB80

Type

WO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slcsf_dbgrd

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-383: cmn_hns_cfg_slcsf_dbgrd

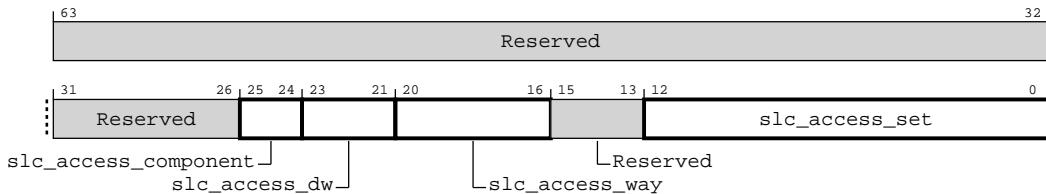


Table 4-399: cmn_hns_cfg_slcsf_dbgrd attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25:24]	slc_access_component	Specifies SLC/SF array debug read 2'b01 SLC data read 2'b10 SLC tag read 2'b11 SF tag read	WO	2'b00
[23:21]	slc_access_dw	64-bit chunk address for SLC data debug read access	WO	3'h0
[20:16]	slc_access_way	Way address for SLC/SF debug read access	WO	5'h00
[15:13]	Reserved	Reserved	RO	-
[12:0]	slc_access_set	Set address for SLC/SF debug read access	WO	13'h0

4.3.10.103 cmn_hns_slc_cache_access_slc_tag

Contains SLC tag debug read data bits [63:0]

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hB88

Type

RO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slcsf_dbgrd

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-384: cmn_hns_slc_cache_access_slc_tag

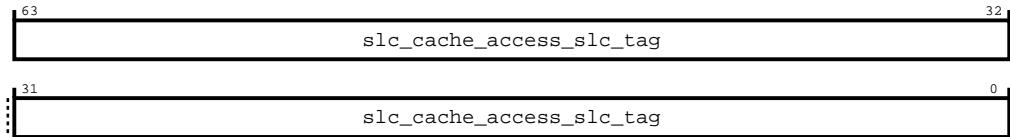


Table 4-400: cmn_hns_slc_cache_access_slc_tag attributes

Bits	Name	Description	Type	Reset
[63:0]	slc_cache_access_slc_tag	SLC tag debug read data	RO	64'h0

4.3.10.104 cmn_hns_slc_cache_access_slc_tag1

Contains SLC tag debug read data bits [127:64] when present

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hB90

Type

RO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slcsf_dbgrd

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-385: cmn_hns_slc_cache_access_slc_tag1

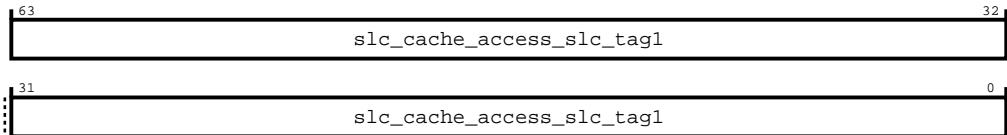


Table 4-401: cmn_hns_slc_cache_access_slc_tag1 attributes

Bits	Name	Description	Type	Reset
[63:0]	slc_cache_access_slc_tag1	SLC tag debug read data	RO	64'h0

4.3.10.105 cmn_hns_slc_cache_access_slc_data

Contains SLC data RAM debug read data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hB98

Type

RO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slcsf_dbgrd

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-386: cmn_hns_slc_cache_access_slc_data

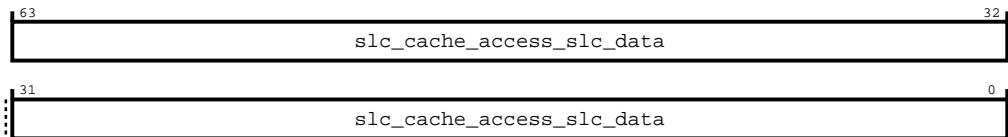


Table 4-402: cmn_hns_slc_cache_access_slc_data attributes

Bits	Name	Description	Type	Reset
[63:0]	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

4.3.10.106 cmn_hns_slc_cache_access_slc_mte_tag

Contains MTE Tag data for the corresponding SLC data RAM debug read.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hBC0

Type

RO

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slcsf_dbgrd`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-387: cmn_hns_slc_cache_access_slc_mte_tag

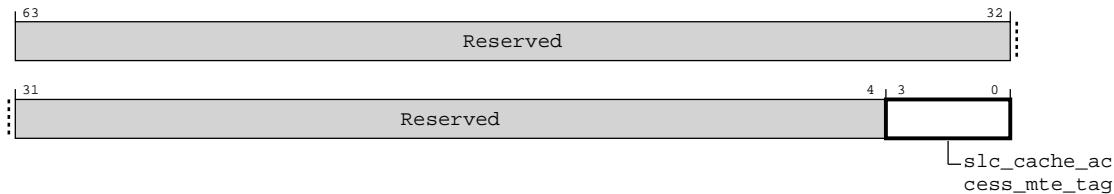


Table 4-403: cmn_hns_slc_cache_access_slc_mte_tag attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3:0]	slc_cache_access_mte_tag	SLC MTE TAG corresponding to data RAM debug read data (128bit chunk of data)	RO	4'h0

4.3.10.107 cmn_hns_slc_cache_access_sf_tag

Contains SF tag debug read data. Bits[63:0]

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hBA0

Type

RO

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.slcsf_dbgrd

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-388: cmn_hns_slc_cache_access_sf_tag

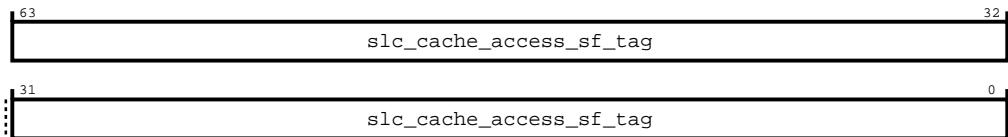


Table 4-404: cmn_hns_slc_cache_access_sf_tag attributes

Bits	Name	Description	Type	Reset
[63:0]	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

4.3.10.108 cmn_hns_slc_cache_access_sf_tag1

Contains SF tag debug read data bits [127:64], when present in SF Tag

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hBA8

Type

RO

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slcsf_dbgrd`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-389: cmn_hns_slc_cache_access_sf_tag1

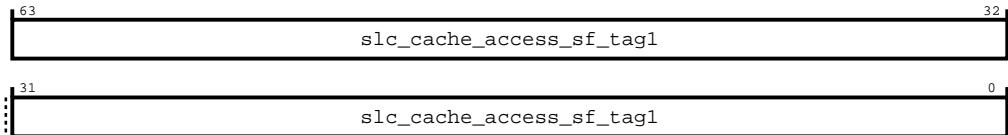


Table 4-405: cmn_hns_slc_cache_access_sf_tag1 attributes

Bits	Name	Description	Type	Reset
[63:0]	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

4.3.10.109 cmn_hns_slc_cache_access_sf_tag2

Contains SF tag debug read data bits [128:191], when present in SF Tag

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hBB0

Type

RO

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.slcsf_dbgrd`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-390: cmn_hns_slc_cache_access_sf_tag2

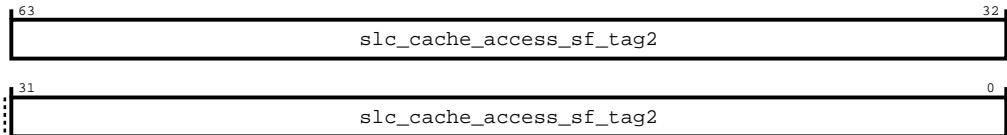


Table 4-406: cmn_hns_slc_cache_access_sf_tag2 attributes

Bits	Name	Description	Type	Reset
[63:0]	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

4.3.10.110 cmn_hns_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-391: cmn_hns_pmu_event_sel

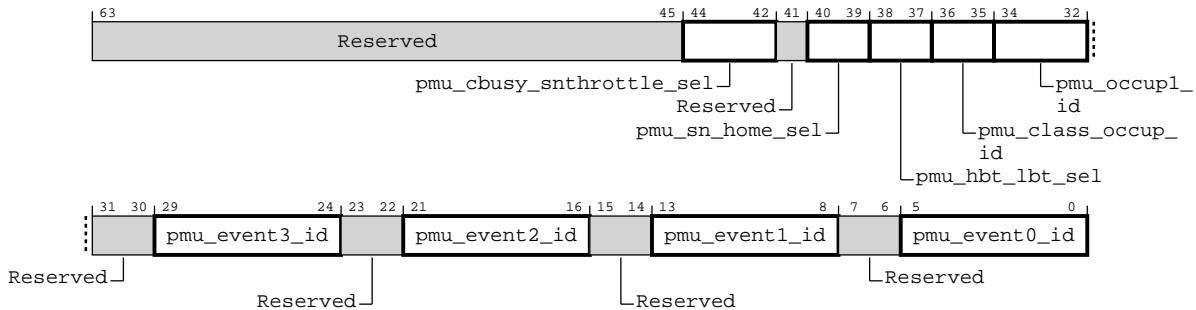


Table 4-407: cmn_hns_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:45]	Reserved	Reserved	RO	-
[44:42]	pmu_cbusy_snthrottle_sel	Filter for selecting specific SN throttle type 3'b000 All SN types throttled 3'b001 SN Group 0 Reads 3'b010 SN Group 0 Non-Reads 3'b011 SN Group 1 Reads 3'b100 SN Group 1 Non-Reads 3'b101 All SN Reads 3'b110 All SN Non-Reads	RW	3'h0
[41]	Reserved	Reserved	RO	-
[40:39]	pmu_sn_home_sel	HN-F PMU SN/Home select 2'b00: All requests selected 2'b01: SN bound requests selected 2'b10: Home bound requests selected	RW	2'h0
[38:37]	pmu_hbt_lbt_sel	HN-F PMU HBT/LBT select 2'b00: All requests selected 2'b01: HBT requests selected 2'b10: LBT requests selected	RW	2'h0
[36:35]	pmu_class_occup_id	HN-F PMU Class select 2'b00 Class 0 selected 2'b01 Class 1 selected 2'b10 Class 2 selected 2'b11 Class 3 selected	RW	2'h0

Bits	Name	Description	Type	Reset
[34:32]	pmu_occup1_id	HN-F PMU occupancy 1 select 3'b000 All occupancy selected 3'b001 Read requests 3'b010 Write requests 3'b011 Atomic operation requests 3'b100 Stash requests 3'b101 RxSnp requests 3'b110 LBT requests 3'b111 HBT requests	RW	3'h0
[31:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	HN-F PMU Event 3 select; see pmu_event0_id for encodings	RW	6'h00
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	HN-F PMU Event 2 select; see pmu_event0_id for encodings	RW	6'h00
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	HN-F PMU Event 1 select; see pmu_event0_id for encodings	RW	6'h00
[7:6]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[5:0]	pmu_event0_id	<p>HN-F PMU Event 0 select</p> <p>6'h00 No event</p> <p>6'h01 PMU_HN_CACHE_MISS_EVENT; counts total cache misses in first lookup result (high priority). Filtering is programmed in pmu_hbt_lbt_sel</p> <p>6'h02 PMU_HN_SLCSF_CACHE_ACCESS_EVENT; counts number of cache accesses in first access (high priority)</p> <p>6'h03 PMU_HN_CACHE_FILL_EVENT; counts total allocations in HN SLC (all cache line allocations to SLC)</p> <p>6'h04 PMU_HN_POCQ_RETRY_EVENT; counts number of retried requests</p> <p>6'h05 PMU_HN_POCQ_REQS_RECVD_EVENT; counts number of requests received by HN</p> <p>6'h06 PMU_HN_SF_HIT_EVENT; counts number of SF hits</p> <p>6'h07 PMU_HN_SF_EVICTIONS_EVENT; counts number of SF eviction cache invalidations initiated</p> <p>6'h08 PMU_HN_DIR_SNOOPS_SENT_EVENT; counts number of directed snoops sent (not including SF back invalidation)</p> <p>6'h09 PMU_HN_BRD_SNOOPS_SENTEVENT; counts number of multicast snoops send (not including SF back invalidation)</p> <p>6'h0A PMU_HN_SLC_EVICTION_EVENT; counts number of SLC evictions (dirty only)</p> <p>6'h0B PMU_HN_SLC_FILL_INVALID_WAY_EVENT; counts number of SLC fills to an invalid way</p> <p>6'h0C PMU_HN_MC_RETRIES_EVENT; counts number of retried transactions by the MC</p> <p>6'h0D PMU_HN_MC_REQS_EVENT; counts number of requests sent to MC</p> <p>6'h0E PMU_HN_QOS_HH_RETRY_EVENT; counts number of times a HighHigh priority request is protocol retried at the HN-F</p> <p>6'h0F PMU_HN_POCQ_OCCUPANCY_EVENT; counts the POCQ occupancy in HN-F; occupancy filtering is programmed in pmu_occup1_id</p> <p>6'h10 PMU_HN_POCQ_ADDRHAZ_EVENT; counts number of POCQ address hazards upon allocation</p> <p>6'h11 PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT; counts number of POCQ address hazards upon allocation for atomic operations</p> <p>6'h12 PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT; counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations</p> <p>6'h13 PMU_HN_CMP_ADQ_FULL_EVENT; counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations</p> <p>6'h14 PMU_HN_TXDAT_STALL_EVENT; counts number of times HN-F has a pending TXDAT flit but no credits to upload</p> <p>6'h15 PMU_HN_TXRSP_STALL_EVENT; counts number of times HN-F has a pending TXRSP flit but no credits to upload</p> <p>6'h16 PMU_HN_SEQ_FULL_EVENT; counts number of times requests are replayed in SLC pipe due to SEQ being full</p> <p>6'h17 PMU_HN_SEQ_HIT_EVENT; counts number of times a request in SLC hit a pending SF eviction in SEQ</p> <p>6'h18 PMU_HN_SNPs_SENT_EVENT; counts number of snoops sent including directed/multicast/SF back invalidation</p> <p>6'h19 PMU_HN_SFBI_DIR_SNPs_SENT_EVENT; counts number of times directed snoops were sent due to SF back invalidation</p> <p>6'h1a PMU_HN_SFBI_BRD_SNPs_SENT_EVENT; counts number of times multicast snoops were sent due to SF back invalidation</p> <p>6'h1b PMU_HN_SNPs_SENT_UNTRK_EVENT; counts number of times snooped were sent due to untracked RN-Fs</p> <p>6'h1c PMU_HN_INTV_DIRTY_EVENT; counts number of times SF back invalidation resulted in dirty line intervention from the RN</p>	RW	6'ho0

Bits	Name	Description	Type	Reset
[5:0]	pmu_event0_id	<p>HN-F PMU Event 0 select</p> <p>6'h1d PMU_HN_STASH_SNP_SENT_EVENT; counts number of times stash snoops sent</p> <p>6'h1e PMU_HN_STASH_DATA_PULL_EVENT; counts number of times stash snoops resulted in data pull from the RN</p> <p>6'h1f PMU_HN_SNP_FWDED_EVENT; counts number of times data forward snoops sent</p> <p>6'h20 PMU_HN_ATOMIC_FWD_EVENT; counts number of times atomic data was forwarded between POC entries</p> <p>6'h21 PMU_HN_MPAM_REQ_OVER_HARDLIM_EVENT; counts number of times write req can't allocate in SLC due to being over hardlimit</p> <p>6'h22 PMU_HN_MPAM_REQ_OVER_SOFTLIM_EVENT; counts number of times write req is above soft limit</p> <p>6'h23 PMU_HN_SNP_SENT_CLUSTER_EVENT; counts number of snoops sent to clusters excluding individual snoops within a cluster</p> <p>6'h24 PMU_HN_SF_IMPRECISE_EVICT_EVENT; counts number of times an evict op was dropped due to SF clustering</p> <p>6'h25 PMU_HN_SF_EVICT_SHARED_LINE_EVENT; counts number of times a shared line was evicted from SF</p> <p>6'h26 PMU_HN_POCQ_CLASS_OCCUPANCY_EVENT; counts the POCQ occupancy for a given class in HN-F; Class occupancy filtering is programmed in pmu_class_occup_id</p> <p>6'h27 PMU_HN_POCQ_CLASS_RETRY_EVENT; counts number of retried requests for a given class; Class filtering is programmed in pmu_class_occup_id</p> <p>6'h28 PMU_HN_CLASS_MC_REQS_EVENT; counts number of requests sent to MC for a given class; Class filtering is programmed in pmu_class_occup_id</p> <p>6'h29 PMU_HN_CLASS_PCRDGNT_BELOW_CONDMIN_EVENT; counts number of protocol credit grants for a given class when it's above dedicated and below conditional min; Class filtering is programmed in pmu_class_occup_id</p> <p>6'h2A PMU_HN_NUM_SN_CBUSY_THROTTLE_EVENT; counts number of times request to SN was throttled due to cbusy; Event filtering is programmed in pmu_cbusy_snthrottle_sel</p> <p>6'h2B PMU_HN_NUM_SN_CBUSY_THROTTLE_MIN_EVENT; counts number of times request to SN was throttled to the minimum due to cbusy; Event filtering is programmed in pmu_cbusy_snthrottle_sel</p> <p>6'h2C PMU_HN_SF_PRECISE_TO_IMPRECISE_EVENT; counts when number sharers exceeds how many RN's could be precisely tracked in SF</p> <p>6'h2D PMU_HN_SNP_INTV_CLN_EVENT; counts the number of times clean data intervened for a snoop request</p> <p>6'h2E PMU_HN_NC_EXCL_EVENT; counts the number of times non-cacheable exclusive request arrived at HNF</p> <p>6'h2F PMU_HN_EXCL_MON_OVFL_EVENT; counts the number of times exclusive monitor overflowed</p>	RW	6'ho0

4.3.10.111 cmn_hns_pmu_mpam_sel

Specifies details of MPAM event to be counted

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2008

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-392: cmn_hns_pmu_mpam_sel

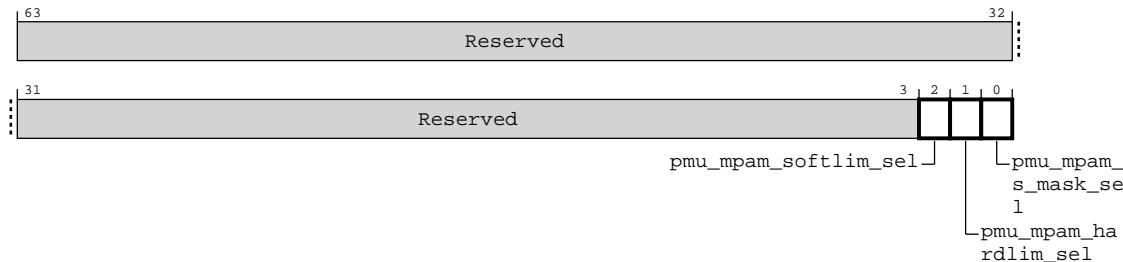


Table 4-408: cmn_hns_pmu_mpam_sel attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	pmu_mpam_softlim_sel	When set, HN-F PMU MPAM Softlimit count is filtered for specific PARTIDs 1'b0: PMU Softlimit count is total for all PARDIDs. 1'b1: PMU Softlimit count is only for PARDIDs indicated in filter register	RW	1'b0
[1]	pmu_mpam_hardlim_sel	When set, HN-F PMU MPAM Hardlimit count is filtered for specific PARTIDs 1'b0: PMU Hardlimit count is total for all PARDIDs. 1'b1: PMU Hardlimit count is only for PARDIDs indicated in filter register	RW	1'b0
[0]	pmu_mpam_s_mask_sel	When set, PARTID Mask is used for Secure MPAM PARTID 1'b0: PMU MPAM mask is for Non-secure MPAMID. 1'b1: PMU MPAM mask is for Secure MPAMID.	RW	1'b0

4.3.10.112 cmn_hns_pmu_mpam_pardid_mask0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Functions as mask for PARTID[#{64*(index+1)-1};#{64*index}] filter for MPM PMU events

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
16'h2010 + #{8*index}
index(0) : 16'h0
```

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-393: cmn_hns_pmu_mpam_pardid_mask0-7

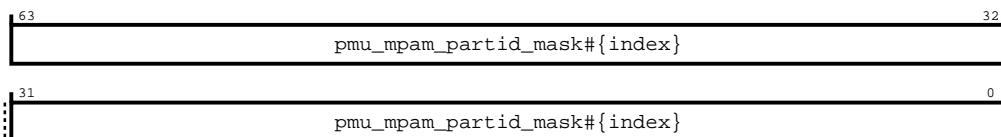


Table 4-409: cmn_hns_pmu_mpam_pardid_mask0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	pmu_mpam_partid_mask#{index}	<p>MPAM PMU hardlimit and softlimit mask for PARTID [#{64*(index+1)-1};#{64*index}]</p> <p>1'b0 PARTID specified is not counted in PMU count. 1'b1 PARTID specified is counted in PMU count. This mask is used only when cmn_hns_pmu_mpam_sel is set for PARTID based counting.</p> <p>Note: This mask is used only when cmn_hns_pmu_mpam_sel is set for PARTID based counting.</p>	RW	64'b0

4.3.10.113 cmn_hns_rn_cluster0-63_physid_reg0

There are 64 iterations of this register. The index ranges from 0 to 63. Configures node IDs for RNs in the system corresponding to each RN ID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3C00 + #{index}*32

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-394: cmn_hns_rn_cluster0-63_physid_reg0

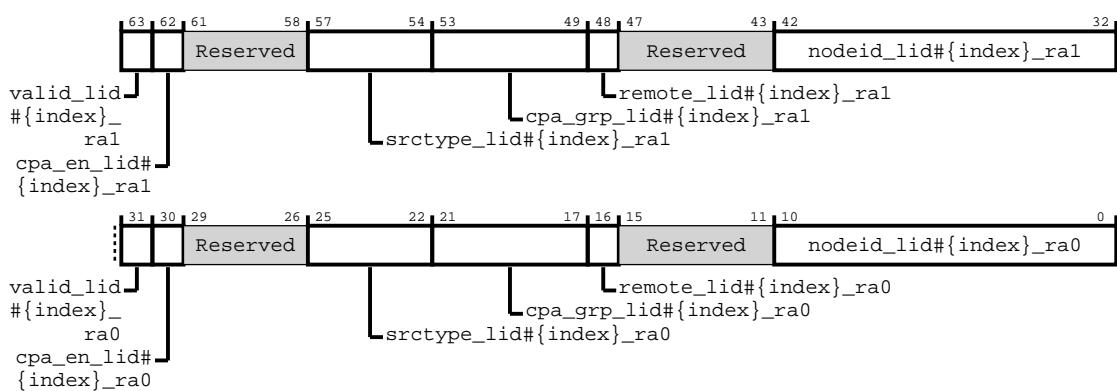


Table 4-410: cmn_hns_rn_cluster0-63_physid_reg0 attributes

Bits	Name	Description	Type	Reset
[63]	valid_lid#{index}_ra1	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[62]	cpa_en_lid#{index}_ra1	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[61:58]	Reserved	Reserved	RO	-
[57:54]	srctype_lid#{index}_ra1	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[53:49]	cpa_grp_lid#{index}_ra1	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[48]	remote_lid#{index}_ra1	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[47:43]	Reserved	Reserved	RO	-
[42:32]	nodeid_lid#{index}_ra1	Specifies the node ID	RW	11'h0
[31]	valid_lid#{index}_ra0	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[30]	cpa_en_lid#{index}_ra0	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[29:26]	Reserved	Reserved	RO	-
[25:22]	srctype_lid#{index}_ra0	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[21:17]	cpa_grp_lid#{index}_ra0	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[16]	remote_lid#{index}_ra0	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[15:11]	Reserved	Reserved	RO	-
[10:0]	nodeid_lid#{index}_ra0	Specifies the node ID	RW	11'h0

4.3.10.114 cmn_hns_rn_cluster64-127_physid_reg0

There are 64 iterations of this register. The index ranges from 64 to 127. Configures node IDs for RNs in the system corresponding to each RN ID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3C00 + #{index}*32

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-395: cmn_hns_rn_cluster64-127_physid_reg0

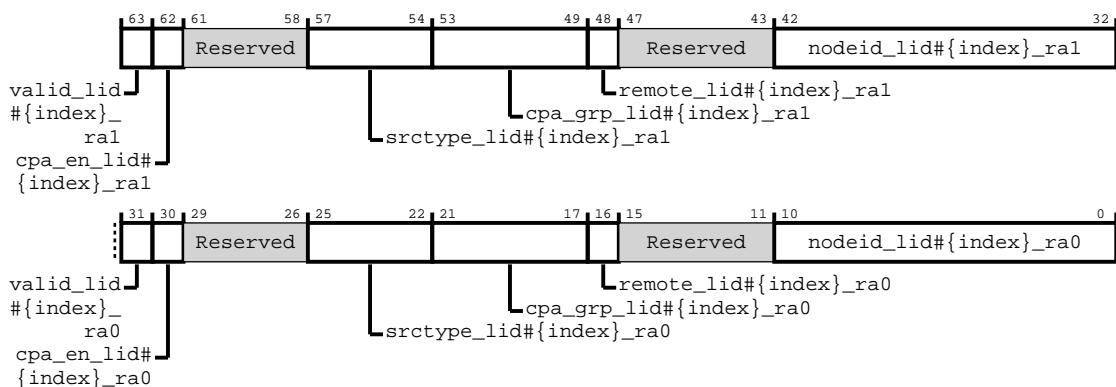


Table 4-411: cmn_hns_rn_cluster64-127_physid_reg0 attributes

Bits	Name	Description	Type	Reset
[63]	valid_lid#{index}_ra1	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[62]	cpa_en_lid#{index}_ra1	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[61:58]	Reserved	Reserved	RO	-
[57:54]	srctype_lid#{index}_ra1	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[53:49]	cpa_grp_lid#{index}_ra1	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[48]	remote_lid#{index}_ra1	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[47:43]	Reserved	Reserved	RO	-
[42:32]	nodeid_lid#{index}_ra1	Specifies the node ID	RW	11'h0
[31]	valid_lid#{index}_ra0	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[30]	cpa_en_lid#{index}_ra0	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[29:26]	Reserved	Reserved	RO	-
[25:22]	srctype_lid#{index}_ra0	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[21:17]	cpa_grp_lid#{index}_ra0	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[16]	remote_lid#{index}_ra0	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[15:11]	Reserved	Reserved	RO	-
[10:0]	nodeid_lid#{index}_ra0	Specifies the node ID	RW	11'h0

4.3.10.115 cmn_hns_rn_cluster0-127_physid_reg1

There are 128 iterations of this register. The index ranges from 0 to 127. Configures node IDs for RNs in the system corresponding to each RN ID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3C08 + #{index}*32

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-396: cmn_hns_rn_cluster0-127_physid_reg1

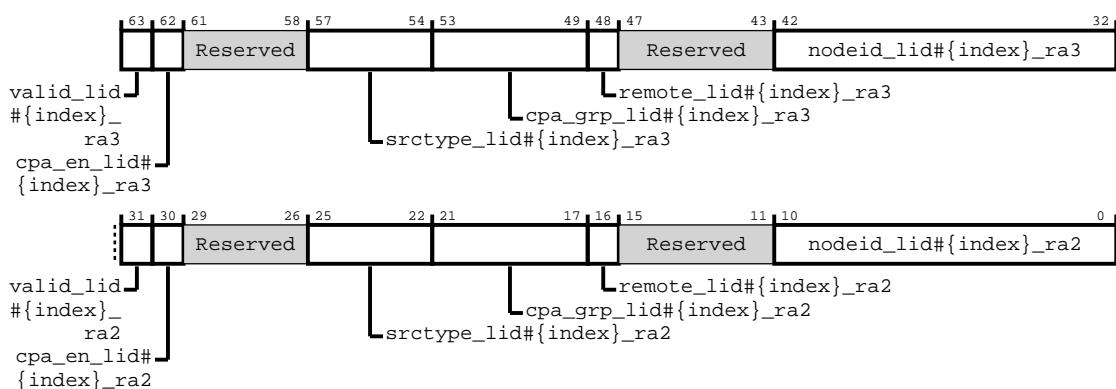


Table 4-412: cmn_hns_rn_cluster0-127_physid_reg1 attributes

Bits	Name	Description	Type	Reset
[63]	valid_lid#{index}_ra3	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[62]	cpa_en_lid#{index}_ra3	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[61:58]	Reserved	Reserved	RO	-
[57:54]	srctype_lid#{index}_ra3	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[53:49]	cpa_grp_lid#{index}_ra3	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[48]	remote_lid#{index}_ra3	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[47:43]	Reserved	Reserved	RO	-
[42:32]	nodeid_lid#{index}_ra3	Specifies the node ID	RW	11'h0
[31]	valid_lid#{index}_ra2	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[30]	cpa_en_lid#{index}_ra2	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[29:26]	Reserved	Reserved	RO	-
[25:22]	srctype_lid#{index}_ra2	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[21:17]	cpa_grp_lid#{index}_ra2	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[16]	remote_lid#{index}_ra2	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[15:11]	Reserved	Reserved	RO	-
[10:0]	nodeid_lid#{index}_ra2	Specifies the node ID	RW	11'h0

4.3.10.116 cmn_hns_rn_cluster0-127_physid_reg2

There are 128 iterations of this register. The index ranges from 0 to 127. Configures node IDs for RNs in the system corresponding to each RN ID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3C10 + #{index}*32

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-397: cmn_hns_rn_cluster0-127_physid_reg2

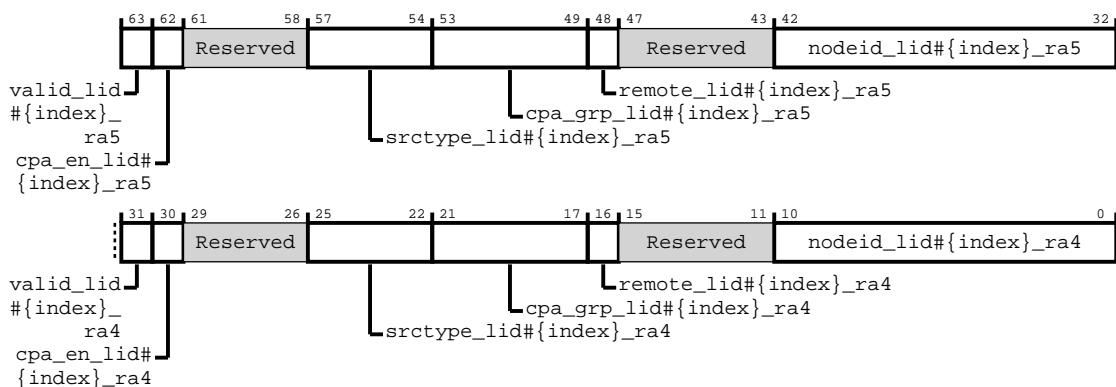


Table 4-413: cmn_hns_rn_cluster0-127_physid_reg2 attributes

Bits	Name	Description	Type	Reset
[63]	valid_lid#{index}_ra5	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[62]	cpa_en_lid#{index}_ra5	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[61:58]	Reserved	Reserved	RO	-
[57:54]	srctype_lid#{index}_ra5	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[53:49]	cpa_grp_lid#{index}_ra5	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[48]	remote_lid#{index}_ra5	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[47:43]	Reserved	Reserved	RO	-
[42:32]	nodeid_lid#{index}_ra5	Specifies the node ID	RW	11'h0
[31]	valid_lid#{index}_ra4	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[30]	cpa_en_lid#{index}_ra4	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[29:26]	Reserved	Reserved	RO	-
[25:22]	srctype_lid#{index}_ra4	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[21:17]	cpa_grp_lid#{index}_ra4	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[16]	remote_lid#{index}_ra4	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[15:11]	Reserved	Reserved	RO	-
[10:0]	nodeid_lid#{index}_ra4	Specifies the node ID	RW	11'h0

4.3.10.117 cmn_hns_rn_cluster0-127_physid_reg3

There are 128 iterations of this register. The index ranges from 0 to 127. Configures node IDs for RNs in the system corresponding to each RN ID.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3C18 + #{index}*32

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-398: cmn_hns_rn_cluster0-127_physid_reg3

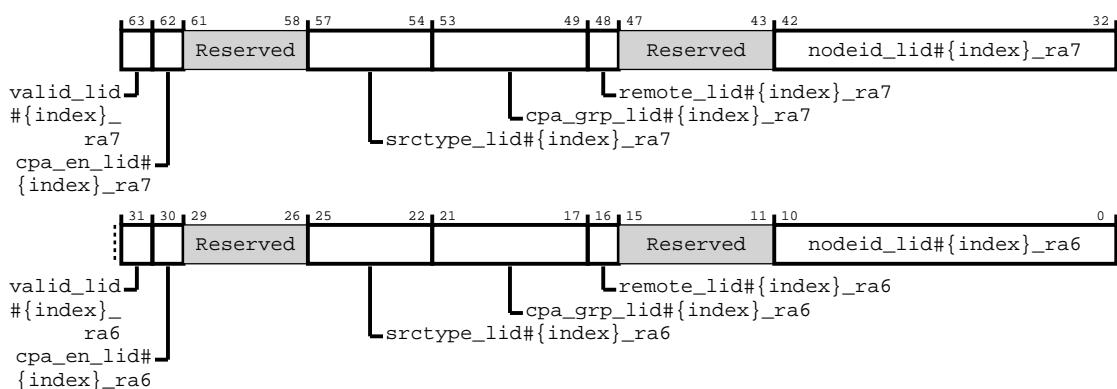


Table 4-414: cmn_hns_rn_cluster0-127_physid_reg3 attributes

Bits	Name	Description	Type	Reset
[63]	valid_lid#{index}_ra7	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[62]	cpa_en_lid#{index}_ra7	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[61:58]	Reserved	Reserved	RO	-
[57:54]	srctype_lid#{index}_ra7	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[53:49]	cpa_grp_lid#{index}_ra7	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[48]	remote_lid#{index}_ra7	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[47:43]	Reserved	Reserved	RO	-
[42:32]	nodeid_lid#{index}_ra7	Specifies the node ID	RW	11'h0
[31]	valid_lid#{index}_ra6	Specifies whether the RN is valid 1'b0 RN ID is not valid 1'b1 RN ID is pointing to a valid CHI device	RW	1'h0
[30]	cpa_en_lid#{index}_ra6	Specifies whether the CCIX port aggregation is enabled 1'b0 CPA not enabled 1'b1 CPA enabled	RW	1'h0
[29:26]	Reserved	Reserved	RO	-
[25:22]	srctype_lid#{index}_ra6	Specifies the CHI source type of the RN 4'b1010 256 bit CHI-B RN-F 4'b1011 256 bit CHI-C RN-F 4'b1100 256 bit CHI-D RN-F 4'b1101 256 bit CHI-E RN-F Others Reserved	RW	4'h0000
[21:17]	cpa_grp_lid#{index}_ra6	Specifies CCIX port aggregation group ID(0-31)	RW	5'h0
[16]	remote_lid#{index}_ra6	Specifies whether the RN is remote or local 1'b0 Local RN 1'b1 Remote RN	RW	1'h0
[15:11]	Reserved	Reserved	RO	-
[10:0]	nodeid_lid#{index}_ra6	Specifies the node ID	RW	11'h0

4.3.10.118 cmn_hns_sam_nonhash_cfg1_memregion2-63

There are 62 iterations of this register. The index ranges from 2 to 63. Configures non-hashed memory region #{index} in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5000 + #{index}*8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-399: cmn_hns_sam_nonhash_cfg1_memregion2-63

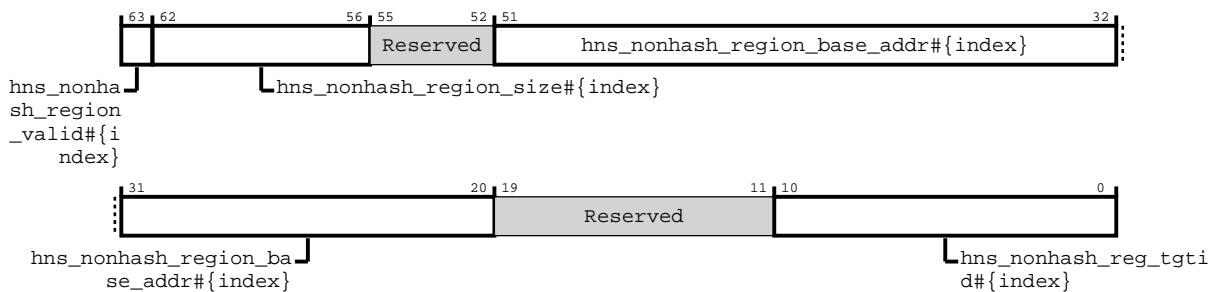


Table 4-415: cmn_hns_sam_nonhash_cfg1_memregion2-63 attributes

Bits	Name	Description	Type	Reset
[63]	hns_nonhash_region_valid#{index}	valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0
[62:56]	hns_nonhash_region_size#{index}	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'b0
[55:52]	Reserved	Reserved	RO	-
[51:20]	hns_nonhash_region_base_addr#{index}	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	32'h0
[19:11]	Reserved	Reserved	RO	-
[10:0]	hns_nonhash_reg_tgtid#{index}	SN TgtID for the non-hashed region	RW	11'h0

4.3.10.119 cmn_hns_sam_nonhash_cfg2_memregion2-63

There are 62 iterations of this register. The index ranges from 2 to 63. Configures non-hashed memory region #{index} in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16^{\text{h}}5200 + \#\{\text{index}\}*8$

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-400: cmn_hns_sam_nonhash_cfg2_memregion2-63

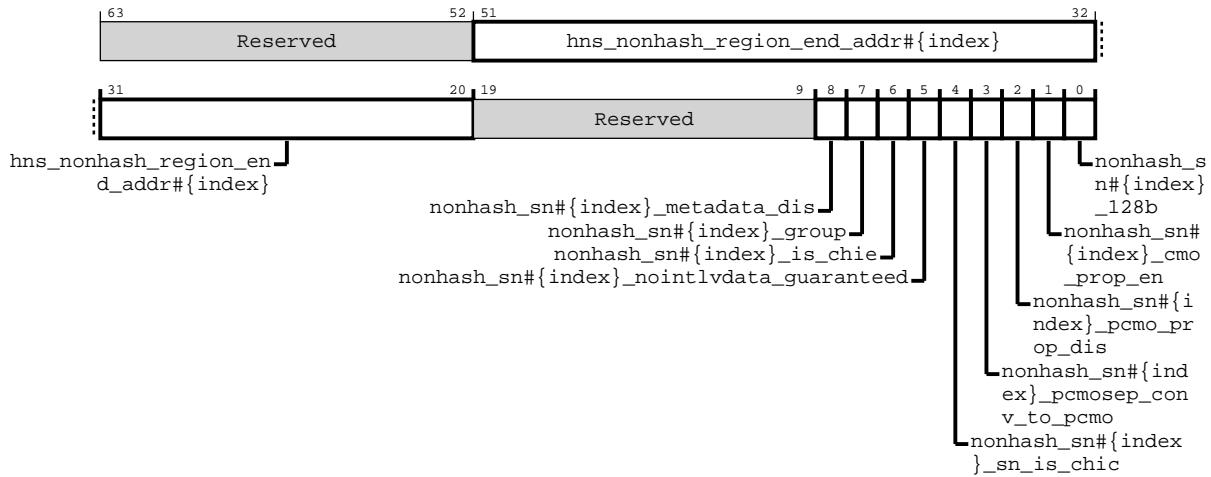


Table 4-416: cmn_hns_sam_nonhash_cfg2_memregion2-63 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:20]	hns_nonhash_region_end_addr#{index}	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	32'h0
[19:9]	Reserved	Reserved	RO	-
[8]	nonhash_sn#{index}_metadata_dis	HNS implements metadata termination flow for nonhash SN #{index} when set	RW	1'b0
[7]	nonhash_sn#{index}_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[6]	nonhash_sn#{index}_is_chie	nonhash SN #{index} supports CHI-E	RW	1'b0
[5]	nonhash_sn#{index}_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[4]	nonhash_sn#{index}_sn_is_chic	Indicates that nonhash sn is a CHI-C SN when set	RW	1'b0
[3]	nonhash_sn#{index}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for nonhash SN #{index} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[2]	nonhash_sn#{index}_pcmo_prop_dis	Disables PCMO propagation for nonhash SN #{index} when set	RW	1'b0
[1]	nonhash_sn#{index}_cmo_prop_en	Enables CMO propagation for nonhash SN #{index} when set	RW	1'b0
[0]	nonhash_sn#{index}_128b	Data width of nonhash SN #{index} 1'b1 128 bits 1'b0 256 bits	RW	1'b0

4.3.10.120 cmn_hns_sam_htg_cfg1_memregion0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures HTG memory region #*{index}* in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5400 + #{index}*8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-401: cmn_hns_sam_htg_cfg1_memregion0-15

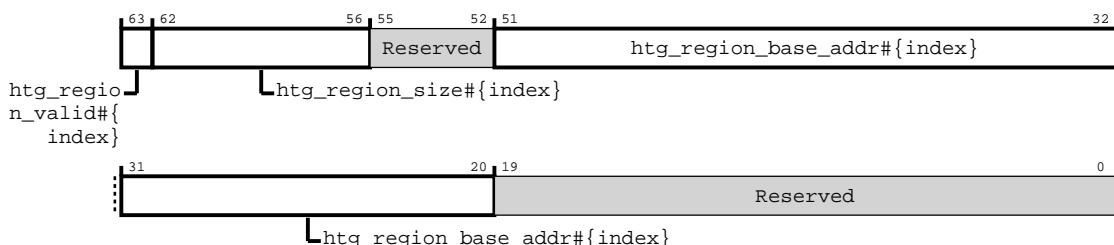


Table 4-417: cmn_hns_sam_htg_cfg1_memregion0-15 attributes

Bits	Name	Description	Type	Reset
[63]	htg_region_valid#{index}	valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0
[62:56]	htg_region_size#{index}	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'b00000
[55:52]	Reserved	Reserved	RO	-
[51:20]	htg_region_base_addr#{index}	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	32'h0
[19:0]	Reserved	Reserved	RO	-

4.3.10.121 cmn_hns_sam_htg_cfg2_memregion0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures htg memory region #{index} in HN-F SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5480 + #{index}*8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-402: cmn_hns_sam_htg_cfg2_memregion0-15

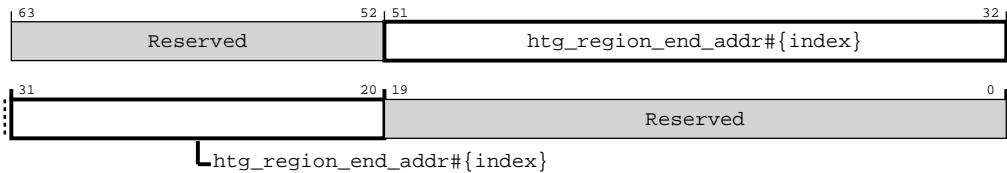


Table 4-418: cmn_hns_sam_htg_cfg2_memregion0-15 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:20]	htg_region_end_addr#{index}	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	32'h0
[19:0]	Reserved	Reserved	RO	-

4.3.10.122 cmn_hns_sam_htg_cfg3_memregion0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures the HTG memory region #{index}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16'h5500 + \#\{index\}*8$

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-403: cmn_hns_sam_htg_cfg3_memregion0-15

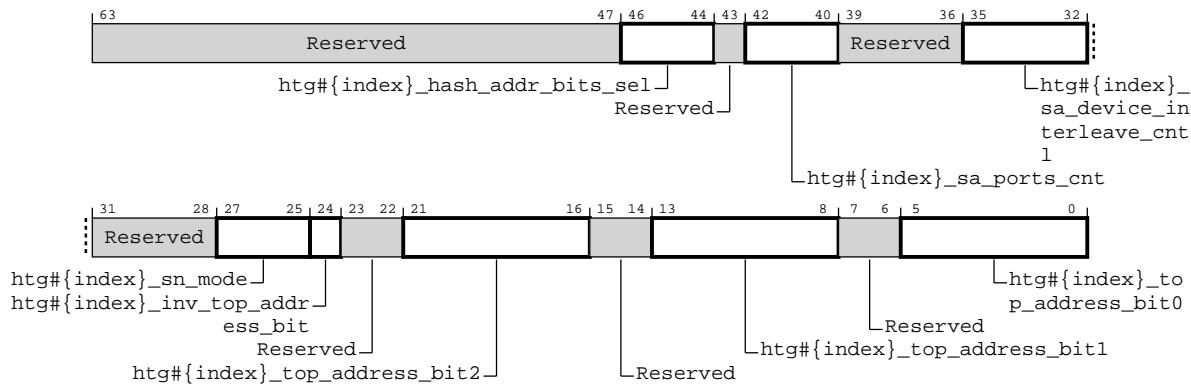


Table 4-419: cmn_hns_sam_htg_cfg3_memregion0-15 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:44]	htg#[index].hash_addr_bits_sel	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[43]	Reserved	Reserved	RO	-
[42:40]	htg#[index].sa_ports_cnt	Specifies the number of CXSA/CXLSA device aggregated 1'b0 Local RN 1'b1 Remote RN	RW	3'b0
[39:36]	Reserved	Reserved	RO	-
[35:32]	htg#[index].sa_device_interleave_cnt	This field controls the interleave size across all aggregated CXSA/CXLSA Devices 4'h0 64B Interleaved 4'h1 128B Interleaved 4'h2 256B Interleaved 4'h3 512B Interleaved 4'hF 2MB Interleaved	RW	4'b0

Bits	Name	Description	Type	Reset
[31:28]	Reserved	Reserved	RO	-
[27:25]	htg#[{index}_sn_mode	SN selection mode 3'b000 Reserved 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing 3'b111 CXSA/CXLSA aggregated SA selection function	RW	3'b0
[24]	htg#[{index}_inv_top_address_bit	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	htg#[{index}_top_address_bit2	Top address bit 2	RW	6'h00
[15:14]	Reserved	Reserved	RO	-
[13:8]	htg#[{index}_top_address_bit1	Top address bit 1	RW	6'h00
[7:6]	Reserved	Reserved	RO	-
[5:0]	htg#[{index}_top_address_bit0	Top address bit 0	RW	6'h00

4.3.10.123 cmn_hns_sam_htg_sn_nodeid_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures SN node IDs for HTGs in the HNSAM . Controls target SN node IDs #{{index}*4 + 0} to #{{index}*4 + 3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5600 + #{index}*8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-404: cmn_hns_sam_htg_sn_nodeid_reg0-15

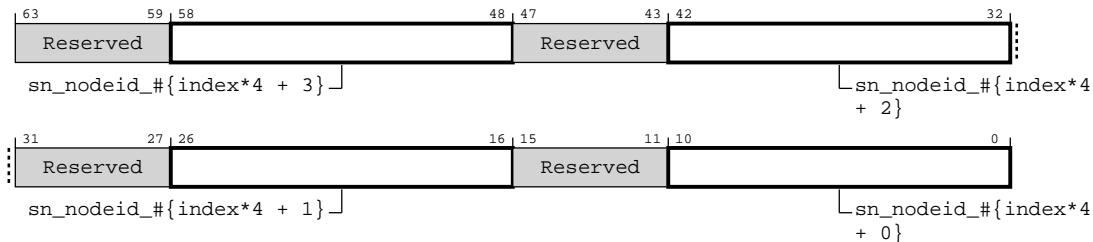


Table 4-420: cmn_hns_sam_htg_sn_nodeid_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:48]	sn_nodeid_{[index*4 + 3]}	Hashed target SN node ID #{index*4 + 3}	RW	11'b0000000000000000
[47:43]	Reserved	Reserved	RO	-
[42:32]	sn_nodeid_{[index*4 + 2]}	Hashed target SN node ID #{index*4 + 2}	RW	11'b0000000000000000
[31:27]	Reserved	Reserved	RO	-
[26:16]	sn_nodeid_{[index*4 + 1]}	Hashed target SN node ID #{index*4 + 1}	RW	11'b0000000000000000
[15:11]	Reserved	Reserved	RO	-
[10:0]	sn_nodeid_{[index*4 + 0]}	Hashed target SN node ID #{index*4 + 0}	RW	11'b0000000000000000

4.3.10.124 cmn_hns_sam_htg_sn_attr0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures SN node attributes HTGs in the HNSAM . Controls SN attributes #{index*4 + 0} to #{index*4 + 3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5680 + #{index}*8

Type

RW

Reset value

See individual bit resets

Secure group override

cmm_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-405: cmn_hns_sam_htg_sn_attr0-15

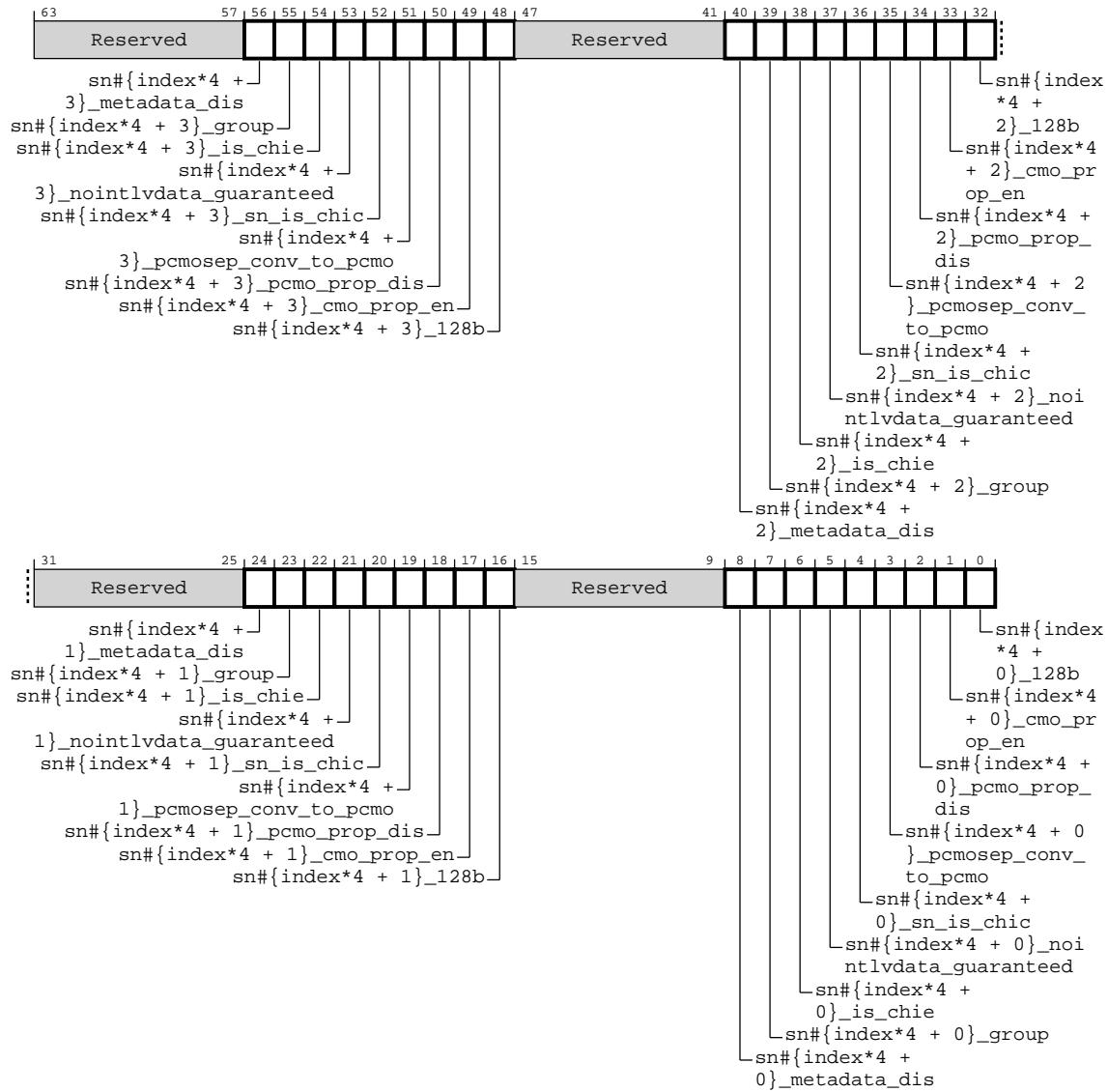


Table 4-421: cmn_hns_sam_htg_sn_attr0-15 attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56]	sn#{index*4 + 3}_metadata_dis	HNS implements metadata termination flow for SN #{index*4 + 3} when set	RW	1'b0
[55]	sn#{index*4 + 3}_group	Specifies the SN-F grouping	RW	1'b0
	1'b0	Group A		
	1'b1	Group B		
[54]	sn#{index*4 + 3}_is_chie	SN #{index*4 + 3} supports CHI-E	RW	1'b0

Bits	Name	Description	Type	Reset
[53]	sn#{index*4 + 3}_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[52]	sn#{index*4 + 3}_sn_is_chic	Indicates that sn is a CHI-C SN when set	RW	1'b0
[51]	sn#{index*4 + 3}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN #{index*4 + 3} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[50]	sn#{index*4 + 3}_pcmoe_prop_dis	Disables PCMO propagation for SN #{index*4 + 3} when set	RW	1'b0
[49]	sn#{index*4 + 3}_cmo_prop_en	Enables CMO propagation for SN #{index*4 + 3} when set	RW	1'b0
[48]	sn#{index*4 + 3}_128b	Data width of SN #{index*4 + 3} 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[47:41]	Reserved	Reserved	RO	-
[40]	sn#{index*4 + 2}_metadata_dis	HNS implements metadata termination flow for SN #{index*4 + 2} when set	RW	1'b0
[39]	sn#{index*4 + 2}_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[38]	sn#{index*4 + 2}_is_chie	SN #{index*4 + 2} supports CHI-E	RW	1'b0
[37]	sn#{index*4 + 2}_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[36]	sn#{index*4 + 2}_sn_is_chic	Indicates that sn is a CHI-C SN when set	RW	1'b0
[35]	sn#{index*4 + 2}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN #{index*4 + 2} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[34]	sn#{index*4 + 2}_pcmoe_prop_dis	Disables PCMO propagation for SN #{index*4 + 2} when set	RW	1'b0
[33]	sn#{index*4 + 2}_cmo_prop_en	Enables CMO propagation for SN #{index*4 + 2} when set	RW	1'b0
[32]	sn#{index*4 + 2}_128b	Data width of SN #{index*4 + 2} 1'b1 128 bits 1'b0 256 bits	RW	1'b0
[31:25]	Reserved	Reserved	RO	-
[24]	sn#{index*4 + 1}_metadata_dis	HNS implements metadata termination flow for SN #{index*4 + 1} when set	RW	1'b0
[23]	sn#{index*4 + 1}_group	Specifies the SN-F grouping 1'b0 Group A 1'b1 Group B	RW	1'b0
[22]	sn#{index*4 + 1}_is_chie	SN #{index*4 + 1} supports CHI-E	RW	1'b0
[21]	sn#{index*4 + 1}_nointlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[20]	sn#{index*4 + 1}_sn_is_chic	Indicates that sn is a CHI-C SN when set	RW	1'b0
[19]	sn#{index*4 + 1}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN #{index*4 + 1} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0

Bits	Name	Description	Type	Reset
[18]	sn#{index*4 + 1}_pcmo_prop_dis	Disables PCMO propagation for SN #{index*4 + 1} when set	RW	1'b0
[17]	sn#{index*4 + 1}_cmo_prop_en	Enables CMO propagation for SN #{index*4 + 1} when set	RW	1'b0
[16]	sn#{index*4 + 1}_128b	Data width of SN #{index*4 + 1}	RW	1'b0
		1'b1 128 bits 1'b0 256 bits		
[15:9]	Reserved	Reserved	RO	-
[8]	sn#{index*4 + 0}_metadata_dis	HNS implements metadata termination flow for SN #{index*4 + 0} when set	RW	1'b0
[7]	sn#{index*4 + 0}_group	Specifies the SN-F grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[6]	sn#{index*4 + 0}_is_chie	SN #{index*4 + 0} supports CHI-E	RW	1'b0
[5]	sn#{index*4 + 0}_noIntlvdata_guaranteed	SN guarantees the return data will not be interleaved	RW	1'b0
[4]	sn#{index*4 + 0}_sn_is_chic	Indicates that sn is a CHI-C SN when set	RW	1'b0
[3]	sn#{index*4 + 0}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN #{index*4 + 0} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[2]	sn#{index*4 + 0}_pcmo_prop_dis	Disables PCMO propagation for SN #{index*4 + 0} when set	RW	1'b0
[1]	sn#{index*4 + 0}_cmo_prop_en	Enables CMO propagation for SN #{index*4 + 0} when set	RW	1'b0
[0]	sn#{index*4 + 0}_128b	Data width of SN #{index*4 + 0}	RW	1'b0
		1'b1 128 bits 1'b0 256 bits		

4.3.10.125 cmn_hns_sam_ccg_sa_nodeid_reg0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Configures CCG SA node IDs for HTGs in the HNSAM

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5700 + #{index}*8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-406: cmn_hns_sam_ccg_sa_nodeid_reg0-3

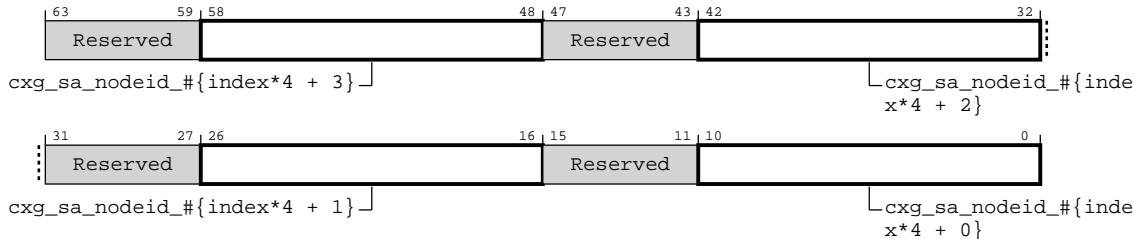


Table 4-422: cmn_hns_sam_ccg_sa_nodeid_reg0-3 attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:48]	cxg_sa_nodeid_{index*4 + 3}	Hashed target CCG SA node ID #{index*4 + 3}	RW	11'b000000000000
[47:43]	Reserved	Reserved	RO	-
[42:32]	cxg_sa_nodeid_{index*4 + 2}	Hashed target CCG SA node ID #{index*4 + 2}	RW	11'b000000000000
[31:27]	Reserved	Reserved	RO	-
[26:16]	cxg_sa_nodeid_{index*4 + 1}	Hashed target CCG SA node ID #{index*4 + 1}	RW	11'b000000000000
[15:11]	Reserved	Reserved	RO	-
[10:0]	cxg_sa_nodeid_{index*4 + 0}	Hashed target CCG SA node ID #{index*4 + 0}	RW	11'b000000000000

4.3.10.126 cmn_hns_sam_ccg_sa_attr0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Configures CCG SA node attributes.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h5740 + #{index}*8`

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.cfg_ctl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-407: cmn_hns_sam_ccg_sa_attr0-3

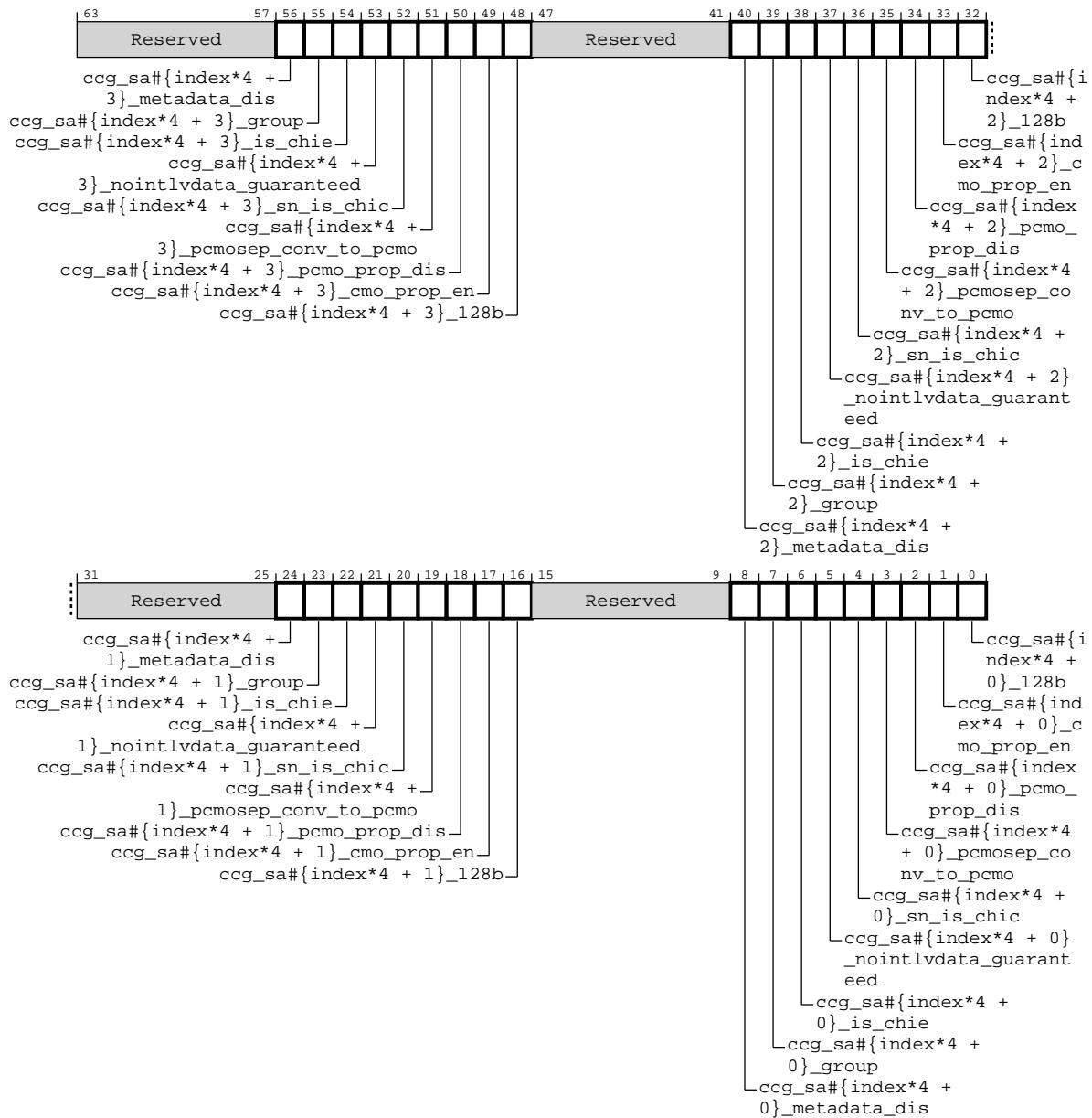


Table 4-423: cmn_hns_sam_ccg_sa_attr0-3 attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56]	<code>ccg_sa#{index*4 + 3}_metadata_dis</code>	HNS implements metadata termination flow for CCG_SA #[index*4 + 3] when set	RW	1'b0
[55]	<code>ccg_sa#{index*4 + 3}_group</code>	Specifies the CCG_SA grouping 1'b0 Group A 1'b1 Group B	RW	1'b0

Bits	Name	Description	Type	Reset
[54]	ccg_sa#{index*4 + 3}_is_chie	CCG_SA #{index*4 + 3} supports CHI-E	RW	1'b0
[53]	ccg_sa#{index*4 + 3}_nointlvdata_guaranteed	CCG_SA guarantees the return data will not be interleaved	RW	1'b0
[52]	ccg_sa#{index*4 + 3}_sn_is_chic	Indicates that CCG_SA is a CHI-C CCG_SA when set	RW	1'b0
[51]	ccg_sa#{index*4 + 3}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for CCG_SA #{index*4 + 3} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[50]	ccg_sa#{index*4 + 3}_pcmoe_prop_dis	Disables PCMO propagation for CCG_SA #{index*4 + 3} when set	RW	1'b0
[49]	ccg_sa#{index*4 + 3}_cmo_prop_en	Enables CMO propagation for CCG_SA #{index*4 + 3} when set	RW	1'b0
[48]	ccg_sa#{index*4 + 3}_128b	Data width of CCG_SA #{index*4 + 3}	RW	1'b0
		1'b1 128 bits 1'b0 256 bits		
[47:41]	Reserved	Reserved	RO	-
[40]	ccg_sa#{index*4 + 2}_metadata_dis	HNS implements metadata termination flow for CCG_SA #{index*4 + 2} when set	RW	1'b0
[39]	ccg_sa#{index*4 + 2}_group	Specifies the CCG_SA grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[38]	ccg_sa#{index*4 + 2}_is_chie	CCG_SA #{index*4 + 2} supports CHI-E	RW	1'b0
[37]	ccg_sa#{index*4 + 2}_nointlvdata_guaranteed	CCG_SA guarantees the return data will not be interleaved	RW	1'b0
[36]	ccg_sa#{index*4 + 2}_sn_is_chic	Indicates that CCG_SA is a CHI-C CCG_SA when set	RW	1'b0
[35]	ccg_sa#{index*4 + 2}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for CCG_SA #{index*4 + 2} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[34]	ccg_sa#{index*4 + 2}_pcmoe_prop_dis	Disables PCMO propagation for CCG_SA #{index*4 + 2} when set	RW	1'b0
[33]	ccg_sa#{index*4 + 2}_cmo_prop_en	Enables CMO propagation for CCG_SA #{index*4 + 2} when set	RW	1'b0
[32]	ccg_sa#{index*4 + 2}_128b	Data width of CCG_SA #{index*4 + 2}	RW	1'b0
		1'b1 128 bits 1'b0 256 bits		
[31:25]	Reserved	Reserved	RO	-
[24]	ccg_sa#{index*4 + 1}_metadata_dis	HNS implements metadata termination flow for CCG_SA #{index*4 + 1} when set	RW	1'b0
[23]	ccg_sa#{index*4 + 1}_group	Specifies the CCG_SA grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[22]	ccg_sa#{index*4 + 1}_is_chie	CCG_SA #{index*4 + 1} supports CHI-E	RW	1'b0

Bits	Name	Description	Type	Reset
[21]	ccg_sa#{index*4 + 1}_nointlvdata_guaranteed	CCG_SA guarantees the return data will not be interleaved	RW	1'b0
[20]	ccg_sa#{index*4 + 1}_sn_is_chic	Indicates that CCG_SA is a CHI-C CCG_SA when set	RW	1'b0
[19]	ccg_sa#{index*4 + 1}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for CCG_SA #{index*4 + 1} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[18]	ccg_sa#{index*4 + 1}_pcmoe_prop_dis	Disables PCMO propagation for CCG_SA #{index*4 + 1} when set	RW	1'b0
[17]	ccg_sa#{index*4 + 1}_cmo_prop_en	Enables CMO propagation for CCG_SA #{index*4 + 1} when set	RW	1'b0
[16]	ccg_sa#{index*4 + 1}_128b	Data width of CCG_SA #{index*4 + 1}	RW	1'b0
		1'b1 128 bits 1'b0 256 bits		
[15:9]	Reserved	Reserved	RO	-
[8]	ccg_sa#{index*4 + 0}_metadata_dis	HNS implements metadata termination flow for CCG_SA #{index*4 + 0} when set	RW	1'b0
[7]	ccg_sa#{index*4 + 0}_group	Specifies the CCG_SA grouping	RW	1'b0
		1'b0 Group A 1'b1 Group B		
[6]	ccg_sa#{index*4 + 0}_is_chie	CCG_SA #{index*4 + 0} supports CHI-E	RW	1'b0
[5]	ccg_sa#{index*4 + 0}_nointlvdata_guaranteed	CCG_SA guarantees the return data will not be interleaved	RW	1'b0
[4]	ccg_sa#{index*4 + 0}_sn_is_chic	Indicates that CCG_SA is a CHI-C CCG_SA when set	RW	1'b0
[3]	ccg_sa#{index*4 + 0}_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for CCG_SA #{index*4 + 0} when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
[2]	ccg_sa#{index*4 + 0}_pcmoe_prop_dis	Disables PCMO propagation for CCG_SA #{index*4 + 0} when set	RW	1'b0
[1]	ccg_sa#{index*4 + 0}_cmo_prop_en	Enables CMO propagation for CCG_SA #{index*4 + 0} when set	RW	1'b0
[0]	ccg_sa#{index*4 + 0}_128b	Data width of CCG_SA #{index*4 + 0}	RW	1'b0
		1'b1 128 bits 1'b0 256 bits		

4.3.10.127 hns_generic_regs0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Configuration register for the custom logic

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h5780 + #{index}*8`

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.cfg_ctl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-408: hns_generic_regs0-7

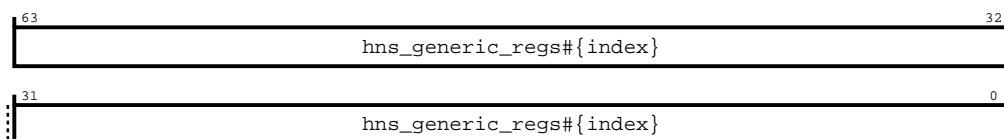


Table 4-424: hns_generic_regs0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	<code>hns_generic_regs#{index}</code>	Configuration register for the custom logic	RW	<code>64'h0</code>

4.3.10.128 cmn_hns_pa2setaddr_slc

Functions as the control register of PA to SetAddr and vice versa conversion for HNS-SLC

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5900

Type

RW

Reset value

See individual bit resets

Secure group override

cnn_hns_secure_register_groups_override.pa2setaddr_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-409: cmn_hns_pa2setaddr_slc

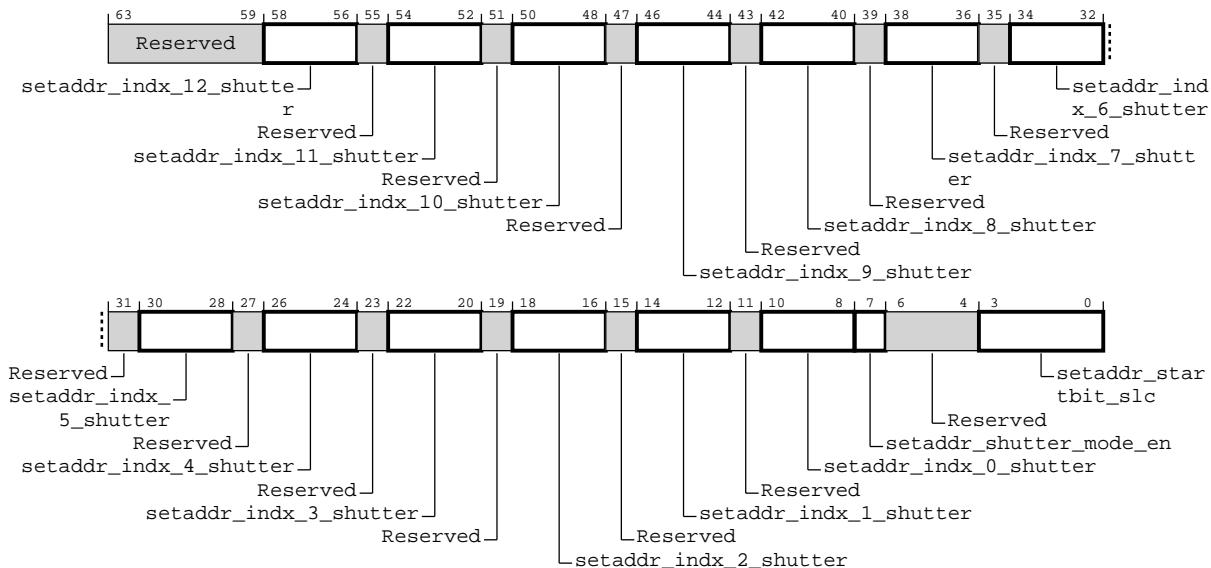


Table 4-425: cmn_hns_pa2setaddr_slc attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[58:56]	setaddr_idx_12_shutter	Program to specify address bit shuttering for setaddr index 12 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[55]	Reserved	Reserved	RO	-
[54:52]	setaddr_idx_11_shutter	Program to specify address bit shuttering for setaddr index 11 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[51]	Reserved	Reserved	RO	-
[50:48]	setaddr_idx_10_shutter	Program to specify address bit shuttering for setaddr index 10 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[47]	Reserved	Reserved	RO	-
[46:44]	setaddr_idx_9_shutter	Program to specify address bit shuttering for setaddr index 9 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[43]	Reserved	Reserved	RO	-
[42:40]	setaddr_idx_8_shutter	Program to specify address bit shuttering for setaddr index 8 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[39]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[38:36]	setaddr_idx_7_shutter	Program to specify address bit shuttering for setaddr index 7 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[35]	Reserved	Reserved	RO	-
[34:32]	setaddr_idx_6_shutter	Program to specify address bit shuttering for setaddr index 6 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[31]	Reserved	Reserved	RO	-
[30:28]	setaddr_idx_5_shutter	Program to specify address bit shuttering for setaddr index 5 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[27]	Reserved	Reserved	RO	-
[26:24]	setaddr_idx_4_shutter	Program to specify address bit shuttering for setaddr index 4 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[23]	Reserved	Reserved	RO	-
[22:20]	setaddr_idx_3_shutter	Program to specify address bit shuttering for setaddr index 3 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[19]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[18:16]	setaddr_idx_2_shutter	Program to specify address bit shuttering for setaddr index 2 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[15]	Reserved	Reserved	RO	-
[14:12]	setaddr_idx_1_shutter	Program to specify address bit shuttering for setaddr index 1 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[11]	Reserved	Reserved	RO	-
[10:8]	setaddr_idx_0_shutter	Program to specify address bit shuttering for setaddr index 0 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[7]	setaddr_shutter_mode_en	Enables address shuttering mode for SLC as programmed by setaddr_idx_X_shutter registers	RW	1'b0
[6:4]	Reserved	Reserved	RO	-
[3:0]	setaddr_startbit_slc	SLC: SetAddr starting bit for SLC TODO add a description here abt contiguous bits 4'b0110 Setaddr starts from PA[6] 4'b0111 Setaddr starts from PA[7] 4'b1000 Setaddr starts from PA[8] 4'b1001 Setaddr starts from PA[9] 4'b1010 Setaddr starts from PA[10] 4'b1011 Setaddr starts from PA[11] 4'b1100 Setaddr starts from PA[12]	RW	4'b0110

4.3.10.129 cmn_hns_pa2setaddr_sf

Functions as the control register of PA to Set/TagAddr and vice versa conversion for HNS-SF

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5908

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.pa2setaddr_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-410: cmn_hns_pa2setaddr_sf

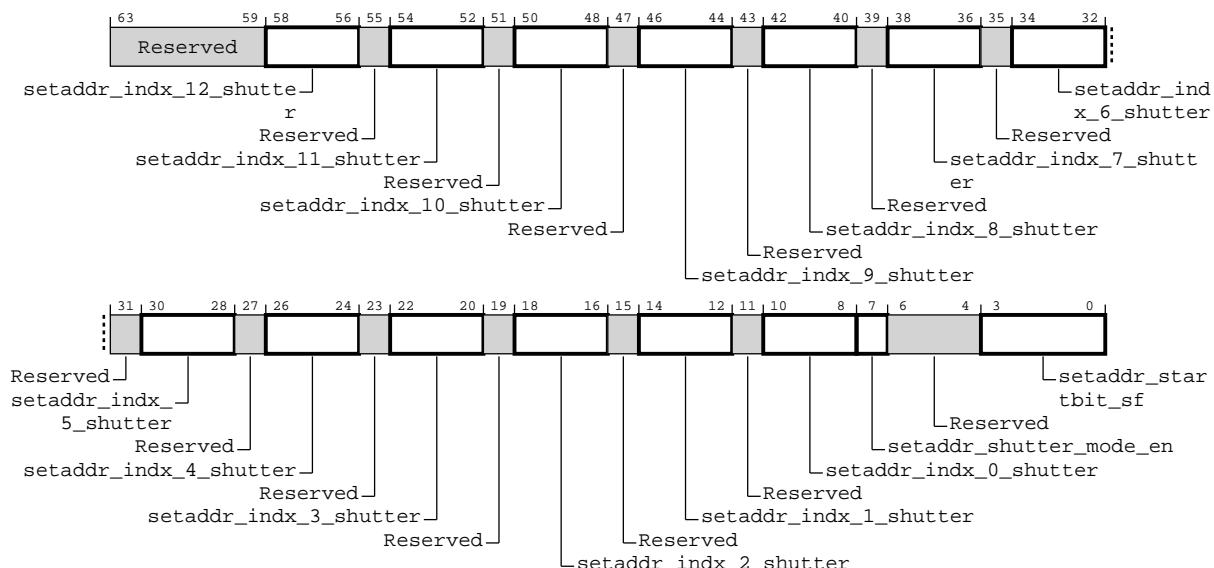


Table 4-426: cmn_hns_pa2setaddr_sf attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[58:56]	setaddr_idx_12_shutter	Program to specify address bit shuttering for setaddr index 12 from the setaddr_startbit_sf	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[55]	Reserved	Reserved	RO	-
[54:52]	setaddr_idx_11_shutter	Program to specify address bit shuttering for setaddr index 11 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[51]	Reserved	Reserved	RO	-
[50:48]	setaddr_idx_10_shutter	Program to specify address bit shuttering for setaddr index 10 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[47]	Reserved	Reserved	RO	-
[46:44]	setaddr_idx_9_shutter	Program to specify address bit shuttering for setaddr index 9 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[43]	Reserved	Reserved	RO	-
[42:40]	setaddr_idx_8_shutter	Program to specify address bit shuttering for setaddr index 8 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[39]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[38:36]	setaddr_idx_7_shutter	Program to specify address bit shuttering for setaddr index 7 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[35]	Reserved	Reserved	RO	-
[34:32]	setaddr_idx_6_shutter	Program to specify address bit shuttering for setaddr index 6 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[31]	Reserved	Reserved	RO	-
[30:28]	setaddr_idx_5_shutter	Program to specify address bit shuttering for setaddr index 5 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[27]	Reserved	Reserved	RO	-
[26:24]	setaddr_idx_4_shutter	Program to specify address bit shuttering for setaddr index 4 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[23]	Reserved	Reserved	RO	-
[22:20]	setaddr_idx_3_shutter	Program to specify address bit shuttering for setaddr index 3 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[19]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[18:16]	setaddr_idx_2_shutter	Program to specify address bit shuttering for setaddr index 2 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[15]	Reserved	Reserved	RO	-
[14:12]	setaddr_idx_1_shutter	Program to specify address bit shuttering for setaddr index 1 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[11]	Reserved	Reserved	RO	-
[10:8]	setaddr_idx_0_shutter	Program to specify address bit shuttering for setaddr index 0 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[7]	setaddr_shutter_mode_en	Enables address shuttering mode for SF as programmed by setaddr_idx_X_shutter registers	RW	1'b0
[6:4]	Reserved	Reserved	RO	-
[3:0]	setaddr_startbit_sf	SF: SetAddr starting bit for SF	RW	4'b0110
		4'b0110 Setaddr starts from PA[6] 4'b0111 Setaddr starts from PA[7] 4'b1000 Setaddr starts from PA[8] 4'b1001 Setaddr starts from PA[9] 4'b1010 Setaddr starts from PA[10] 4'b1011 Setaddr starts from PA[11] 4'b1100 Setaddr starts from PA[12]		

4.3.10.130 cmn_hns_pa2setaddr flex_slc

Functions as the SLC control register of PA to Set/TagAddr and vice versa conversion for HNS (flexible)

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5910

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.pa2setaddr_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-411: cmn_hns_pa2setaddr_flex_slc

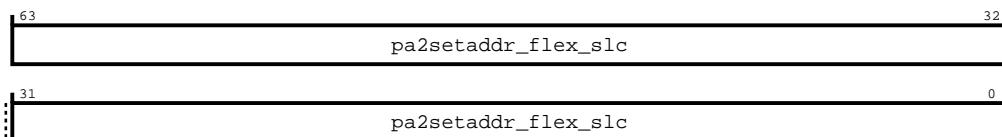


Table 4-427: cmn_hns_pa2setaddr_flex_slc attributes

Bits	Name	Description	Type	Reset
[63:0]	pa2setaddr_flex_slc	FLEXIBLE: PA to SET/TAG ADDR and vice versa conversion config field for SLC	RW	64'b0

4.3.10.131 cmn_hns_pa2setaddr_flex_sf

Functions as the SF control register of PA to Set/TagAddr and vice versa conversion for HNS (flexible)

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h5918

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.pa2setaddr_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-412: cmn_hns_pa2setaddr_flex_sf

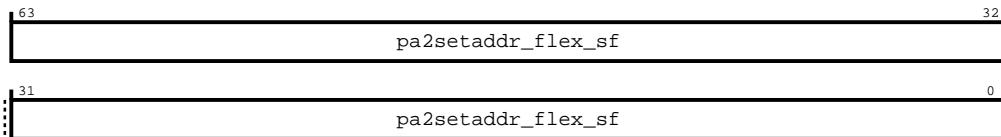


Table 4-428: cmn_hns_pa2setaddr_flex_sf attributes

Bits	Name	Description	Type	Reset
[63:0]	pa2setaddr_flex_sf	FLEXIBLE: PA to SET/TAG ADDR conversion and vice versa config field for SF	RW	64'b0

4.3.10.132 lcn_hashed_tgt_grp_cfg1_region0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h7000 + # {8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-413: lcn_hashed_tgt_grp_cfg1_region0-31

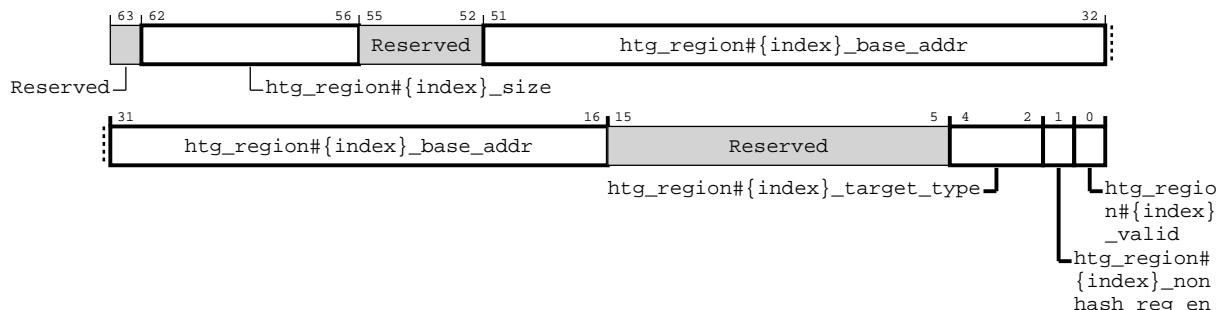


Table 4-429: lcn_hashed_tgt_grp_cfg1_region0-31 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	htg_region#{index}_size	Memory region #{index} size CONSTRANT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'b00000000
[55:52]	Reserved	Reserved	RO	-
[51:16]	htg_region#{index}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'h0
[15:5]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[4:2]	htg_region#{index}_target_type	<p>Indicates node type</p> <p>3'b000 HN-F</p> <p>3'b001 HN-I</p> <p>3'b010 CXRA</p> <p>3'b011 HN-P</p> <p>3'b100 PCI-CXRA</p> <p>3'b101 HN-S</p> <p>Others Reserved</p> <p>CONSTRAINT: Only applicable for RN-I</p>	RW	3'b000
[1]	htg_region#{index}_nonhash_reg_en	Enables hashed region #{index} to select non-hashed node	RW	1'b0
[0]	htg_region#{index}_valid	<p>Memory region #{index} valid</p> <p>1'b0 not valid</p> <p>1'b1 valid for memory region comparison</p>	RW	1'b0

4.3.10.133 lcn_hashed_tgt_grp_cfg2_region0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h7100 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-414: lcn_hashed_tgt_grp_cfg2_region0-31

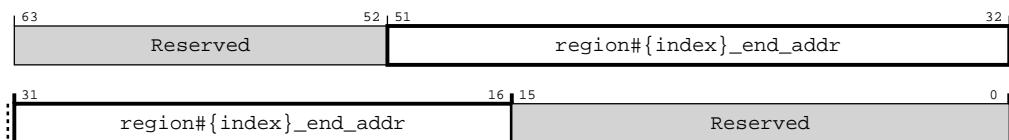


Table 4-430: lcn_hashed_tgt_grp_cfg2_region0-31 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	region#{index}_end_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'h0
[15:0]	Reserved	Reserved	RO	-

4.3.10.134 lcn_hashed_target_grp_secondary_cfg1_reg0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures secondary hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-31) : 16'h7200 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-415: lcn_hashed_target_grp_secondary_cfg1_reg0-31

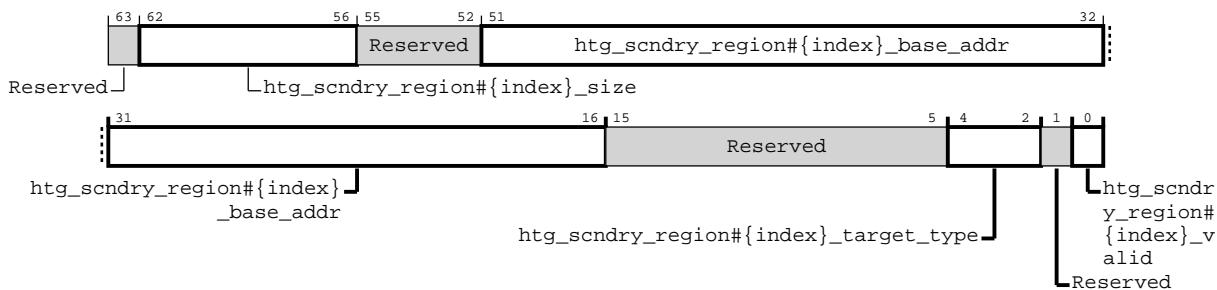


Table 4-431: lcn_hashed_target_grp_secondary_cfg1_reg0-31 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	htg_scndry_region#{index}_size	Secondary memory region #{index} size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
[55:52]	Reserved	Reserved	RO	-
[51:16]	htg_scndry_region#{index}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'h0
[15:5]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[4:2]	htg_scndry_region#{index}_target_type	Indicates node type 3'b000 HN-F 3'b001 HN-I 3'b010 CXRA 3'b011 HN-P 3'b100 PCI-CXRA 3'b101 HN-S Others Reserved CONSTRAINT: Only applicable for RN-I	RW	3'b000
[1]	Reserved	Reserved	RO	-
[0]	htg_scndry_region#{index}_valid	Secondary memory region #{index} valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.10.135 lcn_hashed_target_grp_secondary_cfg2_reg0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h7300 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-416: lcn_hashed_target_grp_secondary_cfg2_reg0-31

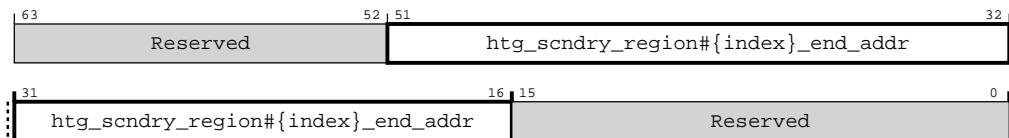


Table 4-432: lcn_hashed_target_grp_secondary_cfg2_reg0-31 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	htg_scndry_region#{index}_end_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'b00000000000000000000000000000000
[15:0]	Reserved	Reserved	RO	-

4.3.10.136 lcn_hashed_target_grp_hash_cntl_reg0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures HTG hash type

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-31) : 16'h7400 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_secure_register_groups_override.sam_control`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-417: lcn_hashed_target_grp_hash_cntl_reg0-31

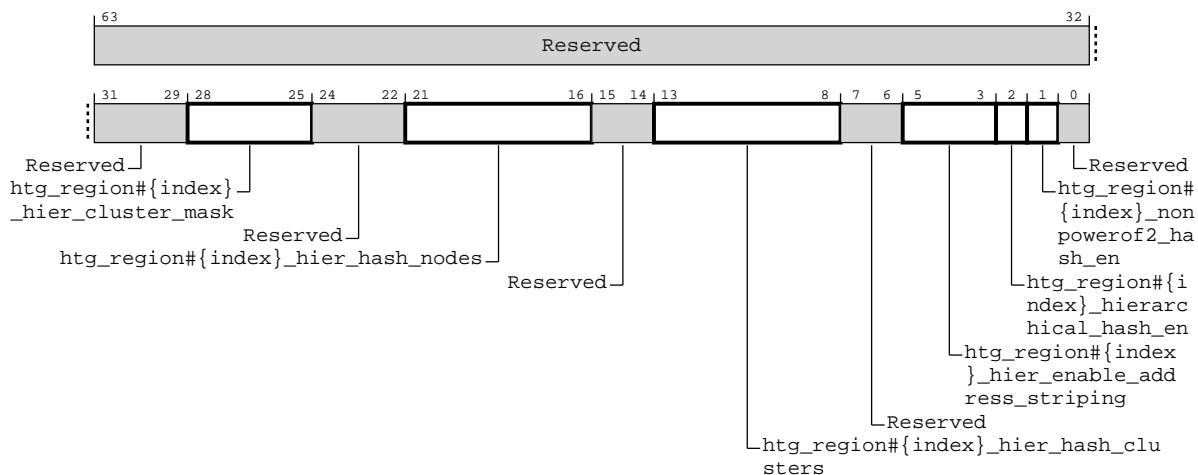


Table 4-433: lcn_hashed_target_grp_hash_cntl_reg0-31 attributes

Bits	Name	Description	Type	Reset
[63:29]	Reserved	Reserved	RO	-
[28:25]	htg_region#{index}_hier_cluster_mask	Hierarchical hashing: Enable cluster masking to achieve different interleave granularity across clusters. 4'b0000 64 byte interleave granularity across clusters 4'b0001 128 byte interleave granularity across clusters 4'b0010 256 byte interleave granularity across clusters 4'b0011 512 byte interleave granularity across clusters 4'b0100 1024 byte interleave granularity across clusters 4'b0101 2048 byte interleave granularity across clusters 4'b0110 4096 byte interleave granularity across clusters 4'b0111 8192 byte interleave granularity across clusters Others Reserved	RW	4'b0
[24:22]	Reserved	Reserved	RO	-
[21:16]	htg_region#{index}_hier_hash_nodes	Hierarchical hashing mode, define number of nodes in each cluster	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	htg_region#{index}_hier_hash_clusters	Hierarchical hashing mode, define number of clusters groups	RW	6'h0
[7:6]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[5:3]	htg_region#{index}_hier_enable_address_striping	Hierarchical hashing: configure number of address bits needs to shuttered (removed) at second hierarchy hash (LSB bit is based on cluster mask). 3'b000 No address shuttering 3'b001 One addr bit shuttered (2 clusters) 3'b010 Two addr bit shuttered (4 clusters) 3'b011 Three addr bit shuttered (8 clusters) 3'b100 Four addr bit shuttered (16 clusters) 3'b101 Five addr bit shuttered (32 clusters) Others Reserved	RW	3'b0
[2]	htg_region#{index}_hierarchical_hash_en	Hierarchical Hashing mode enable configure bit	RW	1'b0
[1]	htg_region#{index}_nonpowerof2_hash_en	Non power of two Hashing mode enable cconfigure bit	RW	1'b0
[0]	Reserved	Reserved	RO	-

4.3.10.137 lcn_hashed_target_group_hn_count_reg0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Indicates number of HN-F/HN-P's in hashed target groups #{index*8} to #{index*8 + 7}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-3) : 16'h7500 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-418: lcn_hashed_target_group_hn_count_reg0-3

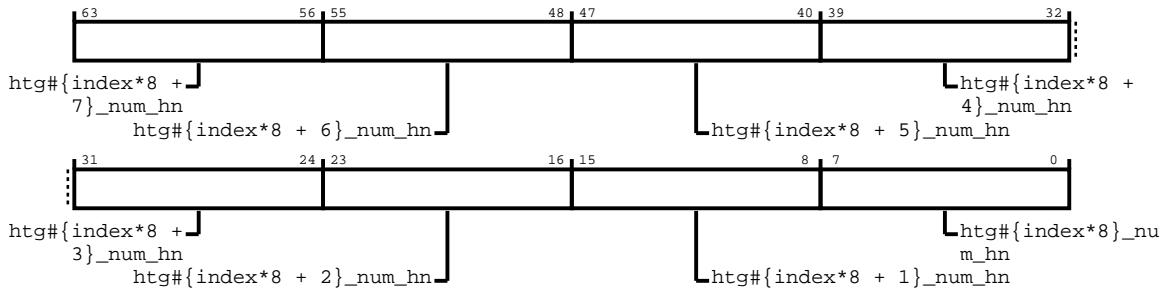


Table 4-434: lcn_hashed_target_group_hn_count_reg0-3 attributes

Bits	Name	Description	Type	Reset
[63:56]	htg#{index*8 + 7}_num_hn	HN count for hashed target group 7	RW	8'h00
[55:48]	htg#{index*8 + 6}_num_hn	HN count for hashed target group 6	RW	8'h00
[47:40]	htg#{index*8 + 5}_num_hn	HN count for hashed target group 5	RW	8'h00
[39:32]	htg#{index*8 + 4}_num_hn	HN count for hashed target group 4	RW	8'h00
[31:24]	htg#{index*8 + 3}_num_hn	HN count for hashed target group 3	RW	8'h00
[23:16]	htg#{index*8 + 2}_num_hn	HN count for hashed target group 2	RW	8'h00
[15:8]	htg#{index*8 + 1}_num_hn	HN count for hashed target group 1	RW	8'h00
[7:0]	htg#{index*8}_num_hn	HN count for hashed target group 0	RW	8'h00

4.3.10.138 lcn_hashed_target_grp_cal_mode_reg0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Configures the HN CAL mode support for all hashed target groups.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-7) : 16'h7520 + # {8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_secure_register_groups_override.sam_control

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-419: lcn_hashed_target_grp_cal_mode_reg0-7

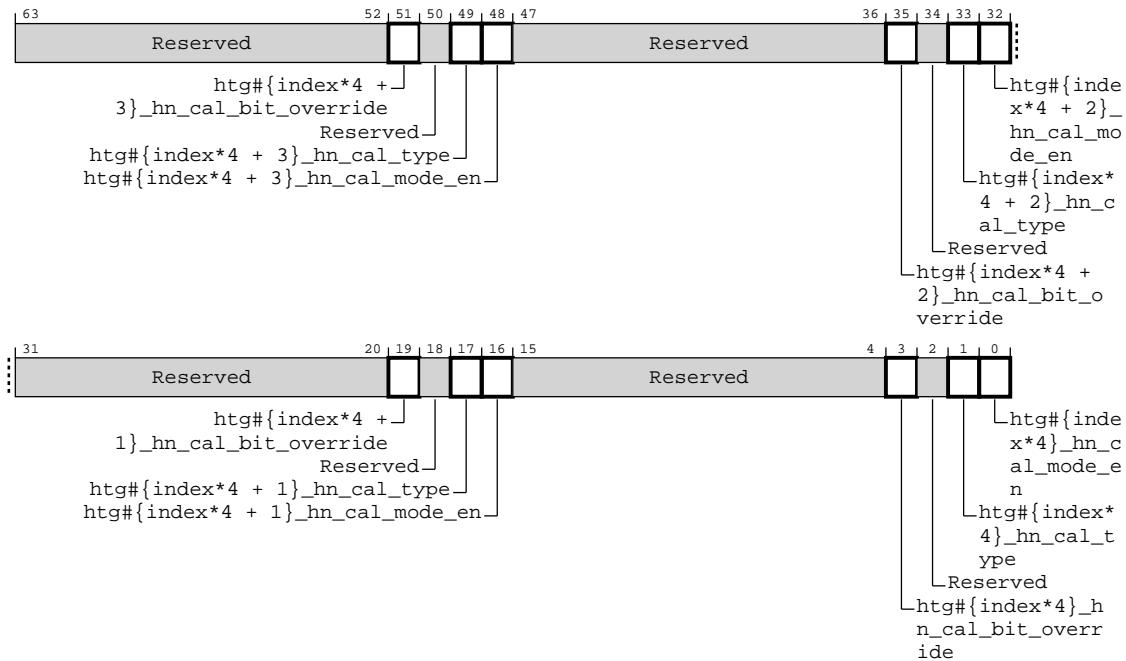


Table 4-435: lcn_hashed_target_grp_cal_mode_reg0-7 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51]	htg#[index*4 + 3]_hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #[index*4 + 3] 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[50]	Reserved	Reserved	RO	-
[49]	htg#[index*4 + 3]_hn_cal_type	Enables type of HN CAL for HTG #[index*4 + 3] 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[48]	htg#[index*4 + 3]_hn_cal_mode_en	Enables support for HN CAL for HTG #[index*4 + 3]	RW	1'b0
[47:36]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[35]	htg#[index*4 + 2]_hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #{{index}*4 + 2} 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[34]	Reserved	Reserved	RO	-
[33]	htg#[index*4 + 2]_hn_cal_type	Enables type of HN CAL for HTG #{{index}*4 + 2} 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[32]	htg#[index*4 + 2]_hn_cal_mode_en	Enables support for HN CAL for HTG #{{index}*4 + 2}	RW	1'b0
[31:20]	Reserved	Reserved	RO	-
[19]	htg#[index*4 + 1]_hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #{{index}*4 + 1} 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[18]	Reserved	Reserved	RO	-
[17]	htg#[index*4 + 1]_hn_cal_type	Enables type of HN CAL for HTG #{{index}*4 + 1} 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[16]	htg#[index*4 + 1]_hn_cal_mode_en	Enables support for HN CAL for HTG #{{index}*4 + 1}	RW	1'b0
[15:4]	Reserved	Reserved	RO	-
[3]	htg#[index*4]_hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #{{index}*4} 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[2]	Reserved	Reserved	RO	-
[1]	htg#[index*4]_hn_cal_type	Enables type of HN CAL for HTG #{{index}*4} 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[0]	htg#[index*4]_hn_cal_mode_en	Enables support for HN CAL for HTG #{{index}*4}	RW	1'b0

4.3.10.139 lcn_hashed_target_grp_hnf_cpa_en_reg0-1

There are 2 iterations of this register. The index ranges from 0 to 1. Configures CCIIX port aggregation mode for hashed HNF node IDs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-1) : 16'h7560 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-420: lcn_hashed_target_grp_hnf_cpa_en_reg0-1

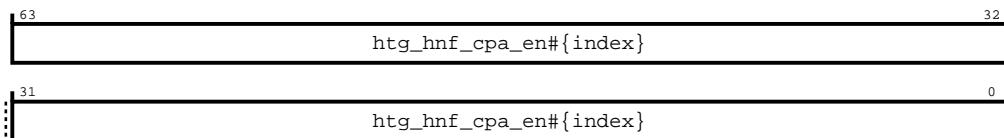


Table 4-436: lcn_hashed_target_grp_hnf_cpa_en_reg0-1 attributes

Bits	Name	Description	Type	Reset
[63:0]	htg_hnf_cpa_en#{index}	Enable CPA for each hashed HNF node ID	RW	64'h0000000000000000

4.3.10.140 lcn_hashed_target_grp_cpag_perhnf_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures CPAG ID for each hashed HNF node IDs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-15) : 16'h7580 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-421: lcn_hashed_target_grp_cpag_perhnf_reg0-15

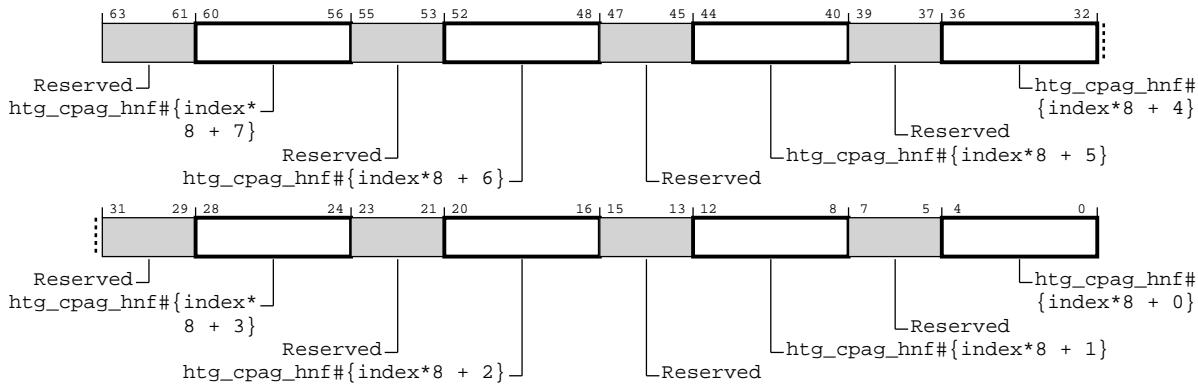


Table 4-437: lcn_hashed_target_grp_cpag_perhnf_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:61]	Reserved	Reserved	RO	-
[60:56]	htg_cpag_hnf#{index*8 + 7}	CPAG associated to the HNF#{index*8 + 7}	RW	5'b0
[55:53]	Reserved	Reserved	RO	-
[52:48]	htg_cpag_hnf#{index*8 + 6}	CPAG associated to the HNF#{index*8 + 6}	RW	5'b0
[47:45]	Reserved	Reserved	RO	-
[44:40]	htg_cpag_hnf#{index*8 + 5}	CPAG associated to the HNF#{index*8 + 5}	RW	5'b0
[39:37]	Reserved	Reserved	RO	-
[36:32]	htg_cpag_hnf#{index*8 + 4}	CPAG associated to the HNF#{index*8 + 4}	RW	5'b0
[31:29]	Reserved	Reserved	RO	-
[28:24]	htg_cpag_hnf#{index*8 + 3}	CPAG associated to the HNF#{index*8 + 3}	RW	5'b0
[23:21]	Reserved	Reserved	RO	-
[20:16]	htg_cpag_hnf#{index*8 + 2}	CPAG associated to the HNF#{index*8 + 2}	RW	5'b0
[15:13]	Reserved	Reserved	RO	-
[12:8]	htg_cpag_hnf#{index*8 + 1}	CPAG associated to the HNF#{index*8 + 1}	RW	5'b0
[7:5]	Reserved	Reserved	RO	-
[4:0]	htg_cpag_hnf#{index*8 + 0}	CPAG associated to the HNF#{index*8 + 0}	RW	5'b0

4.3.10.141 lcn_hashed_target_grp_compact_cpag_ctrl0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures the CPAG control for HTG#{index} valid only when POR_RNSAM_COMPACT_HN_TABLES_EN_PARAM == 1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h7700 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-422: lcn_hashed_target_grp_compact_cpag_ctrl0-31

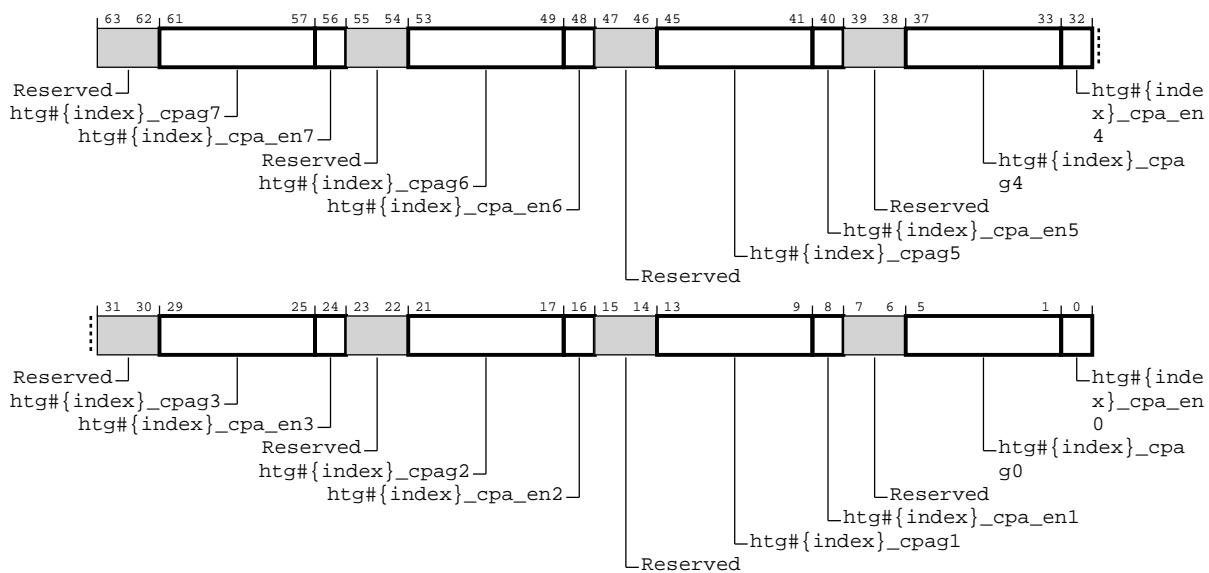


Table 4-438: lcn_hashed_target_grp_compact_cpag_ctrl0-31 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:57]	htg#{index}_cpag7	cpag id for index7	RW	5'b0
[56]	htg#{index}_cpa_en7	cpa enable for index7	RW	1'b0
[55:54]	Reserved	Reserved	RO	-
[53:49]	htg#{index}_cpag6	cpag id for index6	RW	5'b0
[48]	htg#{index}_cpa_en6	cpa enable for index6	RW	1'b0
[47:46]	Reserved	Reserved	RO	-
[45:41]	htg#{index}_cpag5	cpag id for index5	RW	5'b0
[40]	htg#{index}_cpa_en5	cpa enable for index5	RW	1'b0
[39:38]	Reserved	Reserved	RO	-
[37:33]	htg#{index}_cpag4	cpag id for index4	RW	5'b0
[32]	htg#{index}_cpa_en4	cpa enable for index4	RW	1'b0
[31:30]	Reserved	Reserved	RO	-
[29:25]	htg#{index}_cpag3	cpag id for index0	RW	5'b0
[24]	htg#{index}_cpa_en3	cpa enable for index3	RW	1'b0
[23:22]	Reserved	Reserved	RO	-
[21:17]	htg#{index}_cpag2	cpag id for index2	RW	5'b0
[16]	htg#{index}_cpa_en2	cpa enable for index2	RW	1'b0
[15:14]	Reserved	Reserved	RO	-
[13:9]	htg#{index}_cpag1	cpag id for index1	RW	5'b0
[8]	htg#{index}_cpa_en1	cpa enable for index1	RW	1'b0
[7:6]	Reserved	Reserved	RO	-
[5:1]	htg#{index}_cpag0	cpag id for index0	RW	5'b0
[0]	htg#{index}_cpa_en0	cpa enable for index0	RW	1'b0

4.3.10.142 lcn_hashed_target_grp_compact_hash_ctrl0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures the HNF hash selection and CPAG hash selection control information for HTG#{index} valid only when POR_RNSAM_COMPACT_HN_TABLES_EN_PARAM == 1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h7800 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-423: lcn_hashed_target_grp_compact_hash_ctrl0-31

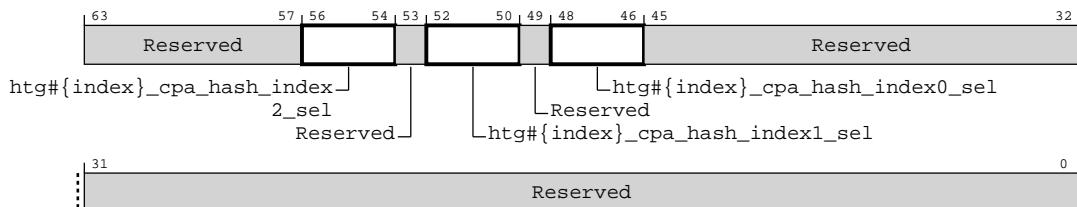


Table 4-439: lcn_hashed_target_grp_compact_hash_ctrl0-31 attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:54]	htg#{index}_cpa_hash_index2_sel	configures the CPAG hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index2. 3'b001 SMP hash index2 + 1. 3'b010 SMP hash index2 + 2. 3'b011 SMP hash index2 + 3. 3'b100 SMP hash index2 + 4. 3'b101 SMP hash index2 + 5 3'b110 SMP hash index2 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[53]	Reserved	Reserved	RO	-
[52:50]	htg#{index}_cpa_hash_index1_sel	configures the CPAG hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index1. 3'b001 SMP hash index1 + 1. 3'b010 SMP hash index1 + 2. 3'b011 SMP hash index1 + 3. 3'b100 SMP hash index1 + 4. 3'b101 SMP hash index1 + 5 3'b110 SMP hash index1 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[49]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[48:46]	htg#{index}_cpa_hash_index0_sel	<p>configures the CPAG hash selection bits from the total hnfs hash across SMP.</p> <p>3'b000 pass through from the SMP hnf_hash_index0. 3'b001 SMP hash index0 + 1. 3'b010 SMP hash index0 + 2. 3'b011 SMP hash index0 + 3. 3'b100 SMP hash index0 + 4. 3'b101 SMP hash index0 + 5 3'b110 SMP hash index0 + 6 3'b111 Hardcoded value (1'b0)</p>	RW	3'b0
[45:0]	Reserved	Reserved	RO	-

4.3.11 HN-F MPAM_NS register descriptions

This section lists the HN-F MPAM_NS registers.

4.3.11.1 cmn_hns_mpam_ns_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-424: cmn_hns_mpam_ns_node_info

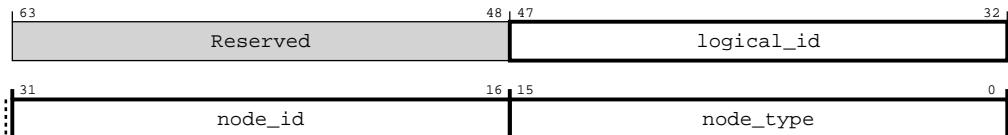


Table 4-440: cmn_hns_mpam_ns_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	\$logical_id_description	RO	Configuration dependent
[31:16]	node_id	\$node_id_description	RO	Configuration dependent
[15:0]	node_type	\$node_type_description	RO	Configuration dependent

4.3.11.2 cmn_hns_mpam_ns_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-425: cmn_hns_mpam_ns_child_info

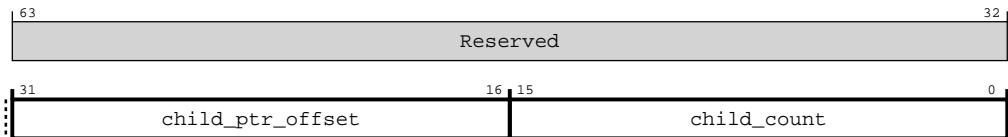


Table 4-441: cmn_hns_mpam_ns_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.11.3 cmn_hns_mpam_idr

MPAM features ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1000

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-426: cmn_hns_mpam_idr

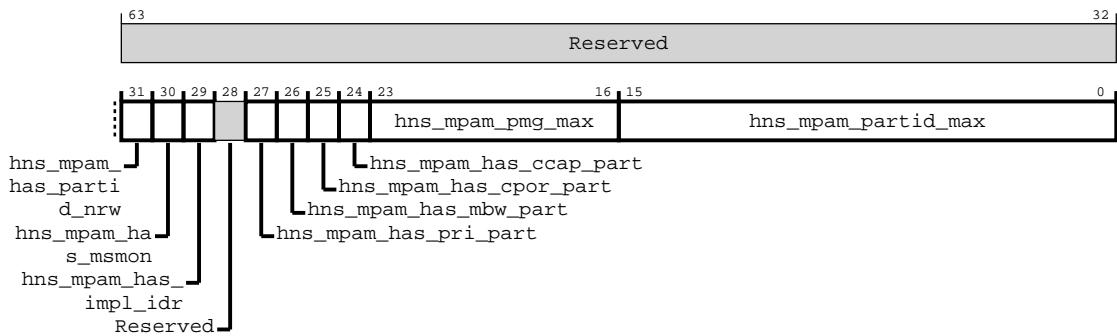


Table 4-442: cmn_hns_mpam_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_has_partid_nrw	<p>0 HN-F does not support MPAM PARTID Narrowing</p> <p>1 HN-F supports MPAM PARTID Narrowing</p>	RO	Configuration dependent
[30]	hns_mpam_has_msmon	<p>0 MPAM performance monitoring is not supported</p> <p>1 MPAM performance monitoring is supported</p>	RO	Configuration dependent
[29]	hns_mpam_has_impl_idr	<p>0 MPAM implementation specific partitioning features not supported</p> <p>1 MPAM implementation specific partitioning features supported</p>	RO	Configuration dependent
[28]	Reserved	Reserved	RO	-
[27]	hns_mpam_has_pri_part	<p>0 MPAM priority partitioning is not supported</p> <p>1 MPAM priority partitioning is supported</p>	RO	Configuration dependent
[26]	hns_mpam_has_mbw_part	<p>0 MPAM memory bandwidth partitioning is not supported</p> <p>1 MPAM memory bandwidth partitioning is supported</p>	RO	Configuration dependent
[25]	hns_mpam_has_cpor_part	<p>0 MPAM cache portion partitioning is not supported</p> <p>1 MPAM cache portion partitioning is supported</p>	RO	Configuration dependent
[24]	hns_mpam_has_ccap_part	<p>0 MPAM cache maximum capacity partitioning is not supported</p> <p>1 MPAM cache maximum capacity partitioning is supported</p>	RO	Configuration dependent
[23:16]	hns_mpam_pmg_max	Maximum value of Non-secure PMG supported by this HN-F	RO	Configuration dependent
[15:0]	hns_mpam_partid_max	Maximum value of Non-secure PARTID supported by this HN-F	RO	Configuration dependent

4.3.11.4 cmn_hns_mpam_iidr

MPAM Implementation ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1018

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-427: cmn_hns_mpam_iidr

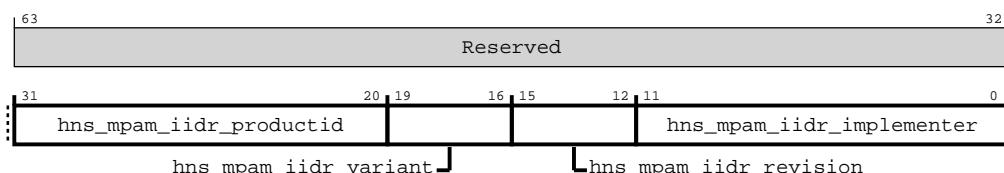


Table 4-443: cmn_hns_mpam_iidr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:20]	hns_mpam_iidr_productid	Implementation defined value identifying MPAM memory system component	RO	12'h000
[19:16]	hns_mpam_iidr_variant	Implementation defined value identifying major revision of the product	RO	4'b0000
[15:12]	hns_mpam_iidr_revision	Implementation defined value identifying minor revision of the product	RO	4'b0000
[11:0]	hns_mpam_iidr_implementer	Implementation defined value identifying company that implemented MPAM memory system component	RO	12'h43B

4.3.11.5 cmn_hns_mpam_aidr

MPAM architecture ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1020

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-428: cmn_hns_mpam_aidr

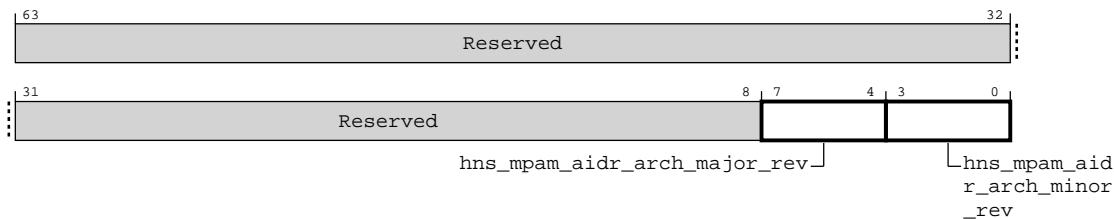


Table 4-444: cmn_hns_mpam_aidr attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7:4]	hns_mpam_aidr_arch_major_rev	Major revision of the MPAM architecture that this memory system component implements	RO	4'b0001
[3:0]	hns_mpam_aidr_arch_minor_rev	Minor revision of the MPAM architecture that this memory system component implements	RO	4'b0000

4.3.11.6 cmn_hns_mpam_impl_idr

MPAM Implementation defined partitioning feature ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1028

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-429: cmn_hns_mpam_impl_idr

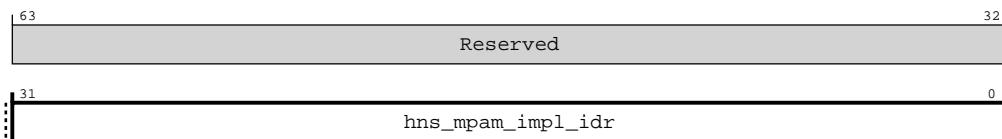


Table 4-445: cmn_hns_mpam_impl_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	hns_mpam_impl_idr	Implementation defined partitioning features.	RO	32'h00000000

4.3.11.7 cmn_hns_mpam_cpor_idr

MPAM cache portion partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1030

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-430: cmn_hns_mpam_cpor_idr

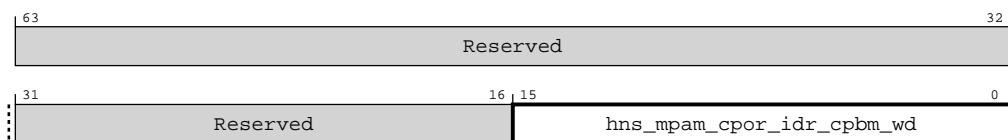


Table 4-446: cmn_hns_mpam_cpor_idr attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_cpor_idr_cpbm_wd	Number of bits in the cache portion partitioning bit map of this device.	RO	Configuration dependent

4.3.11.8 cmn_hns_mpam_ccap_idr

MPAM cache capacity partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1038

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-431: cmn_hns_mpam_ccap_idr

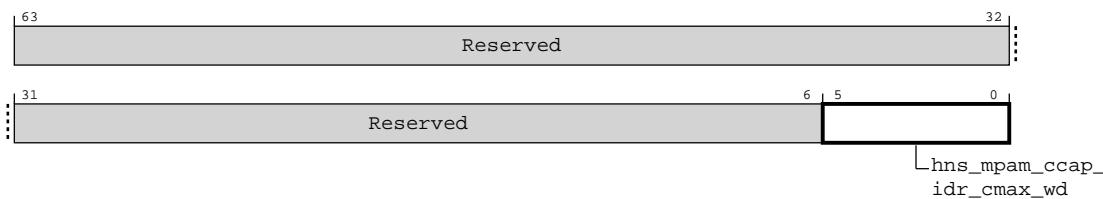


Table 4-447: cmn_hns_mpam_ccap_idr attributes

Bits	Name	Description	Type	Reset
[63:6]	Reserved	Reserved	RO	-
[5:0]	hns_mpam_ccap_idr_cmax_wd	Number of fractional bits implemented in the cache capacity partitioning.	RO	Configuration dependent

4.3.11.9 cmn_hns_mpam_mbw_idr

MPAM Memory Bandwidth partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1040

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-432: cmn_hns_mpam_mbw_idr

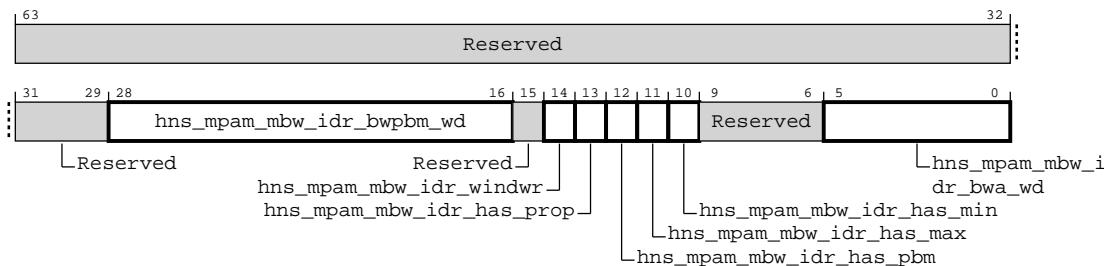


Table 4-448: cmn_hns_mpam_mbw_idr attributes

Bits	Name	Description	Type	Reset
[63:29]	Reserved	Reserved	RO	-
[28:16]	hns_mpam_mbw_idr_bwpbm_wd	Number of bits indication portions in MPAMCFG_MBW_PBM register.	RO	13'h0
[15]	Reserved	Reserved	RO	-
[14]	hns_mpam_mbw_idr_windwr	<p>0 The bandwidth accounting period should be read from MPAMCFG_MBW_WINDWR register, which might be fixed</p> <p>1 The bandwidth accounting width is readable and writable per partition in MPAMCFG_MBW_WINDWR register.</p>	RO	1'h0
[13]	hns_mpam_mbw_idr_has_prop	<p>0 There is no memory bandwidth proportional stride control and no MPAMCFG_MBW_PROP register</p> <p>1 MPAMCFG_MBW_PROP register exists and memory bandwidth proportional stride memory bandwidth allocation scheme is supported.</p>	RO	1'h0
[12]	hns_mpam_mbw_idr_has_pbm	<p>0 There is no memory bandwidth portion control and no MPAMCFG_MBW_PBM register</p> <p>1 MPAMCFG_MBW_PBM register exists and memory bandwidth portion allocation scheme is supported.</p>	RO	1'h0
[11]	hns_mpam_mbw_idr_has_max	<p>0 There is no maximum memory bandwidth control and no MPAMCFG_MBW_MAX register</p> <p>1 MPAMCFG_MBW_MAX register exists and maximum memory bandwidth allocation scheme is supported.</p>	RO	1'h0
[10]	hns_mpam_mbw_idr_has_min	<p>0 There is no minimum memory bandwidth control and no MPAMCFG_MBW_MIN register</p> <p>1 MPAMCFG_MBW_MIN register exists and minimum memory bandwidth allocation scheme is supported.</p>	RO	1'h0
[9:6]	Reserved	Reserved	RO	-
[5:0]	hns_mpam_mbw_idr_bwa_wd	Number of implemented bits in bandwidth allocation fields: MIN, MAX, and STRIDE. Value must be between 1 to 16	RO	4'b0000

4.3.11.10 cmn_hns_mpam_pri_idr

MPAM Priority partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1048

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-433: cmn_hns_mpam_pri_idr

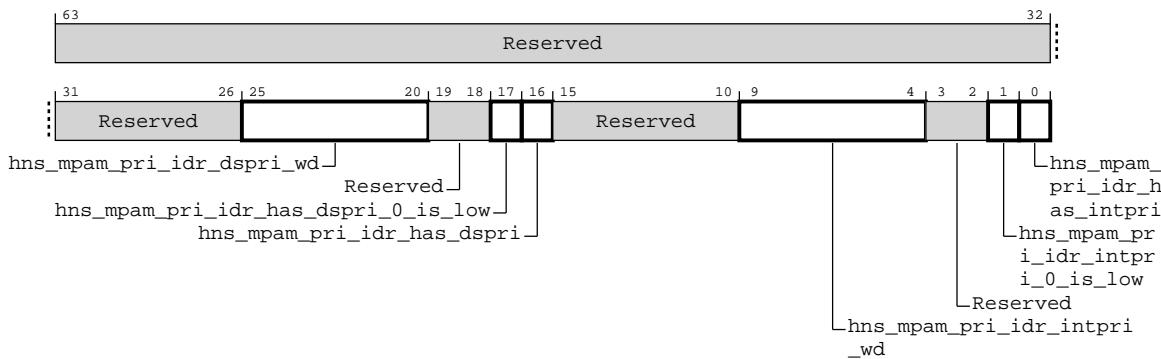


Table 4-449: cmn_hns_mpam_pri_idr attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25:20]	hns_mpam_pri_idr_dspri_wd	Number of bits in downstream priority field (DSPRI) in MPAMCFG_PRI.	RO	6'h0
[19:18]	Reserved	Reserved	RO	-
[17]	hns_mpam_pri_idr_has_dspri_0_is_low	0 In the DSPRI field, a value of 0 means highest priority 1 In the DSPRI field, a value of 0 means lowest priority.	RO	1'h0

Bits	Name	Description	Type	Reset
[16]	hns_mpam_pri_idr_has_dspri	0 This memory system component supports priority, but doesn't have a downstream priority (DSPRI) field in MPAMCFG_PRI. 1 This memory system component supports downstream priority and has an DSPRI field.	RO	1'h0
[15:10]	Reserved	Reserved	RO	-
[9:4]	hns_mpam_pri_idr_intpri_wd	Number of bits in the internal priority field (INTPRI) in MPAMCFG_PRI.	RO	6'h0
[3:2]	Reserved	Reserved	RO	-
[1]	hns_mpam_pri_idr_intpri_0_is_low	0 In the INTPRI field, a value of 0 means highest priority. 1 In the INTPRI field, a value of 0 means lowest priority.	RO	1'h0
[0]	hns_mpam_pri_idr_has_intpri	0 This memory system component supports priority, but doesn't have an internal priority field in MPAMCFG_PRI. 1 This memory system component supports internal priority and has an INTPRI field.	RO	1'h0

4.3.11.11 cmn_hns_mpam_partid_nrw_idr

MPAM PARTID narrowing ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1050

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-434: cmn_hns_mpam_partid_nrw_idr

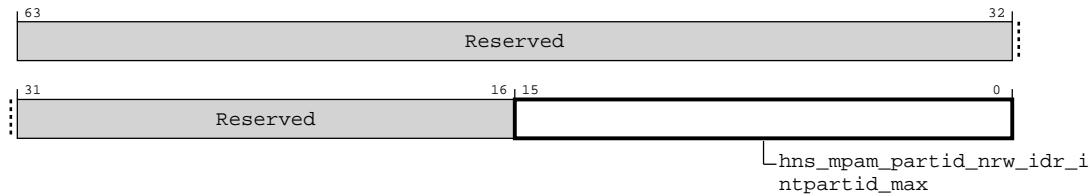


Table 4-450: cmn_hns_mpam_partid_nrw_idr attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_partid_nrw_idr_intpartid_max	This field indicates the largest intPARTID supported in this component.	RO	16'h00

4.3.11.12 cmn_hns_mpam_msmon_idr

MPAM performance monitoring ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1080

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-435: cmn_hns_mpam_msmon_idr

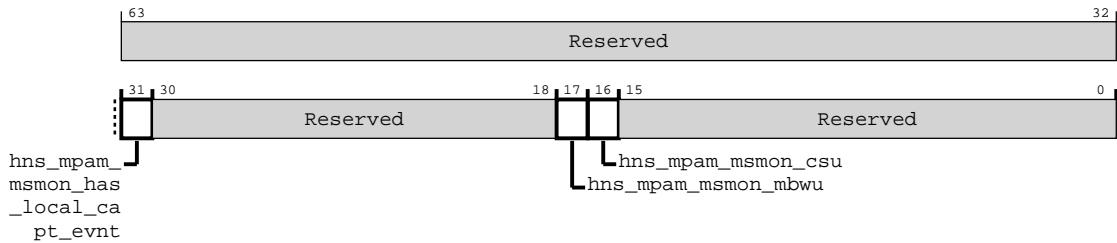


Table 4-451: cmn_hns_mpam_msmon_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_msmon_has_local_capt_evnt	Has the local capture event generator and the MSMON_CAPT_EVNT register.	RO	1'h1
[30:18]	Reserved	Reserved	RO	-
[17]	hns_mpam_msmon_mbwu	This component has a performance monitor for Memory Bandwidth Usage by PARTID and PMG.	RO	Configuration dependent
[16]	hns_mpam_msmon_csu	This component has a performance monitor for Cache Storage Usage by PARTID and PMG.	RO	Configuration dependent
[15:0]	Reserved	Reserved	RO	-

4.3.11.13 cmn_hns_mpam_csumon_idr

MPAM cache storage usage monitor ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1088

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-436: cmn_hns_mpam_csumon_idr

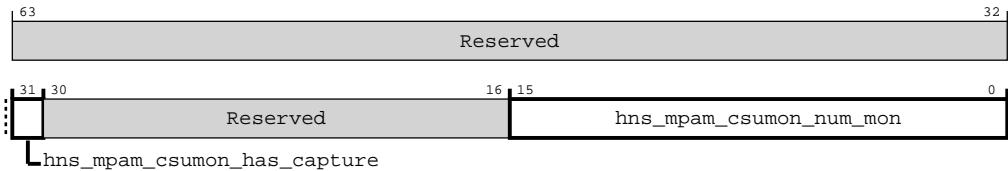


Table 4-452: cmn_hns_mpam_csumon_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_csumon_has_capture	<p>0 MSMON_CSU_CAPTURE is not implemented and there is no support for capture events in this component's CSU monitor feature</p> <p>1 This component's CSU monitor feature has an MSMON_CSU_CAPTURE register for every MSMON_CSU and supports the capture event behaviour.</p>	RO	1'h1
[30:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_csumon_num_mon	The number of CSU monitoring counters implemented in this component.	RO	Configuration dependent

4.3.11.14 cmn_hns_mpam_mbwumon_idr

MPAM memory bandwidth usage monitor ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1090

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-437: cmn_hns_mpam_mbwumon_idr

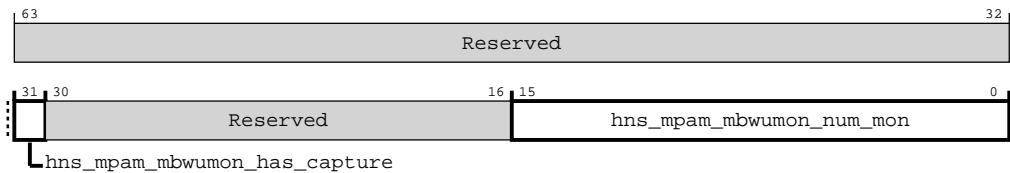


Table 4-453: cmn_hns_mpam_mbwumon_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_mbwumon_has_capture	<p>0 MSMON_MBWU_CAPTURE is not implemented and there is no support for capture events in this component's MBWU monitor feature.</p> <p>1 This component's MBWU monitor feature has an MSMON_MBWU_CAPTURE register for every MSMON_MBWU and supports the capture event behaviour.</p>	RO	1'h0
[30:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_mbwumon_num_mon	The number of MBWU monitoring counters implemented in this component.	RO	16'h0

4.3.11.15 cmn_hns_ns_mpam_ecr

MPAM Error Control Register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Note

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h10F0

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-438: cmn_hns_ns_mpam_ecr

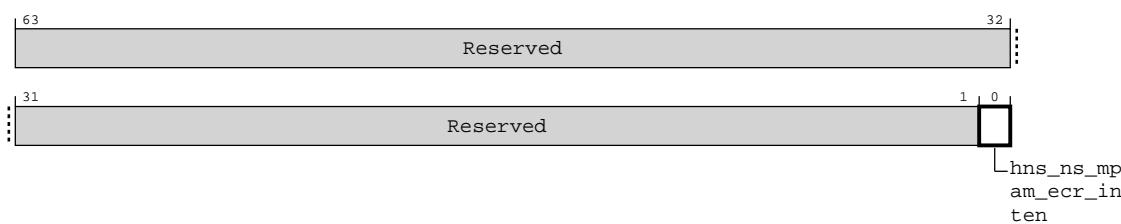


Table 4-454: cmn_hns_ns_mpam_ecr attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	hns_ns_mpam_ecr_inten	Interrupt Enable. When INTEN = 0, MPAM error interrupts are not generated. When INTEN = 1, MPAM error interrupts are generated.	RW	1'h0

4.3.11.16 cmn_hns_ns_mpam_esr

MPAM Error Status Register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h10F8

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-439: cmn_hns_ns_mpam_esr

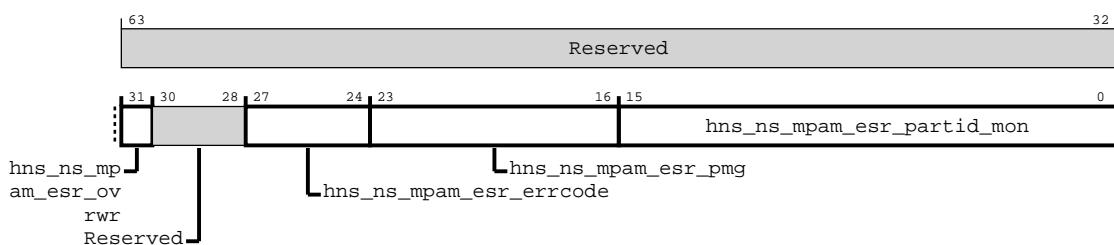


Table 4-455: cmn_hns_ns_mpam_esr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_mpam_esr_ovrwr	Overwritten. If 0 and ERRCODE is zero, no errors have occurred. If 0 and ERRCODE is non-zero, a single error has occurred and is recorded in this register. If 1 and ERRCODE is non-zero, multiple errors have occurred and this register records the most recent error. The state where this bit is 1 and ERRCODE is zero is not produced by hardware and is only reached when software writes this combination into this register.	RW	1'h0
[30:28]	Reserved	Reserved	RO	-
[27:24]	hns_ns_mpam_esr_errcode	Error code	RW	4'h0
[23:16]	hns_ns_mpam_esr_pmg	PMG captured if the error code captures PMG, otherwise 0x0000.	RW	8'h0
[15:0]	hns_ns_mpam_esr_partid_mon	PARTID captured if the error code captures PARTID. MON selector captured if the error code captures MON. Otherwise 0x0000.	RW	16'h0

4.3.11.17 cmn_hns_ns_mpamcfg_part_sel

MPAM partition configuration selection register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1100

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-440: cmn_hns_ns_mpamcfg_part_sel

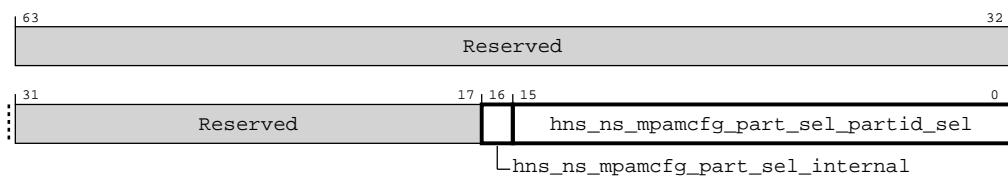


Table 4-456: cmn_hns_ns_mpamcfg_part_sel attributes

Bits	Name	Description	Type	Reset
[63:17]	Reserved	Reserved	RO	-
[16]	hns_ns_mpamcfg_part_sel_internal	If MPAMF_IDR.HAS_PARTID_NRW = 0, this field is RAZ/WI. If MPAMF_IDR.HAS_PARTID_NRW = 1, this bit decides how to interpret PARTID_SEL.	RW	1'h0
[15:0]	hns_ns_mpamcfg_part_sel_partid_sel	Selects the partition ID to configure.	RW	16'h0

4.3.11.18 cmn_hns_ns_mpamcfg_cmax

MPAM cache maximum capacity partition configuration register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1108

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-441: cmn_hns_ns_mpamcfg_cmax

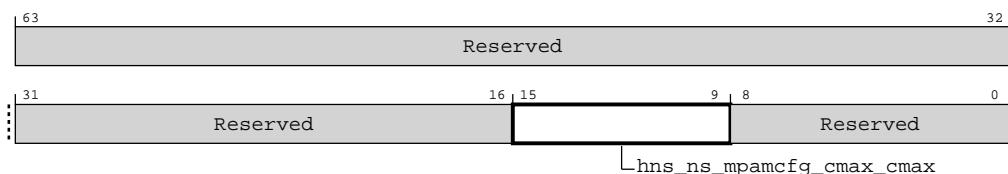


Table 4-457: cmn_hns_ns_mpamcfg_cmax attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:9]	hns_ns_mpamcfg_cmax_cmax	Maximum cache capacity usage in fixed-point fraction of the cache capacity by the partition selected by MPAMCFG_PART_SEL.	RW	7'b1111111
[8:0]	Reserved	Reserved	RO	-

4.3.11.19 cmn_hns_ns_mpamcfg_mbw_min

MPAM memory minimum bandwidth partitioning configuration register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1200

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-442: cmn_hns_ns_mpamcfg_mbw_min

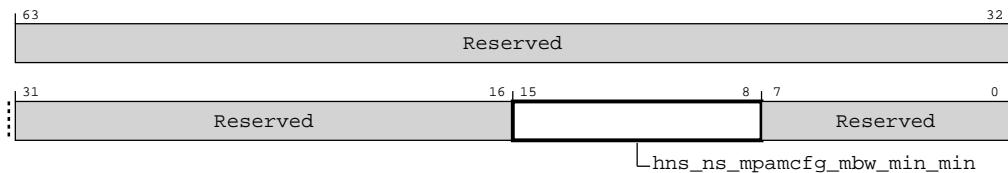


Table 4-458: cmn_hns_ns_mpamcfg_mbw_min attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:8]	hns_ns_mpamcfg_mbw_min_min	Memory minimum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
[7:0]	Reserved	Reserved	RO	-

4.3.11.20 cmn_hns_ns_mpamcfg_mbw_max

MPAM memory maximum bandwidth partitioning configuration register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1208

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-443: cmn_hns_ns_mpamcfg_mbw_max

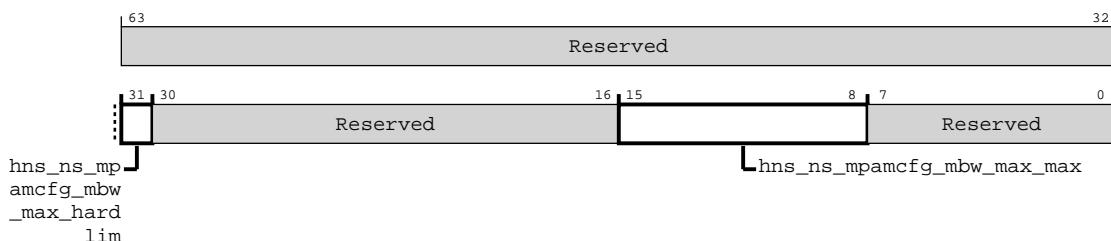


Table 4-459: cmn_hns_ns_mpamcfg_mbw_max attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	<code>hns_ns_mpamcfg_mbw_max_hardlim</code>	<p>0 When MAX bandwidth is exceeded, the partition may contend with a low preference for downstream bandwidth beyond its maximum bandwidth</p> <p>1 When MAX bandwidth is exceeded, the partition may not be use any more bandwidth until its memory bandwidth measurement falls below the maximum limit.</p>	RW	1'h0
[30:16]	Reserved	Reserved	RO	-
[15:8]	<code>hns_ns_mpamcfg_mbw_max_max</code>	Memory maximum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
[7:0]	Reserved	Reserved	RO	-

4.3.11.21 cmn_hns_ns_mpamcfg_mbw_winwd

MPAM memory bandwidth partitioning window width register.



Note This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1220

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-444: cmn_hns_ns_mpamcfg_mbw_winwd

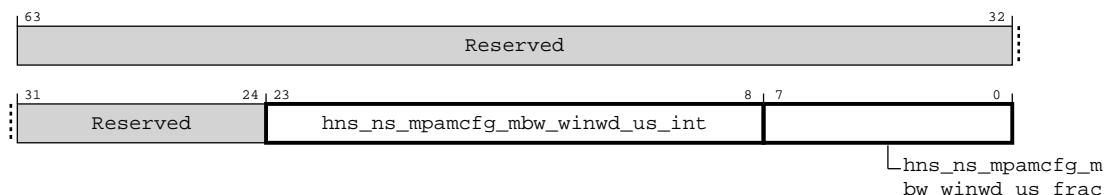


Table 4-460: cmn_hns_ns_mpamcfg_mbw_winwd attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:8]	hns_ns_mpamcfg_mbw_winwd_us_int	Memory bandwidth accounting period integer microseconds.	RW	16'h0
[7:0]	hns_ns_mpamcfg_mbw_winwd_us_frac	Memory bandwidth accounting period fractions of a microsecond.	RW	8'h0

4.3.11.22 cmn_hns_ns_mpamcfg_pri

MPAM priority partitioning configuration register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1400

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-445: cmn_hns_ns_mpamcfg_pri

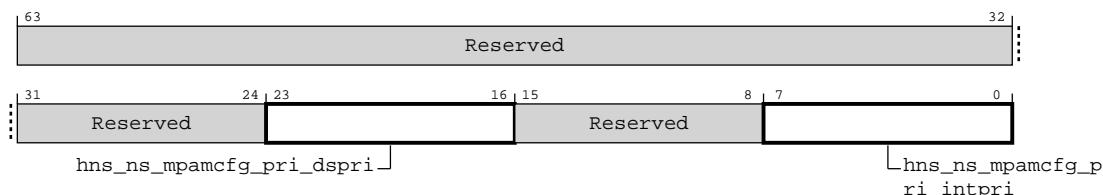


Table 4-461: cmn_hns_ns_mpamcfg_pri attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	hns_ns_mpamcfg_pri_dspri	If HAS_DSPRI is 1, this field is a priority value applied to downstream communications from this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
[15:8]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[7:0]	hns_ns_mpamcfg_pri_intpri	If HAS_INTPRI is 1, this field is a priority value applied internally inside this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0

4.3.11.23 cmn_hns_ns_mpamcfg_mbw_prop

Memory bandwidth proportional stride partitioning configuration register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1500

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-446: cmn_hns_ns_mpamcfg_mbw_prop

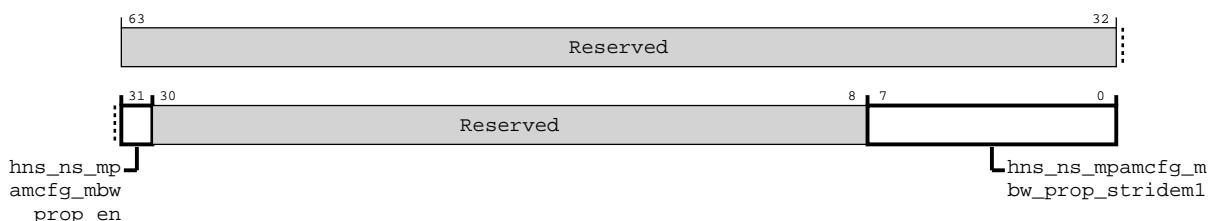


Table 4-462: cmn_hns_ns_mpamcfg_mbw_prop attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_mpamcfg_mbw_prop_en	<p>0 The selected partition is not regulated by proportional stride bandwidth partitioning.</p> <p>1 The selected partition has bandwidth usage regulated by proportional stride bandwidth partitioning as controlled by STRIDEM1.</p>	RW	1'h0
[30:8]	Reserved	Reserved	RO	-
[7:0]	hns_ns_mpamcfg_mbw_prop_stridem1	Normalized cost of a bandwidth consumption by the partition. STRIDEM1 is the stride for the partition minus one.	RW	8'h0

4.3.11.24 cmn_hns_ns_mpamcfg_intpartid

MPAM internal partition narrowing configuration register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1600

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-447: cmn_hns_ns_mpamcfg_intpartid

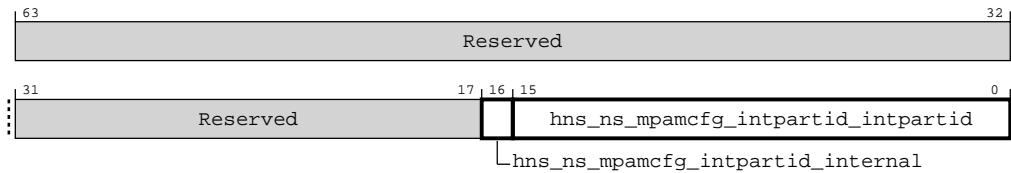


Table 4-463: cmn_hns_ns_mpamcfg_intpartid attributes

Bits	Name	Description	Type	Reset
[63:17]	Reserved	Reserved	RO	-
[16]	hns_ns_mpamcfg_intpartid_internal	This bit must be 1 when written to the register. If written as 0, the write will not update the reqPARTID to intPARTID association.	RW	1'h0
[15:0]	hns_ns_mpamcfg_intpartid_intpartid	This field contains the intPARTID mapped to the reqPARTID in MPAMCFG_PART_SEL.	RW	16'h0

4.3.11.25 cmn_hns_ns_msmon_cfg_mon_sel

Memory system performance monitor selection register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1800

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-448: cmn_hns_ns_msmon_cfg_mon_sel

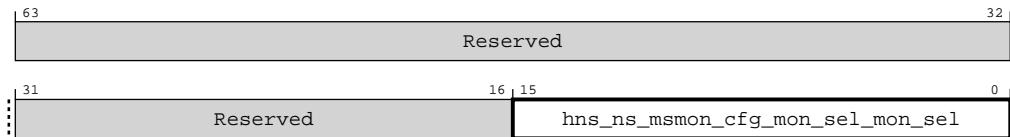


Table 4-464: cmn_hns_ns_msmon_cfg_mon_sel attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_ns_msmon_cfg_mon_sel_mon_sel	Selects the performance monitor to configure.	RW	16'h0

4.3.11.26 cmn_hns_ns_msmon_capt_evnt

Memory system performance monitoring capture event generation register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1808

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-449: cmn_hns_ns_msmon_capt_evnt

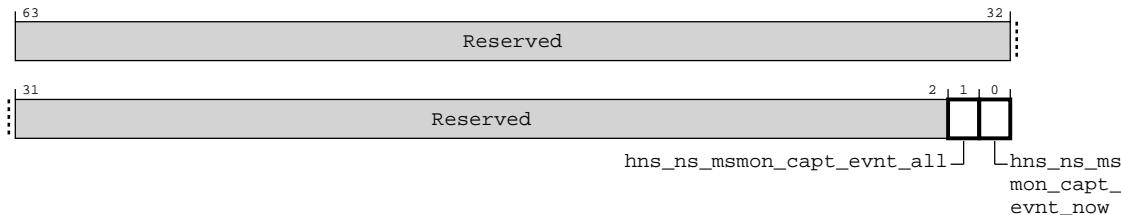


Table 4-465: cmn_hns_ns_msmon_capt_evnt attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	hns_ns_msmon_capt_evnt_all	In Secure version, if ALL written as 1 and NOW is also written as 1, signal a capture event to Secure and Non-secure monitors in this memory system component with CAPT_EVNT = 7. If written as 0 and NOW is written as 1, signal a capture event to Secure monitors in this memory system component with CAPT_EVNT = 7. In Non-secure version if NOW is written as 1, signal a capture event to Non-secure monitors in this memory system component with CAPT_EVNT = 7.	RW	1'h0
[0]	hns_ns_msmon_capt_evnt_now	When written as 1, this bit causes an event to all monitors in this memory system component with CAPT_EVNT set to the value of 7. When this bit is written as 0, no event is signalled.	RW	1'h0

4.3.11.27 cmn_hns_ns_msmon_cfg_csu_filt

Memory system performance monitor configure cache storage usage monitor filter register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1810

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-450: cmn_hns_ns_msmon_cfg_csu_flt

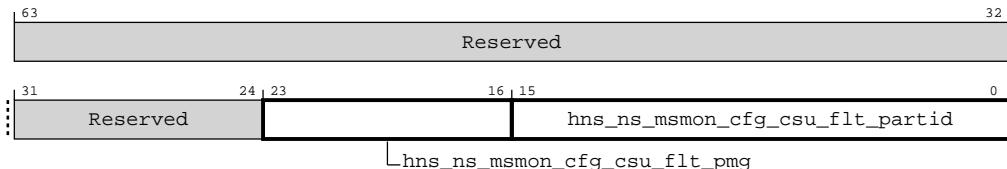


Table 4-466: cmn_hns_ns_msmon_cfg_csu_flt attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	hns_ns_msmon_cfg_csu_flt_pmg	Configures the cache storage usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	8'h0
[15:0]	hns_ns_msmon_cfg_csu_flt_partid	Configures the cache storage usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	16'h0

4.3.11.28 cmn_hns_ns_msmon_cfg_csu_ctl

Memory system performance monitor configure cache storage usage monitor control register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1818

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-451: cmn_hns_ns_msmon_cfg_csu_ctl

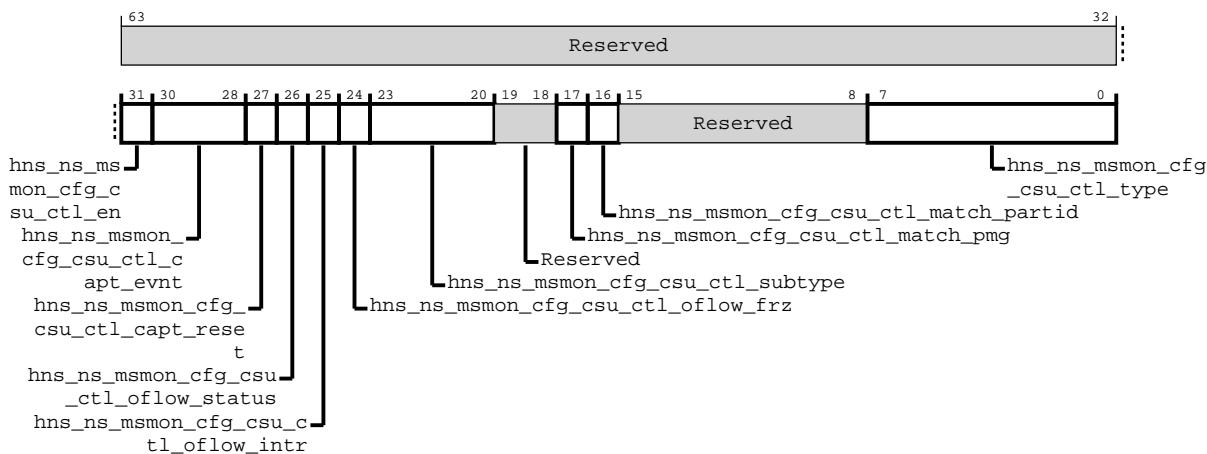


Table 4-467: cmn_hns_ns_msmon_cfg_csu_ctl attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_msmon_cfg_csu_ctl_en	<p>0 The monitor is disabled and must not collect any information.</p> <p>1 The monitor is enabled to collect information according to its configuration.</p>	RW	1'h0
[30:28]	hns_ns_msmon_cfg_csu_ctl_capt_evnt	Select the event that triggers capture from the following:	RW	3'h0
		<p>0 No capture event is triggered</p> <p>1 External capture event 1 (optional but recommended)</p>		
[27]	hns_ns_msmon_cfg_csu_ctl_capt_reset	Capture is not implemented for the CSU monitor type.	RW	1'h0
[26]	hns_ns_msmon_cfg_csu_ctl_oflow_status	<p>0 No overflow has occurred</p> <p>1 At least one overflow has occurred since this bit was last written.</p>	RW	1'h0
[25]	hns_ns_msmon_cfg_csu_ctl_oflow_intr	<p>0 No interrupt.</p> <p>1 On overflow, an implementation-specific interrupt is signalled.</p>	RW	1'h0

Bits	Name	Description	Type	Reset
[24]	hns_ns_msmon_cfg_csu_ctl_oflow_frz	0 Monitor count wraps on overflow. 1 Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1	RW	1'h0
[23:20]	hns_ns_msmon_cfg_csu_ctl_subtype	Not currently used for CSU monitors, but reserved for future use.	RW	4'h0
[19:18]	Reserved	Reserved	RO	-
[17]	hns_ns_msmon_cfg_csu_ctl_match_pmg	0 Monitor storage used by all PMG values. 1 Only monitor storage used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0
[16]	hns_ns_msmon_cfg_csu_ctl_match_partid	0 Monitor storage used by all PARTIDs. 1 Only monitor storage used with the PARTID matching MSMON_CFG_CSU_FLT.PARTID.	RW	1'h0
[15:8]	Reserved	Reserved	RO	-
[7:0]	hns_ns_msmon_cfg_csu_ctl_type	Read-only: Constant type indicating the type of the monitor. CSU monitor is TYPE = 0x43.	RW	8'h43

4.3.11.29 cmn_hns_ns_msmon_cfg_mbwu_filt

Memory system performance monitor configure memory bandwidth usage monitor filter register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1820

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-452: cmn_hns_ns_msmon_cfg_mbwu_flt

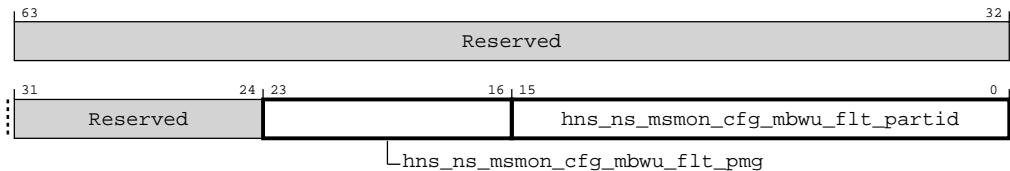


Table 4-468: cmn_hns_ns_msmon_cfg_mbwu_flt attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	hns_ns_msmon_cfg_mbwu_flt_pmg	Configures the memory bandwidth usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	8'h0
[15:0]	hns_ns_msmon_cfg_mbwu_flt_partid	Configures the memory bandwidth usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	16'h0

4.3.11.30 cmn_hns_ns_msmon_cfg_mbwu_ctl

Memory system performance monitor configure memory bandwidth usage monitor control register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1828

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-453: cmn_hns_ns_msmon_cfg_mbwu_ctl

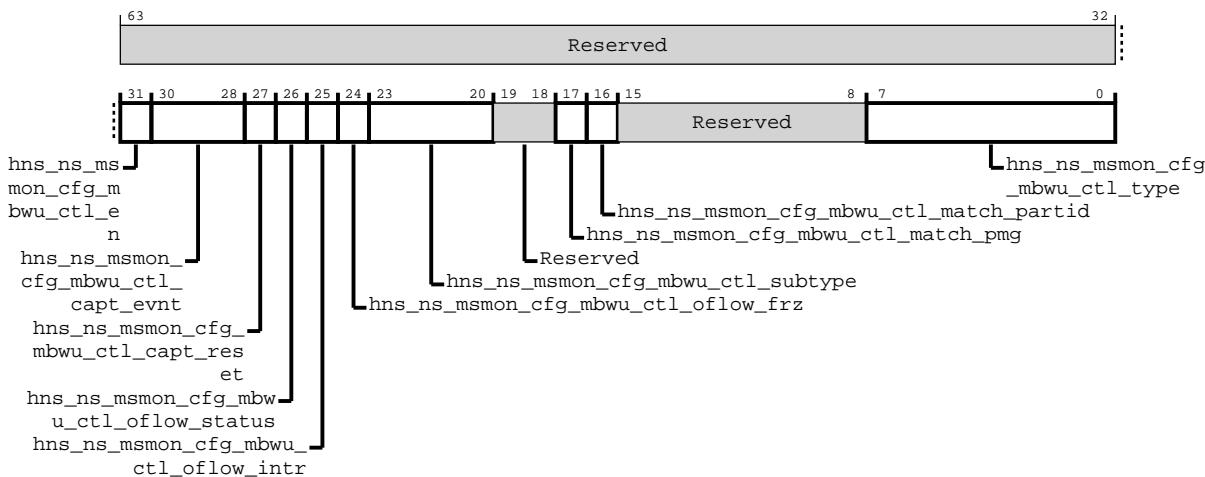


Table 4-469: cmn_hns_ns_msmon_cfg_mbwu_ctl attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_msmon_cfg_mbwu_ctl_en	0 The monitor is disabled and must not collect any information. 1 The monitor is enabled to collect information according to its configuration.	RW	1'h0
[30:28]	hns_ns_msmon_cfg_mbwu_ctl_capt_evnt	Select the event that triggers capture from the following: 0: No capture event is triggered 1: External capture event 1 (optional but recommended)	RW	3'h0
[27]	hns_ns_msmon_cfg_mbwu_ctl_capt_reset	0: Monitor is not reset on capture. 1: Monitor is reset on capture.	RW	1'h0
[26]	hns_ns_msmon_cfg_mbwu_ctl_oflow_status	0: No overflow has occurred 1: At least one overflow has occurred since this bit was last written.	RW	1'h0
[25]	hns_ns_msmon_cfg_mbwu_ctl_oflow_intr	0: No interrupt. 1: On overflow, an implementation-specific interrupt is signalled.	RW	1'h0
[24]	hns_ns_msmon_cfg_mbwu_ctl_oflow_frz	0: Monitor count wraps on overflow. 1: Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1	RW	1'h0
[15:8]	hns_ns_msmon_cfg_mbwu_ctl_type	hns_ns_msmon_cfg_mbwu_ctl_match_partid hns_ns_msmon_cfg_mbwu_ctl_match_pmg hns_ns_msmon_cfg_mbwu_ctl_subtype hns_ns_msmon_cfg_mbwu_ctl_oflow_frz		
[7:0]	hns_ns_msmon_cfg_mbwu_ctl_oflow_intr	hns_ns_msmon_cfg_mbwu_ctl_oflow_intr		

Bits	Name	Description	Type	Reset
[23:20]	hns_ns_msmon_cfg_mbwu_ctl_subtype	A monitor can have other event matching criteria. The meaning of values in this field varies by monitor type. The MBWU monitor type supports: 0 Do not count any bandwidth. 1 Count bandwidth used by memory reads 2 Count bandwidth used by memory writes 3 Count bandwidth used by memory reads and memory writes All other values are reserved and behaviour of a monitor with SUBTYPE set to one of the reserved values is UNPREDICTABLE.	RW	4'h0
[19:18]	Reserved	Reserved	RO	-
[17]	hns_ns_msmon_cfg_mbwu_ctl_match_pmg	0 Monitor bandwidth used by all PMG values. 1 Only monitor bandwidth used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0
[16]	hns_ns_msmon_cfg_mbwu_ctl_match_partid	0 Monitor bandwidth used by all PARTIDs 1 Only monitor bandwidth used with the PARTID matching MSMON_CFG_MBWU_FLT.PARTID.	RW	1'h0
[15:8]	Reserved	Reserved	RO	-
[7:0]	hns_ns_msmon_cfg_mbwu_ctl_type	Read-only: Constant type indicating the type of the monitor. MBWU monitor is TYPE = 0x42.	RW	8'h42

4.3.11.31 cmn_hns_ns_msmon_csu

Memory system performance monitor cache storage usage monitor register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1840

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-454: cmn_hns_ns_msmon_csu

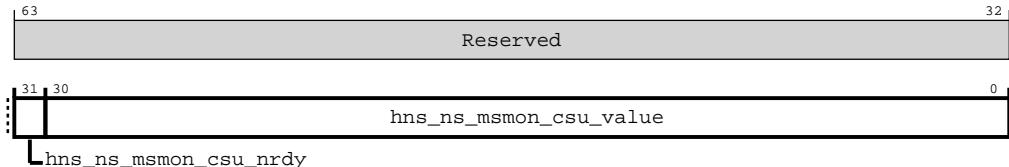


Table 4-470: cmn_hns_ns_msmon_csu attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_msmon_csu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_ns_msmon_csu_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

4.3.11.32 cmn_hns_ns_msmon_csu_capture

Memory system performance monitor cache storage usage capture register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1848

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-455: cmn_hns_ns_msmon_csu_capture

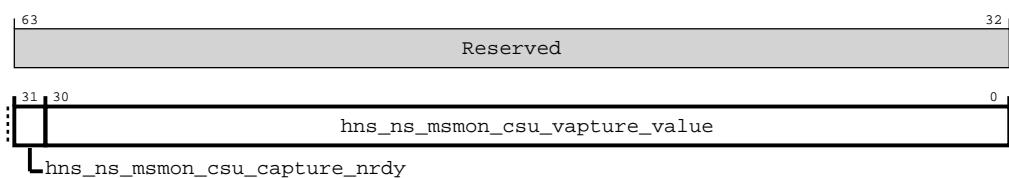


Table 4-471: cmn_hns_ns_msmon_csu_capture attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_msmon_csu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_ns_msmon_csu_vapture_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

4.3.11.33 cmn_hns_ns_msmon_mbwu

Memory system performance monitor memory bandwidth usage monitor register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1860

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-456: cmn_hns_ns_msmon_mbwu

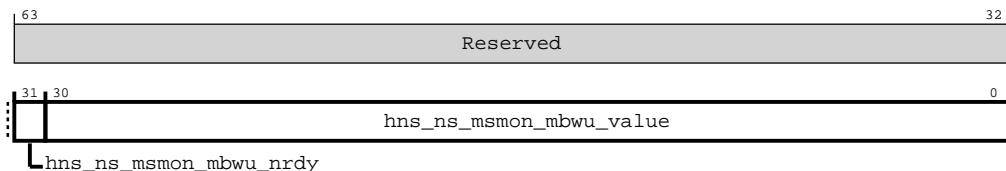


Table 4-472: cmn_hns_ns_msmon_mbwu attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_msmon_mbwu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_ns_msmon_mbwu_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

4.3.11.34 cmn_hns_ns_msmon_mbwu_capture

Memory system performance monitor memory bandwidth usage capture register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1868

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-457: cmn_hns_ns_msmon_mbwu_capture

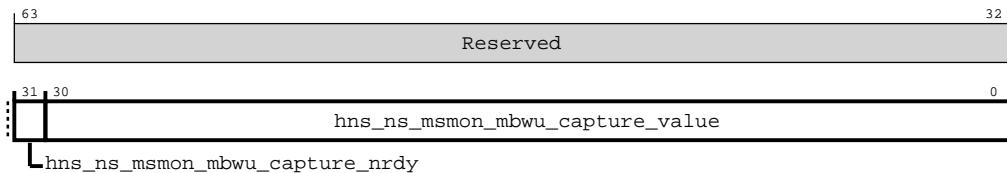


Table 4-473: cmn_hns_ns_msmon_mbwu_capture attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_ns_msmon_mbwu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_ns_msmon_mbwu_capture_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

4.3.11.35 cmn_hns_ns_mpamcfg_cpbm

MPAM cache portion bitmap partition configuration register.



This register is unique for cmn_hns_ns. There is also similar but distinct register available in cmn_hns_s.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-458: cmn_hns_ns_mpamcfg_cpbm

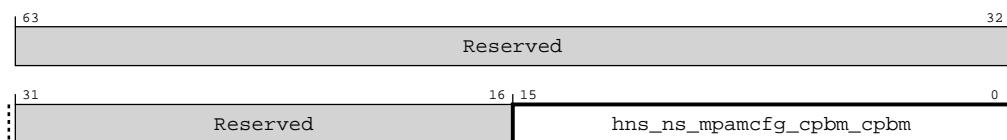


Table 4-474: cmn_hns_ns_mpamcfg_cpbm attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_ns_mpamcfg_cpbm_cpbm	Bitmap of portions of cache capacity allocable by the partition selected by MPAMCFG_PART_SEL. NOTE: CPBM can not be all zeros for any PARTID.	RW	16'hFFFF

4.3.12 HN-F MPAM_S register descriptions

This section lists the HN-F MPAM_S registers.

4.3.12.1 cmn_hns_mpam_s_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-459: cmn_hns_mpam_s_node_info

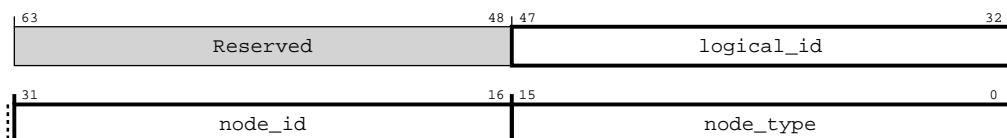


Table 4-475: cmn_hns_mpam_s_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	\$logical_id_description	RO	Configuration dependent
[31:16]	node_id	\$node_id_description	RO	Configuration dependent
[15:0]	node_type	\$node_type_description	RO	Configuration dependent

4.3.12.2 cmn_hns_mpam_s_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-460: cmn_hns_mpam_s_child_info

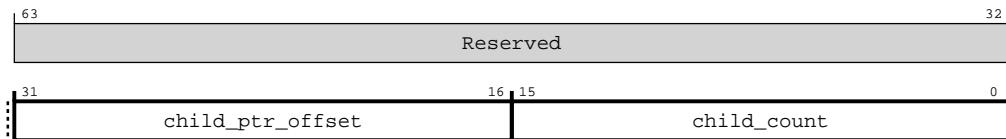


Table 4-476: cmn_hns_mpam_s_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.12.3 cmn_hns_mpam_s_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-461: cmn_hns_mpam_s_secure_register_groups_override

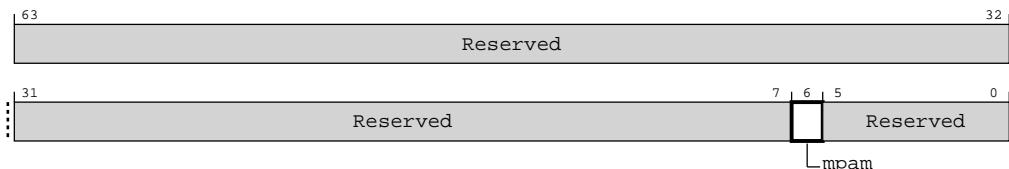


Table 4-477: cmn_hns_mpam_s_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6]	mpam	Allows Non-secure access to Secure MPAM registers	RW	1'b0
[5:0]	Reserved	Reserved	RO	-

4.3.12.4 cmn_hns_s_mpam_idr

MPAM features ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1000

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-462: cmn_hns_s_mpam_idr

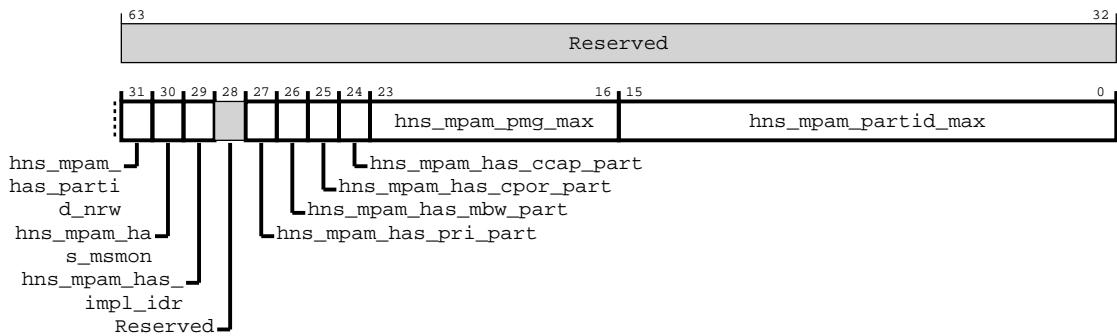


Table 4-478: cmn_hns_s_mpam_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_has_partid_nrw	<p>0 HN-F does not support MPAM PARTID Narrowing</p> <p>1 HN-F supports MPAM PARTID Narrowing</p>	RO	Configuration dependent
[30]	hns_mpam_has_msmon	<p>0 MPAM performance monitoring is not supported</p> <p>1 MPAM performance monitoring is supported</p>	RO	Configuration dependent
[29]	hns_mpam_has_impl_idr	<p>0 MPAM implementation specific partitioning features not supported</p> <p>1 MPAM implementation specific partitioning features supported</p>	RO	Configuration dependent
[28]	Reserved	Reserved	RO	-
[27]	hns_mpam_has_pri_part	<p>0 MPAM priority partitioning is not supported</p> <p>1 MPAM priority partitioning is supported</p>	RO	Configuration dependent
[26]	hns_mpam_has_mbw_part	<p>0 MPAM memory bandwidth partitioning is not supported</p> <p>1 MPAM memory bandwidth partitioning is supported</p>	RO	Configuration dependent
[25]	hns_mpam_has_cpor_part	<p>0 MPAM cache portion partitioning is not supported</p> <p>1 MPAM cache portion partitioning is supported</p>	RO	Configuration dependent
[24]	hns_mpam_has_ccap_part	<p>0 MPAM cache maximum capacity partitioning is not supported</p> <p>1 MPAM cache maximum capacity partitioning is supported</p>	RO	Configuration dependent
[23:16]	hns_mpam_pmg_max	Maximum value of Non-secure PMG supported by this HN-F	RO	Configuration dependent
[15:0]	hns_mpam_partid_max	Maximum value of Non-secure PARTID supported by this HN-F	RO	Configuration dependent

4.3.12.5 cmn_hns_mpam_sidr

MPAM features Secure ID register. This is Secure (S) register only.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1008

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-463: cmn_hns_mpam_sidr

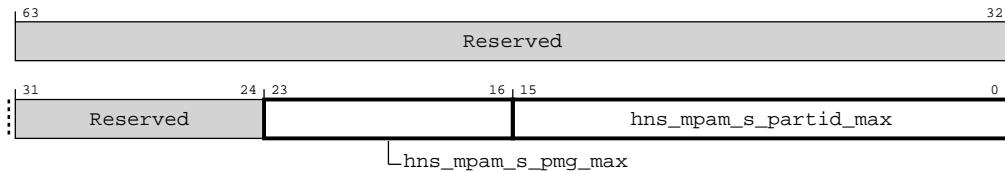


Table 4-479: cmn_hns_mpam_sidr attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	hns_mpam_s_pmg_max	Maximum value of Secure PMG supported by this HN-F	RO	Configuration dependent
[15:0]	hns_mpam_s_partid_max	Maximum value of Secure PARTID supported by this HN-F	RO	Configuration dependent

4.3.12.6 cmn_hns_s_mpam_iidr

MPAM Implementation ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1018

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-464: cmn_hns_s_mpam_iidr

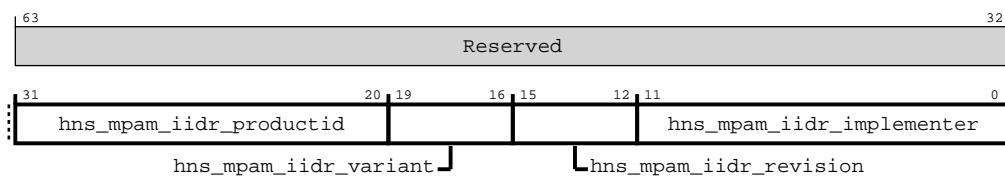


Table 4-480: cmn_hns_s_mpam_iidr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:20]	hns_mpam_iidr_productid	Implementation defined value identifying MPAM memory system component	RO	12'h000
[19:16]	hns_mpam_iidr_variant	Implementation defined value identifying major revision of the product	RO	4'b0000
[15:12]	hns_mpam_iidr_revision	Implementation defined value identifying minor revision of the product	RO	4'b0000
[11:0]	hns_mpam_iidr_implementer	Implementation defined value identifying company that implemented MPAM memory system component	RO	12'h43B

4.3.12.7 cmn_hns_s_mpam_aidr

MPAM architecture ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1020

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-465: cmn_hns_s_mpam_aidr

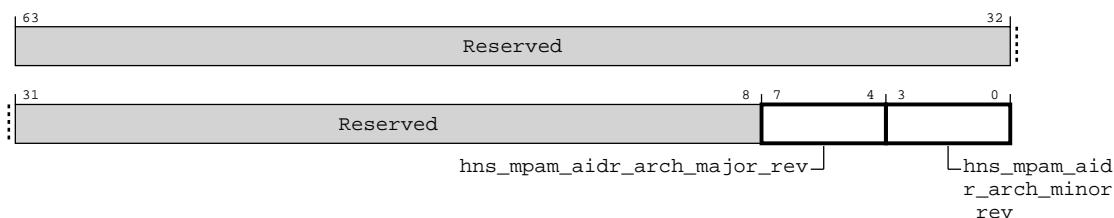


Table 4-481: cmn_hns_s_mpam_aidr attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7:4]	hns_mpam_aidr_arch_major_rev	Major revision of the MPAM architecture that this memory system component implements	RO	4'b0001
[3:0]	hns_mpam_aidr_arch_minor_rev	Minor revision of the MPAM architecture that this memory system component implements	RO	4'b0000

4.3.12.8 cmn_hns_s_mpam_impl_idr

MPAM Implementation defined partitioning feature ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1028

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-466: cmn_hns_s_mpam_impl_idr

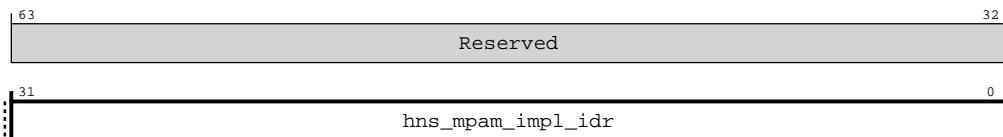


Table 4-482: cmn_hns_s_mpam_impl_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	hns_mpam_impl_idr	Implementation defined partitioning features.	RO	32'h00000000

4.3.12.9 cmn_hns_s_mpam_cpor_idr

MPAM cache portion partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1030

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-467: cmn_hns_s_mpam_cpor_idr

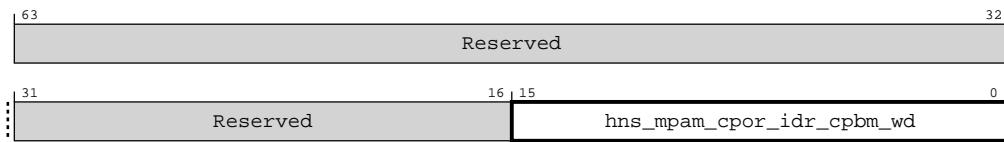


Table 4-483: cmn_hns_s_mpam_cpor_idr attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_cpor_idr_cpbm_wd	Number of bits in the cache portion partitioning bit map of this device.	RO	Configuration dependent

4.3.12.10 cmn_hns_s_mpam_ccap_idr

MPAM cache capacity partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1038

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-468: cmn_hns_s_mpam_ccap_idr

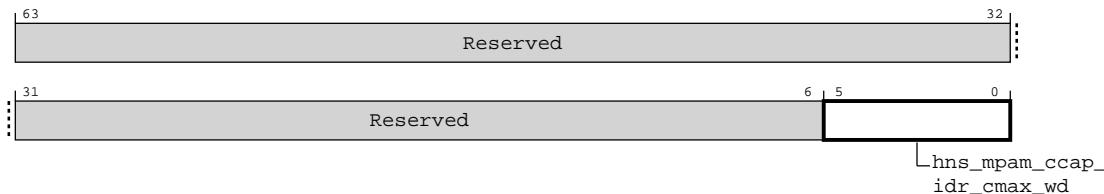


Table 4-484: cmn_hns_s_mpam_ccap_idr attributes

Bits	Name	Description	Type	Reset
[63:6]	Reserved	Reserved	RO	-
[5:0]	hns_mpam_ccap_idr_cmax_wd	Number of fractional bits implemented in the cache capacity partitioning.	RO	Configuration dependent

4.3.12.11 cmn_hns_s_mpam_mbw_idr

MPAM Memory Bandwidth partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1040

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-469: cmn_hns_s_mpam_mbw_idr

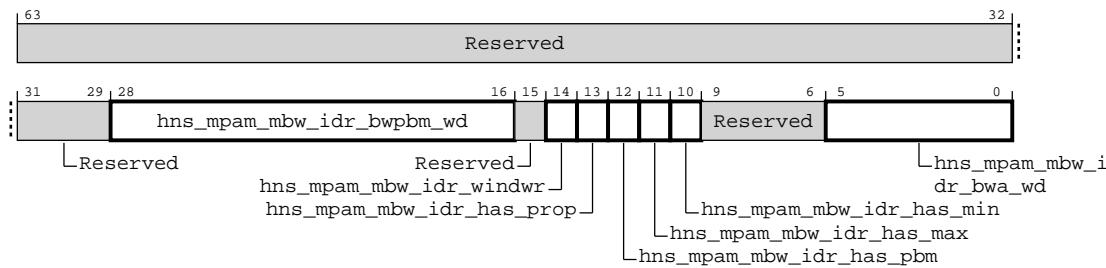


Table 4-485: cmn_hns_s_mpam_mbw_idr attributes

Bits	Name	Description	Type	Reset
[63:29]	Reserved	Reserved	RO	-
[28:16]	hns_mpam_mbw_idr_bwpbm_wd	Number of bits indication portions in MPAMCFG_MBW_PBM register.	RO	13'h0
[15]	Reserved	Reserved	RO	-
[14]	hns_mpam_mbw_idr_windwr	<p>0 The bandwidth accounting period should be read from MPAMCFG_MBW_WINDWR register, which might be fixed</p> <p>1 The bandwidth accounting width is readable and writable per partition in MPAMCFG_MBW_WINDWR register.</p>	RO	1'h0
[13]	hns_mpam_mbw_idr_has_prop	<p>0 There is no memory bandwidth proportional stride control and no MPAMCFG_MBW_PROP register</p> <p>1 MPAMCFG_MBW_PROP register exists and memory bandwidth proportional stride memory bandwidth allocation scheme is supported.</p>	RO	1'h0
[12]	hns_mpam_mbw_idr_has_pbm	<p>0 There is no memory bandwidth portion control and no MPAMCFG_MBW_PBM register</p> <p>1 MPAMCFG_MBW_PBM register exists and memory bandwidth portion allocation scheme is supported.</p>	RO	1'h0
[11]	hns_mpam_mbw_idr_has_max	<p>0 There is no maximum memory bandwidth control and no MPAMCFG_MBW_MAX register</p> <p>1 MPAMCFG_MBW_MAX register exists and maximum memory bandwidth allocation scheme is supported.</p>	RO	1'h0
[10]	hns_mpam_mbw_idr_has_min	<p>0 There is no minimum memory bandwidth control and no MPAMCFG_MBW_MIN register</p> <p>1 MPAMCFG_MBW_MIN register exists and minimum memory bandwidth allocation scheme is supported.</p>	RO	1'h0
[9:6]	Reserved	Reserved	RO	-
[5:0]	hns_mpam_mbw_idr_bwa_wd	Number of implemented bits in bandwidth allocation fields: MIN, MAX, and STRIDE. Value must be between 1 to 16	RO	4'b0000

4.3.12.12 cmn_hns_s_mpam_pri_idr

MPAM Priority partitioning ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1048

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-470: cmn_hns_s_mpam_pri_idr

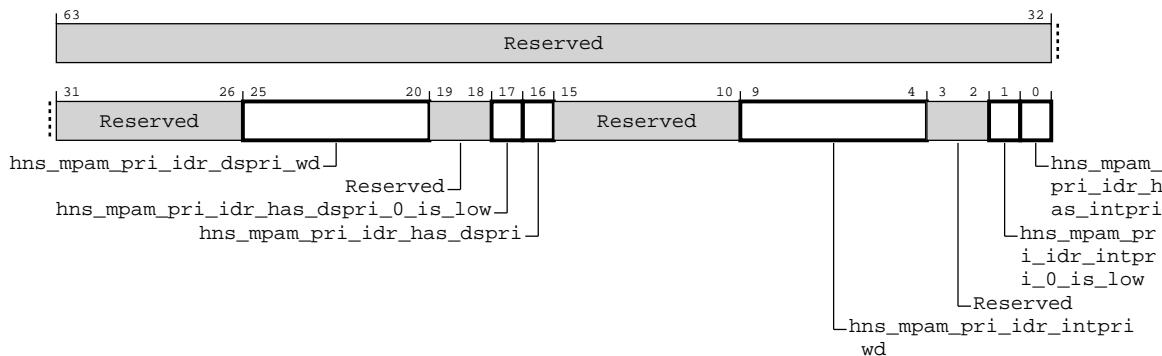


Table 4-486: cmn_hns_s_mpam_pri_idr attributes

Bits	Name	Description	Type	Reset
[63:26]	Reserved	Reserved	RO	-
[25:20]	hns_mpam_pri_idr_dspri_wd	Number of bits in downstream priority field (DSPRI) in MPAMCFG_PRI.	RO	6'h0
[19:18]	Reserved	Reserved	RO	-
[17]	hns_mpam_pri_idr_has_dspri_0_is_low	0 In the DSPRI field, a value of 0 means highest priority 1 In the DSPRI field, a value of 0 means lowest priority.	RO	1'h0
[16]	hns_mpam_pri_idr_has_dspri	0 This memory system component supports priority, but doesn't have a downstream priority (DSPRI) field in MPAMCFG_PRI. 1 This memory system component supports downstream priority and has an DSPRI field.	RO	1'h0
[15:10]	Reserved	Reserved	RO	-
[9:4]	hns_mpam_pri_idr_intpri_wd	Number of bits in the internal priority field (INTPRI) in MPAMCFG_PRI.	RO	6'h0
[3:2]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[1]	hns_mpam_pri_idr_intpri_0_is_low	0 In the INTPRI field, a value of 0 means highest priority. 1 In the INTPRI field, a value of 0 means lowest priority.	RO	1'h0
[0]	hns_mpam_pri_idr_has_intpri	0 This memory system component supports priority, but doesn't have an internal priority field in MPAMCFG_PRI. 1 This memory system component supports internal priority and has an INTPRI field.	RO	1'h0

4.3.12.13 cmn_hns_s_mpam_partid_nrw_idr

MPAM PARTID narrowing ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1050

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-471: cmn_hns_s_mpam_partid_nrw_idr

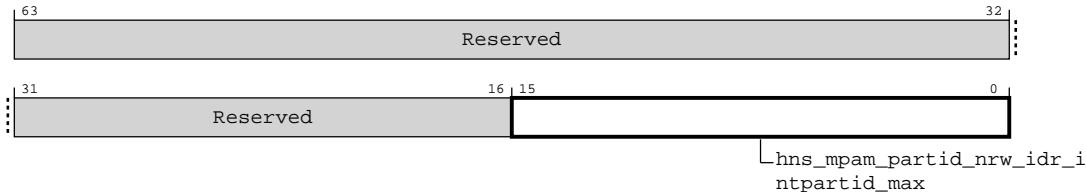


Table 4-487: cmn_hns_s_mpam_partid_nrw_idr attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_partid_nrw_idr_intpartid_max	This field indicates the largest intPARTID supported in this component.	RO	16'h00

4.3.12.14 cmn_hns_s_mpam_msmon_idr

MPAM performance monitoring ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1080

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-472: cmn_hns_s_mpam_msmon_idr

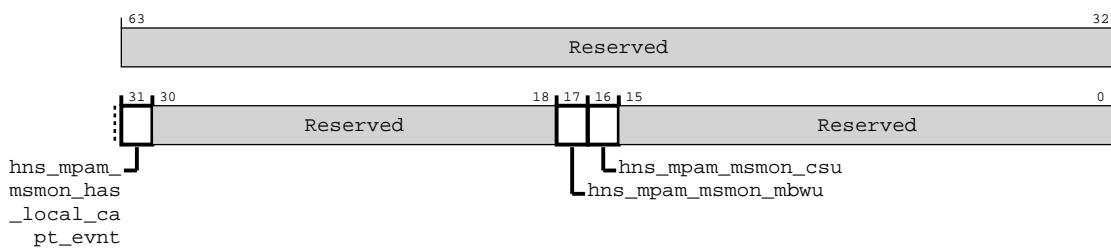


Table 4-488: cmn_hns_s_mpam_msmon_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_msmon_has_local_capt_evt	Has the local capture event generator and the MSMON_CAPT_EVNT register.	RO	1'h1
[30:18]	Reserved	Reserved	RO	-
[17]	hns_mpam_msmon_mbwu	This component has a performance monitor for Memory Bandwidth Usage by PARTID and PMG.	RO	Configuration dependent
[16]	hns_mpam_msmon_csu	This component has a performance monitor for Cache Storage Usage by PARTID and PMG.	RO	Configuration dependent

Bits	Name	Description	Type	Reset
[15:0]	Reserved	Reserved	RO	-

4.3.12.15 cmn_hns_s_mpam_csumon_idr

MPAM cache storage usage monitor ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1088

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-473: cmn_hns_s_mpam_csumon_idr

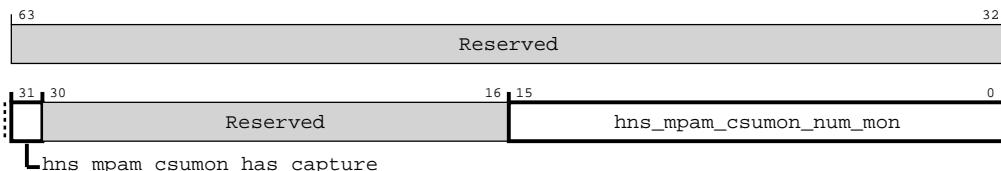


Table 4-489: cmn_hns_s_mpam_csumon_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_csumon_has_capture	<p>0 MSMON_CSU_CAPTURE is not implemented and there is no support for capture events in this component's CSU monitor feature</p> <p>1 This component's CSU monitor feature has an MSMON_CSU_CAPTURE register for every MSMON_CSU and supports the capture event behaviour.</p>	RO	1'h1
[30:16]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[15:0]	hns_mpam_csumon_num_mon	The number of CSU monitoring counters implemented in this component.	RO	Configuration dependent

4.3.12.16 cmn_hns_s_mpam_mbwumon_idr

MPAM memory bandwidth usage monitor ID register. This is a shared register for S and NS

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1090

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-474: cmn_hns_s_mpam_mbwumon_idr

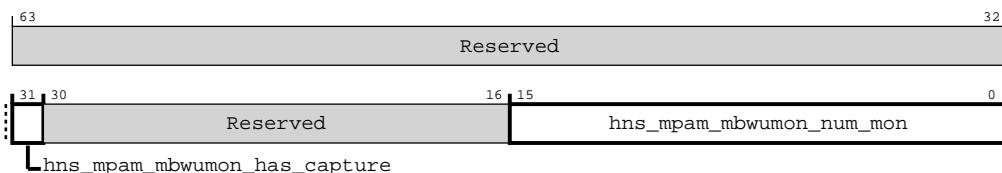


Table 4-490: cmn_hns_s_mpam_mbwumon_idr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_mpam_mbwumon_has_capture	<p>0 MSMON_MBWU_CAPTURE is not implemented and there is no support for capture events in this component's MBWU monitor feature.</p> <p>1 This component's MBWU monitor feature has an MSMON_MBWU_CAPTURE register for every MSMON_MBWU and supports the capture event behaviour.</p>	RO	1'h0

Bits	Name	Description	Type	Reset
[30:16]	Reserved	Reserved	RO	-
[15:0]	hns_mpam_mbwumon_num_mon	The number of MBWU monitoring counters implemented in this component.	RO	16'h0

4.3.12.17 cmn_hns_s_mpam_ecr

MPAM Error Control Register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h10F0

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-475: cmn_hns_s_mpam_ecr

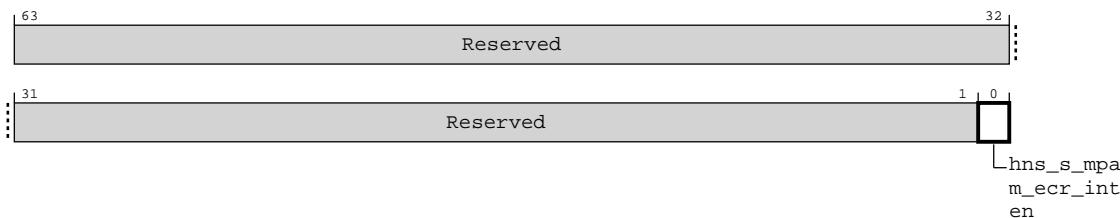


Table 4-491: cmn_hns_s_mpam_ecr attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	hns_s_mpam_ecr_inten	Interrupt Enable. When INTEN = 0, MPAM error interrupts are not generated. When INTEN = 1, MPAM error interrupts are generated.	RW	1'h0

4.3.12.18 cmn_hns_s_mpam_esr

MPAM Error Status Register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h10F8

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-476: cmn_hns_s_mpam_esr

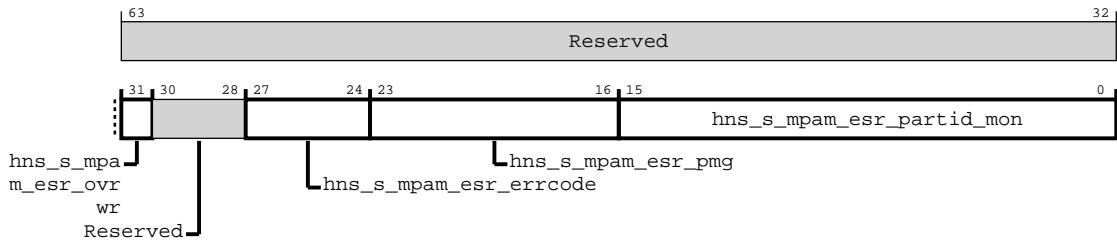


Table 4-492: cmn_hns_s_mpam_esr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_mpam_esr_ovrwr	Overwritten. If 0 and ERRCODE is zero, no errors have occurred. If 0 and ERRCODE is non-zero, a single error has occurred and is recorded in this register. If 1 and ERRCODE is non-zero, multiple errors have occurred and this register records the most recent error. The state where this bit is 1 and ERRCODE is zero is not produced by hardware and is only reached when software writes this combination into this register.	RW	1'h0
[30:28]	Reserved	Reserved	RO	-
[27:24]	hns_s_mpam_esr_errcode	Error code	RW	4'h0
[23:16]	hns_s_mpam_esr_pmg	PMG captured if the error code captures PMG, otherwise 0x0000.	RW	8'h0
[15:0]	hns_s_mpam_esr_partid_mon	PARTID captured if the error code captures PARTID. MON selector captured if the error code captures MON. Otherwise 0x0000.	RW	16'h0

4.3.12.19 cmn_hns_s_mpamcfg_part_sel

MPAM partition configuration selection register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1100

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-477: cmn_hns_s_mpamcfg_part_sel

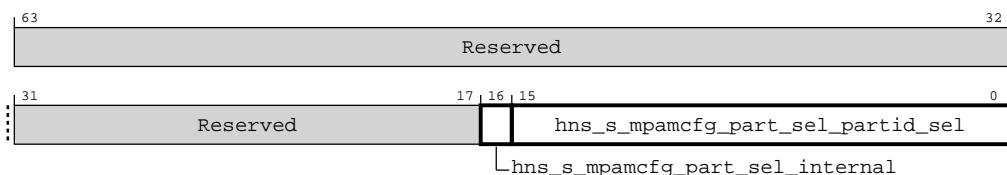


Table 4-493: cmn_hns_s_mpamcfg_part_sel attributes

Bits	Name	Description	Type	Reset
[63:17]	Reserved	Reserved	RO	-
[16]	hns_s_mpamcfg_part_sel_internal	If MPAMF_IDR.HAS_PARTID_NRW = 0, this field is RAZ/WI. If MPAMF_IDR.HAS_PARTID_NRW = 1, this bit decides how to interpret PARTID_SEL.	RW	1'h0
[15:0]	hns_s_mpamcfg_part_sel_partid_sel	Selects the partition ID to configure.	RW	16'h0

4.3.12.20 cmn_hns_s_mpamcfg_cmax

MPAM cache maximum capacity partition configuration register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1108

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-478: cmn_hns_s_mpamcfg_cmax

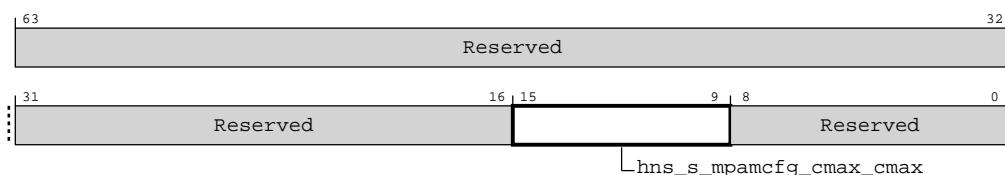


Table 4-494: cmn_hns_s_mpamcfg_cmax attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:9]	hns_s_mpamcfg_cmax_cmax	Maximum cache capacity usage in fixed-point fraction of the cache capacity by the partition selected by MPAMCFG_PART_SEL.	RW	7'b1111111
[8:0]	Reserved	Reserved	RO	-

4.3.12.21 cmn_hns_s_mpamcfg_mbw_min

MPAM memory minimum bandwidth partitioning configuration register.



Note This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1200

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-479: cmn_hns_s_mpamcfg_mbw_min

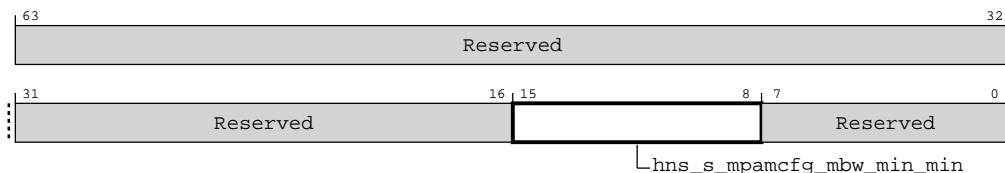


Table 4-495: cmn_hns_s_mpamcfg_mbw_min attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:8]	hns_s_mpamcfg_mbw_min_min	Memory minimum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0

Bits	Name	Description	Type	Reset
[7:0]	Reserved	Reserved	RO	-

4.3.12.22 cmn_hns_s_mpamcfg_mbw_max

MPAM memory maximum bandwidth partitioning configuration register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Note

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1208

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-480: cmn_hns_s_mpamcfg_mbw_max

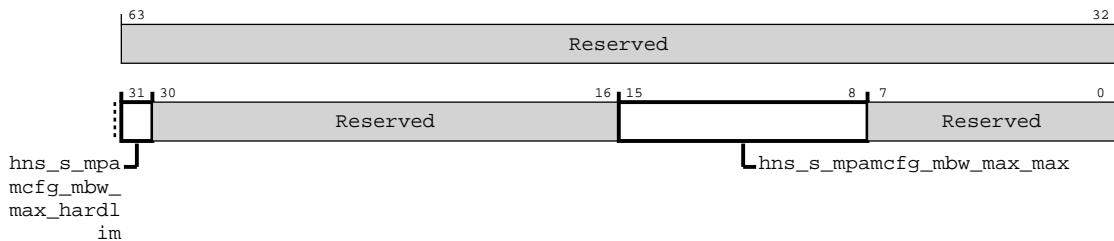


Table 4-496: cmn_hns_s_mpamcfg_mbw_max attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_mpamcfg_mbw_max_hardlim	0 When MAX bandwidth is exceeded, the partition may contend with a low preference for downstream bandwidth beyond its maximum bandwidth 1 When MAX bandwidth is exceeded, the partition may not be use any more bandwidth until its memory bandwidth measurement falls below the maximum limit.	RW	1'h0
[30:16]	Reserved	Reserved	RO	-
[15:8]	hns_s_mpamcfg_mbw_max_max	Memory maximum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
[7:0]	Reserved	Reserved	RO	-

4.3.12.23 cmn_hns_s_mpamcfg_mbw_winwd

MPAM memory bandwidth partitioning window width register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1220

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-481: cmn_hns_s_mpamcfg_mbw_winwd

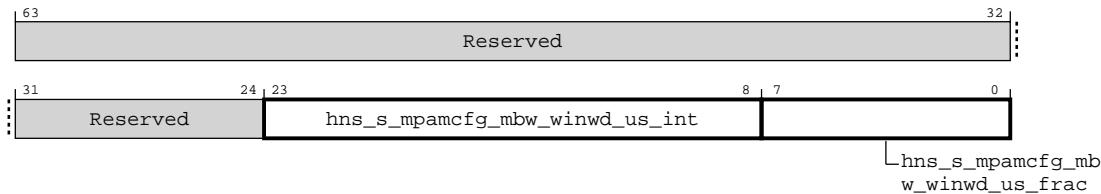


Table 4-497: cmn_hns_s_mpamcfg_mbw_winwd attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:8]	hns_s_mpamcfg_mbw_winwd_us_int	Memory bandwidth accounting period integer microseconds.	RW	16'h0
[7:0]	hns_s_mpamcfg_mbw_winwd_us_frac	Memory bandwidth accounting period fractions of a microsecond.	RW	8'h0

4.3.12.24 cmn_hns_s_mpamcfg_pri

MPAM priority partitioning configuration register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1400

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-482: cmn_hns_s_mpamcfg_pri

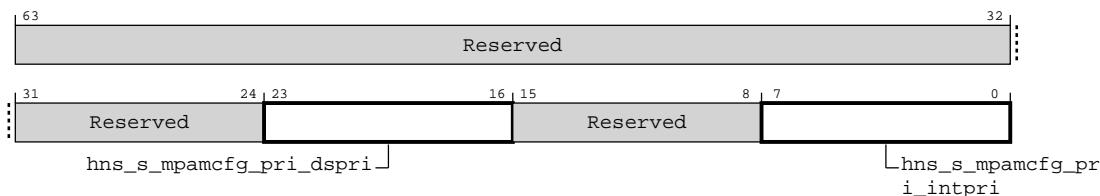


Table 4-498: cmn_hns_s_mpamcfg_pri attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	hns_s_mpamcfg_pri_dspri	If HAS_DSPRI is 1, this field is a priority value applied to downstream communications from this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
[15:8]	Reserved	Reserved	RO	-
[7:0]	hns_s_mpamcfg_pri_intpri	If HAS_INTPRI is 1, this field is a priority value applied internally inside this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0

4.3.12.25 cmn_hns_s_mpamcfg_mbw_prop

Memory bandwidth proportional stride partitioning configuration register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1500

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_mpam_s_secure_register_groups_override.mpam`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-483: cmn_hns_s_mpamcfg_mbw_prop

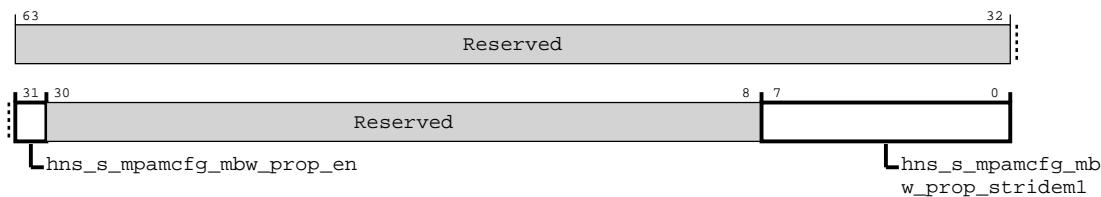


Table 4-499: cmn_hns_s_mpamcfg_mbw_prop attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_mpamcfg_mbw_prop_en	<p>0 The selected partition is not regulated by proportional stride bandwidth partitioning.</p> <p>1 The selected partition has bandwidth usage regulated by proportional stride bandwidth partitioning as controlled by STRIDEM1.</p>	RW	1'h0
[30:8]	Reserved	Reserved	RO	-
[7:0]	hns_s_mpamcfg_mbw_prop_stridem1	Normalized cost of a bandwidth consumption by the partition. STRIDEM1 is the stride for the partition minus one.	RW	8'h0

4.3.12.26 cmn_hns_s_mpamcfg_intpartid

MPAM internal partition narrowing configuration register.



This register is unique for `cmn_hns_s`. There is also similar but distinct register available in `cmn_hns_ns`.

Note

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1600

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-484: cmn_hns_s_mpamcfg_intpartid

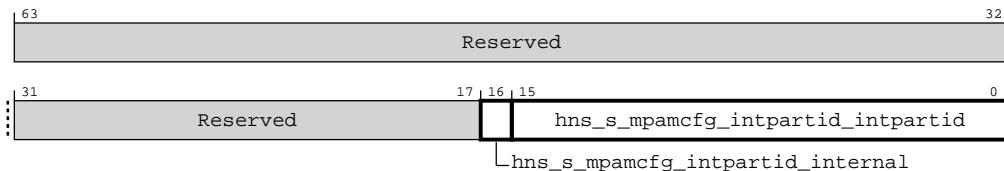


Table 4-500: cmn_hns_s_mpamcfg_intpartid attributes

Bits	Name	Description	Type	Reset
[63:17]	Reserved	Reserved	RO	-
[16]	hns_s_mpamcfg_intpartid_internal	This bit must be 1 when written to the register. If written as 0, the write will not update the reqPARTID to intPARTID association.	RW	1'h0
[15:0]	hns_s_mpamcfg_intpartid_intpartid	This field contains the intPARTID mapped to the reqPARTID in MPAMCFG_PART_SEL.	RW	16'h0

4.3.12.27 cmn_hns_s_msmon_cfg_mon_sel

Memory system performance monitor selection register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Note

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1800

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-485: cmn_hns_s_msmon_cfg_mon_sel

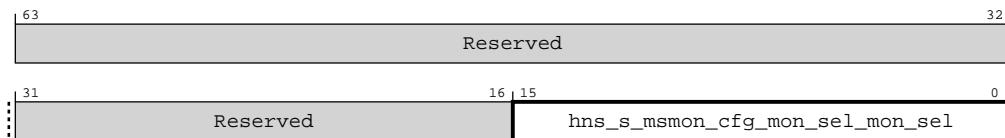


Table 4-501: cmn_hns_s_msmon_cfg_mon_sel attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_s_msmon_cfg_mon_sel_mon_sel	Selects the performance monitor to configure.	RW	16'h0

4.3.12.28 cmn_hns_s_msmon_capt_evnt

Memory system performance monitoring capture event generation register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1808

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-486: cmn_hns_s_msmon_capt_evnt

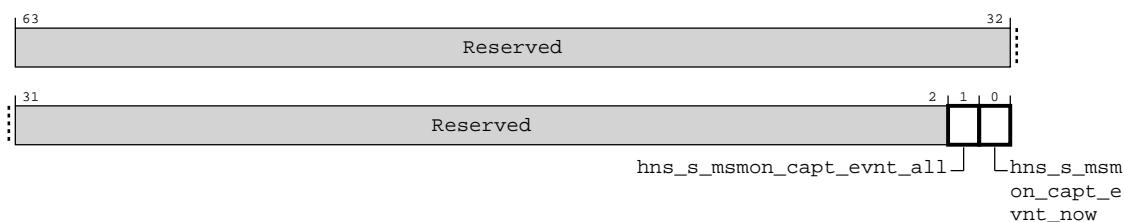


Table 4-502: cmn_hns_s_msmon_capt_evnt attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1]	hns_s_msmon_capt_evnt_all	In Secure version, if ALL written as 1 and NOW is also written as 1, signal a capture event to Secure and Non-secure monitors in this memory system component with CAPT_EVNT = 7. If written as 0 and NOW is written as 1, signal a capture event to Secure monitors in this memory system component with CAPT_EVNT = 7. In Non-secure version if NOW is written as 1, signal a capture event to Non-secure monitors in this memory system component with CAPT_EVNT = 7.	RW	1'h0
[0]	hns_s_msmon_capt_evnt_now	When written as 1, this bit causes an event to all monitors in this memory system component with CAPT_EVNT set to the value of 7. When this bit is written as 0, no event is signalled.	RW	1'h0

4.3.12.29 cmn_hns_s_msmon_cfg_csu_flt

Memory system performance monitor configure cache storage usage monitor filter register.



Note This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1810

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-487: cmn_hns_s_msmon_cfg_csu_flt

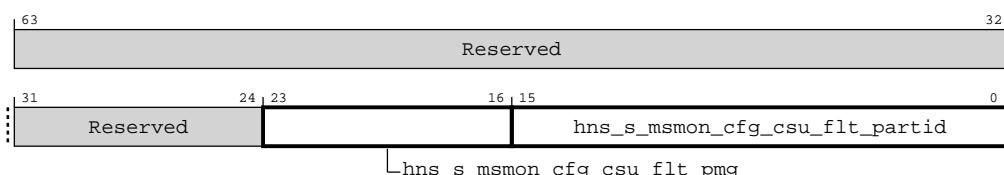


Table 4-503: cmn_hns_s_msmon_cfg_csu_flt attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[23:16]	hns_s_msmon_cfg_csu_flt_pmg	Configures the cache storage usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	8'h0
[15:0]	hns_s_msmon_cfg_csu_flt_partid	Configures the cache storage usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	16'h0

4.3.12.30 cmn_hns_s_msmon_cfg_csu_ctl

Memory system performance monitor configure cache storage usage monitor control register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1818

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-488: cmn_hns_s_msmon_cfg_csu_ctl

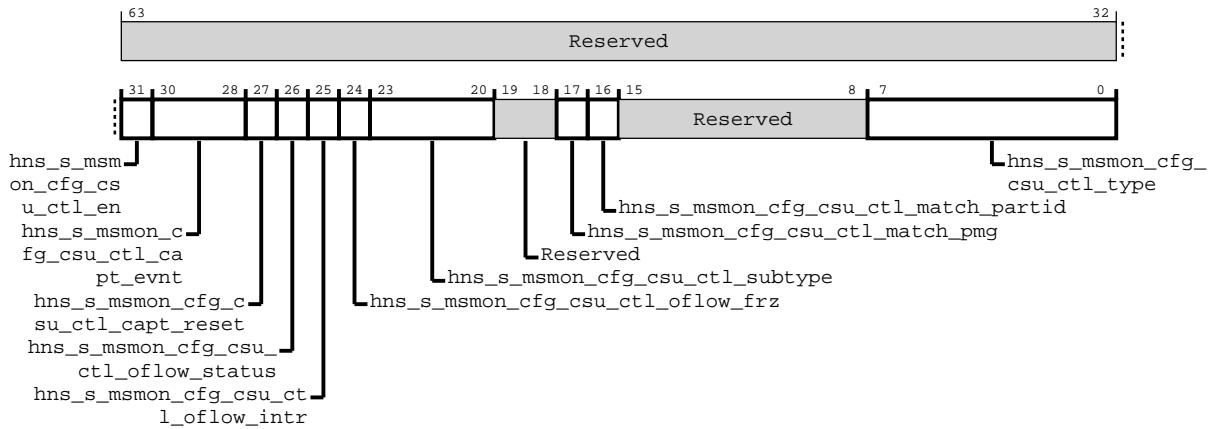


Table 4-504: cmn_hns_s_msmon_cfg_csu_ctl attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_msmon_cfg_csu_ctl_en	<p>0 The monitor is disabled and must not collect any information.</p> <p>1 The monitor is enabled to collect information according to its configuration.</p>	RW	1'h0
[30:28]	hns_s_msmon_cfg_csu_ctl_capt_evnt	Select the event that triggers capture from the following:	RW	3'h0
		<p>0 No capture event is triggered</p> <p>1 External capture event 1 (optional but recommended)</p>		
[27]	hns_s_msmon_cfg_csu_ctl_capt_reset	Capture is not implemented for the CSU monitor type.	RW	1'h0
[26]	hns_s_msmon_cfg_csu_ctl_oflow_status	<p>0 No overflow has occurred</p> <p>1 At least one overflow has occurred since this bit was last written.</p>	RW	1'h0
[25]	hns_s_msmon_cfg_csu_ctl_oflow_intr	<p>0 No interrupt.</p> <p>1 On overflow, an implementation-specific interrupt is signalled.</p>	RW	1'h0
[24]	hns_s_msmon_cfg_csu_ctl_oflow_frz	<p>0 Monitor count wraps on overflow.</p> <p>1 Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1</p>	RW	1'h0
[23:20]	hns_s_msmon_cfg_csu_ctl_subtype	Not currently used for CSU monitors, but reserved for future use.	RW	4'h0
[19:18]	Reserved	Reserved	RO	-
[17]	hns_s_msmon_cfg_csu_ctl_match_pmg	<p>0 Monitor storage used by all PMG values.</p> <p>1 Only monitor storage used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.</p>	RW	1'h0
[16]	hns_s_msmon_cfg_csu_ctl_match_partid	<p>0 Monitor storage used by all PARTIDs.</p> <p>1 Only monitor storage used with the PARTID matching MSMON_CFG_CSU_FLT.PARTID.</p>	RW	1'h0
[15:8]	Reserved	Reserved	RO	-
[7:0]	hns_s_msmon_cfg_csu_ctl_type	Read-only: Constant type indicating the type of the monitor. CSU monitor is TYPE = 0x43.	RW	8'h43

4.3.12.31 cmn_hns_s_msmon_cfg_mbwu_flt

Memory system performance monitor configure memory bandwidth usage monitor filter register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1820

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-489: cmn_hns_s_msmon_cfg_mbwu_flt

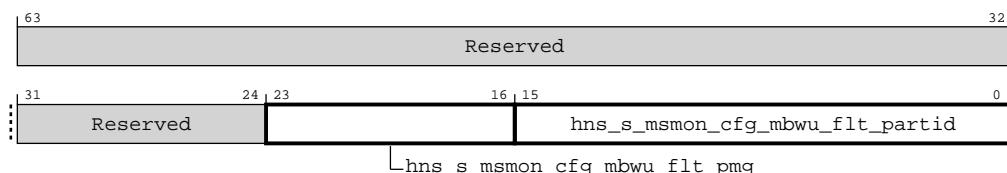


Table 4-505: cmn_hns_s_msmon_cfg_mbwu_flt attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[23:16]	hns_s_msmon_cfg_mbwu_flt_pmg	Configures the memory bandwidth usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	8'h0
[15:0]	hns_s_msmon_cfg_mbwu_flt_partid	Configures the memory bandwidth usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	16'h0

4.3.12.32 cmn_hns_s_msmon_cfg_mbwu_ctl

Memory system performance monitor configure memory bandwidth usage monitor control register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1828

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-490: cmn_hns_s_msmon_cfg_mbwu_ctl

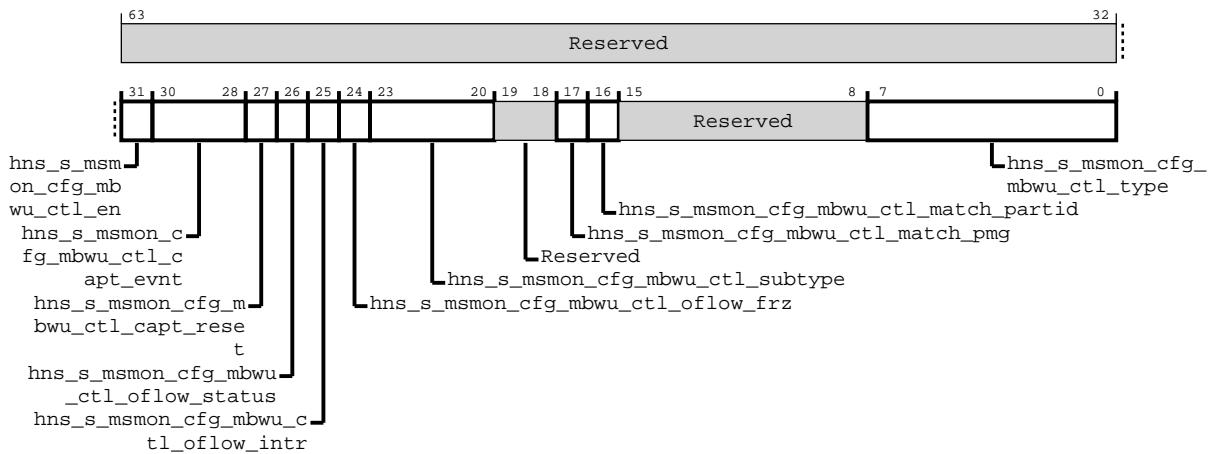


Table 4-506: cmn_hns_s_msmon_cfg_mbwu_ctl attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_msmon_cfg_mbwu_ctl_en	0 The monitor is disabled and must not collect any information. 1 The monitor is enabled to collect information according to its configuration.	RW	1'h0
[30:28]	hns_s_msmon_cfg_mbwu_ctl_capt_evnt	Select the event that triggers capture from the following: 0 No capture event is triggered 1 External capture event 1 (optional but recommended)	RW	3'h0
[27]	hns_s_msmon_cfg_mbwu_ctl_capt_reset	0: Monitor is not reset on capture. 1: Monitor is reset on capture.	RW	1'h0
[26]	hns_s_msmon_cfg_mbwu_ctl_oflow_status	0 No overflow has occurred 1 At least one overflow has occurred since this bit was last written.	RW	1'h0
[25]	hns_s_msmon_cfg_mbwu_ctl_oflow_intr	0 No interrupt. 1 On overflow, an implementation-specific interrupt is signalled.	RW	1'h0
[24]	hns_s_msmon_cfg_mbwu_ctl_oflow_frz	0 Monitor count wraps on overflow. 1 Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1	RW	1'h0
[23:20]	hns_s_msmon_cfg_mbwu_ctl_subtype	A monitor can have other event matching criteria. The meaning of values in this field varies by monitor type. The MBWU monitor type supports: 0 Do not count any bandwidth. 1 Count bandwidth used by memory reads 2 Count bandwidth used by memory writes 3 Count bandwidth used by memory reads and memory writes All other values are reserved and behaviour of a monitor with SUBTYPE set to one of the reserved values is UNPREDICTABLE.	RW	4'h0
[19:18]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[17]	hns_s_msmon_cfg_mbwu_ctl_match_pmg	0 Monitor bandwidth used by all PMG values. 1 Only monitor bandwidth used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0
[16]	hns_s_msmon_cfg_mbwu_ctl_match_partid	0 Monitor bandwidth used by all PARTIDs 1 Only monitor bandwidth used with the PARTID matching MSMON_CFG_MBWU_FLT.PARTID.	RW	1'h0
[15:8]	Reserved	Reserved	RO	-
[7:0]	hns_s_msmon_cfg_mbwu_ctl_type	Read-only: Constant type indicating the type of the monitor. MBWU monitor is TYPE = 0x42.	RW	8'h42

4.3.12.33 cmn_hns_s_msmon_csu

Memory system performance monitor cache storage usage monitor register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Note

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1840

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-491: cmn_hns_s_msmon_csu

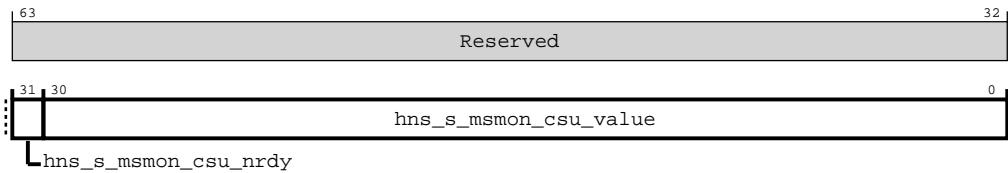


Table 4-507: cmn_hns_s_msmon_csu attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_msmon_csu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_s_msmon_csu_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

4.3.12.34 cmn_hns_s_msmon_csu_capture

Memory system performance monitor cache storage usage capture register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1848

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-492: cmn_hns_s_msmon_csu_capture

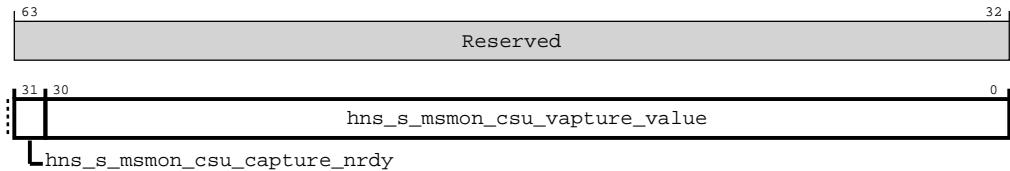


Table 4-508: cmn_hns_s_msmon_csu_capture attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_msmon_csu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_s_msmon_csu_vapture_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

4.3.12.35 cmn_hns_s_msmon_mbwu

Memory system performance monitor memory bandwidth usage monitor register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1860

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-493: cmn_hns_s_msmon_mbwu

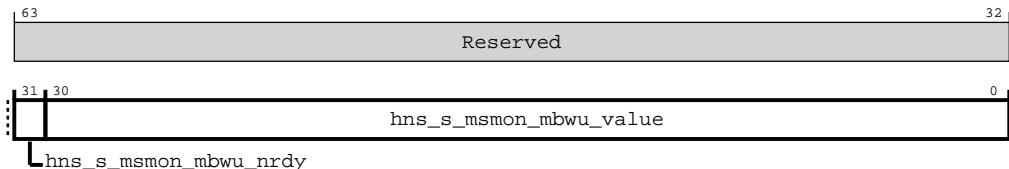


Table 4-509: cmn_hns_s_msmon_mbwu attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	hns_s_msmon_mbwu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	hns_s_msmon_mbwu_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

4.3.12.36 cmn_hns_s_msmon_mbwu_capture

Memory system performance monitor memory bandwidth usage capture register.



This register is unique for cmn_hns_s. There is also similar but distinct register available in cmn_hns_ns.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1868

Type

RW

Reset value

See individual bit resets

Secure group override

`cmn_hns_mpam_s_secure_register_groups_override.mpam`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-494: cmn_hns_s_msmon_mbwu_capture

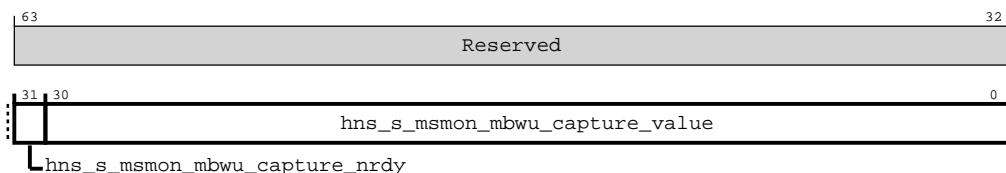


Table 4-510: cmn_hns_s_msmon_mbwu_capture attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	<code>hns_s_msmon_mbwu_capture_nrdy</code>	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
[30:0]	<code>hns_s_msmon_mbwu_capture_value</code>	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

4.3.12.37 cmn_hns_s_mpamcfg_cpbm

MPAM cache portion bitmap partition configuration register.



This register is unique for `cmn_hns_s`. There is also similar but distinct register available in `cmn_hns_ns`.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Secure group override

cmn_hns_mpam_s_secure_register_groups_override.mpam

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-495: cmn_hns_s_mpamcfg_cpbm

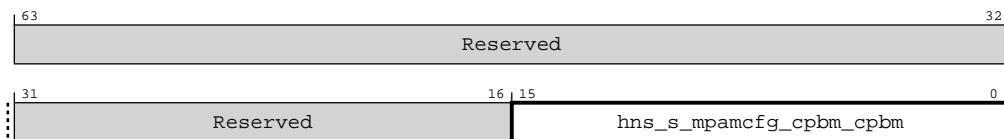


Table 4-511: cmn_hns_s_mpamcfg_cpbm attributes

Bits	Name	Description	Type	Reset
[63:16]	Reserved	Reserved	RO	-
[15:0]	hns_s_mpamcfg_cpbm_cpbm	Bitmap of portions of cache capacity allocable by the partition selected by MPAMCFG_PART_SEL. NOTE: CPBM can not be all zeros for any PARTID.	RW	16'hFFFF

4.3.13 MXP register descriptions

This section lists the MXP registers.

4.3.13.1 por_mxp_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-496: por_mxp_node_info

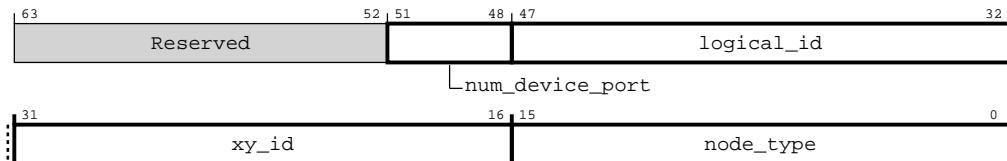


Table 4-512: por_mxp_node_info attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:48]	num_device_port	Number of device ports attached to the MXP. Mesh config = (1x1)? Max. of 6 Device Ports are supported : Max. of 4 Device Ports are supported	RO	Configuration dependent
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	xy_id	Identifies (X,Y) location of XP within the mesh NOTE: The (X,Y) location is specified following the node ID format as defined in Node ID mapping section, with the bottom 3 bits, corresponding to port ID and device ID, set to 0. Bits 31:11 must always be set to 0. The range of bits representing the (X,Y) location varies for different node ID formats.	RO	16'h0000
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0006

4.3.13.2 por_mxp_device_port_connect_info_p0-5

There are 6 iterations of this register. The index ranges from 0 to 5. Contains device port connection information for port #{{index}}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h8 + #{8*index}`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-497: por_mxp_device_port_connect_info_p0-5

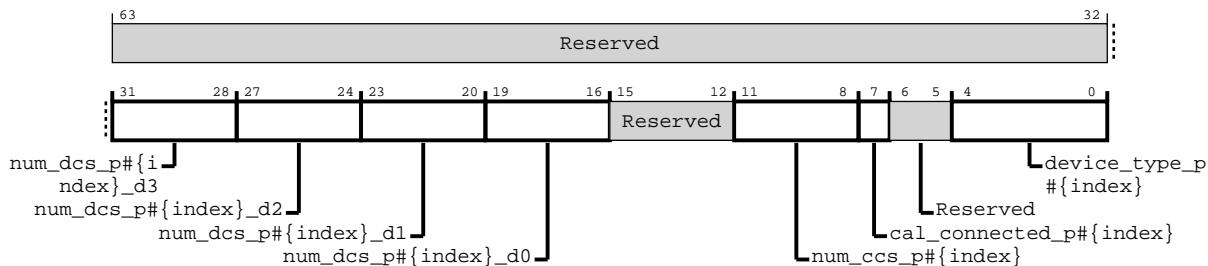


Table 4-513: por_mxp_device_port_connect_info_p0-5 attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:28]	num_dcs_p#{index}_d3	Number of device credited slices connected to port #{index} device 3 (Allowed values: 0-4)	RO	Configuration dependent
[27:24]	num_dcs_p#{index}_d2	Number of device credited slices connected to port #{index} device 2 (Allowed values: 0-4)	RO	Configuration dependent
[23:20]	num_dcs_p#{index}_d1	Number of device credited slices connected to port #{index} device 1 (Allowed values: 0-4)	RO	Configuration dependent
[19:16]	num_dcs_p#{index}_d0	Number of device credited slices connected to port #{index} device 0 (Allowed values: 0-4)	RO	Configuration dependent
[15:12]	Reserved	Reserved	RO	-
[11:8]	num_ccs_p#{index}	Number of CAL credited slices connected to port #{index} (Allowed values: 0-2)	RO	Configuration dependent
[7]	cal_connected_p#{index}	When set, CAL is connected on port #{index} (Allowed values: 0-1)	RO	Configuration dependent
[6:5]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[4:0]	device_type_p#{index}	Connected device type	RO	Configuration dependent
	5'b00000	Reserved		
	5'b00001	RN-I		
	5'b00010	RN-D		
	5'b00011	Reserved		
	5'b00100	RN-F_CHIB		
	5'b00101	RN-F_CHIB_ESAM		
	5'b00110	RN-F_CHIA		
	5'b00111	RN-F_CHIA_ESAM		
	5'b01000	HN-T		
	5'b01001	HN-I		
	5'b01010	HN-D		
	5'b01011	HN-P		
	5'b01100	SN-F_CHIC		
	5'b01101	SBSX		
	5'b01110	HN-F		
	5'b01111	SN-F_CHIE		
	5'b10000	SN-F_CHID		
	5'b10001	CXHA		
	5'b10010	CXRA		
	5'b10011	CXRH		
	5'b10100	RN-F_CHID		
	5'b10101	RN-F_CHID_ESAM		
	5'b10110	RN-F_CHIC		
	5'b10111	RN-F_CHIC_ESAM		
	5'b11000	RN-F_CHIE		
	5'b11001	RN-F_CHIE_ESAM		
	5'b11010	Reserved		
	5'b11011	Reserved		
	5'b11100	MTSX		
	5'b11101	HN-V		
	5'b11110	CCG		
	5'b11111	Reserved		

4.3.13.3 por_mxp_mesh_port_connect_info_east

Contains port connection information for East port.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h38

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-498: por_mxp_mesh_port_connect_info_east

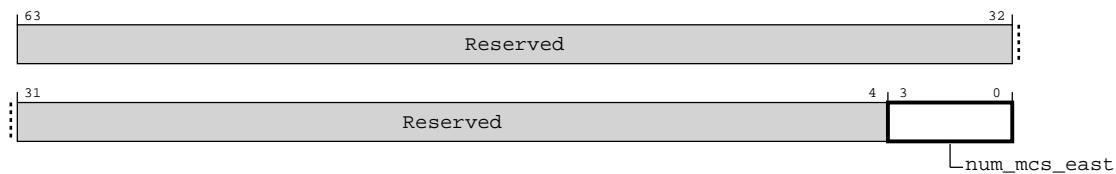


Table 4-514: por_mxp_mesh_port_connect_info_east attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3:0]	num_mcs_east	Number of mesh credited slices connected to East port (Allowed values: 0-4)	RO	Configuration dependent

4.3.13.4 por_mxp_mesh_port_connect_info_north

Contains port connection information for North port.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h40

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-499: por_mxp_mesh_port_connect_info_north

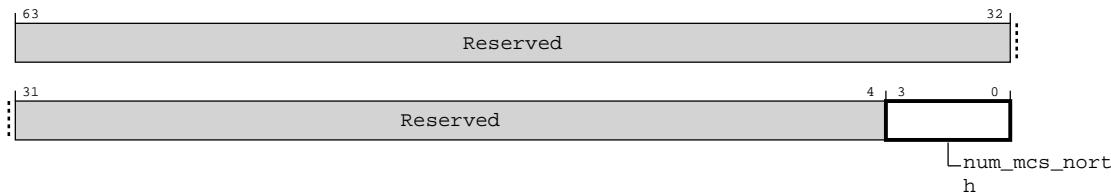


Table 4-515: por_mxp_mesh_port_connect_info_north attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3:0]	num_mcs_north	Number of mesh credited slices connected to North port (Allowed values: 0-4)	RO	Configuration dependent

4.3.13.5 por_mxp_device_port_connect_ldid_info_p0-5

There are 6 iterations of this register. The index ranges from 0 to 5. Contains LDID information for devices connected to port #{{index}}. Valid only for RNFs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h48 + #{8*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-500: por_mxp_device_port_connect_ldid_info_p0-5

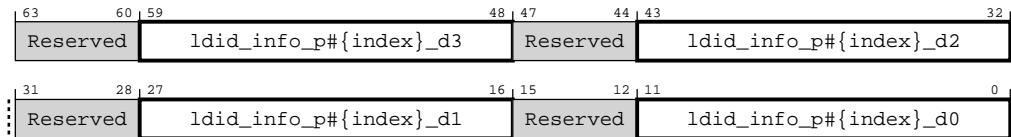


Table 4-516: por_mxp_device_port_connect_ldid_info_p0-5 attributes

Bits	Name	Description	Type	Reset
[63:60]	Reserved	Reserved	RO	-
[59:48]	ldid_info_p#{index}_d3	LDID value of the device connected to port P#{index}_D3	RO	Configuration dependent
[47:44]	Reserved	Reserved	RO	-
[43:32]	ldid_info_p#{index}_d2	LDID value of the device connected to port P#{index}_D2	RO	Configuration dependent
[31:28]	Reserved	Reserved	RO	-
[27:16]	ldid_info_p#{index}_d1	LDID value of the device connected to port P#{index}_D1	RO	Configuration dependent
[15:12]	Reserved	Reserved	RO	-
[11:0]	ldid_info_p#{index}_d0	LDID value of the device connected to port P#{index}_D0	RO	Configuration dependent

4.3.13.6 por_mxp_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-501: por_mxp_child_info

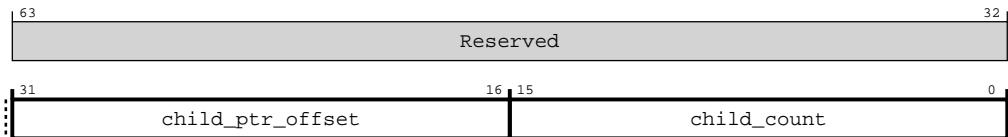


Table 4-517: por_mxp_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
[15:0]	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

4.3.13.7 por_mxp_child_pointer_0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Contains base address of the configuration subordinate for child #{{index}}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h100 + #{8*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-502: por_mxp_child_pointer_0-31

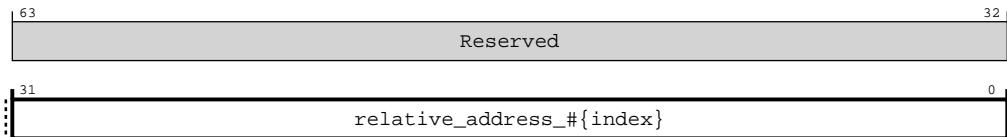


Table 4-518: por_mxp_child_pointer_0-31 attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	relative_address_{index}	<p>Bit</p> <p>[31] External or internal child node</p> <p>[30] Set to 1'b0 Bits</p> <p>[29:0] Child node address offset relative to PERIPHBASE</p> <p>1'b1 Indicates child pointer points to a configuration node that is external to CMN-700</p> <p>1'b0 Indicates child pointer points to a configuration node that is internal to CMN-700</p>	RO	32'b0

4.3.13.8 por_mxp_p0-5_info

There are 6 iterations of this register. The index ranges from 0 to 5. Provides component identification information for XP port # {index}. NOTE: There will be max. of 6 MXP Port Info registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port Info register will be at the next 8 byte address boundary. Each successive MXP Port Info register will be named with the suffix. For example por_mxp_p<0:5>_info

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900 + #{16*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-503: por_mxp_p0-5_info

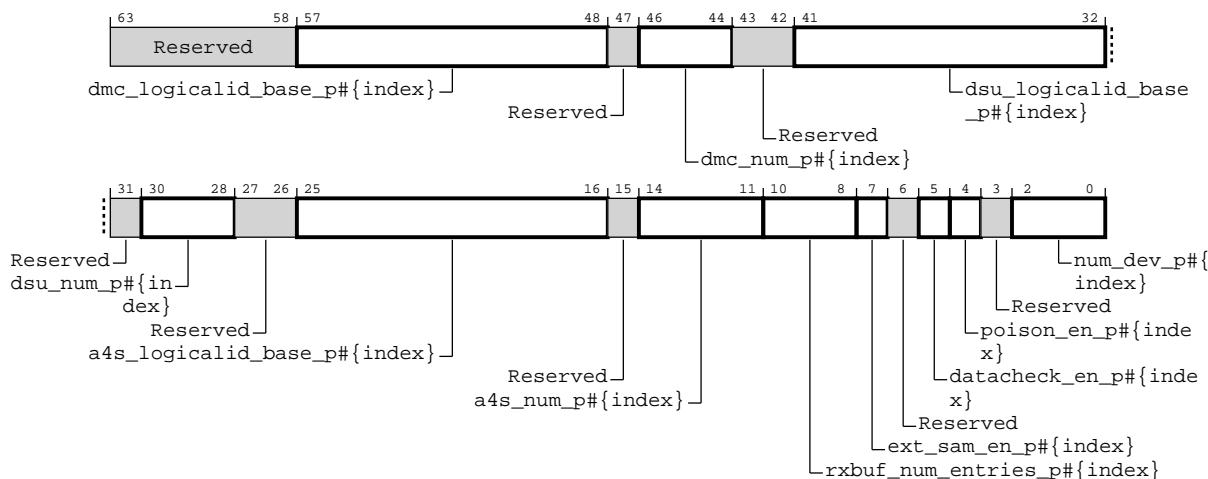


Table 4-519: por_mxp_p0-5_info attributes

Bits	Name	Description	Type	Reset
[63:58]	Reserved	Reserved	RO	-
[57:48]	dmc_logicalid_base_p#{index}	DMC AXIU interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
[47]	Reserved	Reserved	RO	-
[46:44]	dmc_num_p#{index}	Total number of SN-F AXIU interfaces at this port (0 to 4)	RO	Configuration dependent
[43:42]	Reserved	Reserved	RO	-
[41:32]	dsu_logicalid_base_p#{index}	DSU AXIU interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
[31]	Reserved	Reserved	RO	-
[30:28]	dsu_num_p#{index}	Total number of RN-F AXIU interfaces at this port (0 to 4)	RO	Configuration dependent
[27:26]	Reserved	Reserved	RO	-
[25:16]	a4s_logicalid_base_p#{index}	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
[15]	Reserved	Reserved	RO	-
[14:11]	a4s_num_p#{index}	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
[10:8]	rxbuf_num_entries_p#{index}	Number of input buffers at this port (2 to 4)	RO	Configuration dependent
[7]	ext_sam_en_p#{index}	ESAM enable	RO	Configuration dependent
[6]	Reserved	Reserved	RO	-
[5]	datacheck_en_p#{index}	Datacheck enable	RO	Configuration dependent
[4]	poison_en_p#{index}	Poison enable	RO	Configuration dependent
[3]	Reserved	Reserved	RO	-
[2:0]	num_dev_p#{index}	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

4.3.13.9 por_mxp_p0-5_info_1

There are 6 iterations of this register. The index ranges from 0 to 5. Provides component identification information for XP port #*{index}*. NOTE: There will be max. of 6 MXP Port Info registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port Info register will be at the next 8 byte address boundary. Each successive MXP Port Info register will be named with the suffix. For example por_mxp_p<0:5>_info_1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908 + # {16*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-504: por_mxp_p0-5_info_1

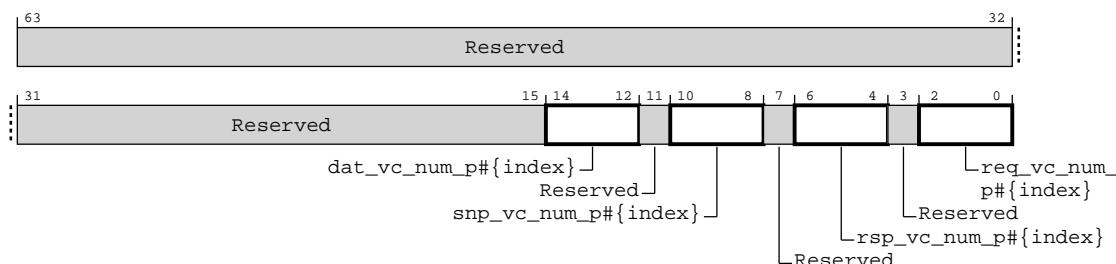


Table 4-520: por_mxp_p0-5_info_1 attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	dat_vc_num_p#{index}	Number of replicated channels on DAT VC at this port	RO	Configuration dependent
[11]	Reserved	Reserved	RO	-
[10:8]	snp_vc_num_p#{index}	Number of replicated channels on SNP VC at this port	RO	Configuration dependent

Bits	Name	Description	Type	Reset
[7]	Reserved	Reserved	RO	-
[6:4]	rsp_vc_num_p#[index]	Number of replicated channels on RSP VC at this port	RO	Configuration dependent
[3]	Reserved	Reserved	RO	-
[2:0]	req_vc_num_p#[index]	Number of replicated channels on REQ VC at this port	RO	Configuration dependent

4.3.13.10 por_dtm_unit_info

Provides component identification information for XP port 0 and 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h960

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-505: por_dtm_unit_info

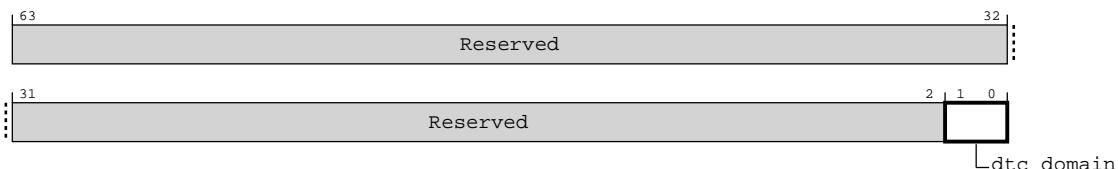


Table 4-521: por_dtm_unit_info attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	dtc_domain	DTC domain number associated with this DTM	RO	Configuration dependent

4.3.13.11 por_dtm_unit_info_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Provides component identification information for XP ports # $\{2^*\text{index}\}$ and # $\{(2^*\text{index})+1\}$. NOTE: There will be max. of 3 DTM Unit Info registers based on MXP_MULTIPLE_DTM_EN_PARAM and MXP_NUM_DEV_PORT_PARAM value. Each successive DTM Unit Info register will be at the next 8 byte address boundary. Each successive DTM Unit Info register will be named with the suffix corresponding to the DT register number. For example por_dtm_unit_info_dt<1:3>

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16^{'}h968 + \#\{8^*(\text{index}-1)\}$

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-506: por_dtm_unit_info_dt1-3

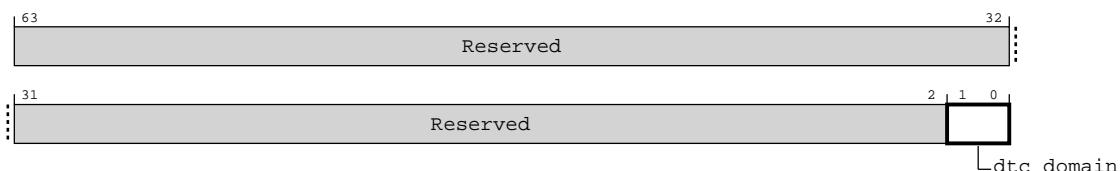


Table 4-522: por_dtm_unit_info_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:2]	Reserved	Reserved	RO	-
[1:0]	dtc_domain	DTC domain number associated with this DTM	RO	Configuration dependent

4.3.13.12 por_mxp_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-507: por_mxp_secure_register_groups_override

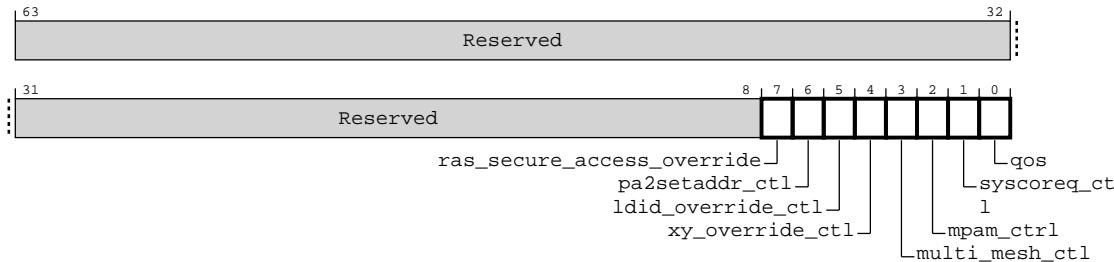


Table 4-523: por_mxp_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7]	ras_secure_access_override	Allow Non-secure access to Secure RAS registers	RW	1'b0
[6]	pa2setaddr_ctl	Allows Non-secure access to Secure PA to SETADDR control registers	RW	1'b0
[5]	ldid_override_ctl	Allows Non-secure access to Secure LDID override registers	RW	1'b0
[4]	xy_override_ctl	Allows Non-secure access to Secure XY override registers	RW	1'b0
[3]	multi_mesh_ctl	Allows Non-secure access to Secure Multi Mesh control registers	RW	1'b0
[2]	mpam_ctrl	Allows Non-secure access to Secure CHI port MPAM override register	RW	1'b0

Bits	Name	Description	Type	Reset
[1]	syscoreq_ctl	Allows Non-secure access to Secure syscoreq_ctl registers	RW	1'b0
[0]	qos	Allows Non-secure access to Secure QoS registers	RW	1'b0

4.3.13.13 por_mxp_aux_ctl

Functions as the auxiliary control register for XP.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-508: por_mxp_aux_ctl

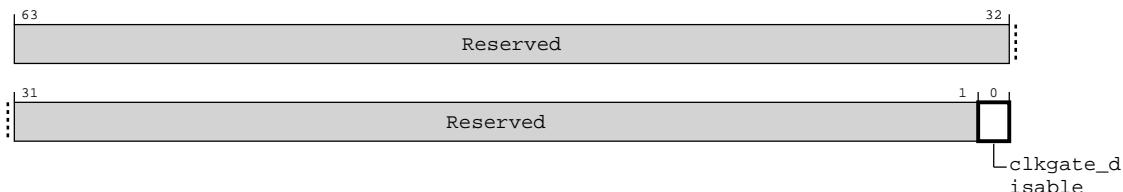


Table 4-524: por_mxp_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	clkgate_disable	Disables clock gating when set	RW	1'b0

4.3.13.14 por_mxp_device_port_ctl

Functions as the control register for XP device ports.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-509: por_mxp_device_port_ctl

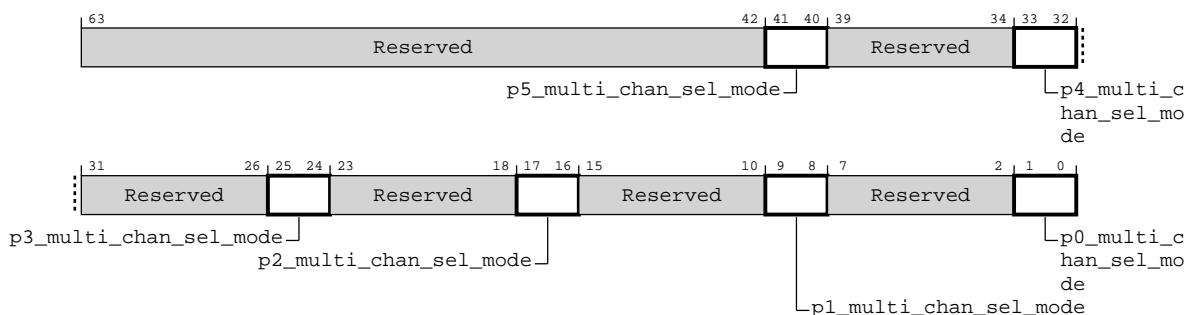


Table 4-525: por_mxp_device_port_ctl attributes

Bits	Name	Description	Type	Reset
[63:42]	Reserved	Reserved	RO	-
[41:40]	p5_multi_chan_sel_mode	Selects the mode/scheme for channel selection in multi channel mesh structure 2'h0 Enable channel mapping based on TGTID scheme 2'h1 Enable channel mapping based on dynamic credit availability scheme 2'h2 Enable channel mapping based on direct connect scheme 2'h3 Reserved	RW	2'b0

Bits	Name	Description	Type	Reset
[39:34]	Reserved	Reserved	RO	-
[33:32]	p4_multi_chan_sel_mode	Selects the mode/scheme for channel selection in multi channel mesh structure 2'h0 Enable channel mapping based on TGTID scheme 2'h1 Enable channel mapping based on dynamic credit availability scheme 2'h2 Enable channel mapping based on direct connect scheme 2'h3 Reserved	RW	2'b0
[31:26]	Reserved	Reserved	RO	-
[25:24]	p3_multi_chan_sel_mode	Selects the mode/scheme for channel selection in multi channel mesh structure 2'h0 Enable channel mapping based on TGTID scheme 2'h1 Enable channel mapping based on dynamic credit availability scheme 2'h2 Enable channel mapping based on direct connect scheme 2'h3 Reserved	RW	2'b0
[23:18]	Reserved	Reserved	RO	-
[17:16]	p2_multi_chan_sel_mode	Selects the mode/scheme for channel selection in multi channel mesh structure 2'h0 Enable channel mapping based on TGTID scheme 2'h1 Enable channel mapping based on dynamic credit availability scheme 2'h2 Enable channel mapping based on direct connect scheme 2'h3 Reserved	RW	2'b0
[15:10]	Reserved	Reserved	RO	-
[9:8]	p1_multi_chan_sel_mode	Selects the mode/scheme for channel selection in multi channel mesh structure 2'h0 Enable channel mapping based on TGTID scheme 2'h1 Enable channel mapping based on dynamic credit availability scheme 2'h2 Enable channel mapping based on direct connect scheme 2'h3 Reserved	RW	2'b0
[7:2]	Reserved	Reserved	RO	-
[1:0]	p0_multi_chan_sel_mode	Selects the mode/scheme for channel selection in multi channel mesh structure 2'h0 Enable channel mapping based on TGTID scheme 2'h1 Enable channel mapping based on dynamic credit availability scheme 2'h2 Enable channel mapping based on direct connect scheme 2'h3 Reserved	RW	2'b0

4.3.13.15 por_mxp_p0-5_mpam_override

There are 6 iterations of this register. The index ranges from 0 to 5. Controls MPAM fields for devices connected to port #{{index}}. Valid only if the devices doesn't support MPAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hA10 + #{8*index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.mpam_ctrl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-510: por_mxp_p0-5_mpam_override

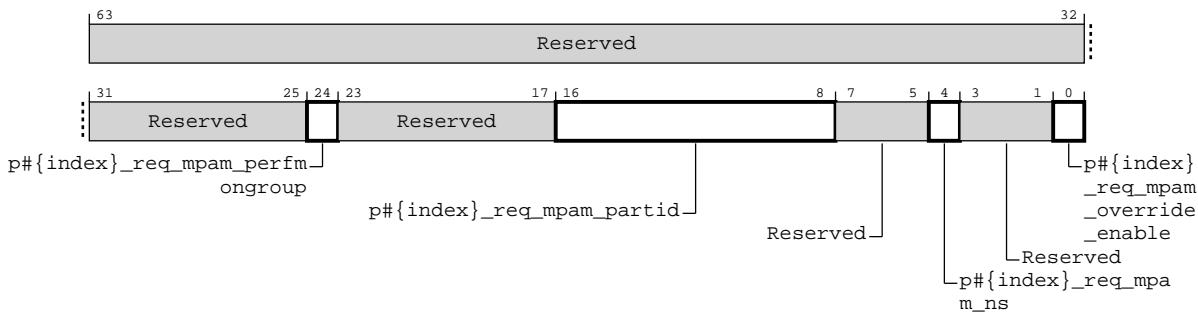


Table 4-526: por_mxp_p0-5_mpam_override attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	p#{index}_req_mpam_perfmongroup	MPAM.PerfMonGroup sub-field that overrides the REQ channel MPAM.PerfMonGroup when p#{index}_req_mpam_override_enable is set	RW	1'b0
[23:17]	Reserved	Reserved	RO	-
[16:8]	p#{index}_req_mpam_partid	MPAM.PartID sub-field that overrides the REQ channel MPAM.PartID when p#{index}_req_mpam_override_enable is set	RW	9'b0
[7:5]	Reserved	Reserved	RO	-
[4]	p#{index}_req_mpam_ns	MPAM.NS sub-field that overrides the REQ channel MPAM.NS when p#{index}_req_mpam_override_enable is set	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	p#{index}_req_mpam_override_enable	P#{index} DEV MPAM Override Enable on REQ Channel: 1 - Drive the MPAM fields on REQ channel with the values from this register, 0 - Override of MPAM fields in REQ channel is disabled	RW	1'b0

4.3.13.16 por_mxp_p0-5_ldid_override

There are 6 iterations of this register. The index ranges from 0 to 5. Controls LDID fields in REQ FLIT for devices connected to port #*{index}*. Valid only if POR_MXP_RNF_CLUSTER_EN_PARAM is 1.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA40 + #{8*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.ldid_override_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-511: por_mxp_p0-5_ldid_override

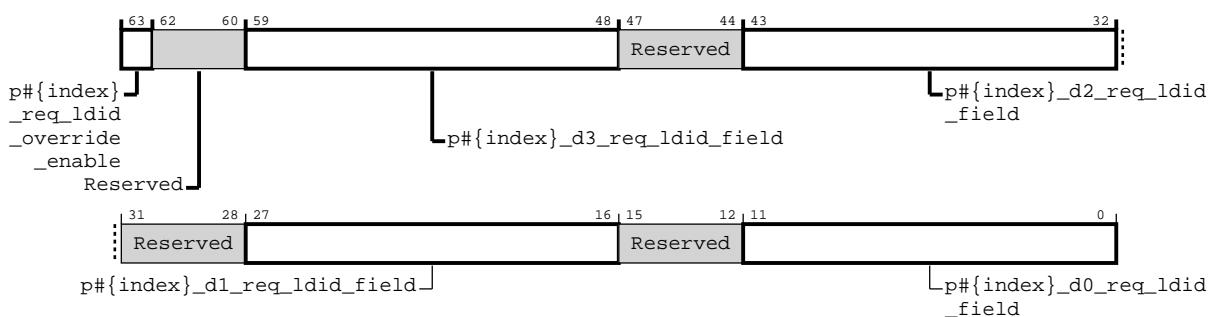


Table 4-527: por_mxp_p0-5_ldid_override attributes

Bits	Name	Description	Type	Reset
[63]	p#{index}_req_ldid_override_enable	P#{index} DEV LDID Override Enable on REQ Channel: 1 - Drive the LDID fields on REQ channel with the values from this register, 0 - Override of LDID fields in REQ channel is disabled	RW	1'b0
[62:60]	Reserved	Reserved	RO	-
[59:48]	p#{index}_d3_req_ldid_field	LDID value that overrides the P#{index}_D3 REQ channel LDID field when p#{index}_req_ldid_override_enable is set	RW	12'b0
[47:44]	Reserved	Reserved	RO	-
[43:32]	p#{index}_d2_req_ldid_field	LDID value that overrides the P#{index}_D2 REQ channel LDID field when p#{index}_req_ldid_override_enable is set	RW	12'b0
[31:28]	Reserved	Reserved	RO	-
[27:16]	p#{index}_d1_req_ldid_field	LDID value that overrides the P#{index}_D1 REQ channel LDID field when p#{index}_req_ldid_override_enable is set	RW	12'b0
[15:12]	Reserved	Reserved	RO	-
[11:0]	p#{index}_d0_req_ldid_field	LDID value that overrides the P#{index}_D0 REQ channel LDID field when p#{index}_req_ldid_override_enable is set	RW	12'b0

4.3.13.17 por_mxp_p0-5_qos_control

There are 6 iterations of this register. The index ranges from 0 to 5. Controls QoS settings for devices connected to port #{index}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA80 + #{32*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-512: por_mxp_p0-5_qos_control

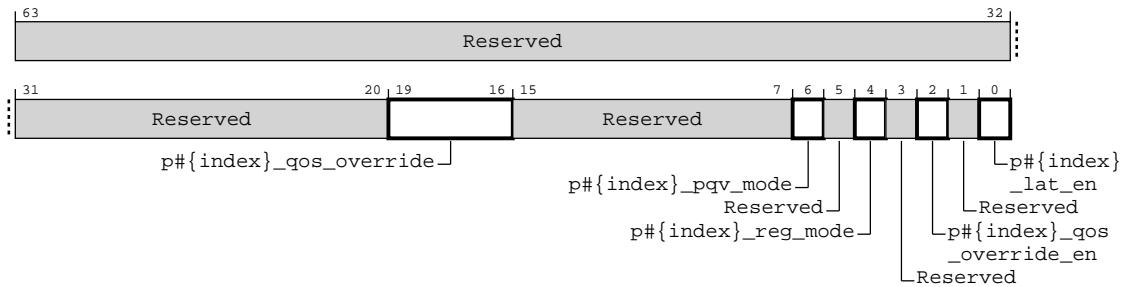


Table 4-528: por_mxp_p0-5_qos_control attributes

Bits	Name	Description	Type	Reset
[63:20]	Reserved	Reserved	RO	-
[19:16]	p#{index}_qos_override	QoS override value for port #{index}	RW	4'b0000
[15:7]	Reserved	Reserved	RO	-
[6]	p#{index}_pqv_mode	Configures the QoS regulator mode during period mode 1'b0 Normal mode; QoS value is stable when the manager is idle 1'b1 Quiesce high mode; QoS value tends to the maximum value when the manager is idle	RW	1'b0
[5]	Reserved	Reserved	RO	-
[4]	p#{index}_reg_mode	Configures the QoS regulator mode 1'b0 Latency mode 1'b1 Period mode; used for bandwidth regulation	RW	1'b0
[3]	Reserved	Reserved	RO	-
[2]	p#{index}_qos_override_en	Enables port #{index} QoS override; when set, allows QoS value on inbound transactions to be overridden	RW	1'b0
[1]	Reserved	Reserved	RO	-
[0]	p#{index}_lat_en	Enables port #{index} QoS regulation when set	RW	1'b0

4.3.13.18 por_mxp_p0-5_qos_lat_tgt

There are 6 iterations of this register. The index ranges from 0 to 5. Controls QoS target latency/period (in cycles) for regulation of devices connected to port #{index}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hA88 + # {32 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.qos`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-513: por_mxp_p0-5_qos_lat_tgt

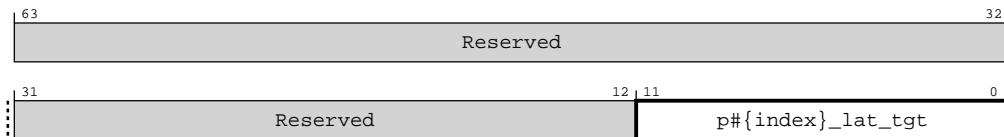


Table 4-529: por_mxp_p0-5_qos_lat_tgt attributes

Bits	Name	Description	Type	Reset
[63:12]	Reserved	Reserved	RO	-
[11:0]	p#{index}_lat_tgt	Port #{index} transaction target latency/period; a value of 0 corresponds to no regulation	RW	12'h000

4.3.13.19 por_mxp_p0-5_qos_lat_scale

There are 6 iterations of this register. The index ranges from 0 to 5. Controls the QoS target scale factor for devices connected to port #{index}. The scale factor is represented in powers of two from the range 2^{-3} to 2^{-10} .

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hA90 + # {32 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.qos

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-514: por_mxp_p0-5_qos_lat_scale

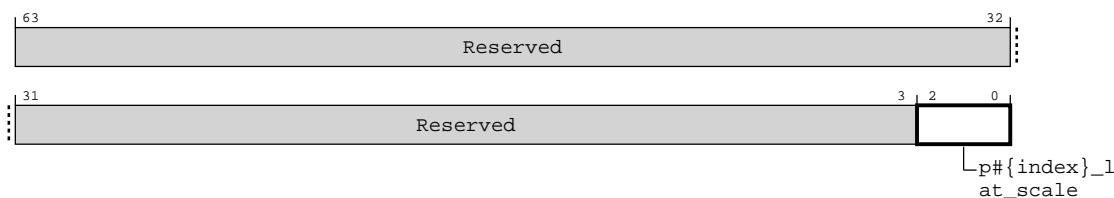


Table 4-530: por_mxp_p0-5_qos_lat_scale attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2:0]	p#{index}_lat_scale	Port 0 QoS scale factor 3'b000 2^(-3) 3'b001 2^(-4) 3'b010 2^(-5) 3'b011 2^(-6) 3'b100 2^(-7) 3'b101 2^(-8) 3'b110 2^(-9) 3'b111 2^(-10)	RW	3'h0

4.3.13.20 por_mxp_p0-5_qos_lat_range

There are 6 iterations of this register. The index ranges from 0 to 5. Controls the minimum and maximum QoS values generated by the QoS regulator for devices connected to port #{index}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hA98 + # {32 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.qos`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-515: por_mxp_p0-5_qos_lat_range

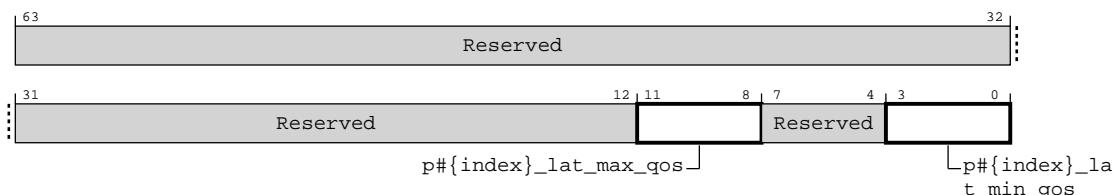


Table 4-531: por_mxp_p0-5_qos_lat_range attributes

Bits	Name	Description	Type	Reset
[63:12]	Reserved	Reserved	RO	-
[11:8]	p#{index}_lat_max_qos	Port #{index} QoS maximum value	RW	4'h0
[7:4]	Reserved	Reserved	RO	-
[3:0]	p#{index}_lat_min_qos	Port #{index} QoS minimum value	RW	4'h0

4.3.13.21 por_mxp_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-516: por_mxp_pmu_event_sel

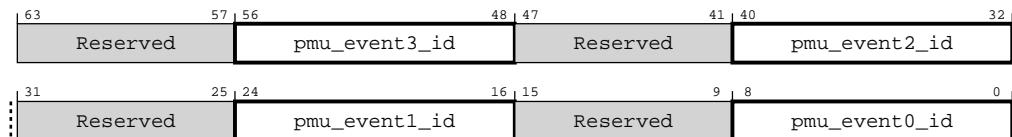


Table 4-532: por_mxp_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:48]	pmu_event3_id	XP PMU Event 3 ID; see pmu_event0_id for encodings	RW	9'b0
[47:41]	Reserved	Reserved	RO	-
[40:32]	pmu_event2_id	XP PMU Event 2 ID; see pmu_event0_id for encodings	RW	9'b0
[31:25]	Reserved	Reserved	RO	-
[24:16]	pmu_event1_id	XP PMU Event 1 ID; see pmu_event0_id for encodings	RW	9'b0
[15:9]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[8:0]	pmu_event0_id	<p>XP PMU Event 0 ID Bits [8:5]:</p> <p>4'b0000 REQ; REQ channel when POR_REQ_VC_NUM_PARAM = 1 ; REQ Sub-channel 1: when POR_REQ_VC_NUM_PARAM > 1</p> <p>4'b0001 RSP; RSP channel when POR_RSP_VC_NUM_PARAM = 1 ; RSP Sub-channel 1: when POR_RSP_VC_NUM_PARAM > 1</p> <p>4'b0010 SNP; SNP channel when POR_SNP_VC_NUM_PARAM = 1 ; SNP Sub-channel 1: when POR_SNP_VC_NUM_PARAM > 1</p> <p>4'b0011 DAT; DAT channel when POR_DAT_VC_NUM_PARAM = 1 ; DAT Sub-channel 1: when POR_DAT_VC_NUM_PARAM > 1</p> <p>4'b0100 PUB</p> <p>4'b0101 RSP2; RSP Sub-channel 2: Applicable when POR_RSP_VC_NUM_PARAM > 1</p> <p>4'b0110 DAT2; DAT Sub-channel 2: Applicable when POR_DAT_VC_NUM_PARAM > 1</p> <p>4'b0111 REQ2; REQ Sub-channel 2: Applicable when POR_REQ_VC_NUM_PARAM > 1</p> <p>4'b1000 SNP2; SNP Sub-channel 2: Applicable when POR_SNP_VC_NUM_PARAM > 1</p> <p>4'b1100 AXI W Subordinate Error</p> <p>4'b1101 AXI W Decode Error</p> <p>4'b1110 PA out of range Error</p> <p>3'b000 East when NUM_XP > 1 ; Device port 0 when NUM_XP == 1 (Single XP config)</p> <p>3'b001 West when NUM_XP > 1 ; Device port 1 when NUM_XP == 1 (Single XP config)</p> <p>3'b010 North when NUM_XP > 1 ; Device port 2 when NUM_XP == 1 (Single XP config)</p> <p>3'b011 South when NUM_XP > 1 ; Device port 3 when NUM_XP == 1 (Single XP config)</p> <p>3'b100 Device port 0 when NUM_XP > 1 ; Device port 4 when NUM_XP == 1 (Single XP config)</p> <p>3'b101 Device port 1 when NUM_XP > 1 ; Device port 5 when NUM_XP == 1 (Single XP config)</p> <p>3'b110 Device port 2 when NUM_XP > 1 ; No Selection when NUM_XP == 1 (Single XP config)</p> <p>3'b111 Device port 3 when NUM_XP > 1 ; No Selection when NUM_XP == 1 (Single XP config)</p> <p>Bits [1:0]: Event specifier</p> <p>2'b00 No event</p> <p>2'b01 TX flit valid; signaled when a flit is successfully transmitted</p> <p>2'b10 TX flit stall; signaled when flit transmission is stalled and waiting on credits</p> <p>2'b11 Partial DAT flit; signaled when 128-bit DAT flits could not be merged into a 256-bit DAT flit; only applicable on the DAT PC on RN-F CHIA and RN-F CHIA ESAM ports</p>	RW	9'b0

4.3.13.22 por_mxp_errfr

Functions as the error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3000

Type

RO

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.ras_secure_access_override`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-517: por_mxp_errfr

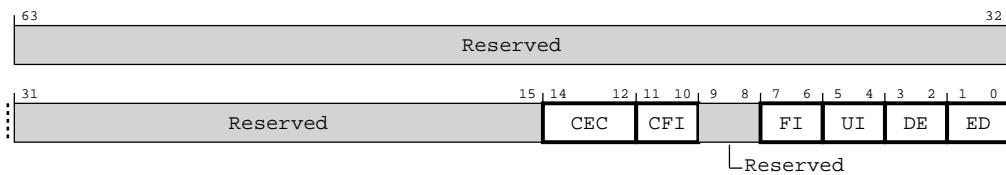


Table 4-533: por_mxp_errfr attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors for data poison	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.13.23 por_mxp_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3008

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-518: por_mxp_errctlr

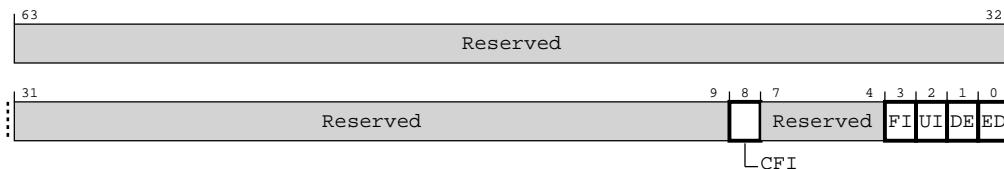


Table 4-534: por_mxp_errctlr attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_mxp_errfr.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mxp_errfr.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_mxp_errfr.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_mxp_errfr.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_mxp_errfr.ED	RW	1'b0

4.3.13.24 por_mxp_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3010

Type

W1C

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-519: por_mxp_errstatus

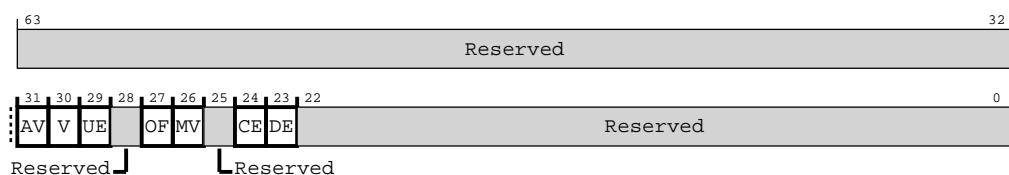


Table 4-535: por_mxp_errstatus attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid 1'b0 Address is not valid	W1C	1'b0

Bits	Name	Description	Type	Reset
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	por_mxp_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.13.25 por_mxp_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16' h3028

Type

RW

Reset value

See individual bit resets

Secure group override

por mxp secure register groups override.ras secure access override

Usage constraints

Only accessible by Secure access.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-520: por mxp errmisc

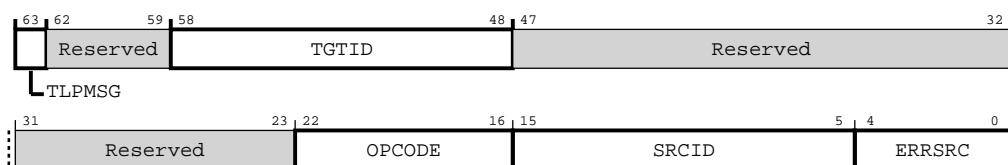


Table 4-536: por_mxp_errmisc attributes

Bits	Name	Description	Type	Reset
[63]	TLPMSG	Error flit TLPMSG Status	RW	1'b0
[62:59]	Reserved	Reserved	RO	-
[58:48]	TGTID	Error flit target ID	RW	11'b0
[47:23]	Reserved	Reserved	RO	-
[22:16]	OPCODE	Error flit opcode	RW	7'b0
[15:5]	SRCID	Error flit source ID	RW	11'b0

Bits	Name	Description	Type	Reset																								
[4:0]	ERRSRC	<p>Error source for Mesh With Replicated Channels: Bits [4:2]: Transaction type</p> <table> <tr><td>3'b000</td><td>REQ</td></tr> <tr><td>3'b001</td><td>RSP</td></tr> <tr><td>3'b010</td><td>SNP</td></tr> <tr><td>3'b011</td><td>DAT</td></tr> <tr><td>3'b100</td><td>REQ2</td></tr> <tr><td>3'b101</td><td>RSP2</td></tr> <tr><td>3'b110</td><td>SNP2</td></tr> <tr><td>3'b111</td><td>DAT2</td></tr> </table> <p>Bits [1:0]: Port</p> <table> <tr><td>2'b00</td><td>Port 0</td></tr> <tr><td>2'b01</td><td>Port 1</td></tr> <tr><td>2'b10</td><td>Port 2</td></tr> <tr><td>2'b11</td><td>Port 3</td></tr> </table>	3'b000	REQ	3'b001	RSP	3'b010	SNP	3'b011	DAT	3'b100	REQ2	3'b101	RSP2	3'b110	SNP2	3'b111	DAT2	2'b00	Port 0	2'b01	Port 1	2'b10	Port 2	2'b11	Port 3	RW	5'b0
3'b000	REQ																											
3'b001	RSP																											
3'b010	SNP																											
3'b011	DAT																											
3'b100	REQ2																											
3'b101	RSP2																											
3'b110	SNP2																											
3'b111	DAT2																											
2'b00	Port 0																											
2'b01	Port 1																											
2'b10	Port 2																											
2'b11	Port 3																											
[4:0]	ERRSRC	<p>Mesh Without Replicated Channels: Bits [4:2]: Transaction type</p> <table> <tr><td>3'b000</td><td>REQ</td></tr> <tr><td>3'b001</td><td>RSP</td></tr> <tr><td>3'b010</td><td>SNP</td></tr> <tr><td>3'b011</td><td>DAT</td></tr> <tr><td>3'b100</td><td>Reserved</td></tr> <tr><td>3'b101</td><td>Reserved</td></tr> <tr><td>3'b110</td><td>Reserved</td></tr> <tr><td>3'b111</td><td>Reserved</td></tr> </table> <p>Bits [1:0]: Port</p> <table> <tr><td>2'b00</td><td>Port 0</td></tr> <tr><td>2'b01</td><td>Port 1</td></tr> <tr><td>2'b10</td><td>Port 2</td></tr> <tr><td>2'b11</td><td>Port 3</td></tr> </table>	3'b000	REQ	3'b001	RSP	3'b010	SNP	3'b011	DAT	3'b100	Reserved	3'b101	Reserved	3'b110	Reserved	3'b111	Reserved	2'b00	Port 0	2'b01	Port 1	2'b10	Port 2	2'b11	Port 3	RW	5'b0
3'b000	REQ																											
3'b001	RSP																											
3'b010	SNP																											
3'b011	DAT																											
3'b100	Reserved																											
3'b101	Reserved																											
3'b110	Reserved																											
3'b111	Reserved																											
2'b00	Port 0																											
2'b01	Port 1																											
2'b10	Port 2																											
2'b11	Port 3																											

4.3.13.26 por_mxp_p0-5_byte_par_err_inj

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the byte parity error injection register for XP port #{{index}}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3030 + #{8*index}

Type

WO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-521: por_mxp_p0-5_byte_par_err_inj

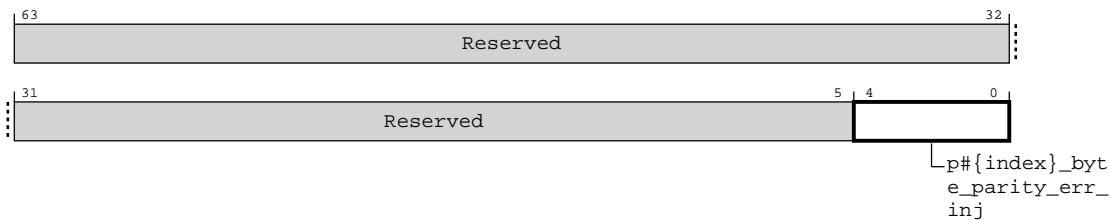


Table 4-537: por_mxp_p0-5_byte_par_err_inj attributes

Bits	Name	Description	Type	Reset
[63:5]	Reserved	Reserved	RO	-
[4:0]	p#{index}_byte_parity_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next DAT flit upload NOTE: Only applicable if an RN-F is attached to port #{index}. Byte parity error is only injected if the RN-F is configured to not support Datacheck.	WO	5'h00

4.3.13.27 por_mxp_errfr_NS

Functions as the Non-secure error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3100

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-522: por_mxp_errfr_NS

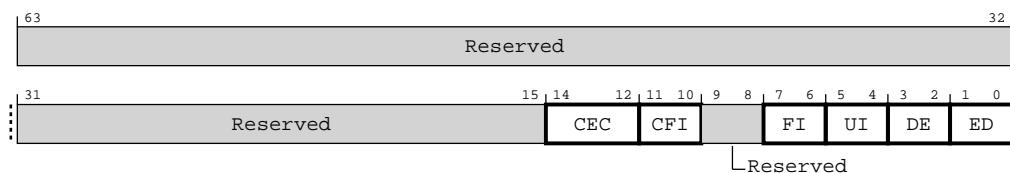


Table 4-538: por_mxp_errfr_NS attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors for data poison	RO	2'b01
[1:0]	ED	Error detection	RO	2'b01

4.3.13.28 por_mxp_errctr_NS

Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferral are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3108

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-523: por_mxp_errctlr_NS

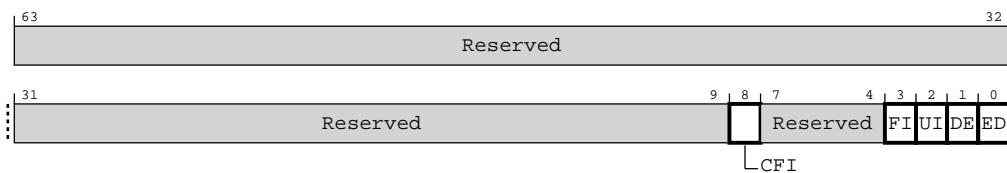


Table 4-539: por_mxp_errctlr_NS attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_mxp_errfr_NS.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mxp_errfr_NS.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_mxp_errfr_NS.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_mxp_errfr_NS.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_mxp_errfr_NS.ED	RW	1'b0

4.3.13.29 por_mxp_errstatus_NS

Functions as the Non-secure error status register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3110

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-524: por_mxp_errstatus_NS

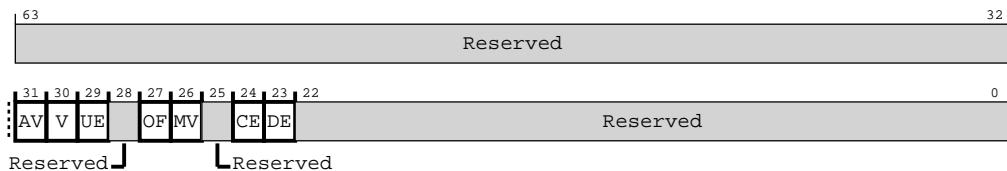


Table 4-540: por_mxp_errstatus_NS attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Bits	Name	Description	Type	Reset
[26]	MV	por_mxp_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.13.30 por_mxp_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3128

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-525: por_mxp_errmisc_NS

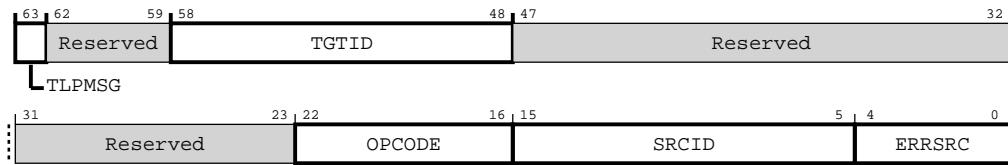


Table 4-541: por_mxp_errmisc_NS attributes

Bits	Name	Description	Type	Reset
[63]	TLPMSG	Error flit TLPMSG Status	RW	1'b0
[62:59]	Reserved	Reserved	RO	-
[58:48]	TGTID	Error flit target ID	RW	11'b0
[47:23]	Reserved	Reserved	RO	-
[22:16]	OPCODE	Error flit opcode	RW	7'b0
[15:5]	SRCID	Error flit source ID	RW	11'b0
[4:0]	ERRSRC	Error source for Mesh With Replicated Channels: Bits [4:2]: Transaction type 3'b000 REQ 3'b001 RSP 3'b010 SNP 3'b011 DAT 3'b100 REQ2 3'b101 RSP2 3'b110 SNP2 3'b111 DAT2 Bits [1:0]: Port 2'b00 Port 0 2'b01 Port 1 2'b10 Port 2 2'b11 Port 3	RW	5'b0

Bits	Name	Description	Type	Reset
[4:0]	ERRSRC	Mesh Without Replicated Channels: Bits [4:2]: Transaction type 3'b000 REQ 3'b001 RSP 3'b010 SNP 3'b011 DAT 3'b100 Reserved 3'b101 Reserved 3'b110 Reserved 3'b111 Reserved Bits [1:0]: Port 2'b00 Port 0 2'b01 Port 1 2'b10 Port 2 2'b11 Port 3	RW	5'b0

4.3.13.31 por_mxp_p0-5_syscoreq_ctl

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the port #{{index}} snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p#{{index}}_syscoack_status. NOTE: Only valid on RN-F ports.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C00 + #{16*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.syscoreq_ctl

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-526: por_mxp_p0-5_syscoreq_ctl

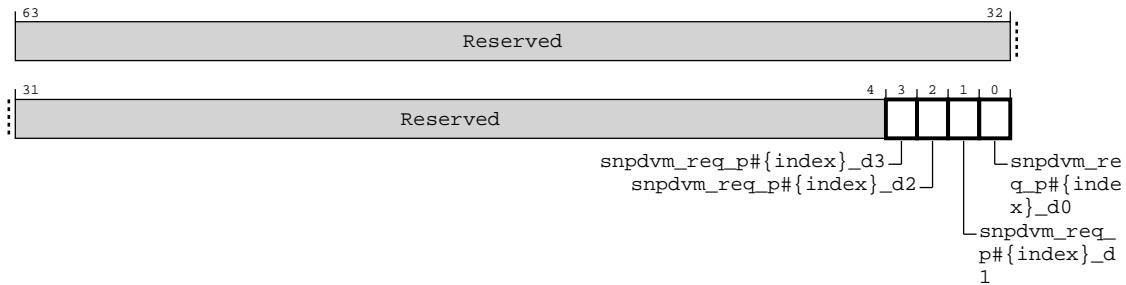


Table 4-542: por_mxp_p0-5_syscoreq_ctl attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	snpdvm_req_p#{index}_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port #{index}	RW	1'b0
[2]	snpdvm_req_p#{index}_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port #{index}	RW	1'b0
[1]	snpdvm_req_p#{index}_d1	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port #{index}	RW	1'b0
[0]	snpdvm_req_p#{index}_d0	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port #{index}	RW	1'b0

4.3.13.32 por_mxp_p0-5_syscoack_status

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the port #{index} snoop and DVM domain status register. Provides a software alternative to hardware SYSREQ/SYSACK handshake. Works with por_mxp_p#{index}_syscoreq_ctl. NOTE: Only valid on RN-F ports.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16'h1C08 + \#(16*index)$

Type

RO

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.syscoreq_ctl`

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-527: por_mxp_p0-5_syscoack_status

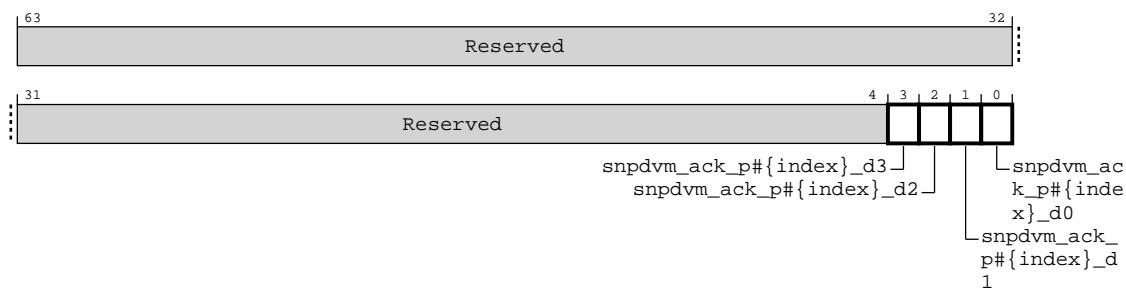


Table 4-543: por_mxp_p0-5_syscoack_status attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	snpdvm_ack_p#{index}_d3	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port #{index}	RO	1'b0
[2]	snpdvm_ack_p#{index}_d2	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port #{index}	RO	1'b0
[1]	snpdvm_ack_p#{index}_d1	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port #{index}	RO	1'b0
[0]	snpdvm_ack_p#{index}_d0	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port #{index}	RO	1'b0

4.3.13.33 por_dtm_control

Functions as the DTM control register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2100`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-528: por_dtm_control

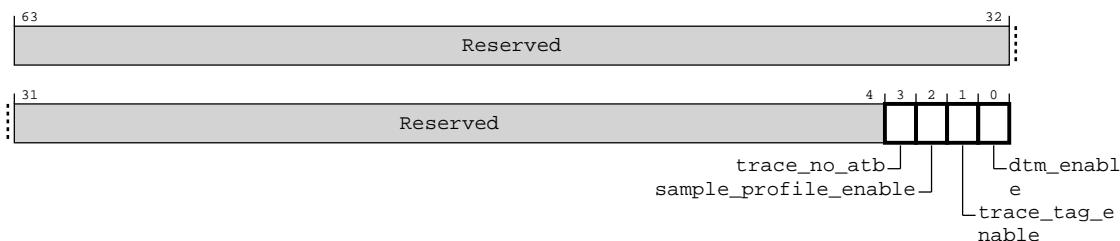


Table 4-544: por_dtm_control attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	trace_no_atb	When set, trace packet is not delivered out of ATB, and FIFO entry holds the first trace packet. NOTE: if any MXP has this bit set, ATB protocol will not be functional.	RW	1'b0
[2]	sample_profile_enable	Enables sample profile function	RW	1'b0
[1]	trace_tag_enable	Watchpoint trace tag enable 1'b1: Trace tag enabled 1'b0: No trace tag	RW	1'b0
[0]	dtm_enable	Enables debug watchpoint and PMU function; prior to writing this bit, all other DT configuration registers must be programmed; once this bit is set, other DT configuration registers must not be modified	RW	1'b0

4.3.13.34 por_dtm_fifo_entry_ready

Controls status of DTM FIFO entries.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2118

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-529: por_dtm_fifo_entry_ready

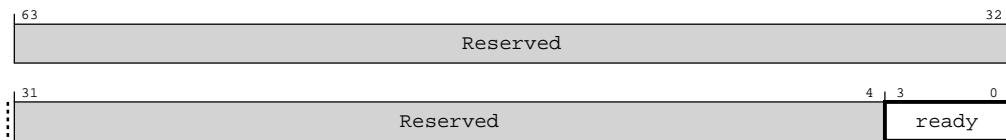


Table 4-545: por_dtm_fifo_entry_ready attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3:0]	ready	Indicates which DTM FIFO entries are ready; write a 1 to clear Bit [3]: Entry 3 ready when set Bit [2]: Entry 2 ready when set Bit [1]: Entry 1 ready when set Bit [0]: Entry 0 ready when set	W1C	4'b0

4.3.13.35 por_dtm_fifo_entry0-3_0

There are 4 iterations of this register. The index ranges from 0 to 3. Contains DTM FIFO entry #{{index}} data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2120 + #{24*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-530: por_dtm_fifo_entry0-3_0

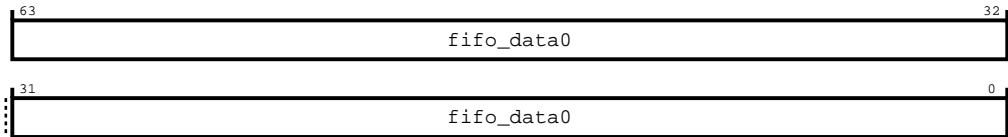


Table 4-546: por_dtm_fifo_entry0-3_0 attributes

Bits	Name	Description	Type	Reset
[63:0]	fifo_data0	Entry data bit vector 63:0	RO	64'b0

4.3.13.36 por_dtm_fifo_entry0-3_1

There are 4 iterations of this register. The index ranges from 0 to 3. Contains DTM FIFO entry #{{index}} data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2128 + #{24*index}`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-531: por_dtm_fifo_entry0-3_1

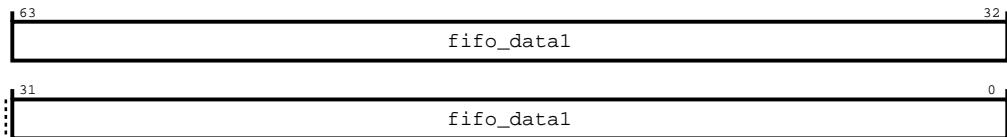


Table 4-547: por_dtm_fifo_entry0-3_1 attributes

Bits	Name	Description	Type	Reset
[63:0]	fifo_data1	Entry data bit vector 127:64	RO	64'b0

4.3.13.37 por_dtm_fifo_entry0-3_2

There are 4 iterations of this register. The index ranges from 0 to 3. Contains DTM FIFO entry #*{index}* data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2130 + # {24*index}

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-532: por_dtm_fifo_entry0-3_2



Table 4-548: por_dtm_fifo_entry0-3_2 attributes

Bits	Name	Description	Type	Reset
[63:48]	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
[47:0]	fifo_data2	Entry data bit vector 143:128	RO	48'b0

4.3.13.38 por_dtm_wp0-3_config

There are 4 iterations of this register. The index ranges from 0 to 3. Configures watchpoint #{{index}}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h21A0 + #{{24*index}}

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-533: por_dtm_wp0-3_config

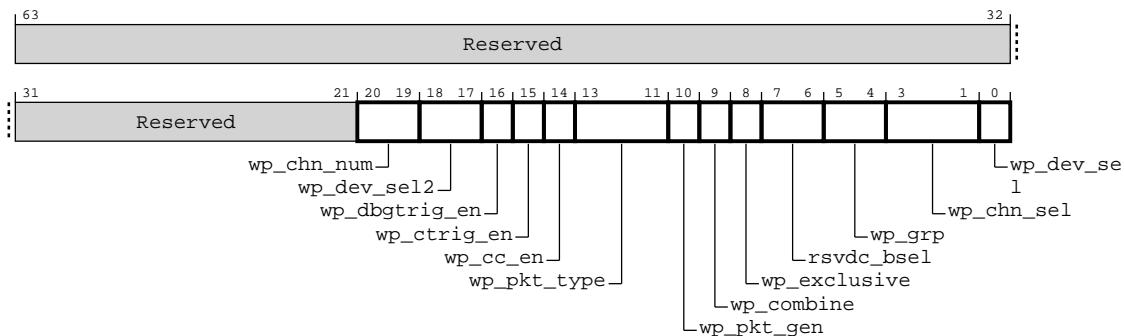


Table 4-549: por_dtm_wp0-3_config attributes

Bits	Name	Description	Type	Reset
[63:21]	Reserved	Reserved	RO	-
[20:19]	wp_chn_num	VC number index for replicated channels in specified SMXP	RW	2'b0
[18:17]	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
[16]	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
[15]	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
[14]	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
[13:11]	wp_pkt_type	Trace packet type	RW	3'b000
		3'b000 TXNID (up to X18) 3'b001 TXNID + opcode (up to X9) 3'b010 TXNID + opcode + source ID + target ID (up to X4) 3'b011 Reserved 3'b100 Control flit 3'b101 DAT flit DATA [127:0] 3'b110 DAT flit DATA [255:128] 3'b111 Reserved		
[10]	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
[9]	wp_combine	Enables combination of watchpoints #{{index}} and #{{index+1}}	RW	1'b0
[8]	wp_exclusive	Watchpoint mode	RW	1'b0
		1'b0 Regular mode 1'b1 Exclusive mode		
[7:6]	rsvdc_bsel	Byte select of RSVDC in trace packet	RW	1'b0
		2'h0 Select RSVDC[7:0] 2'h1 Select RSVDC[15:8] 2'h2 Select RSVDC[23:16] 2'h3 Select RSVDC[31:24]		
[5:4]	wp_grp	Watchpoint register format group	RW	1'b0
		2'h0 Select primary group 2'h1 Select secondary group 2'h2 Select tertiary group 2'h3 Reserved		
[3:1]	wp_chn_sel	VC selection	RW	3'b000
		3'b000 Select REQ VC 3'b001 Select RSP VC 3'b010 Select SNP VC 3'b011 Select DATA VC All other values are reserved.		
[0]	wp_dev_sel	Device port selection in specified SMXP	RW	1'b0
		1'b0 Select device port 0 1'b1 Select device port 1		

4.3.13.39 por_dtm_wp0-3_val

There are 4 iterations of this register. The index ranges from 0 to 3. Configures watchpoint #{{index}} comparison value.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h21A8 + #{24*index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-534: por_dtm_wp0-3_val

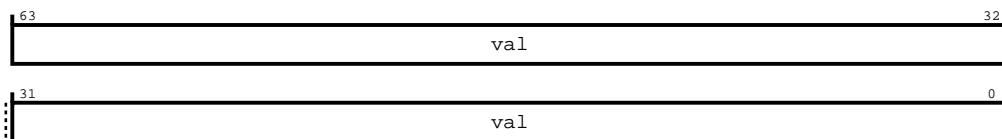


Table 4-550: por_dtm_wp0-3_val attributes

Bits	Name	Description	Type	Reset
[63:0]	val	Refer to DTM watchpoint section for details	RW	64'b0

4.3.13.40 por_dtm_wp0-3_mask

There are 4 iterations of this register. The index ranges from 0 to 3. Configures watchpoint #{{index}} comparison mask.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h21B0 + #{24*index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-535: por_dtm_wp0-3_mask

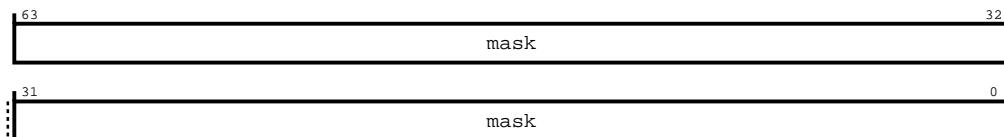


Table 4-551: por_dtm_wp0-3_mask attributes

Bits	Name	Description	Type	Reset
[63:0]	mask	Refer to DTM watchpoint section for details	RW	64'b0

4.3.13.41 por_dtm_pmsicr

Functions as the sampling interval counter register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2200`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-536: por_dtm_pmsicr

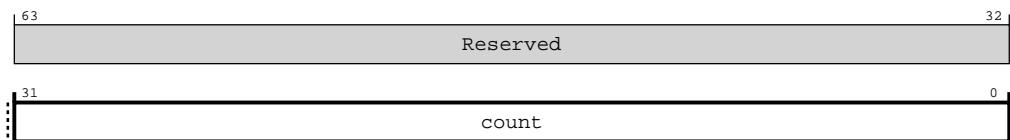


Table 4-552: por_dtm_pmsicr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	count	Current value of sample counter	RW	32'b0

4.3.13.42 por_dtm_pmsirr

Functions as the sampling interval reload register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2208

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-537: por_dtm_pmsirr

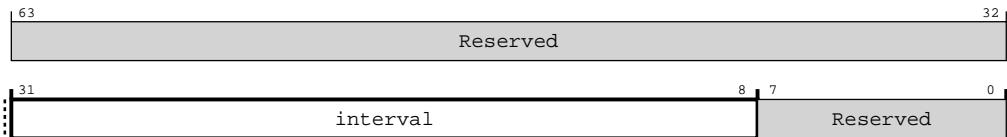


Table 4-553: por_dtm_pmsirr attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:8]	interval	Sampling interval to be reloaded	RW	24'b0
[7:0]	Reserved	Reserved	RO	-

4.3.13.43 por_dtm_pmu_config

Configures the DTM PMU.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2210

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-538: por_dtm_pmu_config

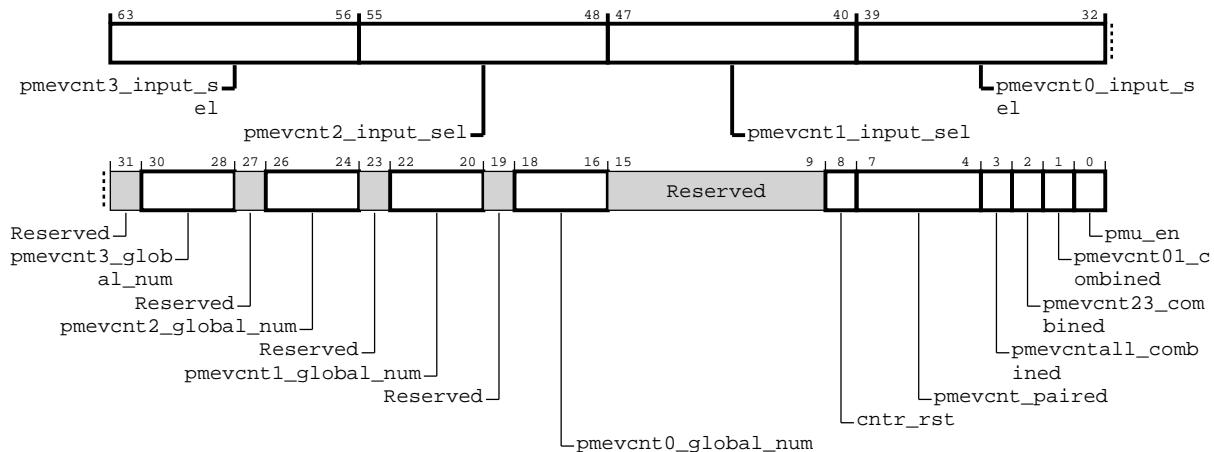


Table 4-554: por_dtm_pmu_config attributes

Bits	Name	Description	Type	Reset
[63:56]	pmevcnt3_input_sel	Source to be counted in PMU counter 3; see pmevcnt0_input_sel for encodings	RW	8'b0
[55:48]	pmevcnt2_input_sel	Source to be counted in PMU counter 2; see pmevcnt0_input_sel for encodings	RW	8'b0
[47:40]	pmevcnt1_input_sel	Source to be counted in PMU counter 1; see pmevcnt0_input_sel for encodings	RW	8'b0
[39:32]	pmevcnt0_input_sel	Source to be counted in PMU counter 0: Port2, Port3, Port4 and Port5 encodings are applicable when (MXP_NUM_DEV_PORT_PARAM > 2 and MXP_MULTIPLE_DTM_EN_PARAM = 0)	RW	8'b0
		8'h00 Watchpoint 0 8'h01 Watchpoint 1 8'h02 Watchpoint 2 8'h03 Watchpoint 3 8'h04 XP PMU Event 0 8'h05 XP PMU Event 1 8'h06 XP PMU Event 2 8'h07 XP PMU Event 3		
[39:32]	pmevcnt0_input_sel	8'h10 Port 0 Device 0 PMU Event 0 8'h11 Port 0 Device 0 PMU Event 1 8'h12 Port 0 Device 0 PMU Event 2 8'h13 Port 0 Device 0 PMU Event 3 8'h14 Port 0 Device 1 PMU Event 0 8'h15 Port 0 Device 1 PMU Event 1 8'h16 Port 0 Device 1 PMU Event 2 8'h17 Port 0 Device 1 PMU Event 3 8'h18 Port 0 Device 2 PMU Event 0 8'h19 Port 0 Device 2 PMU Event 1 8'h1A Port 0 Device 2 PMU Event 2 8'h1B Port 0 Device 2 PMU Event 3 8'h1C Port 0 Device 3 PMU Event 0 8'h1D Port 0 Device 3 PMU Event 1 8'h1E Port 0 Device 3 PMU Event 2 8'h1F Port 0 Device 3 PMU Event 3	RW	8'b0

Bits	Name	Description	Type	Reset
[39:32]	pmevcnt0_input_sel	8'h20 Port 1 Device 0 PMU Event 0 8'h21 Port 1 Device 0 PMU Event 1 8'h22 Port 1 Device 0 PMU Event 2 8'h23 Port 1 Device 0 PMU Event 3 8'h24 Port 1 Device 1 PMU Event 0 8'h25 Port 1 Device 1 PMU Event 1 8'h26 Port 1 Device 1 PMU Event 2 8'h27 Port 1 Device 1 PMU Event 3 8'h28 Port 1 Device 2 PMU Event 0 8'h29 Port 1 Device 2 PMU Event 1 8'h2A Port 1 Device 2 PMU Event 2 8'h2B Port 1 Device 2 PMU Event 3 8'h2C Port 1 Device 3 PMU Event 0 8'h2D Port 1 Device 3 PMU Event 1 8'h2E Port 1 Device 3 PMU Event 2 8'h2F Port 1 Device 3 PMU Event 3	RW	8'b0
[39:32]	pmevcnt0_input_sel	8'h30 Port 2 Device 0 PMU Event 0 8'h31 Port 2 Device 0 PMU Event 1 8'h32 Port 2 Device 0 PMU Event 2 8'h33 Port 2 Device 0 PMU Event 3 8'h34 Port 2 Device 1 PMU Event 0 8'h35 Port 2 Device 1 PMU Event 1 8'h36 Port 2 Device 1 PMU Event 2 8'h37 Port 2 Device 1 PMU Event 3 8'h38 Port 2 Device 2 PMU Event 0 8'h39 Port 2 Device 2 PMU Event 1 8'h3A Port 2 Device 2 PMU Event 2 8'h3B Port 2 Device 2 PMU Event 3 8'h3C Port 2 Device 3 PMU Event 0 8'h3D Port 2 Device 3 PMU Event 1 8'h3E Port 2 Device 3 PMU Event 2 8'h3F Port 2 Device 3 PMU Event 3	RW	8'b0
[39:32]	pmevcnt0_input_sel	8'h40 Port 3 Device 0 PMU Event 0 8'h41 Port 3 Device 0 PMU Event 1 8'h42 Port 3 Device 0 PMU Event 2 8'h43 Port 3 Device 0 PMU Event 3 8'h44 Port 3 Device 1 PMU Event 0 8'h45 Port 3 Device 1 PMU Event 1 8'h46 Port 3 Device 1 PMU Event 2 8'h47 Port 3 Device 1 PMU Event 3 8'h48 Port 3 Device 2 PMU Event 0 8'h49 Port 3 Device 2 PMU Event 1 8'h4A Port 3 Device 2 PMU Event 2 8'h4B Port 3 Device 2 PMU Event 3 8'h4C Port 3 Device 3 PMU Event 0 8'h4D Port 3 Device 3 PMU Event 1 8'h4E Port 3 Device 3 PMU Event 2 8'h4F Port 3 Device 3 PMU Event 3	RW	8'b0

Bits	Name	Description	Type	Reset
[39:32]	pmevcnt0_input_sel	8'h50 Port 4 Device 0 PMU Event 0 8'h51 Port 4 Device 0 PMU Event 1 8'h52 Port 4 Device 0 PMU Event 2 8'h53 Port 4 Device 0 PMU Event 3 8'h54 Port 4 Device 1 PMU Event 0 8'h55 Port 4 Device 1 PMU Event 1 8'h56 Port 4 Device 1 PMU Event 2 8'h57 Port 4 Device 1 PMU Event 3 8'h58 Port 4 Device 2 PMU Event 0 8'h59 Port 4 Device 2 PMU Event 1 8'h5A Port 4 Device 2 PMU Event 2 8'h5B Port 4 Device 2 PMU Event 3 8'h5C Port 4 Device 3 PMU Event 0 8'h5D Port 4 Device 3 PMU Event 1 8'h5E Port 4 Device 3 PMU Event 2 8'h5F Port 4 Device 3 PMU Event 3	RW	8'b0
[39:32]	pmevcnt0_input_sel	8'h60 Port 5 Device 0 PMU Event 0 8'h61 Port 5 Device 0 PMU Event 1 8'h62 Port 5 Device 0 PMU Event 2 8'h63 Port 5 Device 0 PMU Event 3 8'h64 Port 5 Device 1 PMU Event 0 8'h65 Port 5 Device 1 PMU Event 1 8'h66 Port 5 Device 1 PMU Event 2 8'h67 Port 5 Device 1 PMU Event 3 8'h68 Port 5 Device 2 PMU Event 0 8'h69 Port 5 Device 2 PMU Event 1 8'h6A Port 5 Device 2 PMU Event 2 8'h6B Port 5 Device 2 PMU Event 3 8'h6C Port 5 Device 3 PMU Event 0 8'h6D Port 5 Device 3 PMU Event 1 8'h6E Port 5 Device 3 PMU Event 2 8'h6F Port 5 Device 3 PMU Event 3	RW	8'b0
[31]	Reserved	Reserved	RO	-
[30:28]	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
[27]	Reserved	Reserved	RO	-
[26:24]	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
[23]	Reserved	Reserved	RO	-
[22:20]	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0
[19]	Reserved	Reserved	RO	-
[18:16]	pmevcnt0_global_num	Global counter to pair with PMU counter 0	RW	3'b0
		3'b000 Global PMU event counter A 3'b001 Global PMU event counter B 3'b010 Global PMU event counter C 3'b011 Global PMU event counter D 3'b100 Global PMU event counter E 3'b101 Global PMU event counter F 3'b110 Global PMU event counter G 3'b111 Global PMU event counter H		
[15:9]	Reserved	Reserved	RO	-
[8]	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0

Bits	Name	Description	Type	Reset
[7:4]	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
[3]	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
[2]	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
[1]	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
[0]	pmu_en	DTM PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

4.3.13.44 por_dtm_pmevcnt

Contains all PMU event counters (0, 1, 2, 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2220

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-539: por_dtm_pmevcnt

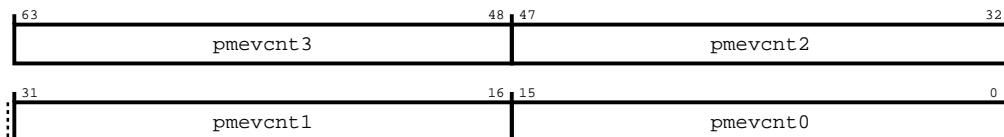


Table 4-555: por_dtm_pmevcnt attributes

Bits	Name	Description	Type	Reset
[63:48]	pmevcnt3	PMU event counter 3	RW	16'h0000
[47:32]	pmevcnt2	PMU event counter 2	RW	16'h0000

Bits	Name	Description	Type	Reset
[31:16]	pmevcnt1	PMU event counter 1	RW	16'h0000
[15:0]	pmevcnt0	PMU event counter 0	RW	16'h0000

4.3.13.45 por_dtm_pmevcntsr

Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2240

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-540: por_dtm_pmevcntsr

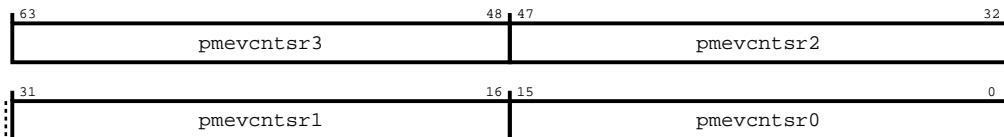


Table 4-556: por_dtm_pmevcntsr attributes

Bits	Name	Description	Type	Reset
[63:48]	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
[47:32]	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000
[31:16]	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
[15:0]	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

4.3.13.46 por_dtm_control_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Functions as the DTM control register. NOTE: There will be max. of 3 DTM registers based on MXP_MULTIPLE_DTM_EN_PARAM and MXP_NUM_DEV_PORT_PARAM value. Each successive DTM register will be at the next 'h200 + 8 byte address boundary. Each successive DTM register will be named with the suffix corresponding to the DT register number. For example por_dtm_control_dt<0:3>

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2100 + # {512 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-541: por_dtm_control_dt1-3

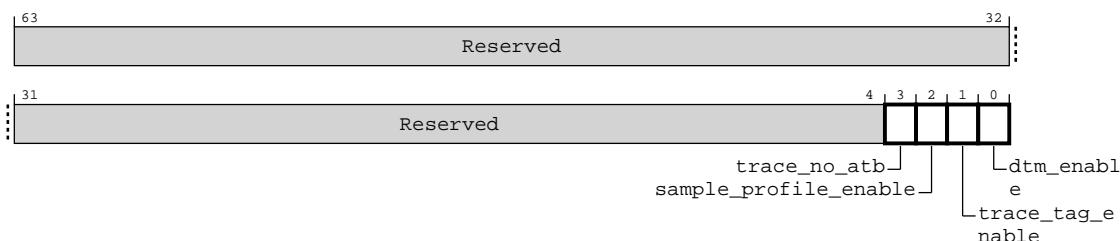


Table 4-557: por_dtm_control_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	trace_no_atb	When set, trace packet is not delivered out of ATB, and FIFO entry holds the first trace packet	RW	1'b0
[2]	sample_profile_enable	Enables sample profile function	RW	1'b0

Bits	Name	Description	Type	Reset
[1]	trace_tag_enable	Watchpoint trace tag enable 1'b1: Trace tag enabled 1'b0: No trace tag	RW	1'b0
[0]	dtm_enable	Enables debug watchpoint and PMU function; prior to writing this bit, all other DT configuration registers must be programmed; once this bit is set, other DT configuration registers must not be modified	RW	1'b0

4.3.13.47 por_dtm_fifo_entry_ready_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Controls status of DTM FIFO entries.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2118 + #{512*index}

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-542: por_dtm_fifo_entry_ready_dt1-3

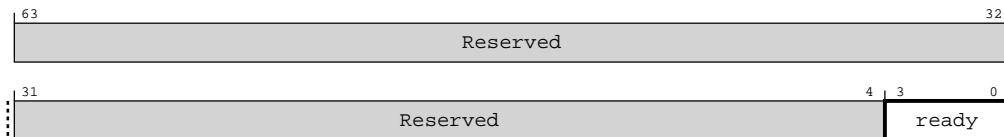


Table 4-558: por_dtm_fifo_entry_ready_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3:0]	ready	Indicates which DTM FIFO entries are ready; write a 1 to clear Bit [3]: Entry 3 ready when set Bit [2]: Entry 2 ready when set Bit [1]: Entry 1 ready when set Bit [0]: Entry 0 ready when set	W1C	4'b0

4.3.13.48 por_dtm_fifo_entry0-11%4_0_dt(0-11/4)+1

There are 12 iterations of this register. The index ranges from 0 to 11. Contains DTM FIFO entry $\#\{index\%4\}$ data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2120 + #{24*(index%4)} + #{512*((index/4)+1)}`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-543: por_dtm_fifo_entry0-11%4_0_dt(0-11/4)+1

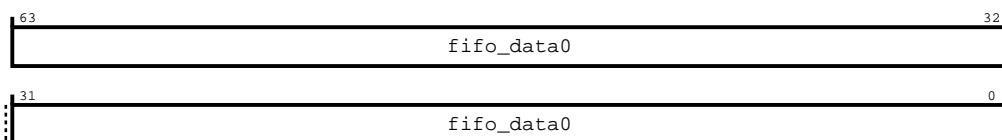


Table 4-559: por_dtm_fifo_entry0-11%4_0_dt(0-11/4)+1 attributes

Bits	Name	Description	Type	Reset
[63:0]	fifo_data0	Entry data bit vector 63:0	RO	64'b0

4.3.13.49 por_dtm_fifo_entry0-11%4_1_dt(0-11/4)+1

There are 12 iterations of this register. The index ranges from 0 to 11. Contains DTM FIFO entry $\#\{index\%4\}$ data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16'h2128 + \#\{24 * (\text{index}\%4)\} + \#\{512 * ((\text{index}/4)+1)\}$

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-544: por_dtm_fifo_entry0-11%4_1_dt(0-11/4)+1

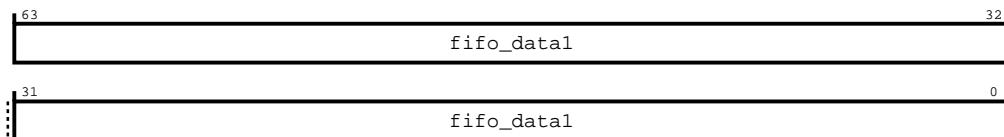


Table 4-560: por_dtm_fifo_entry0-11%4_1_dt(0-11/4)+1 attributes

Bits	Name	Description	Type	Reset
[63:0]	fifo_data1	Entry data bit vector 127:64	RO	64'b0

4.3.13.50 por_dtm_fifo_entry0-11%4_2_dt(0-11/4)+1

There are 12 iterations of this register. The index ranges from 0 to 11. Contains DTM FIFO entry $\#\{\text{index}\%4\}$ data.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16'h2130 + \#\{24 * (\text{index}\%4)\} + \#\{512 * ((\text{index}/4)+1)\}$

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-545: por_dtm_fifo_entry0-11%4_2_dt(0-11/4)+1

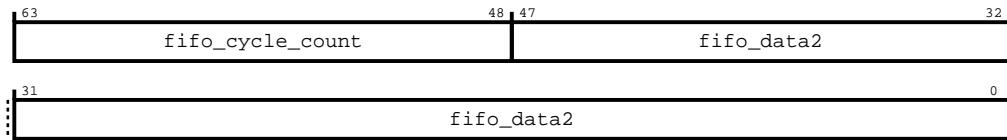


Table 4-561: por_dtm_fifo_entry0-11%4_2_dt(0-11/4)+1 attributes

Bits	Name	Description	Type	Reset
[63:48]	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
[47:0]	fifo_data2	Entry data bit vector 143:128	RO	48'b0

4.3.13.51 por_dtm_wp0-11%4_config_dt(0-11/4)+1

There are 12 iterations of this register. The index ranges from 0 to 11. Configures watchpoint #{{index%4}}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h21A0 + #{24*(index%4)} + #{512*((index/4)+1)}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-546: por_dtm_wp0-11%4_config_dt(0-11/4)+1

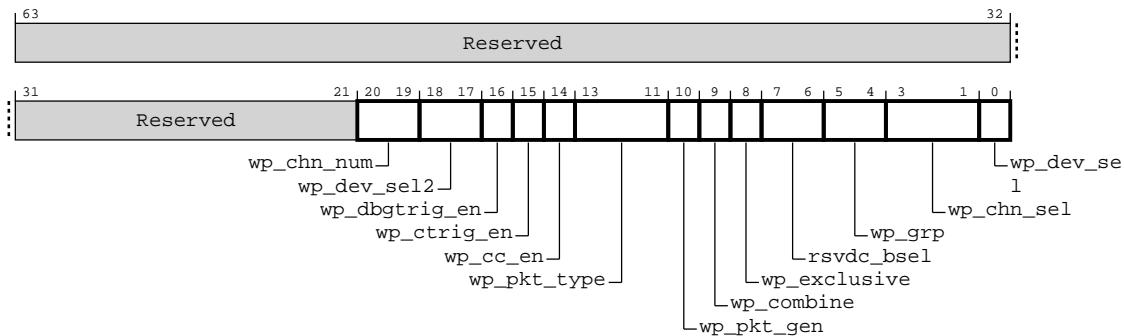


Table 4-562: por_dtm_wp0-11%4_config_dt(0-11/4)+1 attributes

Bits	Name	Description	Type	Reset
[63:21]	Reserved	Reserved	RO	-
[20:19]	wp_chn_num	VC number index for replicated channels in specified SMXP	RW	2'b0
[18:17]	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
[16]	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
[15]	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
[14]	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
[13:11]	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
[10]	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
[9]	wp_combine	Enables combination of watchpoints #{{index%4}} and #{{(index%4)+1}}	RW	1'b0
[8]	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
[7:6]	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
[5:4]	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0
[3:1]	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
[0]	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

4.3.13.52 por_dtm_wp0-11%4_val_dt(0-11/4)+1

There are 12 iterations of this register. The index ranges from 0 to 11. Configures watchpoint #{{index%4}} comparison value.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h21A8 + #{24*(index%4)} + #{512*((index/4)+1)}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-547: por_dtm_wp0-11%4_val_dt(0-11/4)+1

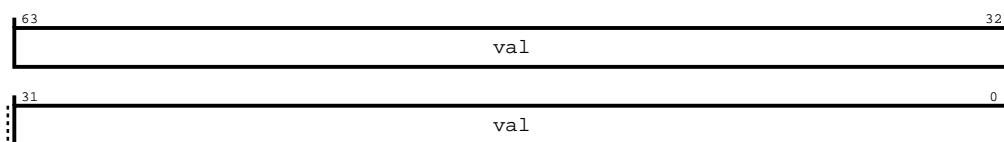


Table 4-563: por_dtm_wp0-11%4_val_dt(0-11/4)+1 attributes

Bits	Name	Description	Type	Reset
[63:0]	val	Refer to DTM watchpoint section for details	RW	64'b0

4.3.13.53 por_dtm_wp0-11%4_mask_dt(0-11/4)+1

There are 12 iterations of this register. The index ranges from 0 to 11. Configures watchpoint #{{index%4}} comparison mask.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h21B0 + #{24*(index%4)} + #{512*((index/4)+1)}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-548: por_dtm_wp0-11%4_mask_dt(0-11/4)+1

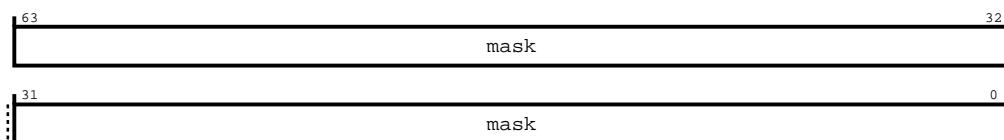


Table 4-564: por_dtm_wp0-11%4_mask_dt(0-11/4)+1 attributes

Bits	Name	Description	Type	Reset
[63:0]	mask	Refer to DTM watchpoint section for details	RW	64'b0

4.3.13.54 por_dtm_pmsicr_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Functions as the sampling interval counter register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2200 + #{512*index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-549: por_dtm_pmsicr_dt1-3

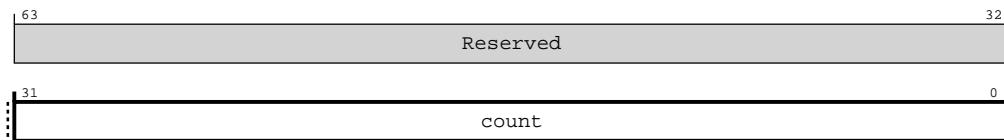


Table 4-565: por_dtm_pmsicr_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:0]	count	Current value of sample counter	RW	32'b0

4.3.13.55 por_dtm_pmsirr_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Functions as the sampling interval reload register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2208 + #{512*index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-550: por_dtm_pmsirr_dt1-3

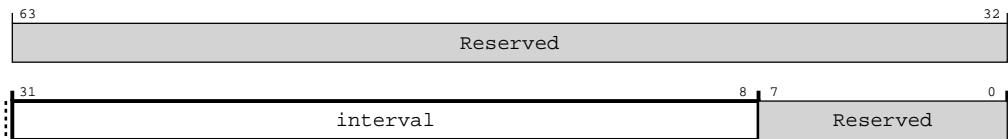


Table 4-566: por_dtm_pmsirr_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:8]	interval	Sampling interval to be reloaded	RW	24'b0
[7:0]	Reserved	Reserved	RO	-

4.3.13.56 por_dtm_pmu_config_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Configures the DTM PMU.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2210 + #{512*index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-551: por_dtm_pmu_config_dt1-3

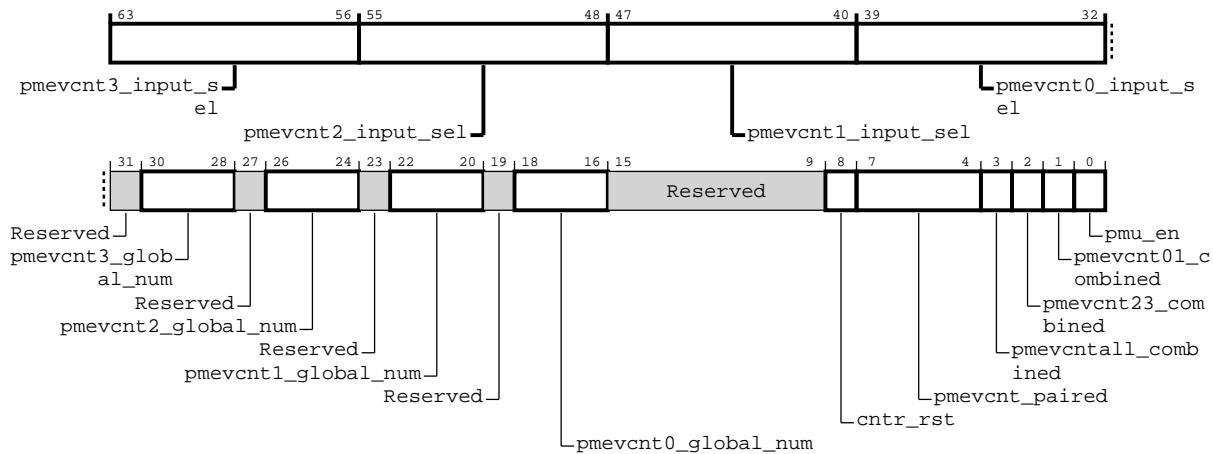


Table 4-567: por_dtm_pmu_config_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:56]	pmevcnt3_input_sel	Source to be counted in PMU counter 3; see pmevcnt0_input_sel for encodings	RW	8'b0
[55:48]	pmevcnt2_input_sel	Source to be counted in PMU counter 2; see pmevcnt0_input_sel for encodings	RW	8'b0
[47:40]	pmevcnt1_input_sel	Source to be counted in PMU counter 1; see pmevcnt0_input_sel for encodings	RW	8'b0

Bits	Name	Description	Type	Reset
[39:32]	pmevcnt0_input_sel	Source to be counted in PMU counter 0: Supports 2 Ports (DT1: P2 and P3, DT2: P4 and P5) when (MXP_NUM_DEV_PORT_PARAM > 2 and MXP_MULTIPLE_DTM_EN_PARAM = 1) 8'h00 Watchpoint 0 8'h01 Watchpoint 1 8'h02 Watchpoint 2 8'h03 Watchpoint 3 8'h04 XP PMU Event 0 8'h05 XP PMU Event 1 8'h06 XP PMU Event 2 8'h07 XP PMU Event 3 8'h10 Port 0 Device 0 PMU Event 0 8'h11 Port 0 Device 0 PMU Event 1 8'h12 Port 0 Device 0 PMU Event 2 8'h13 Port 0 Device 0 PMU Event 3 8'h14 Port 0 Device 1 PMU Event 0 8'h15 Port 0 Device 1 PMU Event 1 8'h16 Port 0 Device 1 PMU Event 2 8'h17 Port 0 Device 1 PMU Event 3 8'h18 Port 0 Device 2 PMU Event 0 8'h19 Port 0 Device 2 PMU Event 1 8'h1A Port 0 Device 2 PMU Event 2 8'h1B Port 0 Device 2 PMU Event 3 8'h1C Port 0 Device 3 PMU Event 0 8'h1D Port 0 Device 3 PMU Event 1 8'h1E Port 0 Device 3 PMU Event 2 8'h1F Port 0 Device 3 PMU Event 3 8'h20 Port 1 Device 0 PMU Event 0 8'h21 Port 1 Device 0 PMU Event 1 8'h22 Port 1 Device 0 PMU Event 2 8'h23 Port 1 Device 0 PMU Event 3 8'h24 Port 1 Device 1 PMU Event 0 8'h25 Port 1 Device 1 PMU Event 1 8'h26 Port 1 Device 1 PMU Event 2 8'h27 Port 1 Device 1 PMU Event 3 8'h28 Port 1 Device 2 PMU Event 0 8'h29 Port 1 Device 2 PMU Event 1 8'h2A Port 1 Device 2 PMU Event 2 8'h2B Port 1 Device 2 PMU Event 3 8'h2C Port 1 Device 3 PMU Event 0 8'h2D Port 1 Device 3 PMU Event 1 8'h2E Port 1 Device 3 PMU Event 2 8'h2F Port 1 Device 3 PMU Event 3	RW	8'b0
[31]	Reserved	Reserved	RO	-
[30:28]	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
[27]	Reserved	Reserved	RO	-
[26:24]	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
[23]	Reserved	Reserved	RO	-
[22:20]	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0
[19]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[18:16]	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000 Global PMU event counter A 3'b001 Global PMU event counter B 3'b010 Global PMU event counter C 3'b011 Global PMU event counter D 3'b100 Global PMU event counter E 3'b101 Global PMU event counter F 3'b110 Global PMU event counter G 3'b111 Global PMU event counter H	RW	3'b0
[15:9]	Reserved	Reserved	RO	-
[8]	cntr_RST	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
[7:4]	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
[3]	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
[2]	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
[1]	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
[0]	pmu_en	DTM PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

4.3.13.57 por_dtm_pmevcnt_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Contains all PMU event counters (0, 1, 2, 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2220 + # {512 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-552: por_dtm_pmevcnt_dt1-3

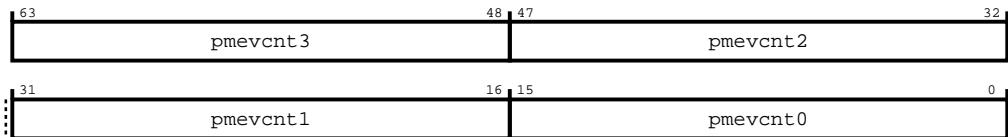


Table 4-568: por_dtm_pmevcnt_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:48]	pmevcnt3	PMU event counter 3	RW	16'h0000
[47:32]	pmevcnt2	PMU event counter 2	RW	16'h0000
[31:16]	pmevcnt1	PMU event counter 1	RW	16'h0000
[15:0]	pmevcnt0	PMU event counter 0	RW	16'h0000

4.3.13.58 por_dtm_pmevcntsr_dt1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h2240 + #{512*index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-553: por_dtm_pmevcntsr_dt1-3

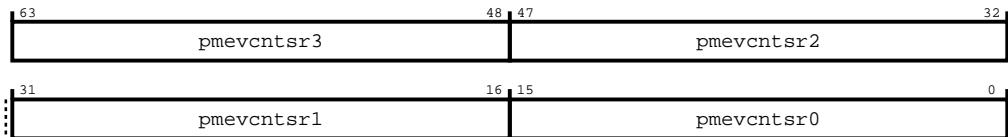


Table 4-569: por_dtm_pmevcntsr_dt1-3 attributes

Bits	Name	Description	Type	Reset
[63:48]	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
[47:32]	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000
[31:16]	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
[15:0]	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

4.3.13.59 por_mxp_multi_mesh_chn_sel_0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Functions as the CHI VC channel select per Target register in Multi-Mesh Channel structure.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC00 + # {8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.multi_mesh_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-554: por_mxp_multi_mesh_chn_sel_0-15

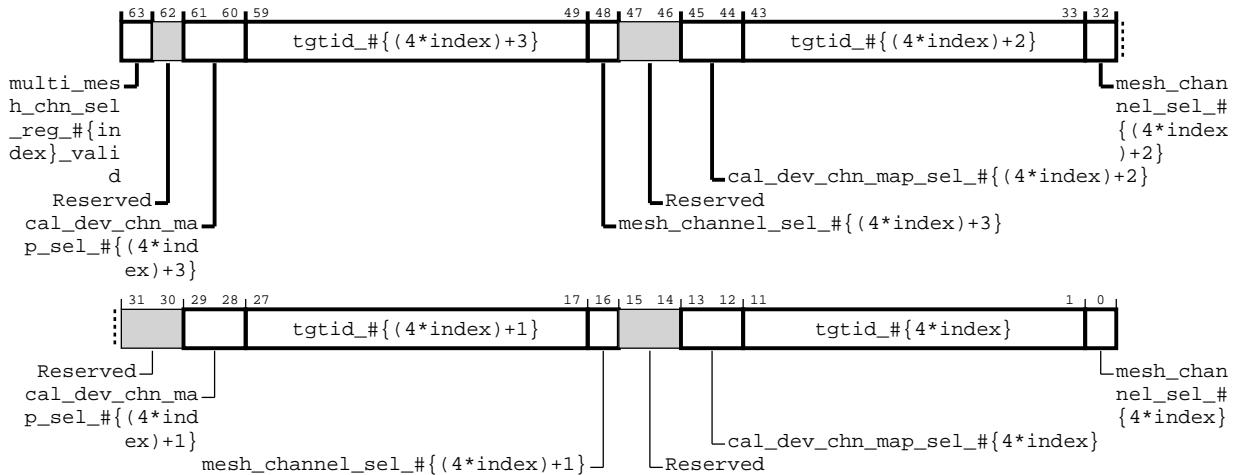


Table 4-570: por_mxp_multi_mesh_chn_sel_0-15 attributes

Bits	Name	Description	Type	Reset
[63]	multi_mesh_chn_sel_reg_{index}_valid	Indicates that multi mesh CHI VC channel configured for the targets specified in this register.	RW	1'b0
[62]	Reserved	Reserved	RO	-
[61:60]	cal_dev_chn_map_sel_{(4*index)+3}	Channel Map select for target devices behind CAL (associated with the corresponding tgtid field): 2'b00 CAL2: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below (applicable for Mesh with > 2 device ports per XP), - CAL2: DEV0,DEV1 are mapped to same channel, 2'b01 CAL4: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below, - CAL4: DEV0,DEV1,DEV2,DEV3 are mapped to same channel, 2'b10 Reserved 2'b11 Each target device behind CAL can be mapped to different channel in the Multi-Channel Mesh structure as specified below, - CAL2: DEV0,DEV1 can be mapped to different channel, - CAL4: DEV0,DEV1,DEV2,DEV3 can be mapped to different channel	RW	2'b0
[59:49]	tgtid_{(4*index)+3}	11-bit Target ID associated with the corresponding channel_sel field. This field is used in the LUP to determine which CHI VC channel the FLIT has to be routed to for this target.	RW	11'b0
[48]	mesh_channel_sel_{(4*index)+3}	CHI VC channel select: 1 - CHI VC channel 1 is selected, 0 - CHI VC channel 0 is selected	RW	1'b0
[47:46]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[45:44]	cal_dev_chn_map_sel_{(4*index)+2}	<p>Channel Map select for target devices behind CAL (associated with the corresponding tgtid field):</p> <p>2'b00 CAL2: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below (applicable for Mesh with > 2 device ports per XP), - CAL2: DEV0,DEV1 are mapped to same channel,</p> <p>2'b01 CAL4: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below, - CAL4: DEV0,DEV1,DEV2,DEV3 are mapped to same channel,</p> <p>2'b10 Reserved</p> <p>2'b11 Each target device behind CAL can be mapped to different channel in the Multi-Channel Mesh structure as specified below, - CAL2: DEV0,DEV1 can be mapped to different channel, - CAL4: DEV0,DEV1,DEV2,DEV3 can be mapped to different channel</p>	RW	1'b0
[43:33]	tgtid_{(4*index)+2}	11-bit Target ID associated with the corresponding channel_sel field. This field is used in the LUP to determine which CHI VC channel the FLIT has to be routed to for this target.	RW	11'b0
[32]	mesh_channel_sel_{(4*index)+2}	CHI VC channel select: 1 - CHI VC channel 1 is selected, 0 - CHI VC channel 0 is selected	RW	1'b0
[31:30]	Reserved	Reserved	RO	-
[29:28]	cal_dev_chn_map_sel_{(4*index)+1}	<p>Channel Map select for target devices behind CAL (associated with the corresponding tgtid field):</p> <p>2'b00 CAL2: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below (applicable for Mesh with > 2 device ports per XP), - CAL2: DEV0,DEV1 are mapped to same channel,</p> <p>2'b01 CAL4: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below, - CAL4: DEV0,DEV1,DEV2,DEV3 are mapped to same channel,</p> <p>2'b10 Reserved</p> <p>2'b11 Each target device behind CAL can be mapped to different channel in the Multi-Channel Mesh structure as specified below, - CAL2: DEV0,DEV1 can be mapped to different channel, - CAL4: DEV0,DEV1,DEV2,DEV3 can be mapped to different channel</p>	RW	2'b0
[27:17]	tgtid_{(4*index)+1}	11-bit Target ID associated with the corresponding channel_sel field. This field is used in the LUP to determine which CHI VC channel the FLIT has to be routed to for this target.	RW	11'b0
[16]	mesh_channel_sel_{(4*index)+1}	CHI VC channel select: 1 - CHI VC channel 1 is selected, 0 - CHI VC channel 0 is selected	RW	1'b0
[15:14]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[13:12]	cal_dev_chn_map_sel_{4*index}	<p>Channel Map select for target devices behind CAL (associated with the corresponding tgtid field):</p> <p>2'b00 CAL2: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below (applicable for Mesh with > 2 device ports per XP), - CAL2: DEV0,DEV1 are mapped to same channel,</p> <p>2'b01 CAL4: All devices behind CAL are mapped to same channel in the Multi-Channel Mesh structure as specified below, - CAL4: DEV0,DEV1,DEV2,DEV3 are mapped to same channel,</p> <p>2'b10 Reserved</p> <p>2'b11 Each target device behind CAL can be mapped to different channel in the Multi-Channel Mesh structure as specified below, - CAL2: DEV0,DEV1 can be mapped to different channel, - CAL4: DEV0,DEV1,DEV2,DEV3 can be mapped to different channel</p>	RW	2'b0
[11:1]	tgtid_{4*index}	11-bit Target ID associated with the corresponding channel_sel field. This field is used in the LUP to determine which CHI VC channel the FLIT has to be routed to for this target.	RW	11'b0
[0]	mesh_channel_sel_{4*index}	CHI VC channel select: 1 - CHI VC channel 1 is selected, 0 - CHI VC channel 0 is selected	RW	1'b0

4.3.13.60 por_mxp_multi_mesh_chn_ctrl

Functions as the control register for Target based channel selection in Multi-Mesh Channel structure.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC80

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.multi_mesh_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-555: por_mxp_multi_mesh_chn_ctrl

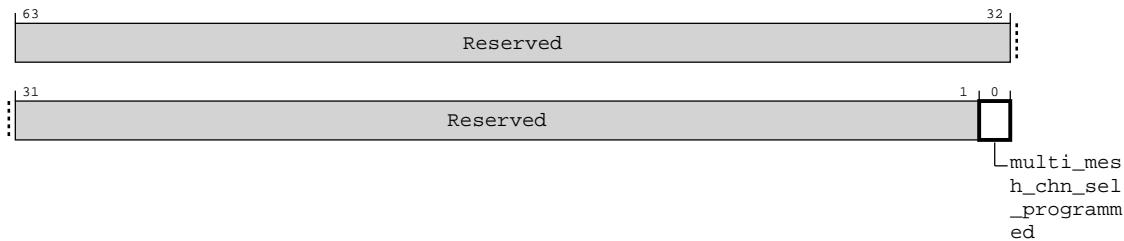


Table 4-571: por_mxp_multi_mesh_chn_ctrl attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	multi_mesh_chn_sel_programmed	Indicates that multi CHI VC channel configured for all the targets specified in the channel select registers.	RW	1'b0

4.3.13.61 por_mxp_xy_override_sel_0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Functions as SRC-TGT pair whose X-Y route path can be overridden (for Non-XY Route feature per Souce-Target pair) per XP.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hC90 + #{8*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.xy_override_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-556: por_mxp_xy_override_sel_0-7

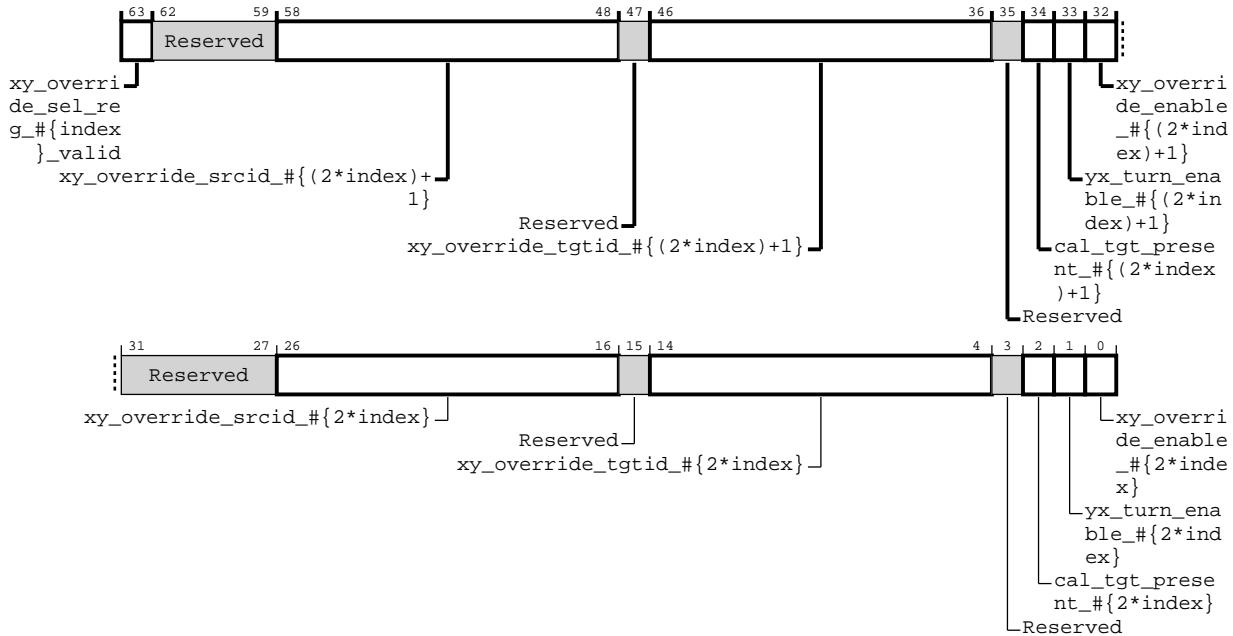


Table 4-572: por_mxp_xy_override_sel_0-7 attributes

Bits	Name	Description	Type	Reset
[63]	xy_override_sel_reg_{index}_valid	Indicates that Source-Target pairs whose X-Y route path can be overridden are configured in this register.	RW	1'b0
[62:59]	Reserved	Reserved	RO	-
[58:48]	xy_override_srcid_{(2*index)+1}	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overridden.	RW	11'b0
[47]	Reserved	Reserved	RO	-
[46:36]	xy_override_tgtid_{(2*index)+1}	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overridden.	RW	11'b0
[35]	Reserved	Reserved	RO	-
[34]	cal_tgt_present_{(2*index)+1}	CAL TGT Presence Indication for XY Route Override of all devices behind CAL: 1 - CAL4 TGT Present for XY Route Override of all devices behind CAL, 0 - CAL2 TGT or no CAL TGT Present for XY Route Override of all devices behind CAL.	RW	1'b0
[33]	yx_turn_enable_{(2*index)+1}	Y-X Turn Enable: 1 - Y-X Turn enabled for associated Source-Target Pair, 0 - Y-X Turn disabled	RW	1'b0
[32]	xy_override_enable_{(2*index)+1}	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0
[31:27]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[26:16]	xy_override_srcid_{2*index}	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overridden.	RW	11'b0
[15]	Reserved	Reserved	RO	-
[14:4]	xy_override_tgtid_{2*index}	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overridden.	RW	11'b0
[3]	Reserved	Reserved	RO	-
[2]	cal_tgt_present_{2*index}	CAL TGT Presence Indication for XY Route Override of all devices behind CAL: 1 - CAL4 TGT Present for XY Route Override of all devices behind CAL, 0 - CAL2 TGT or no CAL TGT Present for XY Route Override of all devices behind CAL.	RW	1'b0
[1]	yx_turn_enable_{2*index}	Y-X Turn Enable: 1 - Y-X Turn enabled for associated Source-Target Pair, 0 - Y-X Turn disabled	RW	1'b0
[0]	xy_override_enable_{2*index}	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

4.3.13.62 por_mxp_p0-5_pa2setaddr_slc

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the control register of PA to SetAddr and vice versa conversion for HNF-SLC on XP port #{index}. NOTE: There will be max. of 6 MXP Port registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port register will be at the next 8 byte address boundary.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCD0 + #{32*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.pa2setaddr_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-557: por_mxp_p0-5_pa2setaddr_slc

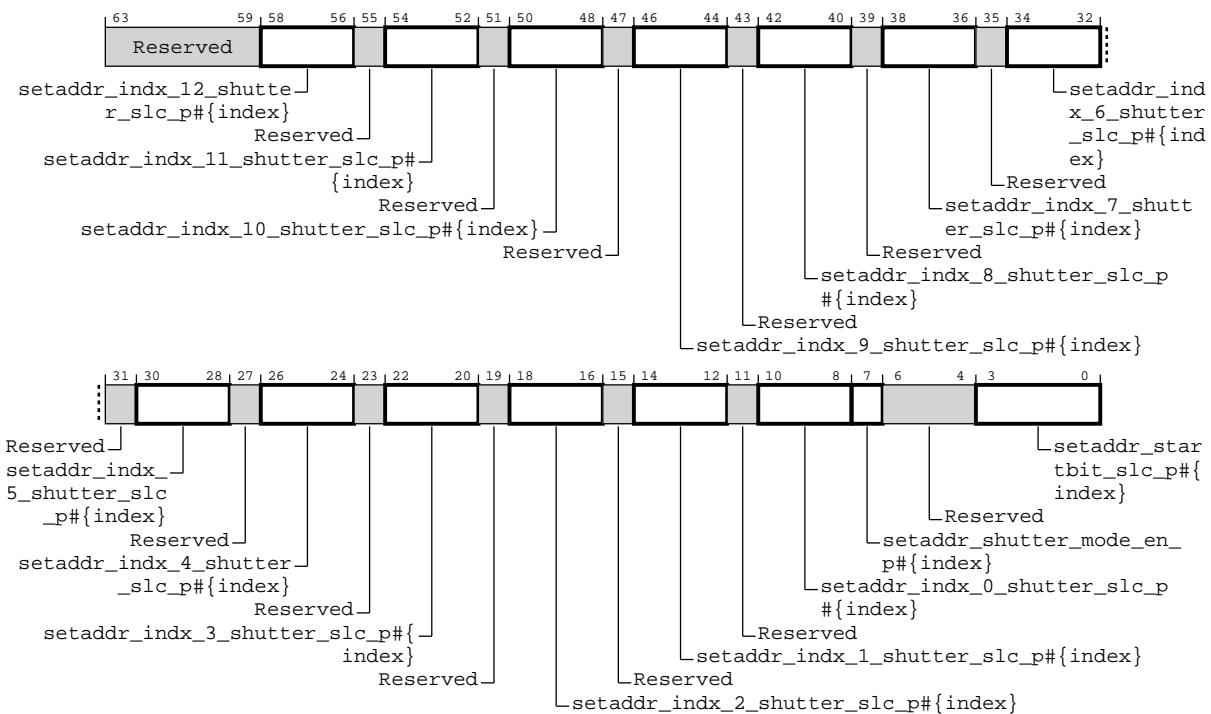


Table 4-573: por_mxp_p0-5_pa2setaddr_slc attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:56]	setaddr_idx_12_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 12 from the setaddr_startbit_slc	RW	3'b0
	3'b000	pass-through		
	3'b001	shift_1		
	3'b010	shift_2		
	3'b011	shift_3		
	3'b100	shift_4		
	3'b101	shift_5		
[55]	Reserved	Reserved	RO	-
[54:52]	setaddr_idx_11_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 11 from the setaddr_startbit_slc	RW	3'b0
	3'b000	pass-through		
	3'b001	shift_1		
	3'b010	shift_2		
	3'b011	shift_3		
	3'b100	shift_4		
	3'b101	shift_5		

Bits	Name	Description	Type	Reset
[51]	Reserved	Reserved	RO	-
[50:48]	setaddr_idx_10_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 10 from the setaddr_startbit_slc	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[47]	Reserved	Reserved	RO	-
[46:44]	setaddr_idx_9_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 9 from the setaddr_startbit_slc	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[43]	Reserved	Reserved	RO	-
[42:40]	setaddr_idx_8_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 8 from the setaddr_startbit_slc	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[39]	Reserved	Reserved	RO	-
[38:36]	setaddr_idx_7_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 7 from the setaddr_startbit_slc	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[35]	Reserved	Reserved	RO	-
[34:32]	setaddr_idx_6_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 6 from the setaddr_startbit_slc	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[31]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[30:28]	setaddr_idx_5_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 5 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[27]	Reserved	Reserved	RO	-
[26:24]	setaddr_idx_4_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 4 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[23]	Reserved	Reserved	RO	-
[22:20]	setaddr_idx_3_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 3 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[19]	Reserved	Reserved	RO	-
[18:16]	setaddr_idx_2_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 2 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[15]	Reserved	Reserved	RO	-
[14:12]	setaddr_idx_1_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 1 from the setaddr_startbit_slc 3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5	RW	3'b0
[11]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[10:8]	setaddr_idx_0_shutter_slc_p#{index}	Program to specify address bit shuttering for setaddr index 0 from the setaddr_startbit_slc	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[7]	setaddr_shutter_mode_en_p#{index}	Enables address shuttering mode for SLC as programmed by setaddr_idx_X_shutter registers	RW	1'b0
[6:4]	Reserved	Reserved	RO	-
[3:0]	setaddr_startbit_slc_p#{index}	SLC: SetAddr starting bit for SLC in HNF connected to port p#{index}	RW	4'b0110
		4'b0110 Setaddr starts from PA[6] 4'b0111 Setaddr starts from PA[7] 4'b1000 Setaddr starts from PA[8] 4'b1001 Setaddr starts from PA[9] 4'b1010 Setaddr starts from PA[10] 4'b1011 Setaddr starts from PA[11] 4'b1100 Setaddr starts from PA[12]		

4.3.13.63 por_mxp_p0-5_pa2setaddr_sf

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the control register of PA to Set/TagAddr and vice versa conversion for HNF-SF on XP port #{index}. NOTE: There will be max. of 6 MXP Port registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port register will be at the next 8 byte address boundary.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCD8 + #{32*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_mxp_secure_register_groups_override.pa2setaddr_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-558: por_mxp_p0-5_pa2setaddr_sf

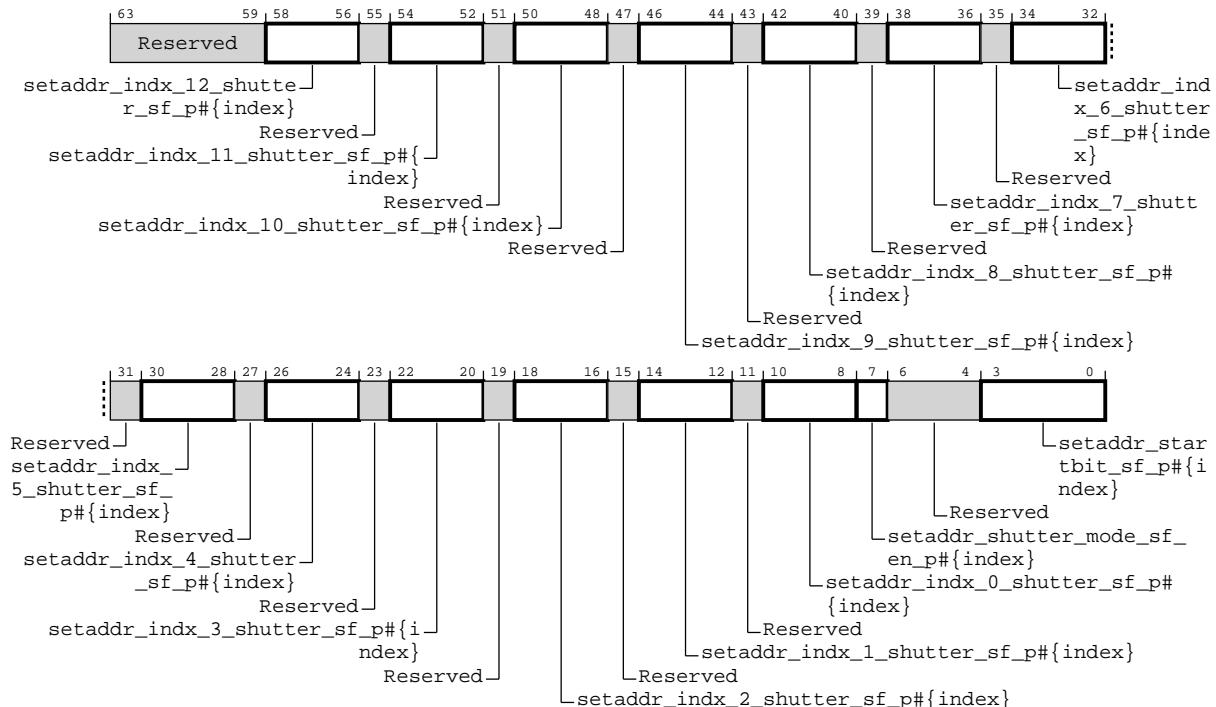


Table 4-574: por_mxp_p0-5_pa2setaddr_sf attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:56]	setaddr_idx_12_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 12 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[55]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[54:52]	setaddr_idx_11_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 11 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[51]	Reserved	Reserved	RO	-
[50:48]	setaddr_idx_10_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 10 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[47]	Reserved	Reserved	RO	-
[46:44]	setaddr_idx_9_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 9 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[43]	Reserved	Reserved	RO	-
[42:40]	setaddr_idx_8_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 8 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[39]	Reserved	Reserved	RO	-
[38:36]	setaddr_idx_7_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 7 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[35]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[34:32]	setaddr_idx_6_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 6 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[31]	Reserved	Reserved	RO	-
[30:28]	setaddr_idx_5_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 5 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[27]	Reserved	Reserved	RO	-
[26:24]	setaddr_idx_4_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 4 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[23]	Reserved	Reserved	RO	-
[22:20]	setaddr_idx_3_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 3 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[19]	Reserved	Reserved	RO	-
[18:16]	setaddr_idx_2_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 2 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[15]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[14:12]	setaddr_idx_1_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 1 from the setaddr_startbit_sf	RW	3'b00
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[11]	Reserved	Reserved	RO	-
[10:8]	setaddr_idx_0_shutter_sf_p#{index}	Program to specify address bit shuttering for setaddr index 0 from the setaddr_startbit_sf	RW	3'b0
		3'b000 pass-through 3'b001 shift_1 3'b010 shift_2 3'b011 shift_3 3'b100 shift_4 3'b101 shift_5		
[7]	setaddr_shutter_mode_sf_en_p#{index}	Enables address shuttering mode for SF as programmed by setaddr_idx_X_shutter_sf registers	RW	1'b0
[6:4]	Reserved	Reserved	RO	-
[3:0]	setaddr_startbit_sf_p#{index}	SF: SetAddr starting bit for SF in HNF connected to port p#{index}	RW	4'b0110
		4'b0110 Setaddr starts from PA[6] 4'b0111 Setaddr starts from PA[7] 4'b1000 Setaddr starts from PA[8] 4'b1001 Setaddr starts from PA[9] 4'b1010 Setaddr starts from PA[10] 4'b1011 Setaddr starts from PA[11] 4'b1100 Setaddr starts from PA[12]		

4.3.13.64 por_mxp_p0-5_pa2setaddr flex_slc

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the SLC control register of PA to Set/TagAddr and vice versa conversion for HNF (flexible) on XP port #{index}.

NOTE: There will be max. of 6 MXP Port registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port register will be at the next 8 byte address boundary.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hCE0 + #{32*index}

Type

RW

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.pa2setaddr_ctl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-559: por_mxp_p0-5_pa2setaddr_flex_slc

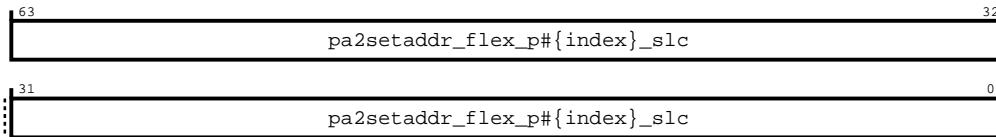


Table 4-575: por_mxp_p0-5_pa2setaddr_flex_slc attributes

Bits	Name	Description	Type	Reset
[63:0]	pa2setaddr_flex_p#{index}_slc	FLEXIBLE: PA to SET/TAG ADDR and vice versa conversion config field for HNF connected to port p#{index}	RW	64'b0

4.3.13.65 por_mxp_p0-5_pa2setaddr_flex_sf

There are 6 iterations of this register. The index ranges from 0 to 5. Functions as the SF control register of PA to Set/TagAddr and vice versa conversion for HNF (flexible) on XP port #{index}.

NOTE: There will be max. of 6 MXP Port registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port register will be at the next 8 byte address boundary.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hCE8 + #{32*index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_mxp_secure_register_groups_override.pa2setaddr_ctl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-560: por_mxp_p0-5_pa2setaddr_flex_sf

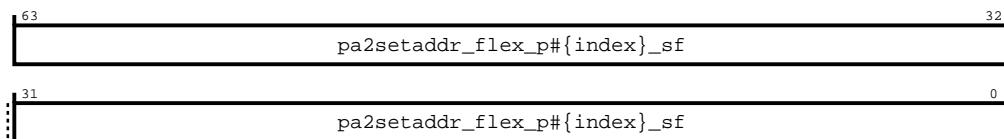


Table 4-576: por_mxp_p0-5_pa2setaddr_flex_sf attributes

Bits	Name	Description	Type	Reset
[63:0]	pa2setaddr_flex_p#{index}_sf	FLEXIBLE: PA to SET/TAG ADDR conversion and vice versa config field for HNF connected to port p#{index}	RW	64'b0

4.3.14 RN-D register descriptions

This section lists the RN-D registers.

4.3.14.1 por_rnd_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'h0`

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-561: por_rnd_node_info

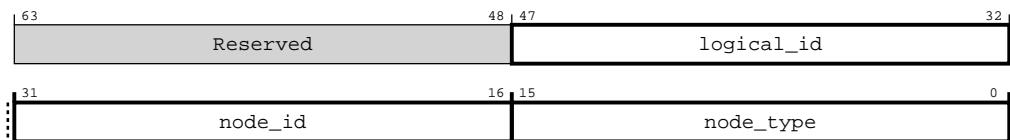


Table 4-577: por_rnd_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h000D

4.3.14.2 por_rnd_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-562: por_rnd_child_info

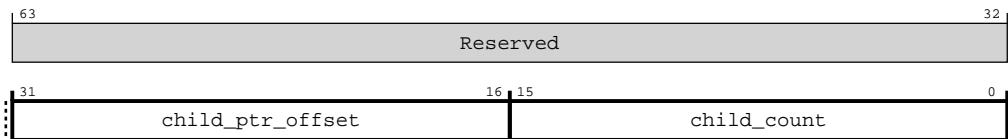


Table 4-578: por_rnd_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'h0

4.3.14.3 por_rnd_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-563: por_rnd_secure_register_groups_override

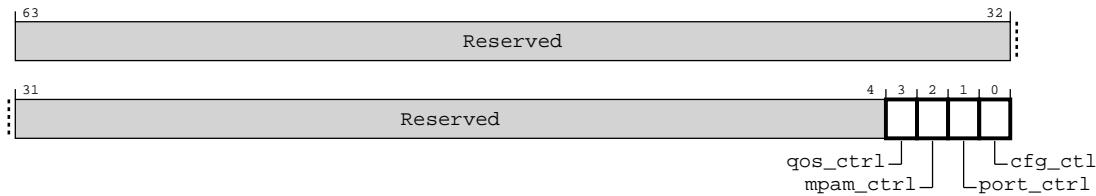


Table 4-579: por_rnd_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	qos_ctrl	Allows Non-secure access to Secure QoS control registers	RW	1'b0
[2]	mpam_ctrl	Allows Non-secure access to Secure AXI port MPAM override register	RW	1'b0
[1]	port_ctrl	Allows Non-secure access to Secure AXI port control registers	RW	1'b0
[0]	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

4.3.14.4 por_rnd_unit_info

Provides component identification information for RN-D.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-564: por_rnd_unit_info

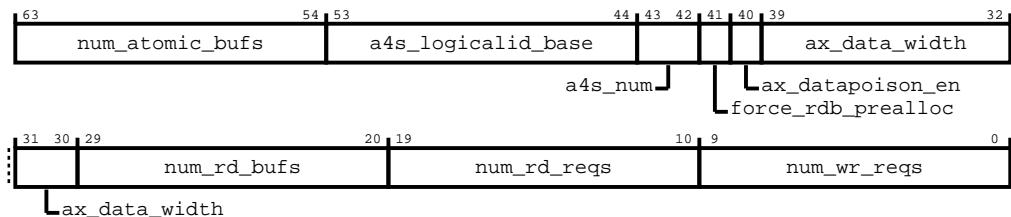


Table 4-580: por_rnd_unit_info attributes

Bits	Name	Description	Type	Reset
[63:54]	num_atomic_bufs	Number of atomic data buffers	RO	Configuration dependent
[53:44]	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
[43:42]	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
[41]	force_rdb_prealloc	Force read data buffer preallocation	RO	Configuration dependent
		1'b1 Yes 1'b0 No		
[40]	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[39:30]	ax_data_width	AXI interface data width in bits	RO	Configuration dependent
[29:20]	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
[19:10]	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
[9:0]	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

4.3.14.5 por_rnd_unit_info2

Provides additional component identification information for RN-D.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-565: por_rnd_unit_info2

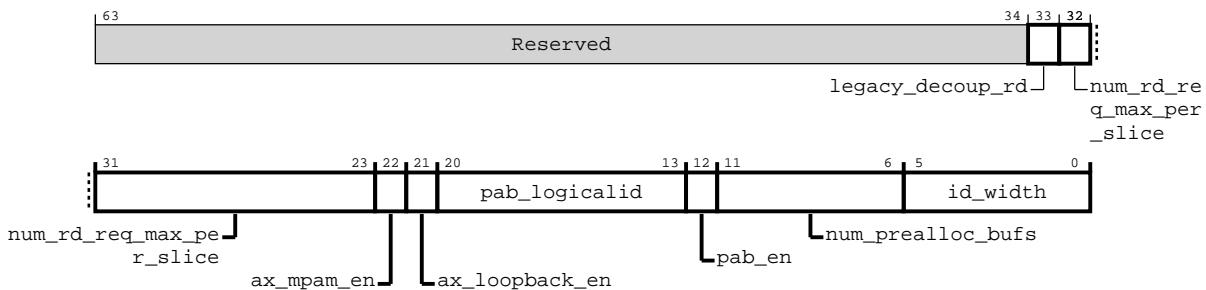


Table 4-581: por_rnd_unit_info2 attributes

Bits	Name	Description	Type	Reset
[63:34]	Reserved	Reserved	RO	-
[33]	legacy_decoup_rd	Legacy decoupled read mode, no read burst propagation	RO	Configuration dependent
[32:23]	num_rd_req_max_per_slice	Number of read request entires per slice	RO	Configuration dependent
[22]	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[21]	ax_loopback_en	LoopBack enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[20:13]	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
[12]	pab_en	PUB AUB bridge enable	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[11:6]	num_prealloc_bufs	Number of Pre-allocated Read Data Buffers	RO	Configuration dependent
[5:0]	id_width	AXI ID width for ACE-Lite subordinate ports	RO	Configuration dependent

4.3.14.6 por_rnd_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnd_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-566: por_rnd_cfg_ctl

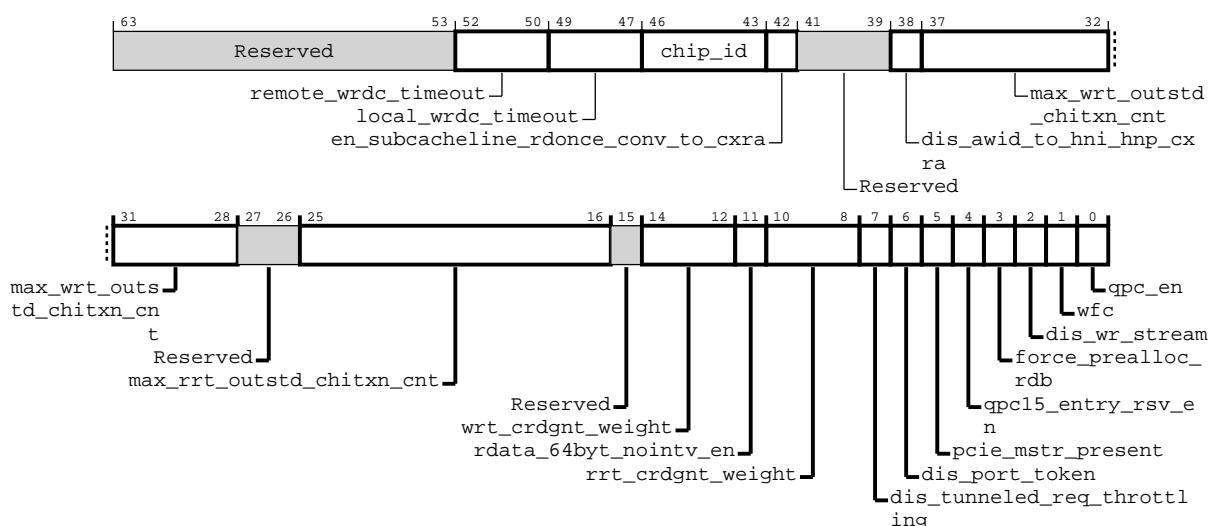


Table 4-582: por_rnd_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:53]	Reserved	Reserved	RO	-
[52:50]	remote_wrdc_timeout	Configurable write data cancel timeout value for remote traffic. 3'b000 ~2000 cycles 3'b001 ~4000 cycles 3'b010 ~8000 cycles 3'b011 ~16000 cycles (default) 3'b100 ~32000 cycles (all other values rsvd)	RW	3'b011
[49:47]	local_wrdc_timeout	Configurable write data cancel timeout value for local traffic. 3'b000 ~2000 cycles 3'b001 ~4000 cycles 3'b010 ~8000 cycles 3'b011 ~16000 cycles (default) 3'b100 ~32000 cycles (all other values rsvd)	RW	3'b010
[46:43]	chip_id	Configurable ChipID for this RNX instance. Must be correctly set for proper handling of remote traffic to HNI/HNP. Only supports values 0..3. Two MSB's are reserved.	RW	4'b0000
[42]	en_subcacheline_rdone_conv_to_cxra	If set, enables the conversion of sub-cacheline RdOnce to RdNoSnp for CXRA targets	RW	1'b0
[41:39]	Reserved	Reserved	RO	-
[38]	dis_awid_to_hni_hnp_cxra	If set, disables compressed AWID to HNI and CXRA, also disables compressed AWID based ordering. Set this bit if uniq-ID write performance is needed.	RW	1'b0
[37:28]	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
[27:26]	Reserved	Reserved	RO	-
[25:16]	max_rrt_outstd_chitxn_cnt	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
[15]	Reserved	Reserved	RO	-
[14:12]	wrt_crdgnt_weight	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
[11]	rdata_64byt_nointv_en	Enables no interleaving property on normal memory read data within 64B granule when set	RW	1'b1
[10:8]	rrt_crdgnt_weight	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
[7]	dis_tunneled_req_throttling	Disables retry based throttling of tunneled write requests	RW	1'b0
[6]	dis_port_token	If set, disables per port reservation in the tracker(rd and wr)	RW	1'b1
[5]	pcie_mstr_present	Indicates PCIe manager is present; must be set if PCIe manager is present upstream of RN-I or RN-D	RW	1'b0

Bits	Name	Description	Type	Reset
[4]	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1 Reserves tracker entry for QoS15 requests 1'b0 Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when porRnd_qpc_en is set	RW	1'b0
[3]	force_prealloc_rdb	When set, all reads from the RN-D are sent with a preallocated read data buffer	RW	Configuration dependent
[2]	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
[1]	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
[0]	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

4.3.14.7 porRnd_aux_ctl

Functions as the auxiliary control register for RN-D.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-567: por_rnd_aux_ctl

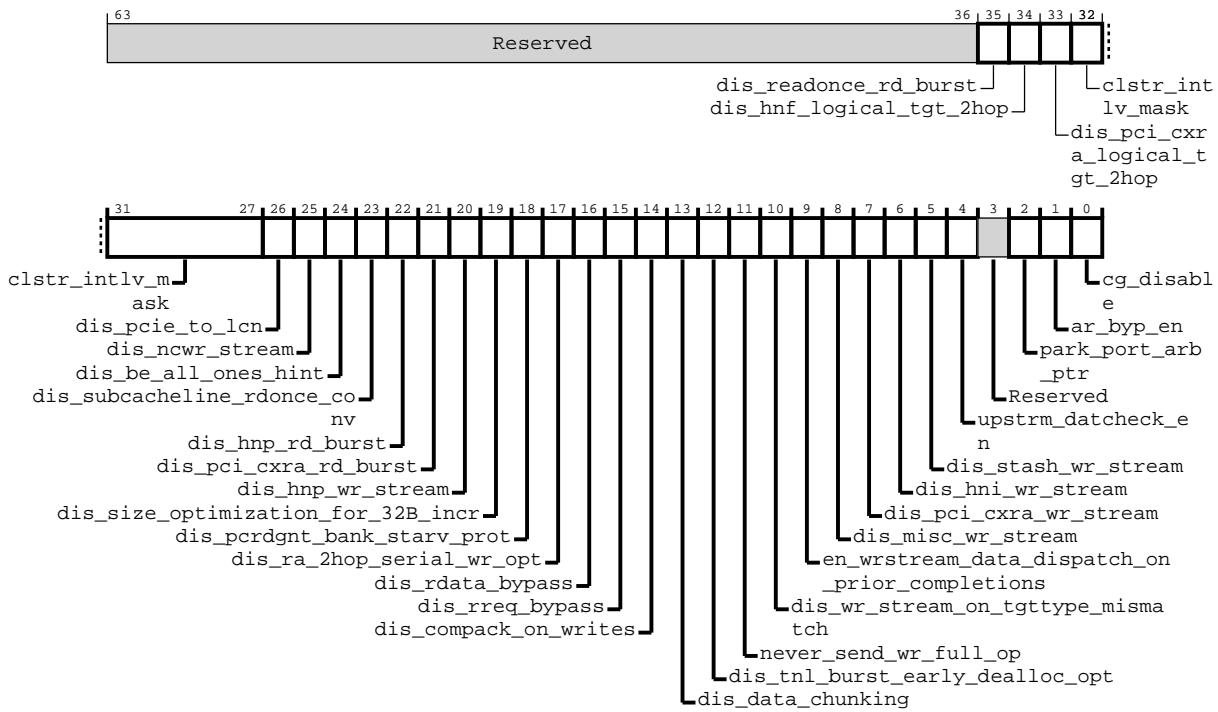


Table 4-583: por_rnd_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset																
[39]	sys_dis_data_interleaving,	<p>System optimized disable read DATA interleaving for all ports. Disables all read data interleaving, including atomic read data being returned for all AXI ports. Read burst preservation is enabled similar to normal mode, but this requires certain system level restrictions:</p> <ol style="list-style-type: none"> 1. Cannot set SYS_DIS_DATA_INTERLEAVING for multi-chip systems. Support for remote HN-P is a future feature. 2. When setting SYS_DIS_DATA_INTERLEAVING for an RN-I/RN-D it is required for that RN-I/RN-D to target only one HN-P with read bursts. It is also required for the path to a single remote HN-P, when remote support is available, to only go through a single CCG and for the ccg_rni to also have SYS_DIS_DATA_INTERLEAVING set. 3. The AXI subordinate downstream of HN-P must not interleave read burst data. 4. Must have NUM_RD_REQ_PARAM==NUM_RD_BUF_PARAM and NUM_RD_REQ_PRAM<=256, otherwise this bit has no effect. 5. The sum of the maximum number of beats of a cracked burst per each port must fit wholly within an arslice - breaking this rule will result in a hang. Must comprehend DIS_PORT_TOKEN AND QPC15_ENTRY_RSV settings, which will limit number of available entries 	RW	1'b0																
[38:36]	Reserved	Reserved	RO	-																
[35]	dis_readonce_rd_burst	If set, disables read burst for ReadOnce from AXI.	RW	1'b0																
[34]	dis_hnf_logical_tgt_2hop	If set, disables tunneling/2hop for case where physical target is pci_cxra and logical target is hnf, otherwise may tunneling/2hop to RA if interleaving granularity settings allow.	RW	1'b0																
[33]	dis_pci_cxra_logical_tgt_2hop	If set, disables tunneling/2hop for case where physical and logical target is pci_cxra, otherwise tunneling/2hop to RA.	RW	1'b0																
[32:27]	clstr_intlv_mask	<p>Encoded static mask for max interleave granularity supported. When this setting is less than or equal to rnsam's programmed interleave granularity for a write to pci_cxra, tunneling/2hop flow will be used.</p> <table> <tbody> <tr> <td>6'b111111</td> <td>64B</td> </tr> <tr> <td>6'b111110</td> <td>128B</td> </tr> <tr> <td>6'b111100</td> <td>256B</td> </tr> <tr> <td>6'b111000</td> <td>512B</td> </tr> <tr> <td>6'b110000</td> <td>1024B</td> </tr> <tr> <td>6'b100000</td> <td>2048B</td> </tr> <tr> <td>6'b000000</td> <td>4096B</td> </tr> <tr> <td>Others</td> <td>Reserved</td> </tr> </tbody> </table>	6'b111111	64B	6'b111110	128B	6'b111100	256B	6'b111000	512B	6'b110000	1024B	6'b100000	2048B	6'b000000	4096B	Others	Reserved	RW	6'b0000000
6'b111111	64B																			
6'b111110	128B																			
6'b111100	256B																			
6'b111000	512B																			
6'b110000	1024B																			
6'b100000	2048B																			
6'b000000	4096B																			
Others	Reserved																			
[26]	dis_PCIE_to_lcn	If set, all PCIe traffic sent directly to HNF/CCG, bypasses LCN. Only has effect when pcie_mstr_present	RW	1'b1																
[25]	dis_ncwr_stream	Disables streaming of ordered non-cacheable writes when set	RW	1'b0																

Bits	Name	Description	Type	Reset
[24]	dis_be_all_ones_hint	If set, disables hint to HNF which signals all BE=1's on writes	RW	1'b0
[23]	dis_subcacheline_rdonce_conv	If set, disables the conversion of sub-cacheline RdOnce to RdNoSnp across all targets	RW	1'b0
[22]	dis_hnp_rd_burst	If set, disables read burst to HNP on CHI request flits . Read burst on CHI is supported only in non-decoupled RDB configuration.	RW	1'b0
[21]	dis_pci_cxra_rd_burst	If set, disables read burst to PCI-CXRA on CHI request flits . Read burst on CHI is supported only in non-decoupled RDB configuration.	RW	1'b0
[20]	dis_hnp_wr_stream	Disables streaming of ordered writes to HNP when set	RW	1'b0
[19]	dis_size_optimization_for_32B_incr	If set, disables the size related optimization for a 32B INCR burst (rh-2512). Only applies to writes.	RW	1'b0
[18]	dis_pcrdgnt_bank_starv_prot	If set, disables across arslice starvation protection	RW	1'b0
[17]	dis_ra_2hop_serial_wr_opt	If set, disables 2 hop indication to ra for serialized writes; will indicate 3 hop	RW	1'b0
[16]	dis_rdata_bypass	If set, disables read data bypass path	RW	1'b0
[15]	dis_rreq_bypass	If set, disables read request bypass path	RW	1'b0
[14]	dis_compack_on_writes	If set, disables comp_ack on streaming writes. WrData is used for ordering writes	RW	1'b1
[13]	dis_data_chunking	If set, disables the data chunking feature	RW	1'b0
[12]	dis_tnl_burst_early_dealloc_opt	If set, disables the optimization related to early deallocation of tunneled writes for intermediate txns of burst	RW	1'b0
[11]	never_send_wr_full_op	If set, RNI will never send WR FULL op. All write ops will be of PTL type	RW	1'b0
[10]	dis_wr_stream_on_tgtype_mismatch	If set, serializes first write when moving from one tgtype to another	RW	1'b0
[9]	en_wrstream_data_dispatch_on_prior_completions	If set, data dispatch for streaming writes waits for completion of all older writes	RW	1'b0
[8]	dis_misc_wr_stream	Disables streaming of ordered writes with following attributes when set : Device memory or EWA=0 or Excl=1	RW	1'b0
[7]	dis_pci_cxra_wr_stream	Disables streaming of ordered writes to PCI-CXRA when set	RW	1'b0
[6]	dis_hni_wr_stream	Disables streaming of ordered writes to HNI when set	RW	1'b0
[5]	dis_stash_wr_stream	Disables streaming of ordered WrUniqStash when set	RW	1'b0
[4]	upstrm_datcheck_en	Upstream supports Datacheck	RW	Configuration dependent
[3]	Reserved	Reserved	RO	-
[2]	park_port_arb_ptr	Parks the AXI port arbitration pointer for Burst	RW	1'b0
[1]	ar_byp_en	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
[0]	cg_disable	Disables clock gating when set	RW	1'b0

4.3.14.8 por_rnd_s0-2_port_control

There are 3 iterations of this register. The index ranges from 0 to 2. Controls port S#{index} AXI/ACE subordinate interface settings.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hA10 + #{index}*8}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnd_secure_register_groups_override.port_ctrl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-568: por_rnd_s0-2_port_control

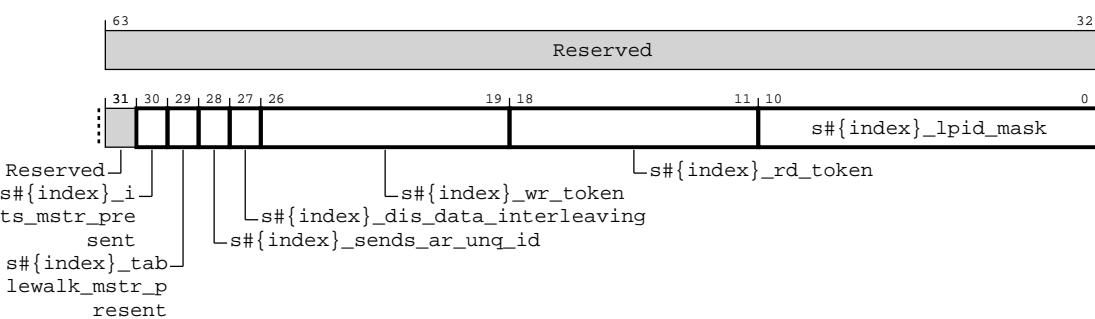


Table 4-584: por_rnd_s0-2_port_control attributes

Bits	Name	Description	Type	Reset
[63:31]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[30]	s#{index}_its_mstr_present	Must be set if translation table walk manager present such as TCU or GIC for non-PCIE case. This affects RND AW channel only.	RW	1'b0
[29]	s#{index}_tablewalk_mstr_present	Must be set if translation table walk manager present such as TCU or GIC. This affects RND AR channel only.	RW	1'b0
[28]	s#{index}_sends_ar_unq_id	If set, indicates AR transactions on Port#{index} are always Unique ID. This bit for a port must be set to 1 to enable Read Burst on the CHI side of RND.	RW	1'b0
[27]	s#{index}_dis_data_interleaving	If set, disables read DATA interleaving on RDATAS#{index} channel. This applies only to RDATA generated as a response to requests on AR channel . This does not apply to RDATA generated as a response to Atomic request on AW channel. I.e. RDATA of an Atomic op, on AW channel, may interleave with RDATA of an AR channel request	RW	1'b0
[26:19]	s#{index}_wr_token	Port S#{index} reserved token count for AW channel This must be less than the number of Wr requests(RNID_NUM_WR_REQ_PARAM) on AW achnnel	RW	8'b0000_0000
[18:11]	s#{index}_rd_token	Port S#{index} reserved token count for AR channel per slice This should be less than the number of Rd requests(RNID_NUM_RD_REQ_PARAM) per slice on AR achnnel	RW	8'b0000_0000
[10:0]	s#{index}_lpid_mask	Port S#{index} LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = !(AXID & mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

4.3.14.9 por_rnd_s0-2_mpam_control

There are 3 iterations of this register. The index ranges from 0 to 2. Controls port S#{index} AXI/ACE subordinate interface MPAM override values

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA28 + #{index}*8}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnd_secure_register_groups_override.mpam_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-569: por_rnd_s0-2_mpam_control

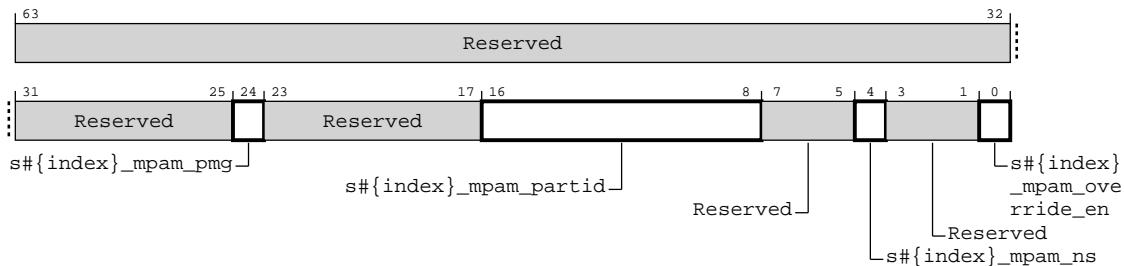


Table 4-585: por_rnd_s0-2_mpam_control attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	s#{index}_mpam_pmg	Port S#{index} MPAM_PMG value	RW	1'b0
[23:17]	Reserved	Reserved	RO	-
[16:8]	s#{index}_mpam_partid	Port S#{index} MPAM_PARTID value	RW	9'b0
[7:5]	Reserved	Reserved	RO	-
[4]	s#{index}_mpam_ns	Port S#{index} MPAM_NS value	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	s#{index}_mpam_override_en	Port S#{index} MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

4.3.14.10 por_rnd_s0-2_qos_control

There are 3 iterations of this register. The index ranges from 0 to 2. Controls QoS settings for port S#{index} AXI/ACE subordinate interface.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA80 + #{index}*32}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnd_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-570: por_rnd_s0-2_qos_control

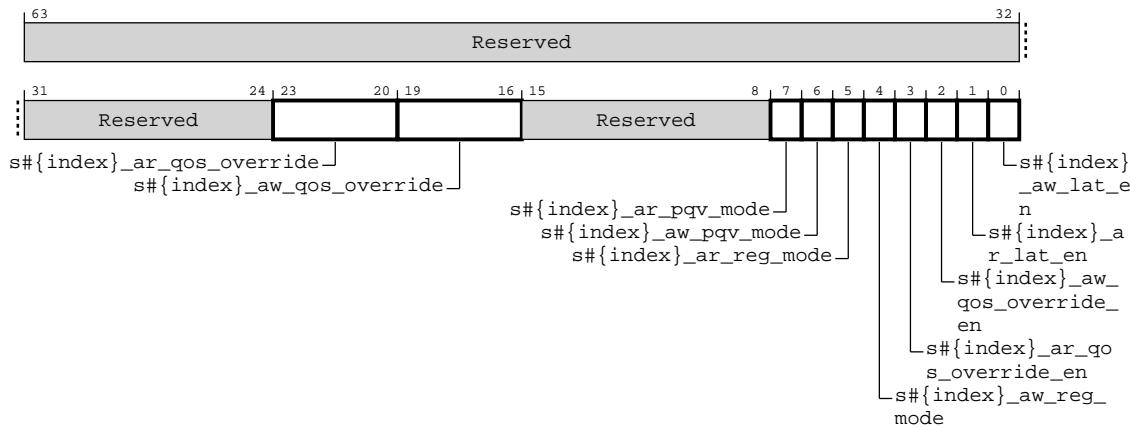


Table 4-586: por_rnd_s0-2_qos_control attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:20]	s#{index}_ar_qos_override	AR QoS override value for port S#{index}	RW	4'b0000
[19:16]	s#{index}_aw_qos_override	AW QoS override value for port S#{index}	RW	4'b0000
[15:8]	Reserved	Reserved	RO	-
[7]	s#{index}_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0 Normal mode; QoS value is stable when the manager is idle 1'b1 Quiesce high mode; QoS value tends to the maximum value when the manager is idle	RW	1'b0
[6]	s#{index}_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0 Normal mode; QoS value is stable when the manager is idle 1'b1 Quiesce high mode; QoS value tends to the maximum value when the manager is idle	RW	1'b0

Bits	Name	Description	Type	Reset
[5]	s#{index}_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0 Latency mode 1'b1 Period mode; used for bandwidth regulation	RW	1'b0
[4]	s#{index}_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0 Latency mode 1'b1 Period mode; used for bandwidth regulation	RW	1'b0
[3]	s#{index}_ar_qos_override_en	Enables port S#{index} AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
[2]	s#{index}_aw_qos_override_en	Enables port S#{index} AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
[1]	s#{index}_ar_lat_en	Enables port S#{index} AR QoS regulation when set	RW	1'b0
[0]	s#{index}_aw_lat_en	Enables port S#{index} AW QoS regulation when set	RW	1'b0

4.3.14.11 por_rnd_s0-2_qos_lat_tgt

There are 3 iterations of this register. The index ranges from 0 to 2. Controls QoS target latency (in cycles) for regulations of port S#{index} read and write transactions.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA88 + #{index*32}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnd_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-571: por_rnd_s0-2_qos_lat_tgt

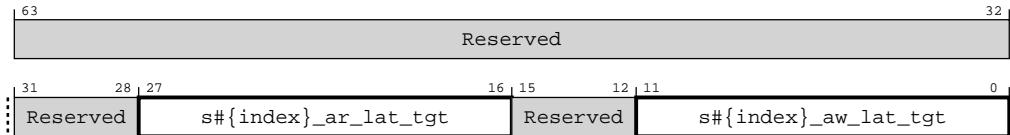


Table 4-587: por_rnd_s0-2_qos_lat_tgt attributes

Bits	Name	Description	Type	Reset
[63:28]	Reserved	Reserved	RO	-
[27:16]	s#{index}_ar_lat_tgt	Port S#{index} AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
[15:12]	Reserved	Reserved	RO	-
[11:0]	s#{index}_aw_lat_tgt	Port S#{index} AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

4.3.14.12 por_rnd_s0-2_qos_lat_scale

There are 3 iterations of this register. The index ranges from 0 to 2. Controls the QoS target latency scale factor for port S#{index} read and write transactions. This register represents powers of two from the range 2^{-5} to 2^{-12} ; it is used to match a 16-bit integrator.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16^{\prime}hA90 + \#\{index*32\}$

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnd_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-572: por_rnd_s0-2_qos_lat_scale

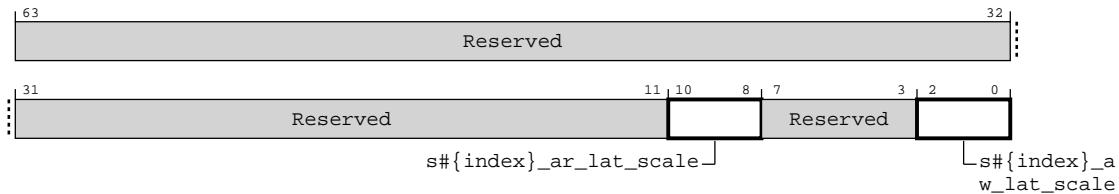


Table 4-588: por_rnd_s0-2_qos_lat_scale attributes

Bits	Name	Description	Type	Reset
[63:11]	Reserved	Reserved	RO	-
[10:8]	s#{index}_ar_lat_scale	Port S#{index} AR QoS scale factor 3'b000 2 ⁽⁻⁵⁾ 3'b001 2 ⁽⁻⁶⁾ 3'b010 2 ⁽⁻⁷⁾ 3'b011 2 ⁽⁻⁸⁾ 3'b100 2 ⁽⁻⁹⁾ 3'b101 2 ⁽⁻¹⁰⁾ 3'b110 2 ⁽⁻¹¹⁾ 3'b111 2 ⁽⁻¹²⁾	RW	3'h0
[7:3]	Reserved	Reserved	RO	-
[2:0]	s#{index}_aw_lat_scale	Port S#{index} AW QoS scale factor 3'b000 2 ⁽⁻⁵⁾ 3'b001 2 ⁽⁻⁶⁾ 3'b010 2 ⁽⁻⁷⁾ 3'b011 2 ⁽⁻⁸⁾ 3'b100 2 ⁽⁻⁹⁾ 3'b101 2 ⁽⁻¹⁰⁾ 3'b110 2 ⁽⁻¹¹⁾ 3'b111 2 ⁽⁻¹²⁾	RW	3'h0

4.3.14.13 por_rnd_s0-2_qos_lat_range

There are 3 iterations of this register. The index ranges from 0 to 2. Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S#{index} read and write transactions.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`16'hA98 + #{index*32}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnd_secure_register_groups_override.qos_ctrl`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-573: por_rnd_s0-2_qos_lat_range

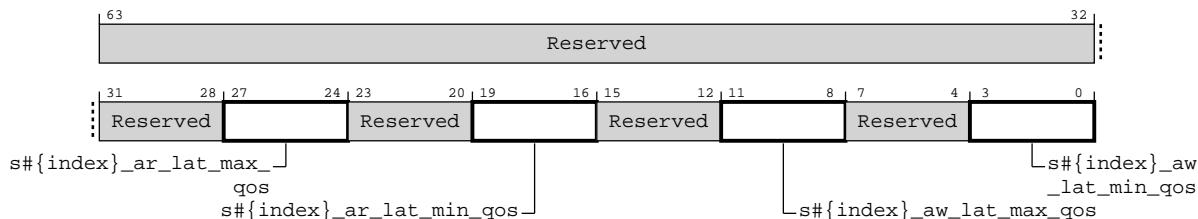


Table 4-589: por_rnd_s0-2_qos_lat_range attributes

Bits	Name	Description	Type	Reset
[63:28]	Reserved	Reserved	RO	-
[27:24]	s#{index}_ar_lat_max_qos	Port S#{index} AR QoS maximum value	RW	4'h0
[23:20]	Reserved	Reserved	RO	-
[19:16]	s#{index}_ar_lat_min_qos	Port S#{index} AR QoS minimum value	RW	4'h0
[15:12]	Reserved	Reserved	RO	-
[11:8]	s#{index}_aw_lat_max_qos	Port S#{index} AW QoS maximum value	RW	4'h0
[7:4]	Reserved	Reserved	RO	-
[3:0]	s#{index}_aw_lat_min_qos	Port S#{index} AW QoS minimum value	RW	4'h0

4.3.14.14 por_rnd_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-574: por_rnd_pmu_event_sel

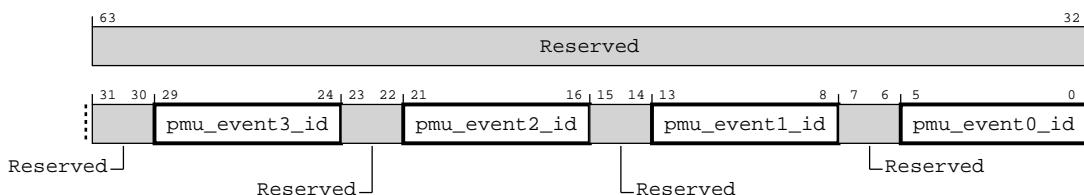


Table 4-590: por_rnd_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	RN-D PMU Event 3 ID; see pmu_event0_id for encodings	RW	6'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	RN-D PMU Event 2 ID; see pmu_event0_id for encodings	RW	6'b0
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	RN-D PMU Event 1 ID; see pmu_event0_id for encodings	RW	6'b0
[7:6]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[5:0]	pmu_event0_id	RN-D PMU Event 0 ID 6'h00 No event 6'h01 Port S0 RDataBeats 6'h02 Port S1 RDataBeats 6'h03 Port S2 RDataBeats 6'h04 RXDAT flits received 6'h05 TXDAT flits sent 6'h06 Total TXREQ flits sent 6'h07 Retried TXREQ flits sent 6'h08 RRT occupancy count overflow_slice0 6'h09 WRT occupancy count overflow 6'h0A Replicated TXREQ flits 6'h0B WriteCancel sent 6'h0C Port S0 WDataBeats 6'h0D Port S1 WDataBeats 6'h0E Port S2 WDataBeats 6'h0F RRT allocation 6'h10 WRT allocation 6'h11 PADB occupancy count overflow 6'h12 RPDB occupancy count overflow 6'h13 RRT occupancy count overflow_slice1 6'h14 RRT occupancy count overflow_slice2 6'h15 RRT occupancy count overflow_slice3 6'h16 WRT request throttled 6'h17 RNI backpressure CHI LDB full 6'h18 RRT normal rd req occupancy count overflow_slice0 6'h19 RRT normal rd req occupancy count overflow_slice1 6'h1A RRT normal rd req occupancy count overflow_slice2 6'h1B RRT normal rd req occupancy count overflow_slice3 6'h1C RRT PCIe RD burst req occupancy count overflow_slice0 6'h1D RRT PCIe RD burst req occupancy count overflow_slice1 6'h1E RRT PCIe RD burst req occupancy count overflow_slice2 6'h1F RRT PCIe RD burst req occupancy count overflow_slice3 6'h20 RRT PCIe RD burst allocation 6'h21 Compressed AWID ordering 6'h22 Atomic data buffer allocation 6'h23 Atomic data buffer occupancy	RW	6'b0

4.3.14.15 por_rnd_syscoreq_ctl

Functions as the RN-D DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoack_status.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C00

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-575: por_rnd_syscoreq_ctl

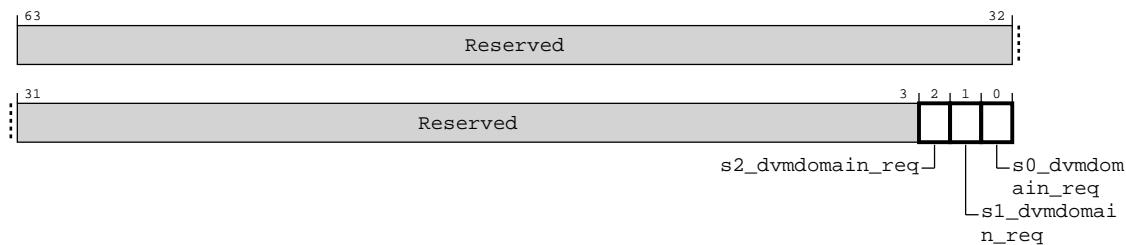


Table 4-591: por_rnd_syscoreq_ctl attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	s2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S2	RW	1'b0
[1]	s1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S1	RW	1'b0
[0]	s0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S0	RW	1'b0

4.3.14.16 por_rnd_syscoack_status

Functions as the RN-D DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoreq_ctl.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1C08

Type

RO

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-576: por_rnd_syscoack_status

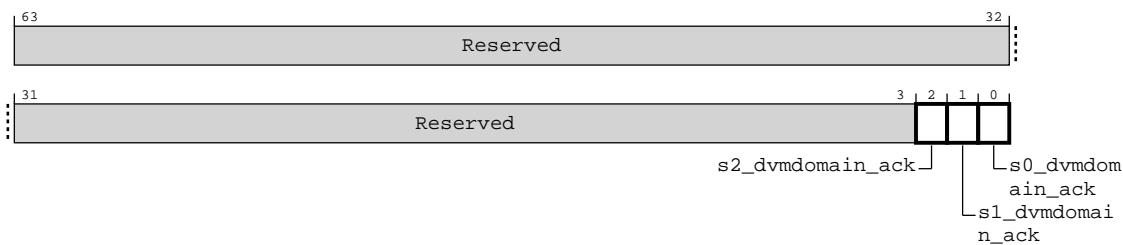


Table 4-592: por_rnd_syscoack_status attributes

Bits	Name	Description	Type	Reset
[63:3]	Reserved	Reserved	RO	-
[2]	s2_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S2	RO	1'b0
[1]	s1_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S1	RO	1'b0
[0]	s0_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S0	RO	1'b0

4.3.15 RN-I register descriptions

This section lists the RN-I registers.

4.3.15.1 por_rni_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-577: por_rni_node_info

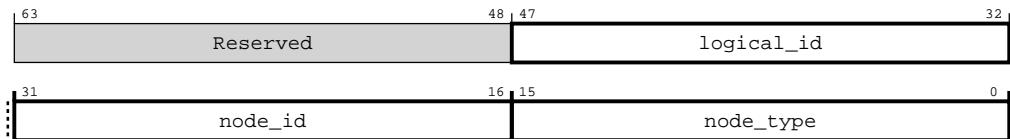


Table 4-593: por_rni_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h000A

4.3.15.2 por_rni_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-578: por_rni_child_info

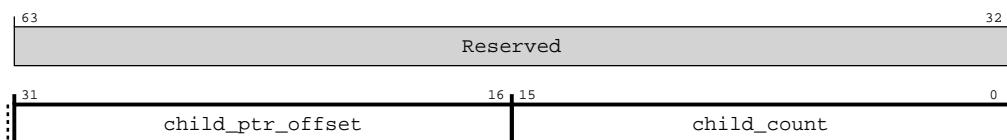


Table 4-594: por_rni_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'h0

4.3.15.3 por_rni_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-579: por_rni_secure_register_groups_override

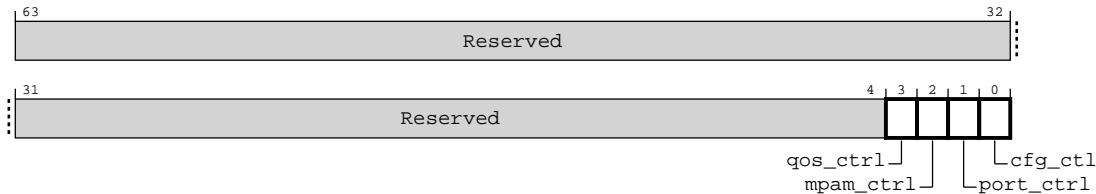


Table 4-595: por_rni_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:4]	Reserved	Reserved	RO	-
[3]	qos_ctrl	Allows Non-secure access to Secure QoS control registers	RW	1'b0
[2]	mpam_ctrl	Allows Non-secure access to Secure AXI port MPAM override register	RW	1'b0
[1]	port_ctrl	Allows Non-secure access to Secure AXI port control registers	RW	1'b0
[0]	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

4.3.15.4 por_rni_unit_info

Provides component identification information for RN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-580: por_rni_unit_info

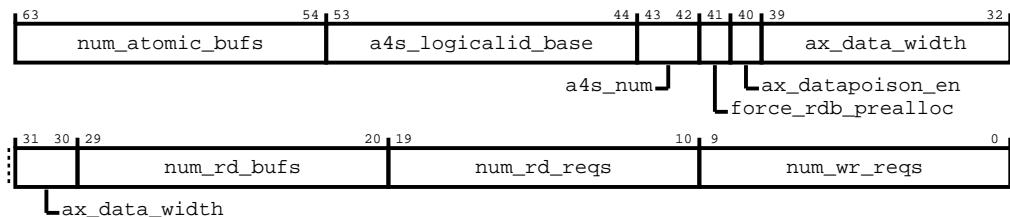


Table 4-596: por_rni_unit_info attributes

Bits	Name	Description	Type	Reset
[63:54]	num_atomic_bufs	Number of atomic data buffers	RO	Configuration dependent
[53:44]	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
[43:42]	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
[41]	force_rdb_prealloc	Force read data buffer preallocation	RO	Configuration dependent
		1'b1 Yes 1'b0 No		
[40]	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[39:30]	ax_data_width	AXI interface data width in bits	RO	Configuration dependent
[29:20]	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
[19:10]	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
[9:0]	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

4.3.15.5 por_rni_unit_info2

Provides additional component identification information for RN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-581: por_rni_unit_info2

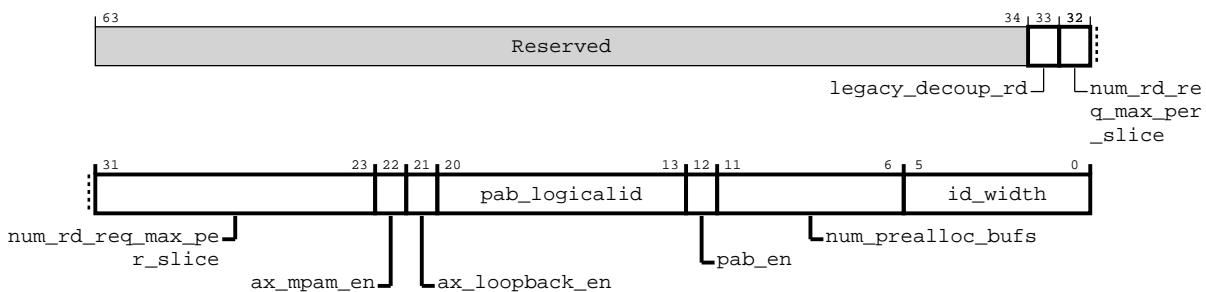


Table 4-597: por_rni_unit_info2 attributes

Bits	Name	Description	Type	Reset
[63:34]	Reserved	Reserved	RO	-
[33]	legacy_decoup_rd	Legacy decoupled read mode, no read burst propagation	RO	Configuration dependent
[32:23]	num_rd_req_max_per_slice	Number of read request entires per slice	RO	Configuration dependent
[22]	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface 1'b1 Enabled 1'b0 Not enabled	RO	Configuration dependent
[21]	ax_loopback_en	LoopBack enable on ACE-Lite/AXI4 interface 1'b1 Enabled 1'b0 Not enabled	RO	Configuration dependent
[20:13]	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
[12]	pab_en	PUB AUB bridge enable 1'b1 Enabled 1'b0 Not enabled	RO	Configuration dependent
[11:6]	num_prealloc_bufs	Number of Pre-allocated Read Data Buffers	RO	Configuration dependent
[5:0]	id_width	AXI ID width for ACE-Lite subordinate ports	RO	Configuration dependent

4.3.15.6 por_rni_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

por_rni_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-582: por_rni_cfg_ctl

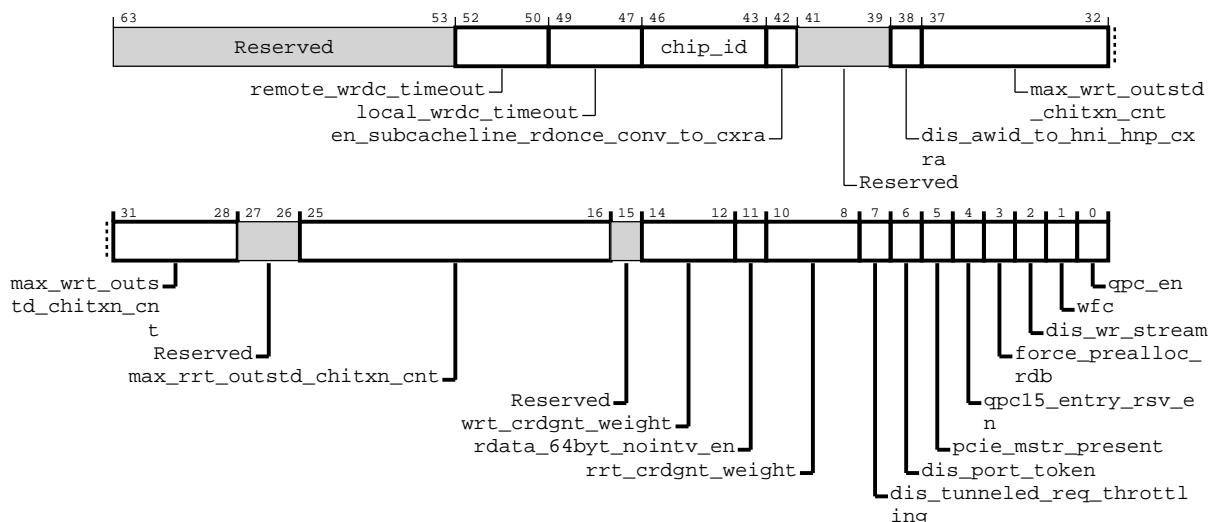


Table 4-598: por_rni_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:53]	Reserved	Reserved	RO	-
[52:50]	remote_wrdc_timeout	Configurable write data cancel timeout value for remote traffic. 3'b000 ~2000 cycles 3'b001 ~4000 cycles 3'b010 ~8000 cycles 3'b011 ~16000 cycles (default) 3'b100 ~32000 cycles (all other values rsvd)	RW	3'b011
[49:47]	local_wrdc_timeout	Configurable write data cancel timeout value for local traffic. 3'b000 ~2000 cycles 3'b001 ~4000 cycles 3'b010 ~8000 cycles 3'b011 ~16000 cycles (default) 3'b100 ~32000 cycles (all other values rsvd)	RW	3'b010
[46:43]	chip_id	Configurable ChipID for this RNX instance. Must be correctly set for proper handling of remote traffic to HNI/HNP. Only supports values 0..3. Two MSB's is reserved.	RW	4'b0000
[42]	en_subcacheline_rdonce_conv_to_cxra	If set, enables the conversion of sub-cacheline RdOnce to RdNoSnp for CXRA targets	RW	1'b0
[41:39]	Reserved	Reserved	RO	-
[38]	dis_awid_to_hni_hnp_cxra	If set, disables compressed AWID to HNI, HNP and CXRA, also disables compressed AWID based ordering. Set this bit if uniq-ID write performance is needed.	RW	1'b0
[37:28]	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
[27:26]	Reserved	Reserved	RO	-
[25:16]	max_rrt_outstd_chitxn_cnt	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
[15]	Reserved	Reserved	RO	-
[14:12]	wrt_crdgnt_weight	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
[11]	rdata_64byt_nointv_en	Enables no interleaving property on normal memory read data within 64B granule when set	RW	1'b1
[10:8]	rrt_crdgnt_weight	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
[7]	dis_tunneled_req_throttling	Disables retry based throttling of tunneled write requests	RW	1'b0
[6]	dis_port_token	If set, disables per port reservation in the tracker(rd and wr)	RW	1'b1
[5]	pcie_mstr_present	Indicates PCIe manager is present; must be set if PCIe manager is present upstream of RN-I or RN-D	RW	1'b0

Bits	Name	Description	Type	Reset
[4]	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1 Reserves tracker entry for QoS15 requests 1'b0 Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when por_rnd_qpc_en is set	RW	1'b0
[3]	force_prealloc_rdb	When set, all reads from the RN-I are sent with a preallocated read data buffer	RW	Configuration dependent
[2]	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
[1]	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
[0]	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

4.3.15.7 por_rni_aux_ctl

Functions as the auxiliary control register for RN-I.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-583: por_rni_aux_ctl

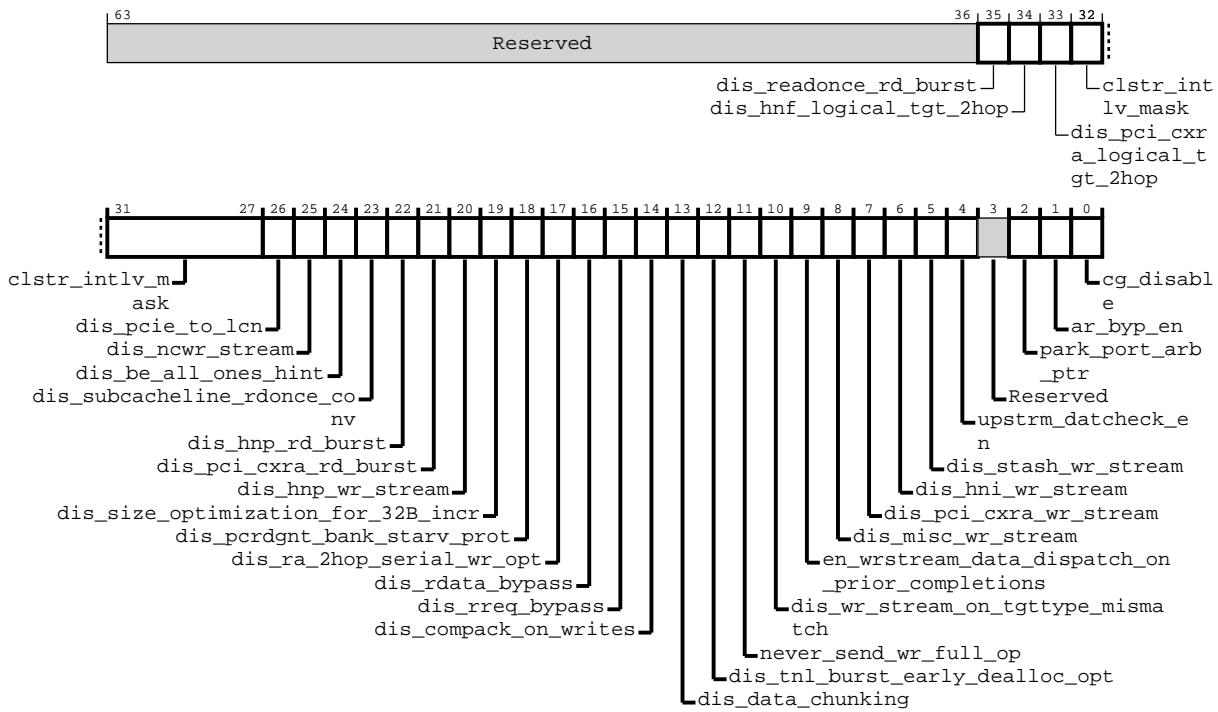


Table 4-599: por_rni_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset																
[39]	sys_dis_data_interleaving,	<p>System optimized disable read DATA interleaving for all ports. Disables all read data interleaving, including atomic read data being returned for all AXI ports. Read burst preservation is enabled similar to normal mode, but this requires certain system level restrictions:</p> <ol style="list-style-type: none"> 1. Cannot set SYS_DIS_DATA_INTERLEAVING for multi-chip systems. Support for remote HN-P is a future feature. 2. When setting SYS_DIS_DATA_INTERLEAVING for an RN-I/RN-D it is required for that RN-I/RN-D to target only one HN-P with read bursts. It is also required for the path to a single remote HN-P, when remote support is available, to only go through a single CCG and for the ccg_rni to also have SYS_DIS_DATA_INTERLEAVING set. 3. The AXI subordinate downstream of HN-P must not interleave read burst data. 4. Must have NUM_RD_REQ_PARAM==NUM_RD_BUF_PARAM and NUM_RD_REQ_PRAM<=256, otherwise this bit has no effect. 5. The sum of the maximum number of beats of a cracked burst per each port must fit wholly within an arslice - breaking this rule will result in a hang. Must comprehend DIS_PORT_TOKEN AND QPC15_ENTRY_RSV settings, which will limit number of available entries 	RW	1'b0																
[38:36]	Reserved	Reserved	RO	-																
[35]	dis_readonce_rd_burst	If set, disables read burst for ReadOnce from AXI.	RW	1'b0																
[34]	dis_hnf_logical_tgt_2hop	If set, disables tunneling/2hop for case where physical target is pci_cxra and logical target is hnf, otherwise may tunneling/2hop to RA if interleaving granularity settings allow.	RW	1'b0																
[33]	dis_pci_cxra_logical_tgt_2hop	If set, disables tunneling/2hop for case where physical and logical target is pci_cxra, otherwise tunneling/2hop to RA.	RW	1'b0																
[32:27]	clstr_intlv_mask	<p>Encoded static mask for max interleave granularity supported. When this setting is less than or equal to rnsam's programmed interleave granularity for a write to pci_cxra, tunneling/2hop flow will be used.</p> <table> <tbody> <tr> <td>6'b111111</td> <td>64B</td> </tr> <tr> <td>6'b111110</td> <td>128B</td> </tr> <tr> <td>6'b111100</td> <td>256B</td> </tr> <tr> <td>6'b111000</td> <td>512B</td> </tr> <tr> <td>6'b110000</td> <td>1024B</td> </tr> <tr> <td>6'b100000</td> <td>2048B</td> </tr> <tr> <td>6'b000000</td> <td>4096B</td> </tr> <tr> <td>Others</td> <td>Reserved</td> </tr> </tbody> </table>	6'b111111	64B	6'b111110	128B	6'b111100	256B	6'b111000	512B	6'b110000	1024B	6'b100000	2048B	6'b000000	4096B	Others	Reserved	RW	6'b0000000
6'b111111	64B																			
6'b111110	128B																			
6'b111100	256B																			
6'b111000	512B																			
6'b110000	1024B																			
6'b100000	2048B																			
6'b000000	4096B																			
Others	Reserved																			
[26]	dis_PCIE_to_lcn	If set, all PCIe traffic sent directly to HNF/CCG, bypasses LCN. Only has effect when pcie_mstr_present	RW	1'b1																
[25]	dis_ncwr_stream	Disables streaming of ordered non-cacheable writes when set	RW	1'b0																

Bits	Name	Description	Type	Reset
[24]	dis_be_all_ones_hint	If set, disables hint to HNF which signals all BE=1's on writes	RW	1'b0
[23]	dis_subcacheline_rdonce_conv	If set, disables the conversion of sub-cacheline RdOnce to RdNoSnp across all targets	RW	1'b0
[22]	dis_hnp_rd_burst	If set, disables read burst to HNP on CHI request flits . Read burst on CHI is supported only in non-decoupled RDB configuration.	RW	1'b0
[21]	dis_pci_cxra_rd_burst	If set, disables read burst to PCI-CXRA on CHI request flits . Read burst on CHI is supported only in non-decoupled RDB configuration.	RW	1'b0
[20]	dis_hnp_wr_stream	Disables streaming of ordered writes to HNP when set	RW	1'b0
[19]	dis_size_optimization_for_32B_incr	If set, disables the size related optimization for a 32B INCR burst (rh-2512). Only applies to writes.	RW	1'b0
[18]	dis_pcrdgnt_bank_starv_prot	If set, disables across arslice starvation protection	RW	1'b0
[17]	dis_ra_2hop_serial_wr_opt	If set, disables 2 hop indication to ra for serialized writes; will indicate 3 hop	RW	1'b0
[16]	dis_rdata_bypass	If set, disables read data bypass path	RW	1'b0
[15]	dis_rreq_bypass	If set, disables read request bypass path	RW	1'b0
[14]	dis_compack_on_writes	If set, disables comp_ack on streaming writes. WrData is used for ordering writes	RW	1'b1
[13]	dis_data_chunking	If set, disables the data chunking feature	RW	1'b0
[12]	dis_tnl_burst_early_dealloc_opt	If set, disables the optimization related to early deallocation of tunneled writes for intermediate txns of burst	RW	1'b0
[11]	never_send_wr_full_op	If set, RNI will never send WR FULL op. All write ops will be of PTL type	RW	1'b0
[10]	dis_wr_stream_on_tgtype_mismatch	If set, serializes first write when moving from one tgtype to another	RW	1'b0
[9]	en_wrstream_data_dispatch_on_prior_completions	If set, data dispatch for streaming writes waits for completion of all older writes	RW	1'b0
[8]	dis_misc_wr_stream	Disables streaming of ordered writes with following attributes when set : Device memory or EWA=0 or Excl=1	RW	1'b0
[7]	dis_pci_cxra_wr_stream	Disables streaming of ordered writes to PCI-CXRA when set	RW	1'b0
[6]	dis_hni_wr_stream	Disables streaming of ordered writes to HNI when set	RW	1'b0
[5]	dis_stash_wr_stream	Disables streaming of ordered WrUniqStash when set	RW	1'b0
[4]	upstrm_datcheck_en	Upstream supports Datacheck	RW	Configuration dependent
[3]	Reserved	Reserved	RO	-
[2]	park_port_arb_ptr	Parks the AXI port arbitration pointer for Burst	RW	1'b0
[1]	ar_byp_en	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
[0]	cg_disable	Disables clock gating when set	RW	1'b0

4.3.15.8 por_rni_s0-2_port_control

There are 3 iterations of this register. The index ranges from 0 to 2. Controls port S#{index} AXI/ACE subordinate interface settings.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
16'hA10 + #{index*8}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por rni secure register groups override.port ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-584: por_rni_s0-2 port control

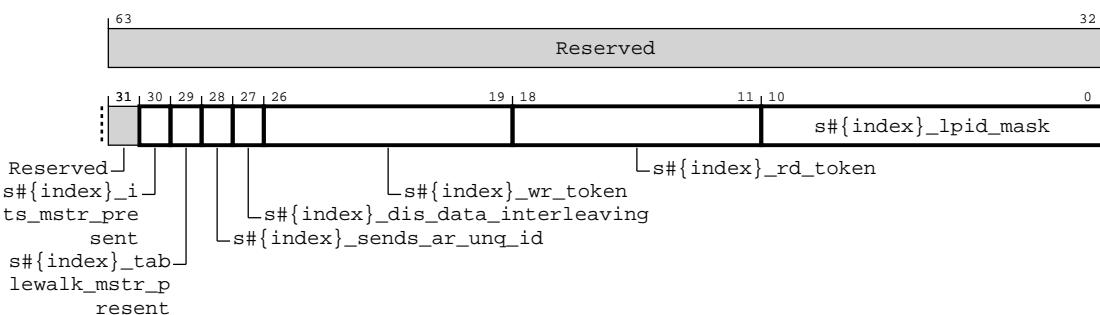


Table 4-600: por_rni_s0-2_port_control attributes

Bits	Name	Description	Type	Reset
[63:31]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[30]	s#{index}_its_mstr_present	Must be set if translation table walk manager present such as TCU or GIC for non-PCIE case. This affects RND AW channel only.	RW	1'b0
[29]	s#{index}_tablewalk_mstr_present	Must be set if translation table walk manager present such as TCU or GIC. This affects RND AR channel only.	RW	1'b0
[28]	s#{index}_sends_ar_unq_id	If set, indicates AR transactions on Port#{index} are always Unique ID. This bit for a port must be set to 1 to enable Read Burst on the CHI side of RND.	RW	1'b0
[27]	s#{index}_dis_data_interleaving	If set, disables read DATA interleaving on RDATAS#{index} channel. This applies only to RDATA generated as a response to requests on AR channel . This does not apply to RDATA generated as a response to Atomic request on AW channel. I.e. RDATA of an Atomic op, on AW channel, may interleave with RDATA of an AR channel request	RW	1'b0
[26:19]	s#{index}_wr_token	Port S#{index} reserved token count for AW channel This must be less than the number of Wr requests(RNID_NUM_XRT_REQ) on AW achnnel	RW	8'b0000_0000
[18:11]	s#{index}_rd_token	Port S#{index} reserved token count for AR channel per slice This should be less than the number of Rd requests(RNID_NUM_XRT_SLICE_REQ) per slice on AR achnnel	RW	8'b0000_0000
[10:0]	s#{index}_lpid_mask	Port S#{index} LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = !(AXID & mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

4.3.15.9 por_rni_s0-2_mpam_control

There are 3 iterations of this register. The index ranges from 0 to 2. Controls port S#{index} AXI/ACE subordinate interface MPAM override values

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA28 + #{index}*8}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rni_secure_register_groups_override.mpam_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-585: por_rni_s0-2_mpam_control

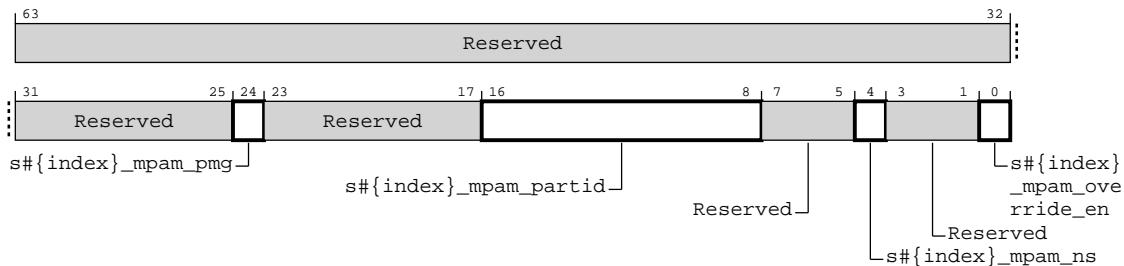


Table 4-601: por_rni_s0-2_mpam_control attributes

Bits	Name	Description	Type	Reset
[63:25]	Reserved	Reserved	RO	-
[24]	s#{index}_mpam_pmg	Port S#{index} MPAM_PMG value	RW	1'b0
[23:17]	Reserved	Reserved	RO	-
[16:8]	s#{index}_mpam_partid	Port S#{index} MPAM_PARTID value	RW	9'b0
[7:5]	Reserved	Reserved	RO	-
[4]	s#{index}_mpam_ns	Port S#{index} MPAM_NS value	RW	1'b0
[3:1]	Reserved	Reserved	RO	-
[0]	s#{index}_mpam_override_en	Port S#{index} MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

4.3.15.10 por_rni_s0-2_qos_control

There are 3 iterations of this register. The index ranges from 0 to 2. Controls QoS settings for port S#{index} AXI/ACE subordinate interface.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA80 + #{index}*32}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rni_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-586: por_rni_s0-2_qos_control

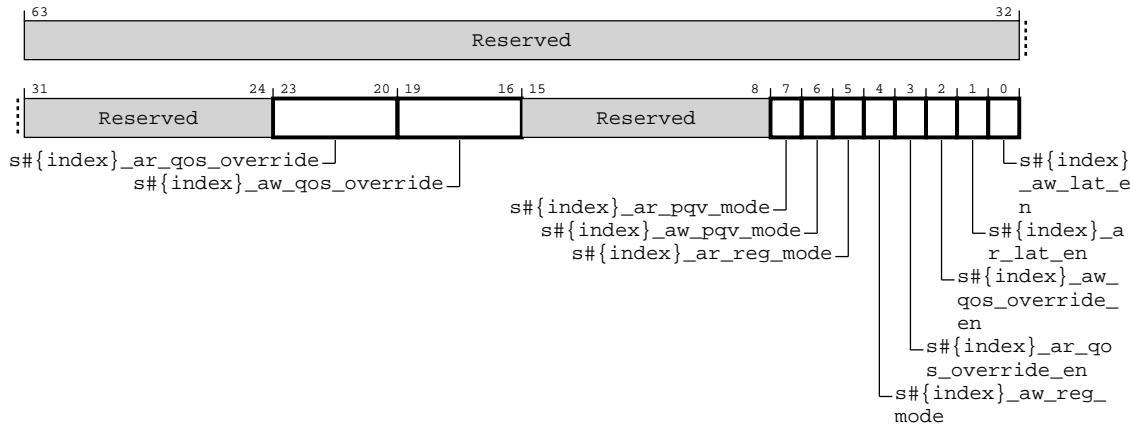


Table 4-602: por_rni_s0-2_qos_control attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:20]	s#{index}_ar_qos_override	AR QoS override value for port S#{index}	RW	4'b0000
[19:16]	s#{index}_aw_qos_override	AW QoS override value for port S#{index}	RW	4'b0000
[15:8]	Reserved	Reserved	RO	-
[7]	s#{index}_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0 Normal mode; QoS value is stable when the manager is idle 1'b1 Quiesce high mode; QoS value tends to the maximum value when the manager is idle	RW	1'b0
[6]	s#{index}_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0 Normal mode; QoS value is stable when the manager is idle 1'b1 Quiesce high mode; QoS value tends to the maximum value when the manager is idle	RW	1'b0

Bits	Name	Description	Type	Reset
[5]	s#{index}_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0 Latency mode 1'b1 Period mode; used for bandwidth regulation	RW	1'b0
[4]	s#{index}_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0 Latency mode 1'b1 Period mode; used for bandwidth regulation	RW	1'b0
[3]	s#{index}_ar_qos_override_en	Enables port S#{index} AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
[2]	s#{index}_aw_qos_override_en	Enables port S#{index} AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
[1]	s#{index}_ar_lat_en	Enables port S#{index} AR QoS regulation when set	RW	1'b0
[0]	s#{index}_aw_lat_en	Enables port S#{index} AW QoS regulation when set	RW	1'b0

4.3.15.11 por_rni_s0-2_qos_lat_tgt

There are 3 iterations of this register. The index ranges from 0 to 2. Controls QoS target latency (in cycles) for regulations of port S#{index} read and write transactions.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA88 + #{index*32}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rni_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-587: por_rni_s0-2_qos_lat_tgt

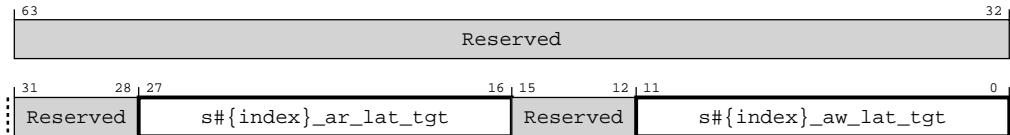


Table 4-603: por_rni_s0-2_qos_lat_tgt attributes

Bits	Name	Description	Type	Reset
[63:28]	Reserved	Reserved	RO	-
[27:16]	s#{index}_ar_lat_tgt	Port S#{index} AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
[15:12]	Reserved	Reserved	RO	-
[11:0]	s#{index}_aw_lat_tgt	Port S#{index} AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

4.3.15.12 por_rni_s0-2_qos_lat_scale

There are 3 iterations of this register. The index ranges from 0 to 2. Controls the QoS target latency scale factor for port S#{index} read and write transactions. This register represents powers of two from the range 2^{-5} to 2^{-12} ; it is used to match a 16-bit integrator.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

$16^{\prime}hA90 + \#\{index*32\}$

Type

RW

Reset value

See individual bit resets

Secure group override

por_rni_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-588: por_rni_s0-2_qos_lat_scale

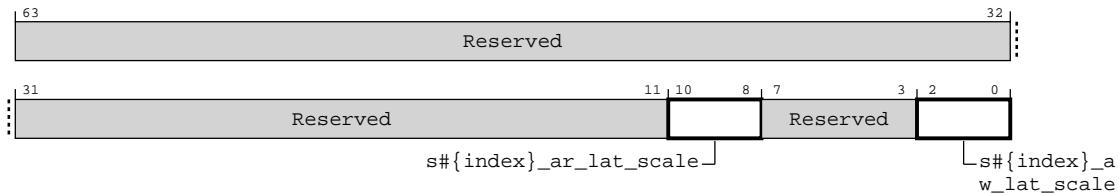


Table 4-604: por_rni_s0-2_qos_lat_scale attributes

Bits	Name	Description	Type	Reset
[63:11]	Reserved	Reserved	RO	-
[10:8]	s#{index}_ar_lat_scale	Port S#{index} AR QoS scale factor	RW	3'h0
	3'b000	2^{-5}		
	3'b001	2^{-6}		
	3'b010	2^{-7}		
	3'b011	2^{-8}		
	3'b100	2^{-9}		
	3'b101	2^{-10}		
	3'b110	2^{-11}		
	3'b111	2^{-12}		
[7:3]	Reserved	Reserved	RO	-
[2:0]	s#{index}_aw_lat_scale	Port S#{index} AW QoS scale factor	RW	3'h0
	3'b000	2^{-5}		
	3'b001	2^{-6}		
	3'b010	2^{-7}		
	3'b011	2^{-8}		
	3'b100	2^{-9}		
	3'b101	2^{-10}		
	3'b110	2^{-11}		
	3'b111	2^{-12}		

4.3.15.13 por_rni_s0-2_qos_lat_range

There are 3 iterations of this register. The index ranges from 0 to 2. Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S#{index} read and write transactions.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA98 + # {index*32}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rni_secure_register_groups_override.qos_ctrl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-589: por_rni_s0-2_qos_lat_range

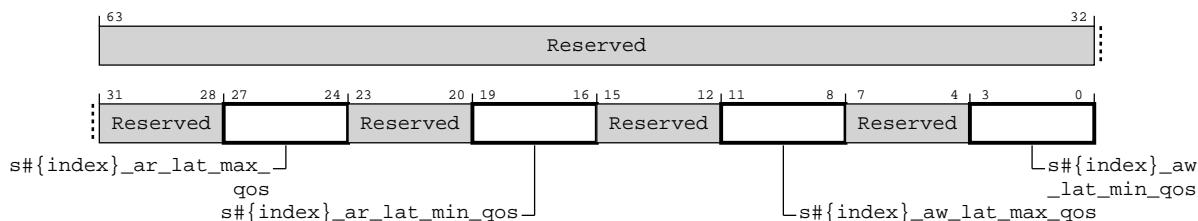


Table 4-605: por_rni_s0-2_qos_lat_range attributes

Bits	Name	Description	Type	Reset
[63:28]	Reserved	Reserved	RO	-
[27:24]	s#{index}_ar_lat_max_qos	Port S#{index} AR QoS maximum value	RW	4'h0
[23:20]	Reserved	Reserved	RO	-
[19:16]	s#{index}_ar_lat_min_qos	Port S#{index} AR QoS minimum value	RW	4'h0
[15:12]	Reserved	Reserved	RO	-
[11:8]	s#{index}_aw_lat_max_qos	Port S#{index} AW QoS maximum value	RW	4'h0
[7:4]	Reserved	Reserved	RO	-
[3:0]	s#{index}_aw_lat_min_qos	Port S#{index} AW QoS minimum value	RW	4'h0

4.3.15.14 por_rni_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-590: por_rni_pmu_event_sel

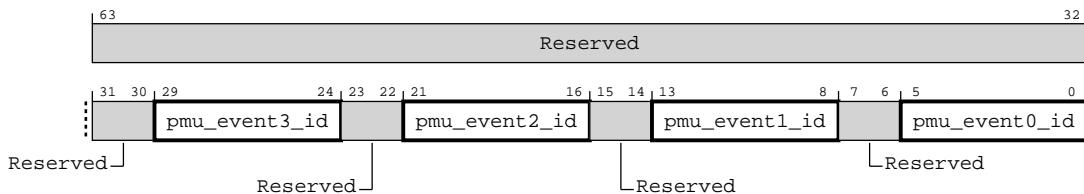


Table 4-606: por_rni_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	RN-I PMU Event 3 ID; see pmu_event0_id for encodings	RW	6'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	RN-I PMU Event 2 ID; see pmu_event0_id for encodings	RW	6'b0
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	RN-I PMU Event 1 ID; see pmu_event0_id for encodings	RW	6'b0
[7:6]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[5:0]	pmu_event0_id	RN-I PMU Event 0 ID 6'h00 No event 6'h01 Port S0 RDataBeats 6'h02 Port S1 RDataBeats 6'h03 Port S2 RDataBeats 6'h04 RXDAT flits received 6'h05 TXDAT flits sent 6'h06 Total TXREQ flits sent 6'h07 Retried TXREQ flits sent 6'h08 RRT occupancy count overflow_slice0 6'h09 WRT occupancy count overflow 6'h0A Replicated TXREQ flits 6'h0B WriteCancel sent 6'h0C Port S0 WDataBeats 6'h0D Port S1 WDataBeats 6'h0E Port S2 WDataBeats 6'h0F RRT allocation 6'h10 WRT allocation 6'h11 PADB occupancy count overflow 6'h12 RPDB occupancy count overflow 6'h13 RRT occupancy count overflow_slice1 6'h14 RRT occupancy count overflow_slice2 6'h15 RRT occupancy count overflow_slice3 6'h16 WRT request throttled 6'h17 RNI backpressure CHI LDB full 6'h18 RRT normal rd req occupancy count overflow_slice0 6'h19 RRT normal rd req occupancy count overflow_slice1 6'h1A RRT normal rd req occupancy count overflow_slice2 6'h1B RRT normal rd req occupancy count overflow_slice3 6'h1C RRT PCIe RD burst req occupancy count overflow_slice0 6'h1D RRT PCIe RD burst req occupancy count overflow_slice1 6'h1E RRT PCIe RD burst req occupancy count overflow_slice2 6'h1F RRT PCIe RD burst req occupancy count overflow_slice3 6'h20 RRT PCIe RD burst allocation 6'h21 Compressed AWID ordering 6'h22 Atomic data buffer allocation 6'h23 Atomic data buffer occupancy	RW	6'b0

4.3.16 RN SAM register descriptions

This section lists the RN SAM registers.

4.3.16.1 por_rnsam_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-591: por_rnsam_node_info

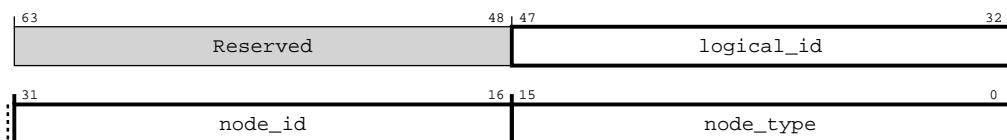


Table 4-607: por_rnsam_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID NOTE: RN SAM logical ID is always set to 16'b0.	RO	16'h0
[31:16]	node_id	Component node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h000F

4.3.16.2 por_rnsam_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-592: por_rnsam_child_info

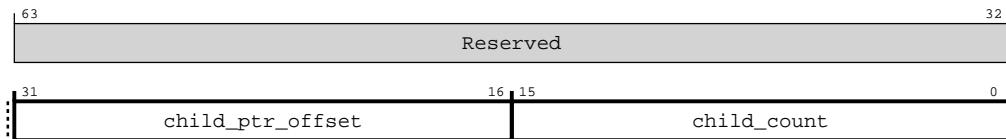


Table 4-608: por_rnsam_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.16.3 por_rnsam_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-593: por_rnsam_secure_register_groups_override

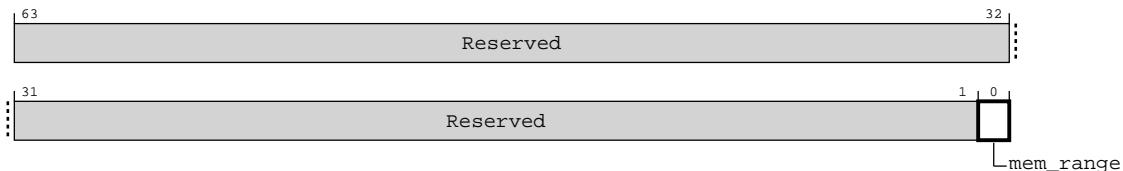


Table 4-609: por_rnsam_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	mem_range	Allows Non-secure access to Secure mem_ranges registers	RW	1'b0

4.3.16.4 por_rnsam_unit_info

Provides component identification information for RN SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-594: por_rnsam_unit_info

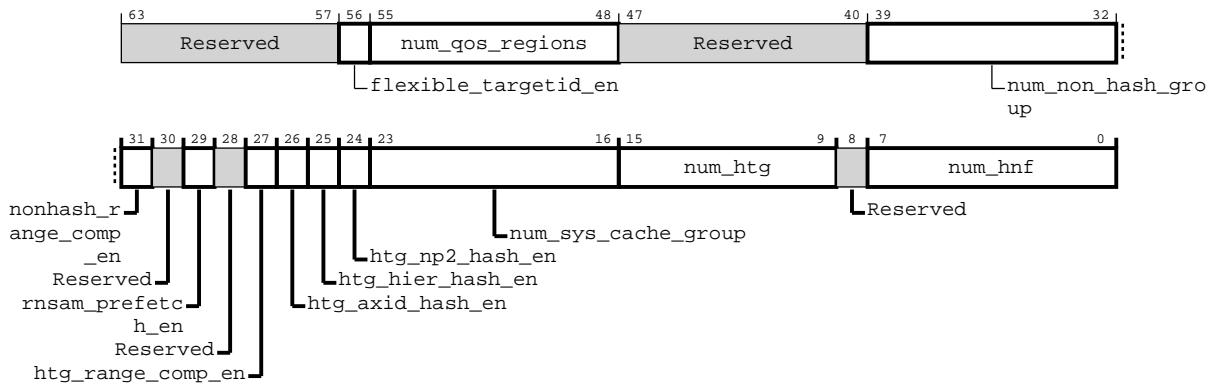


Table 4-610: por_rnsam_unit_info attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56]	flexible_targetid_en	flexible target enable to preserve backward compatibility	RO	Configuration dependent
[55:48]	num_qos_regions	Number of QOS regions	RO	Configuration dependent
[47:40]	Reserved	Reserved	RO	-
[39:32]	num_non_hash_group	Number of non-hashed groups supported	RO	Configuration dependent
[31]	nonhash_range_comp_en	Define start and end address for each HTG region	RO	Configuration dependent
[30]	Reserved	Reserved	RO	-
[29]	rnsam_prefetch_en	RNSAM prefetch enabled	RO	Configuration dependent
[28]	Reserved	Reserved	RO	-
[27]	htg_range_comp_en	Define start and end address for each HTG region	RO	Configuration dependent
[26]	htg_axid_hash_en	Enable AXID based hashing scheme	RO	Configuration dependent
[25]	htg_hier_hash_en	Enable Hierarchical hashing scheme	RO	Configuration dependent
[24]	htg_np2_hash_en	Enable non-power of two hash scheme	RO	Configuration dependent
[23:16]	num_sys_cache_group	Number of system cache groups supported This register field value has deprecated its reset value is always 0	RO	0
[15:9]	num_htg	Number of Hashed target groups	RO	Configuration dependent
[8]	Reserved	Reserved	RO	-
[7:0]	num_hnf	Number of hashed targets supported	RO	Configuration dependent

4.3.16.5 por_rnsam_unit_info1

Provides component identification information for RN SAM.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h908

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-595: por_rnsam_unit_info1

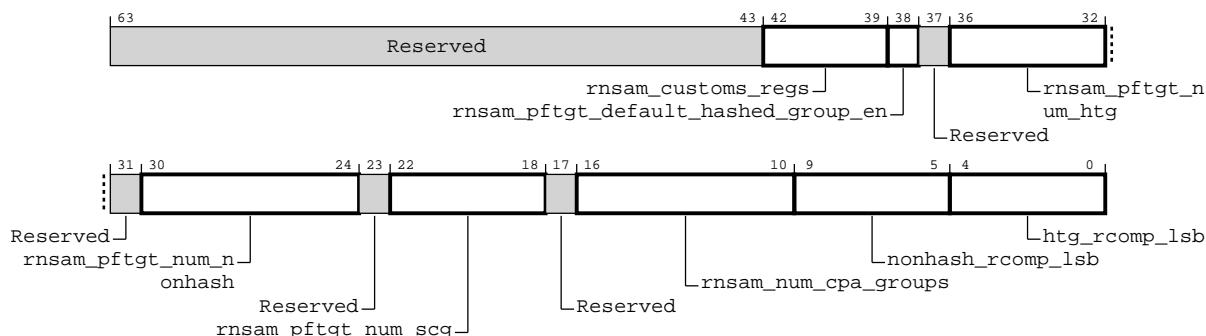


Table 4-611: por_rnsam_unit_info1 attributes

Bits	Name	Description	Type	Reset
[63:43]	Reserved	Reserved	RO	-
[42:39]	rnsam_customs_regs	Number of customer specific registers for customer implemented logic	RO	Configuration dependent
[38]	rnsam_pftgt_default_hashed_group_en	Enable default hashed group for prefetch transactions. To support backward compatible, set this parameter	RO	Configuration dependent
[37]	Reserved	Reserved	RO	-
[36:32]	rnsam_pftgt_num_htg	Number of prefetch HTG regions supported per System Cache Group by the RNSAM	RO	Configuration dependent
[31]	Reserved	Reserved	RO	-
[30:24]	rnsam_pftgt_num_nonhash	Number of prefetch non-hashed regions supported per System Cache Group by the RNSAM	RO	Configuration dependent
[23]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[22:18]	rnsam_pftgt_num_scg	Number of system cache groups enabled for prefetch targets	RO	Configuration dependent
[17]	Reserved	Reserved	RO	-
[16:10]	rnsam_num_cpa_groups	Number of CPA groups	RO	Configuration dependent
[9:5]	nonhash_rcomp_lsb	NONHASH RCOMP LSB bit position defining minimum region size	RO	Configuration dependent
[4:0]	htg_rcomp_lsb	HTG RCOMP LSB bit position defining minimum region size	RO	Configuration dependent

4.3.16.6 non_hash_mem_region_reg0-63

There are 64 iterations of this register. The index ranges from 0 to 63. Configures non-hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-23) : 16'hC00 + #{8 * index}
index(24-63) : 16'h2000 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-596: non_hash_mem_region_reg0-63

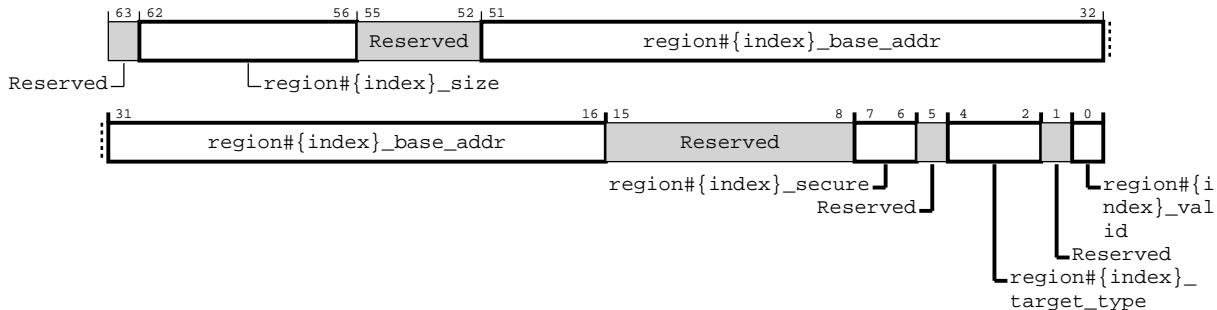


Table 4-612: non_hash_mem_region_reg0-63 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	region#{index}_size	Memory region #{index} size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'h0
[55:52]	Reserved	Reserved	RO	-
[51:16]	region#{index}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAM_NONHASH_RCOMP_LSB_PARAM	RW	36'h0
[15:8]	Reserved	Reserved	RO	-
[7:6]	region#{index}_secure	Indicates Secure type 2'b00 Trusted device. 2'b01 Trusted device attached memory range only 2'b10 Untrusted device 2'b11 Reserved	RW	2'b10
[5]	Reserved	Reserved	RO	-
[4:2]	region#{index}_target_type	Indicates node type 3'b000 HN-F 3'b001 HN-I 3'b010 CXRA 3'b011 HN-P 3'b100 PCI-CXRA 3'b101 HN-S Others Reserved CONSTRAINT: Only applicable for RN-I	RW	3'b000

Bits	Name	Description	Type	Reset
[1]	Reserved	Reserved	RO	-
[0]	region#{index}_valid	Memory region #{index} valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.7 non_hash_mem_region_cfg2_reg0-63

There are 64 iterations of this register. The index ranges from 0 to 63. Configures non-hashed memory region end address

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-23) : 16'hCC0 + #{8 * index}
index(24-151) : 16'h2400 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-597: non_hash_mem_region_cfg2_reg0-63

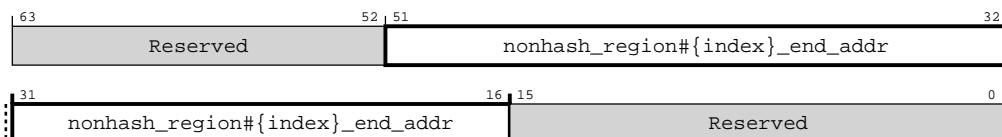


Table 4-613: non_hash_mem_region_cfg2_reg0-63 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	nonhash_region#{index}_end_addr	Bits [51:16] of end address of the range, LSB bit is defined by the parameter POR_RNSAM_NONHASH_RCOMP_LSB_PARAM	RW	36'h0
[15:0]	Reserved	Reserved	RO	-

4.3.16.8 non_hash_tgt_nodeid0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures non-hashed target node IDs # $\{4 * \text{index}\}$ to # $\{4 * \text{index} + 3\}$.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-15) : 16'hD80 + #{8 * index}
index(16-47) : 16'h2800 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-598: non_hash_tgt_nodeid0-15

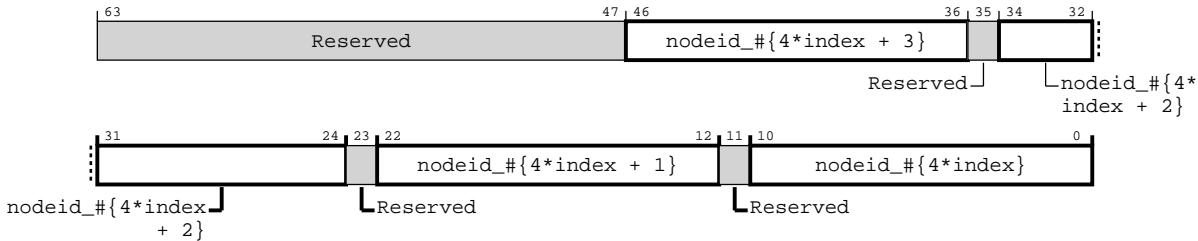


Table 4-614: non_hash_tgt_nodeid0-15 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:36]	nodeid_{4*index + 3}	Non-hashed target node ID #{4*index + 3}	RW	11'b000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	nodeid_{4*index + 2}	Non-hashed target node ID #{4*index + 2}	RW	11'b000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	nodeid_{4*index + 1}	Non-hashed target node ID #{4*index + 1}	RW	11'b000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	nodeid_{4*index}	Non-hashed target node ID #{4*index}	RW	11'b000000000000

4.3.16.9 cml_port_aggr_mode_ctrl_reg

Configures the CCI-X port aggregation modes for all non-hashed memory regions.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h11A0

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-599: cml_port_aggr_mode_ctrl_reg

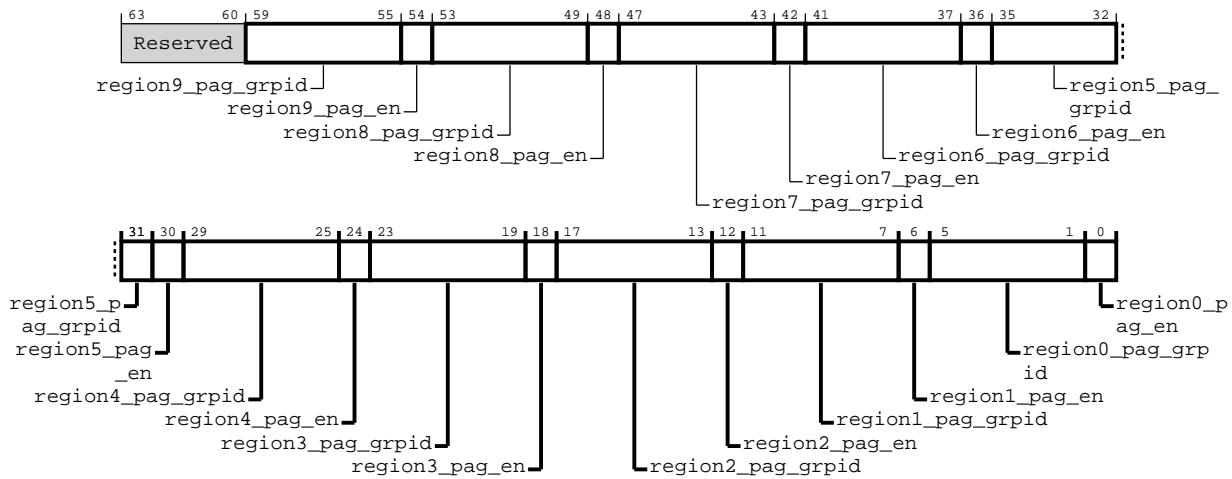


Table 4-615: cml_port_aggr_mode_ctrl_reg attributes

Bits	Name	Description	Type	Reset
[63:60]	Reserved	Reserved	RO	-
[59:55]	region9_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[54]	region9_pag_en	Enables the CPA mode for non-hashed memory region 9	RW	1'b0
[53:49]	region8_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[48]	region8_pag_en	Enables the CPA mode for non-hashed memory region 8	RW	1'b0
[47:43]	region7_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[42]	region7_pag_en	Enables the CPA mode for non-hashed memory region 7	RW	1'b0
[41:37]	region6_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[36]	region6_pag_en	Enables the CPA mode for non-hashed memory region 6	RW	1'b0
[35:31]	region5_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[30]	region5_pag_en	Enables the CPA mode for non-hashed memory region 5	RW	1'b0
[29:25]	region4_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[24]	region4_pag_en	Enables the CPA mode for non-hashed memory region 4	RW	1'b0
[23:19]	region3_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[18]	region3_pag_en	Enables the CPA mode for non-hashed memory region 3	RW	1'b0
[17:13]	region2_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[12]	region2_pag_en	Enables the CPA mode for non-hashed memory region 2	RW	1'b0
[11:7]	region1_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[6]	region1_pag_en	Enables the CPA mode for non-hashed memory region 1	RW	1'b0
[5:1]	region0_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[0]	region0_pag_en	Enables the CPA mode for non-hashed memory region 0	RW	1'b0

4.3.16.10 cml_port_aggr_mode_ctrl_reg1-6

There are 6 iterations of this register. The index ranges from 1 to 6. Configures the CCIX port aggregation modes for all non-hashed memory regions.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-3) : 16'h11A0 + #{8 * index}  
index(4-6) : 16'h2A00 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-600: cml_port_aggr_mode_ctrl_reg1-6

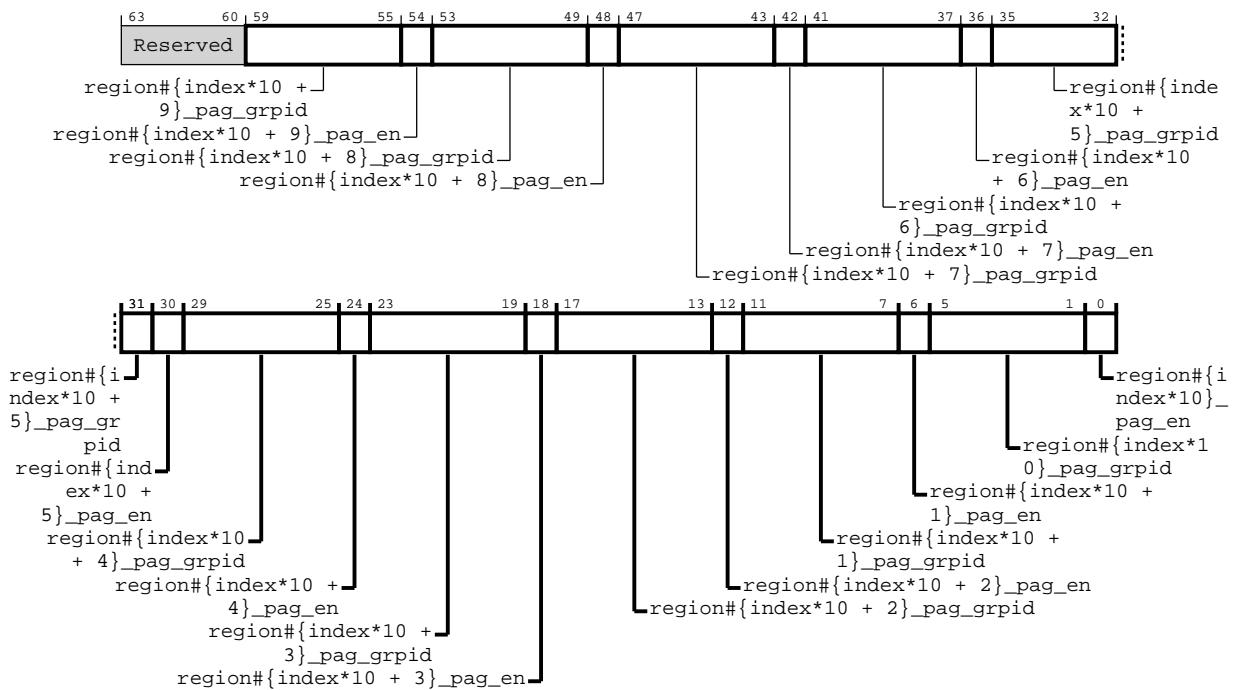


Table 4-616: cml_port_aggr_mode_ctrl_reg1-6 attributes

Bits	Name	Description	Type	Reset
[63:60]	Reserved	Reserved	RO	-
[59:55]	region#{index*10 + 9}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[54]	region#{index*10 + 9}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 9}	RW	1'b0
[53:49]	region#{index*10 + 8}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[48]	region#{index*10 + 8}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 8}	RW	1'b0
[47:43]	region#{index*10 + 7}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[42]	region#{index*10 + 7}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 7}	RW	1'b0
[41:37]	region#{index*10 + 6}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[36]	region#{index*10 + 6}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 6}	RW	1'b0
[35:31]	region#{index*10 + 5}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[30]	region#{index*10 + 5}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 5}	RW	1'b0
[29:25]	region#{index*10 + 4}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[24]	region#{index*10 + 4}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 4}	RW	1'b0
[23:19]	region#{index*10 + 3}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[18]	region#{index*10 + 3}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 3}	RW	1'b0
[17:13]	region#{index*10 + 2}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[12]	region#{index*10 + 2}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 2}	RW	1'b0
[11:7]	region#{index*10 + 1}_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[6]	region#{index*10 + 1}_pag_en	Enables the CPA mode for non-hashed memory region #{index*10 + 1}	RW	1'b0

Bits	Name	Description	Type	Reset
[5:1]	region#[index*10]_pag_grpid	Specifies CCIX port aggregation group ID	RW	5'h0
[0]	region#[index*10]_pag_en	Enables the CPA mode for non-hashed memory region #{index*10}	RW	1'b0

4.3.16.11 sys_cache_grp_region0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE00 + #{8*index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-601: sys_cache_grp_region0-3

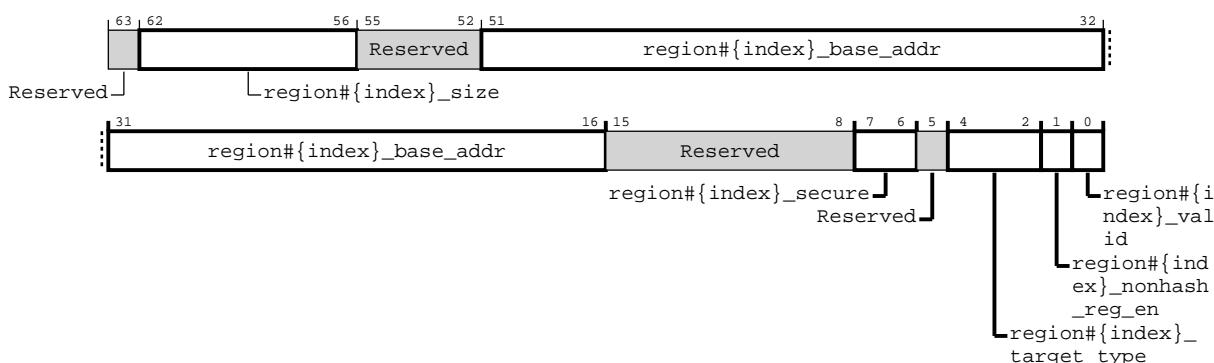


Table 4-617: sys_cache_grp_region0-3 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	region#{index}_size	Memory region #{index} size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	7'b00000000
[55:52]	Reserved	Reserved	RO	-
[51:16]	region#{index}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAM_HTG_RCOMP_LSB_PARAM	RW	36'b00000000000000000000000000000000
[15:8]	Reserved	Reserved	RO	-
[7:6]	region#{index}_secure	Indicates Secure type 2'b00 Trusted device. 2'b01 Trusted device attached memory range only 2'b10 Untrusted device 2'b11 Reserved	RW	2'b10
[5]	Reserved	Reserved	RO	-
[4:2]	region#{index}_target_type	Indicates node type 3'b000 HN-F 3'b001 HN-I 3'b010 CXRA 3'b011 HN-P 3'b100 PCI-CXRA 3'b101 HN-S Others Reserved CONSTRAINT: Only applicable for RN-I	RW	3'b000
[1]	region#{index}_nonhash_reg_en	Enables hashed region #{index} to select non-hashed node	RW	1'b0
[0]	region#{index}_valid	Memory region #{index} valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.12 hashed_tgt_grp_cfg1_region4-31

There are 28 iterations of this register. The index ranges from 4 to 31. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-7) : 16'hE00 + #{8 * index}  
index(8-31) : 16'h3000 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-602: hashed_tgt_grp_cfg1_region4-31

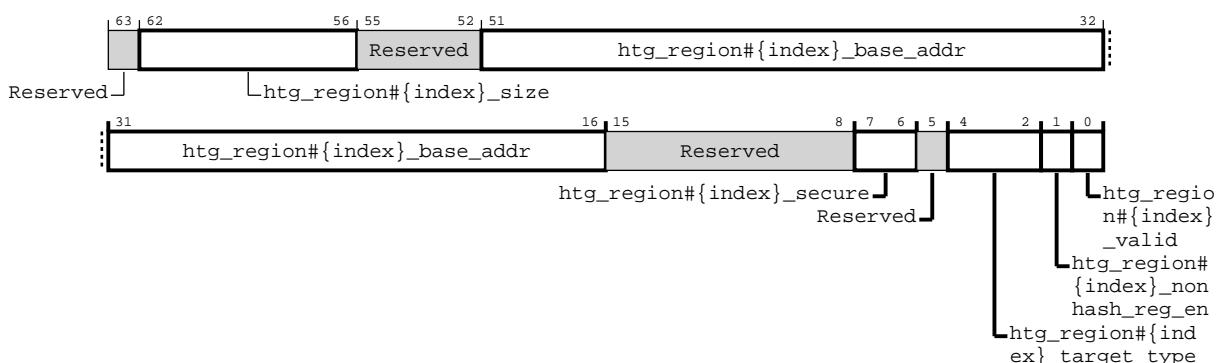


Table 4-618: hashed_tgt_grp_cfg1_region4-31 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	htg_region#{index}_size	Memory region #{index} size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
[55:52]	Reserved	Reserved	RO	-
[51:16]	htg_region#{index}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'h0
[15:8]	Reserved	Reserved	RO	-
[7:6]	htg_region#{index}_secure	Indicates Secure type 2'b00 Trusted device. 2'b01 Trusted device attached memory range only 2'b10 Untrusted device 2'b11 Reserved	RW	2'b10
[5]	Reserved	Reserved	RO	-
[4:2]	htg_region#{index}_target_type	Indicates node type 3'b000 HN-F 3'b001 HN-I 3'b010 CXRA 3'b011 HN-P 3'b100 PCI-CXRA 3'b101 HN-S Others Reserved CONSTRAINT: Only applicable for RN-I	RW	3'b000
[1]	htg_region#{index}_nonhash_reg_en	Enables hashed region #{index} to select non-hashed node	RW	1'b0
[0]	htg_region#{index}_valid	Memory region #{index} valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.13 hashed_tgt_grp_cfg2_region0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-31) : 16'h3100 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnsam_secure_register_groups_override.mem_range`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-603: hashed_tgt_grp_cfg2_region0-31

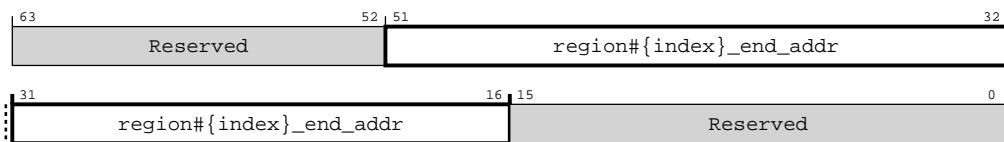


Table 4-619: hashed_tgt_grp_cfg2_region0-31 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	region#{index}_end_addr	Bits [51:16] of end address of the range, LSB bit is defined by the parameter POR_RNSAM_HTG_RCOMP_LSB_PARAM	RW	36'h0
[15:0]	Reserved	Reserved	RO	-

4.3.16.14 sys_cache_grp_secondary_reg0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Configures secondary hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-7) : 16'hE40 + #{8 * index}
index(8-31) : 16'h3200 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-604: sys_cache_grp_secondary_reg0-3

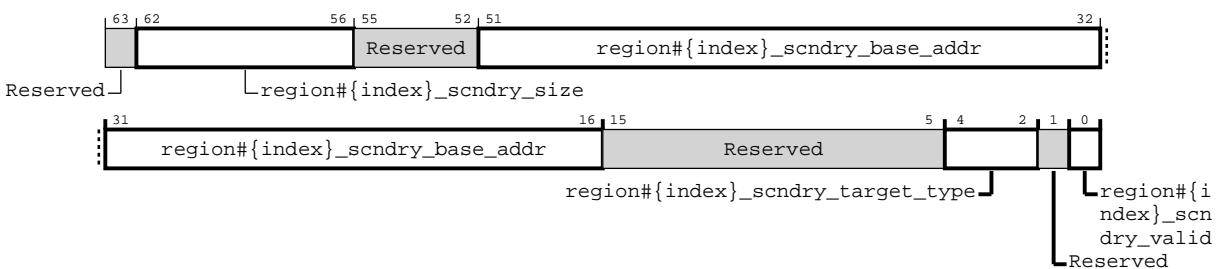


Table 4-620: sys_cache_grp_secondary_reg0-3 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[62:56]	region#{index}_scndry_size	Secondary memory region #{index} size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
[55:52]	Reserved	Reserved	RO	-
[51:16]	region#{index}_scndry_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'h0
[15:5]	Reserved	Reserved	RO	-
[4:2]	region#{index}_scndry_target_type	Indicates node type 3'b000 HN-F 3'b001 HN-I 3'b010 CXRA 3'b011 HN-P 3'b100 PCI-CXRA 3'b101 HN-S Others Reserved CONSTRAINT: Only applicable for RN-I	RW	3'b000
[1]	Reserved	Reserved	RO	-
[0]	region#{index}_scndry_valid	Secondary memory region #{index} valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.15 hashed_target_grp_secondary_cfg1_reg4-31

There are 28 iterations of this register. The index ranges from 4 to 31. Configures secondary hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-7) : 16'hE40 + #{8 * index}
index(8-31) : 16'h3200 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-605: hashed_target_grp_secondary_cfg1_reg4-31

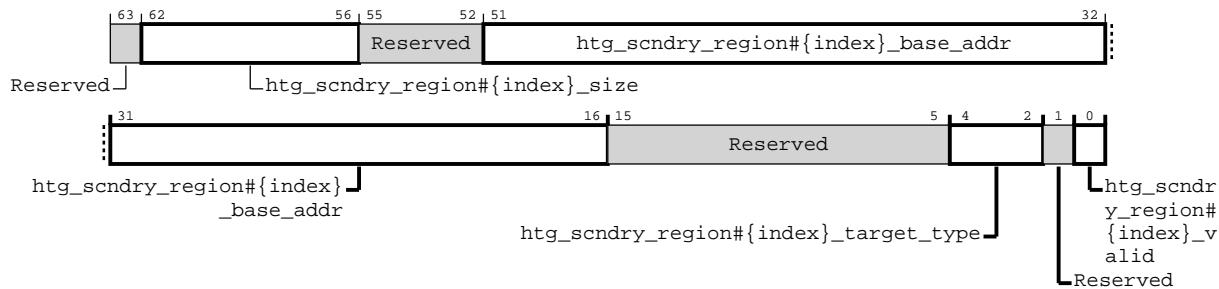


Table 4-621: hashed_target_grp_secondary_cfg1_reg4-31 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	htg_scndry_region#{index}_size	Secondary memory region #{index} size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
[55:52]	Reserved	Reserved	RO	-
[51:16]	htg_scndry_region#{index}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'h0
[15:5]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[4:2]	htg_scndry_region#{index}_target_type	Indicates node type 3'b000 HN-F 3'b001 HN-I 3'b010 CXRA 3'b011 HN-P 3'b100 PCI-CXRA 3'b101 HN-S Others Reserved CONSTRAINT: Only applicable for RN-I	RW	3'b000
[1]	Reserved	Reserved	RO	-
[0]	htg_scndry_region#{index}_valid	Secondary memory region #{index} valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.16 hashed_target_grp_secondary_cfg2_reg0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures hashed memory regions

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h3300 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnsam_secure_register_groups_override.mem_range`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-606: hashed_target_grp_secondary_cfg2_reg0-31

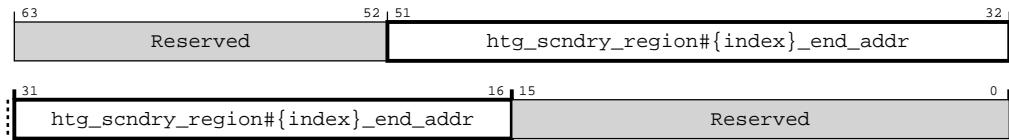


Table 4-622: hashed_target_grp_secondary_cfg2_reg0-31 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	htg_scndry_region#{index}_end_addr	Bits [51:16] of end address of the range, LSB bit is defined by the parameter POR_RNSAMHTG_RCOMP_LSB_PARAM	RW	36'b00000000000000000000000000000000
[15:0]	Reserved	Reserved	RO	-

4.3.16.17 hashed_target_grp_hash_cntl_reg0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures HTG hash type

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-31) : 16'h3400 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnsam_secure_register_groups_override.mem_range`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-607: hashed_target_grp_hash_cntl_reg0-31

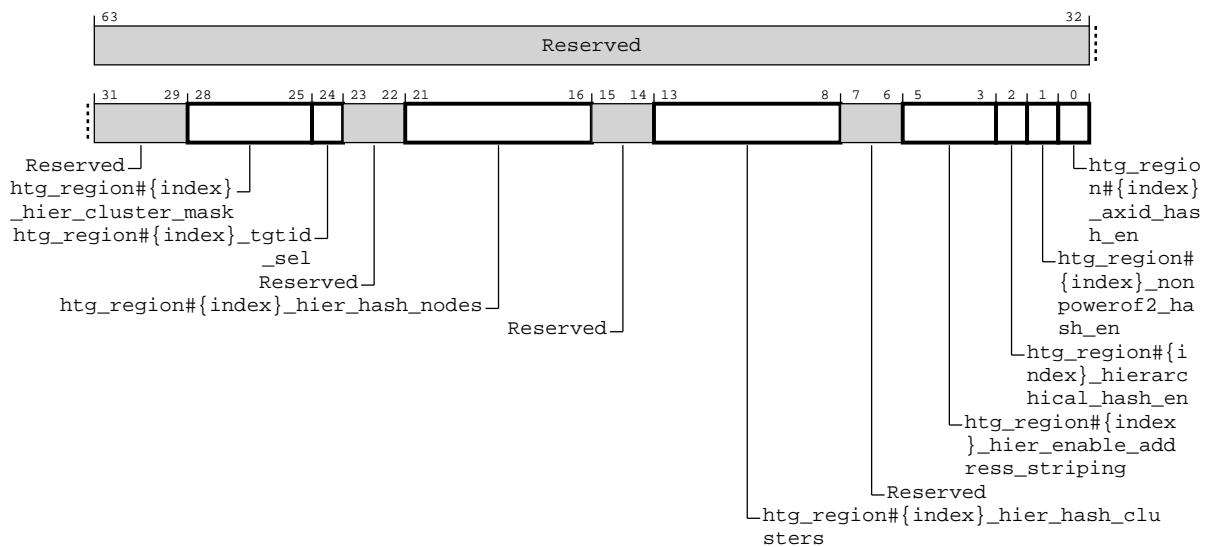


Table 4-623: hashed_target_grp_hash_cntl_reg0-31 attributes

Bits	Name	Description	Type	Reset
[63:29]	Reserved	Reserved	RO	-
[28:25]	htg_region#{index}_hier_cluster_mask	Hierarchical hashing: Enable cluster masking to achieve different interleave granularity across clusters. 4'b0000 64 byte interleave granularity across clusters 4'b0110 4096 byte interleave granularity across clusters 4'b1111 Cluster interleaving disabled Others Reserved	RW	4'b1111
[24]	htg_region#{index}_tgtid_sel	Select the TgtID's from HNF or HNP trgt tables 1'b0 Default, selects from HNF table 1'b1 Selects from HNP table	RW	1'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	htg_region#{index}_hier_hash_nodes	Hierarchical hashing mode, define number of nodes in each cluster	RW	6'h0
[15:14]	Reserved	Reserved	RO	-
[13:8]	htg_region#{index}_hier_hash_clusters	Hierarchical hashing mode, define number of clusters groups	RW	6'h0

Bits	Name	Description	Type	Reset
[7:6]	Reserved	Reserved	RO	-
[5:3]	htg_region#{index}_hier_enable_address_striping	Hierarchical hashing: configure number of address bits needs to shuttered (removed) at second hierarchy hash (LSB bit is based on cluster mask). 3'b000 No address shuttering 3'b001 One addr bit shuttered (2 clusters) 3'b010 Two addr bit shuttered (4 clusters) 3'b011 Three addr bit shuttered (8 clusters) 3'b100 Four addr bit shuttered (16 clusters) 3'b101 Five addr bit shuttered (32 clusters) Others Reserved	RW	3'b0
[2]	htg_region#{index}_hierarchical_hash_en	Hierarchical Hashing mode enable configure bit	RW	1'b0
[1]	htg_region#{index}_nonpowerof2_hash_en	Non power of two Hashing mode enable cconfigure bit	RW	1'b0
[0]	htg_region#{index}_axid_hash_en	AXID based Hashing mode enable configure bit	RW	1'b0

4.3.16.18 sys_cache_group_hn_count

Indicates number of HN-F/HN-P's in hashed target groups 0 to 7.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEA0

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-608: sys_cache_group_hn_count

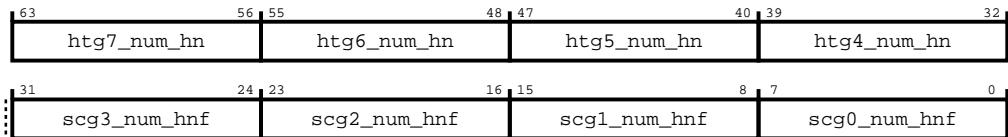


Table 4-624: sys_cache_group_hn_count attributes

Bits	Name	Description	Type	Reset
[63:56]	htg7_num_hn	HN count for hashed target group 7	RW	8'h00
[55:48]	htg6_num_hn	HN count for hashed target group 6	RW	8'h00
[47:40]	htg5_num_hn	HN count for hashed target group 5	RW	8'h00
[39:32]	htg4_num_hn	HN count for hashed target group 4	RW	8'h00
[31:24]	scg3_num_hnf	HN count for hashed target group 3	RW	8'h00
[23:16]	scg2_num_hnf	HN count for hashed target group 2	RW	8'h00
[15:8]	scg1_num_hnf	HN count for hashed target group 1	RW	8'h00
[7:0]	scg0_num_hnf	HN count for hashed target group 0	RW	8'h00

4.3.16.19 hashed_target_group_hn_count_reg1-3

There are 3 iterations of this register. The index ranges from 1 to 3. Indicates number of HN-F/HN-P's in hashed target groups #{{index}*8} to #{{index}*8 + 7}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-1) : 16'hEA0 + #{8 * index}
index(2-3) : 16'h3700 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-609: hashed_target_group_hn_count_reg1-3

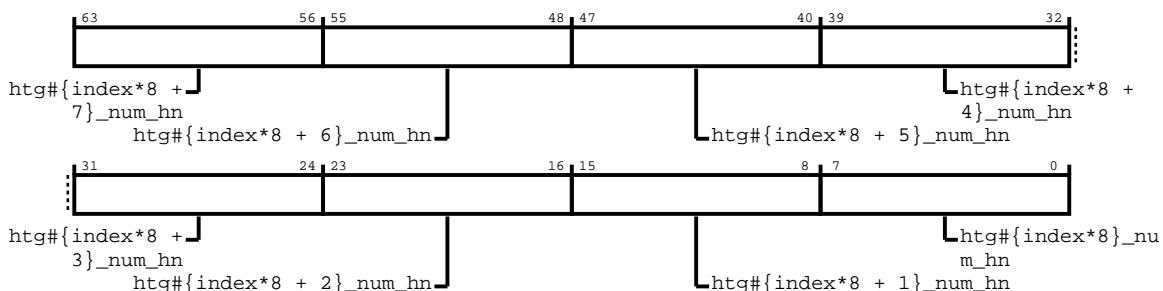


Table 4-625: hashed_target_group_hn_count_reg1-3 attributes

Bits	Name	Description	Type	Reset
[63:56]	htg#{index*8 + 7}_num_hn	HN count for hashed target group 7	RW	8'h00
[55:48]	htg#{index*8 + 6}_num_hn	HN count for hashed target group 6	RW	8'h00
[47:40]	htg#{index*8 + 5}_num_hn	HN count for hashed target group 5	RW	8'h00
[39:32]	htg#{index*8 + 4}_num_hn	HN count for hashed target group 4	RW	8'h00
[31:24]	htg#{index*8 + 3}_num_hn	HN count for hashed target group 3	RW	8'h00
[23:16]	htg#{index*8 + 2}_num_hn	HN count for hashed target group 2	RW	8'h00
[15:8]	htg#{index*8 + 1}_num_hn	HN count for hashed target group 1	RW	8'h00
[7:0]	htg#{index*8}_num_hn	HN count for hashed target group 0	RW	8'h00

4.3.16.20 sys_cache_grp_nonhash_nodeid

Configures non-hashed node IDs for hashed target groups 1 to 5. NOTE: Only applicable in the non-hashed mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEC0

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-610: sys_cache_grp_nonhash_nodeid

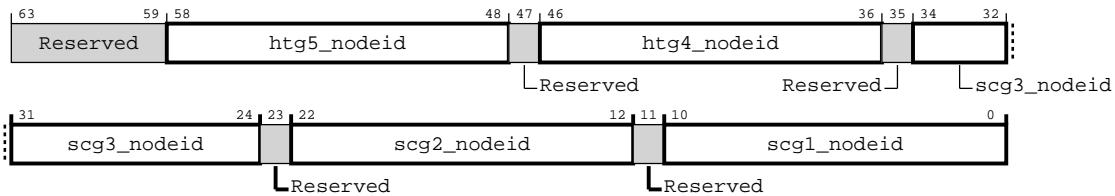


Table 4-626: sys_cache_grp_nonhash_nodeid attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:48]	htg5_nodeid	Non-hashed node ID for Hashed target group 5	RW	11'b000000000000
[47]	Reserved	Reserved	RO	-
[46:36]	htg4_nodeid	Non-hashed node ID for Hashed target group 4	RW	11'b000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	scg3_nodeid	Non-hashed node ID for Hashed target group 3	RW	11'b000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	scg2_nodeid	Non-hashed node ID for Hashed target group 2	RW	11'b000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	scg1_nodeid	Non-hashed node ID for Hashed target group 1	RW	11'b000000000000

4.3.16.21 hashed_target_grp_nonhash_nodeid_reg1-6

There are 6 iterations of this register. The index ranges from 1 to 6. Configures non-hashed node IDs for hashed target groups #{{index}*5 + 1} to #{{index}*5 + 5}. NOTE: Only applicable in the non-hashed mode.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-5) : 16'hEC0 + # {8 * index}

```
index(6-9) : 16'h3800 + #{8 * (index-6)}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-611: hashed_target_grp_nonhash_nodeid_reg1-6

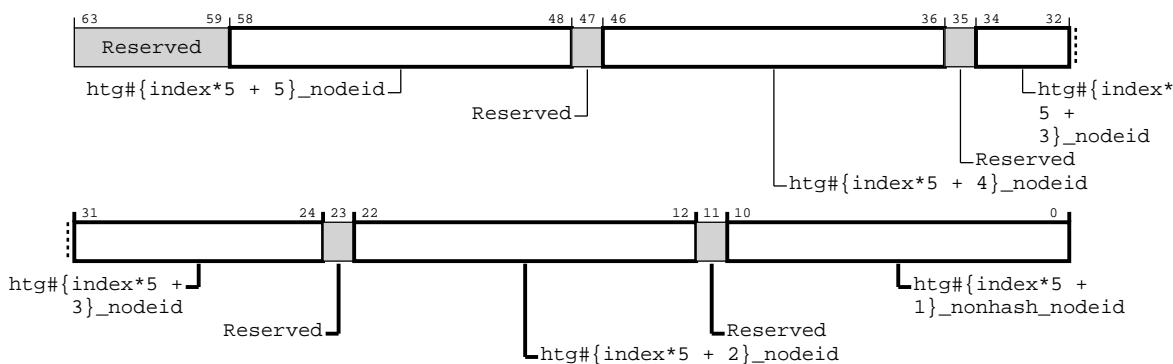


Table 4-627: hashed_target_grp_nonhash_nodeid_reg1-6 attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:48]	htg#{index*5 + 5}_nodeid	Non-hashed node ID for Hashed target group #{index*5 + 5}	RW	11'b00000000000000
[47]	Reserved	Reserved	RO	-
[46:36]	htg#{index*5 + 4}_nodeid	Non-hashed node ID for Hashed target group #{index*5 + 4}	RW	11'b00000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	htg#{index*5 + 3}_nodeid	Non-hashed node ID for Hashed target group #{index*5 + 3}	RW	11'b00000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	htg#{index*5 + 2}_nodeid	Non-hashed node ID for Hashed target group #{index*5 + 2}	RW	11'b00000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	htg#{index*5 + 1}_nonhash_nodeid	Non-hashed node ID for Hashed target group #{index*5 + 1}	RW	11'b00000000000000

4.3.16.22 sys_cache_grp_hn_nodeid_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures HNF node IDs for hashed target groups. Controls target HNF node IDs $\#\{index*4\}$ to $\#\{index*4 + 3\}$.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-31) : 16'hF00 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-612: sys_cache_grp_hn_nodeid_reg0-15

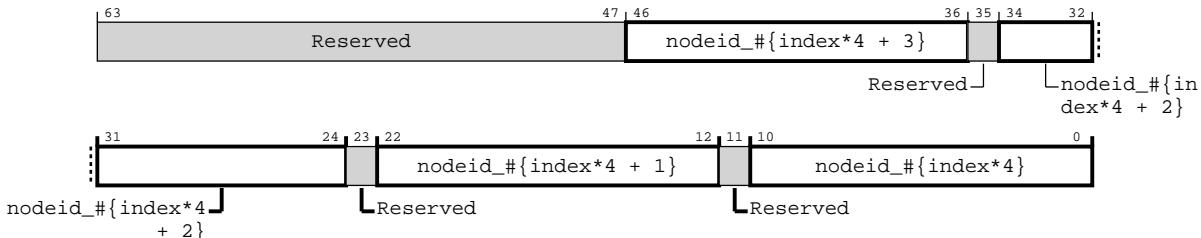


Table 4-628: sys_cache_grp_hn_nodeid_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:36]	nodeid_{index*4 + 3}	HNF target node ID $\#\{index*4 + 3\}$	RW	11'b00000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	nodeid_{index*4 + 2}	HNF target node ID $\#\{index*4 + 2\}$	RW	11'b000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	nodeid_{index*4 + 1}	HNF target node ID $\#\{index*4 + 1\}$	RW	11'b000000000000

Bits	Name	Description	Type	Reset
[11]	Reserved	Reserved	RO	-
[10:0]	nodeid_#{index*4}	HNF target node ID #{index*4}	RW	11'b000000000000

4.3.16.23 hashed_target_grp_hnf_nodeid_reg16-31

There are 16 iterations of this register. The index ranges from 16 to 31. Configures HNF node IDs for hashed target groups. Controls target HNF node IDs #{index*4} to #{index*4 + 3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-31) : 16'hF00 + #{8 * index}
index(32-63) : 16'h3500 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-613: hashed_target_grp_hnf_nodeid_reg16-31

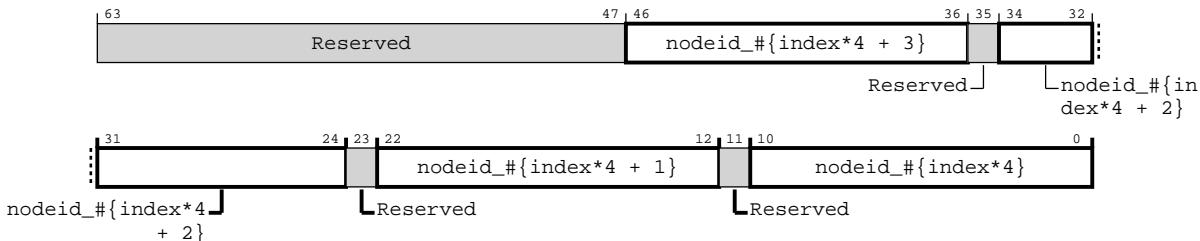


Table 4-629: hashed_target_grp_hnf_nodeid_reg16-31 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[46:36]	nodeid_#{index*4 + 3}	HNF target node ID #{index*4 + 3}	RW	11'b0000000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	nodeid_#{index*4 + 2}	HNF target node ID #{index*4 + 2}	RW	11'b0000000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	nodeid_#{index*4 + 1}	HNF target node ID #{index*4 + 1}	RW	11'b0000000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	nodeid_#{index*4}	HNF target node ID #{index*4}	RW	11'b0000000000000000

4.3.16.24 hashed_target_grp_hnp_nodeid_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures HNP node IDs for hashed target groups. Controls target HNP node IDs #{index*4} to #{index*4 + 3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h3600 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-614: hashed_target_grp_hnp_nodeid_reg0-15

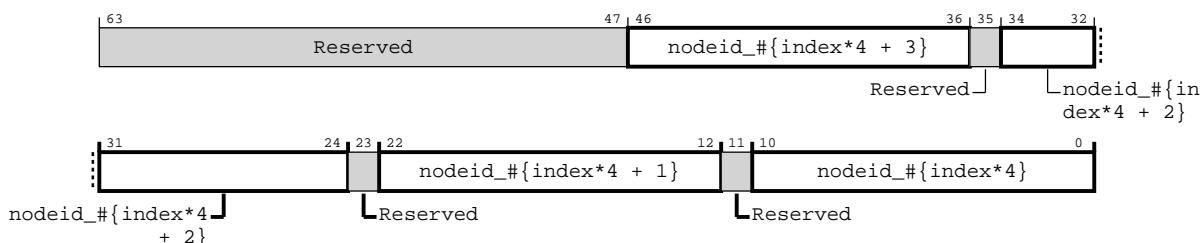


Table 4-630: hashed_target_grp_hnp_nodeid_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:36]	nodeid_{index*4 + 3}	HNP target node ID #{index*4 + 3}	RW	11'b00000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	nodeid_{index*4 + 2}	HNP target node ID #{index*4 + 2}	RW	11'b000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	nodeid_{index*4 + 1}	HNP target node ID #{index*4 + 1}	RW	11'b000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	nodeid_{index*4}	HNP target node ID #{index*4}	RW	11'b000000000000

4.3.16.25 sys_cache_grp_cal_mode_reg

Configures the HN CAL mode support for all hashed target groups.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1120

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-615: sys_cache_grp_cal_mode_reg

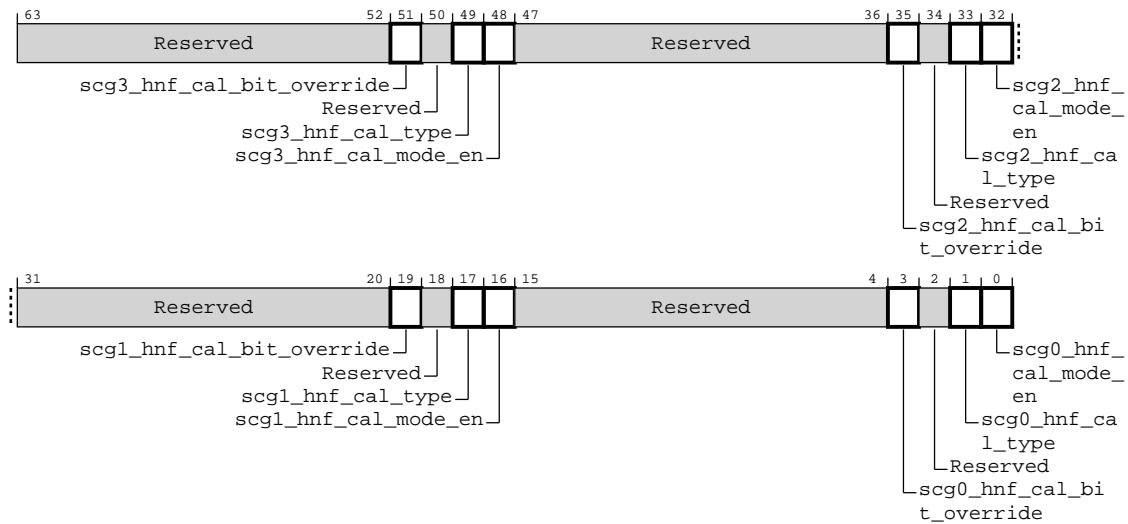


Table 4-631: sys_cache_grp_cal_mode_reg attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51]	scg3_hnf_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG 3 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[50]	Reserved	Reserved	RO	-
[49]	scg3_hnf_cal_type	Enables type of HN CAL for HTG 3 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[48]	scg3_hnf_cal_mode_en	Enables support for HN CAL for HTG 3	RW	1'b0
[47:36]	Reserved	Reserved	RO	-
[35]	scg2_hnf_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG 2 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[34]	Reserved	Reserved	RO	-
[33]	scg2_hnf_cal_type	Enables type of HN CAL for HTG 2 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[32]	scg2_hnf_cal_mode_en	Enables support for HN CAL for HTG 2	RW	1'b0
[31:20]	Reserved	Reserved	RO	-
[19]	scg1_hnf_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG 1 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0

Bits	Name	Description	Type	Reset
[18]	Reserved	Reserved	RO	-
[17]	scg1_hnf_cal_type	Enables type of HN CAL for HTG 1 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[16]	scg1_hnf_cal_mode_en	Enables support for HN CAL for HTG 1	RW	1'b0
[15:4]	Reserved	Reserved	RO	-
[3]	scg0_hnf_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG 0 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[2]	Reserved	Reserved	RO	-
[1]	scg0_hnf_cal_type	Enables type of HN CAL for HTG 0 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[0]	scg0_hnf_cal_mode_en	Enables support for HN CAL for HTG 0	RW	1'b0

4.3.16.26 hashed_target_grp_cal_mode_reg1-7

There are 7 iterations of this register. The index ranges from 1 to 7. Configures the HN CAL mode support for all hashed target groups.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-3) : 16'h1120 + #{8 * index}
index(4-7) : 16'h3780 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-616: hashed_target_grp_cal_mode_reg1-7

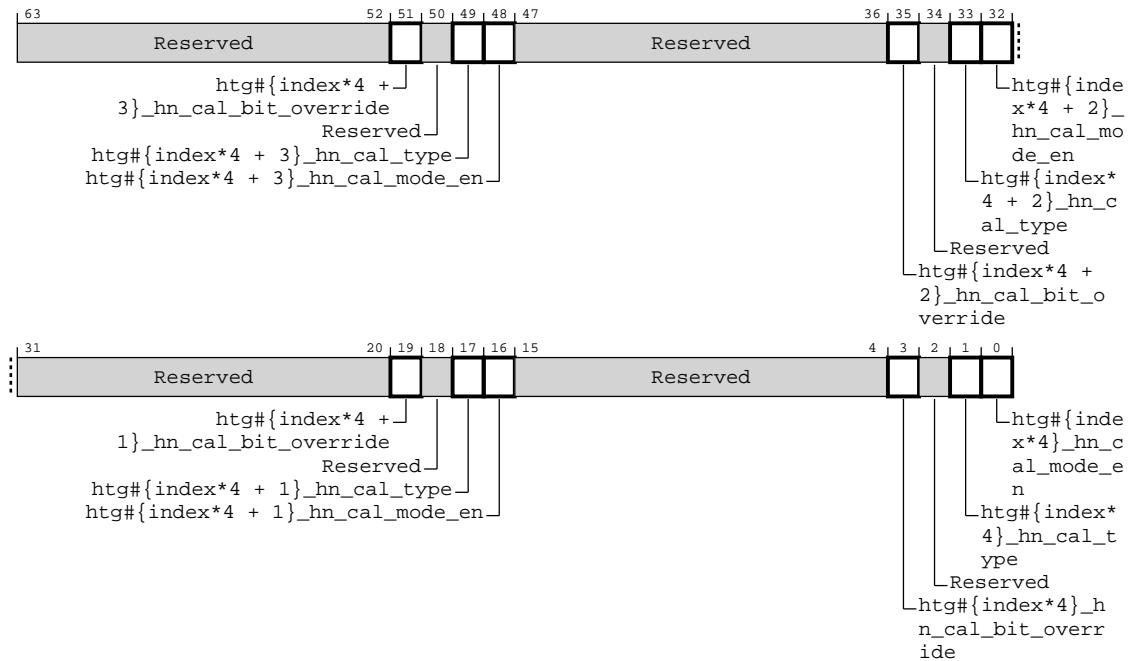


Table 4-632: hashed_target_grp_cal_mode_reg1-7 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51]	htg#[index*4 + 3].hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #{index*4 + 3}	RW	1'b0
		1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID		
[50]	Reserved	Reserved	RO	-
[49]	htg#[index*4 + 3].hn_cal_type	Enables type of HN CAL for HTG #{index*4 + 3}	RW	1'b0
		1'b0 CAL2 mode 1'b1 CAL4 mode		
[48]	htg#[index*4 + 3].hn_cal_mode_en	Enables support for HN CAL for HTG #{index*4 + 3}	RW	1'b0
[47:36]	Reserved	Reserved	RO	-
[35]	htg#[index*4 + 2].hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #{index*4 + 2}	RW	1'b0
		1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID		
[34]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[33]	htg#[index*4 + 2]_hn_cal_type	Enables type of HN CAL for HTG #{index*4 + 2} 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[32]	htg#[index*4 + 2]_hn_cal_mode_en	Enables support for HN CAL for HTG #{index*4 + 2}	RW	1'b0
[31:20]	Reserved	Reserved	RO	-
[19]	htg#[index*4 + 1]_hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #[index*4 + 1] 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[18]	Reserved	Reserved	RO	-
[17]	htg#[index*4 + 1]_hn_cal_type	Enables type of HN CAL for HTG #[index*4 + 1] 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[16]	htg#[index*4 + 1]_hn_cal_mode_en	Enables support for HN CAL for HTG #[index*4 + 1]	RW	1'b0
[15:4]	Reserved	Reserved	RO	-
[3]	htg#[index*4]_hn_cal_bit_override	Configuration to choose LSB/MSB bit to override Device ID for HTG #[index*4] 1'b0 Hash MSB bit to override Device ID 1'b1 Hash LSB bit to override Device ID	RW	1'b0
[2]	Reserved	Reserved	RO	-
[1]	htg#[index*4]_hn_cal_type	Enables type of HN CAL for HTG #[index*4] 1'b0 CAL2 mode 1'b1 CAL4 mode	RW	1'b0
[0]	htg#[index*4]_hn_cal_mode_en	Enables support for HN CAL for HTG #[index*4]	RW	1'b0

4.3.16.27 sys_cache_grp_hn_cpa_en_reg

Configures CCI-X port aggregation mode for hashed HNF node IDs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1180

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-617: sys_cache_grp_hn_cpa_en_reg

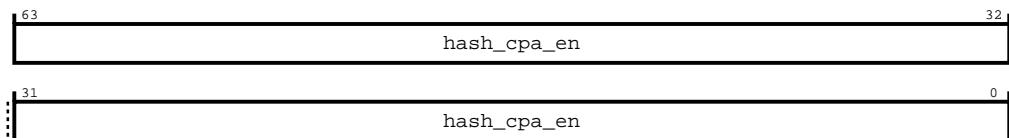


Table 4-633: sys_cache_grp_hn_cpa_en_reg attributes

Bits	Name	Description	Type	Reset
[63:0]	hash_cpa_en	Enable CPA for each hashed HNF node ID	RW	64'h0000000000000000

4.3.16.28 hashed_target_grp_hnf_cpa_en_reg1-1

There are 1 iterations of this register. The index ranges from 1 to 1. Configures CCIX port aggregation mode for hashed HNF node IDs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-1) : 16'h1180 + #{8 * index}
index(2-3) : 16'h3720 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-618: hashed_target_grp_hnf_cpa_en_reg1-1

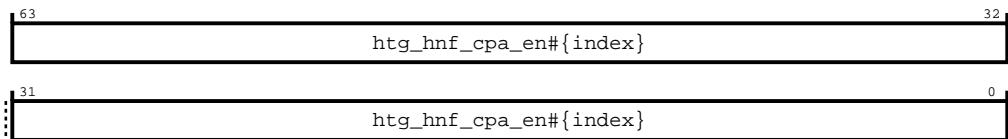


Table 4-634: hashed_target_grp_hnf_cpa_en_reg1-1 attributes

Bits	Name	Description	Type	Reset
[63:0]	htg_hnf_cpa_en#{index}	Enable CPA for each hashed HNF node ID	RW	64'h0000000000000000

4.3.16.29 hashed_target_grp_cpag_perhnf_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures CPAG ID for each hashed HNF node IDs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-15) : 16'h3900 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-619: hashed_target_grp_cpag_perhnf_reg0-15

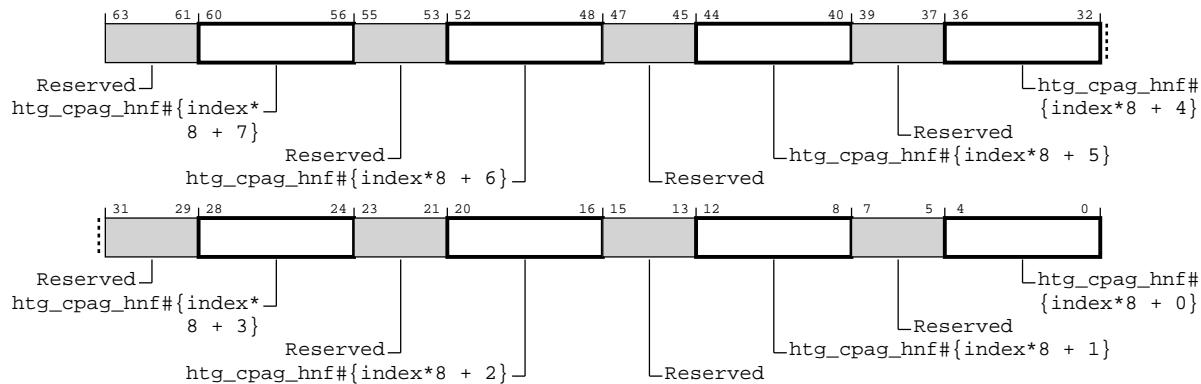


Table 4-635: hashed_target_grp_cpag_perhnf_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:61]	Reserved	Reserved	RO	-
[60:56]	htg_cpag_hnf#{index*8 + 7}	CPAG associated to the HNF#{index*8 + 7}	RW	5'b0
[55:53]	Reserved	Reserved	RO	-
[52:48]	htg_cpag_hnf#{index*8 + 6}	CPAG associated to the HNF#{index*8 + 6}	RW	5'b0
[47:45]	Reserved	Reserved	RO	-
[44:40]	htg_cpag_hnf#{index*8 + 5}	CPAG associated to the HNF#{index*8 + 5}	RW	5'b0
[39:37]	Reserved	Reserved	RO	-
[36:32]	htg_cpag_hnf#{index*8 + 4}	CPAG associated to the HNF#{index*8 + 4}	RW	5'b0
[31:29]	Reserved	Reserved	RO	-
[28:24]	htg_cpag_hnf#{index*8 + 3}	CPAG associated to the HNF#{index*8 + 3}	RW	5'b0
[23:21]	Reserved	Reserved	RO	-
[20:16]	htg_cpag_hnf#{index*8 + 2}	CPAG associated to the HNF#{index*8 + 2}	RW	5'b0
[15:13]	Reserved	Reserved	RO	-
[12:8]	htg_cpag_hnf#{index*8 + 1}	CPAG associated to the HNF#{index*8 + 1}	RW	5'b0
[7:5]	Reserved	Reserved	RO	-
[4:0]	htg_cpag_hnf#{index*8 + 0}	CPAG associated to the HNF#{index*8 + 0}	RW	5'b0

4.3.16.30 sys_cache_grp_hn_cpa_grp_reg

Configures CCIX port aggregation group ID for each System Cache Group

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1190

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-620: sys_cache_grp_hn_cpa_grp_reg

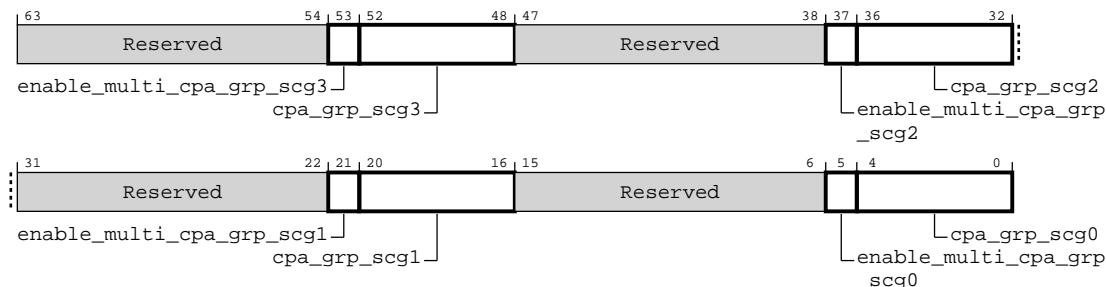


Table 4-636: sys_cache_grp_hn_cpa_grp_reg attributes

Bits	Name	Description	Type	Reset
[63:54]	Reserved	Reserved	RO	-
[53]	enable_multi_cpa_grp_scg3	Enables multiple CPA groups to be configured to SCG3 1'b0: Default/Legacy mode; single CPA group ID is configured in cpa_grp_scg 1'b1: multi_cpag mode: multiple CPA group ID's are configured to SCG3.	RW	1'b0
[52:48]	cpa_grp_scg3	Specifies CCIX port aggregation group ID for Hashed Target Group 3	RW	5'h0
[47:38]	Reserved	Reserved	RO	-
[37]	enable_multi_cpa_grp_scg2	Enables multiple CPA groups to be configured to SCG2 1'b0: Default/Legacy mode; single CPA group ID is configured in cpa_grp_scg 1'b1: multi_cpag mode: multiple CPA group ID's are configured to SCG2.	RW	1'b0
[36:32]	cpa_grp_scg2	Specifies CCIX port aggregation group ID for Hashed target Group 2	RW	5'h0
[31:22]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[21]	enable_multi_cpa_grp_scg1	Enables multiple CPA groups to be configured to SCG1 1'b0 Default/Legacy mode: single CPA group ID is configured in cpa_grp_scg 1'b1 multi_cpag mode: multiple CPA group ID's are configured to SCG1.	RW	1'b0
[20:16]	cpa_grp_scg1	Specifies CCIX port aggregation group ID for Hashed target Group 1	RW	5'h0
[15:6]	Reserved	Reserved	RO	-
[5]	enable_multi_cpa_grp_scg0	Enables multiple CPA groups to be configured to SCG0 1'b0 Default/Legacy mode: single CPA group ID is configured in cpa_grp_scg 1'b1 multi_cpag mode: multiple CPA group ID's are configured to SCG0.	RW	1'b0
[4:0]	cpa_grp_scg0	Specifies CCIX port aggregation group ID for hashed target Group 0	RW	5'h0

4.3.16.31 hashed_target_grp_cpa_grp_reg1-7

There are 7 iterations of this register. The index ranges from 1 to 7. Configures CCIX port aggregation group ID for each System Cache Group

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-1) : 16'h1190 + #{8 * index}
index(2-9) : 16'h3740 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-621: hashed_target_grp_cpa_grp_reg1-7

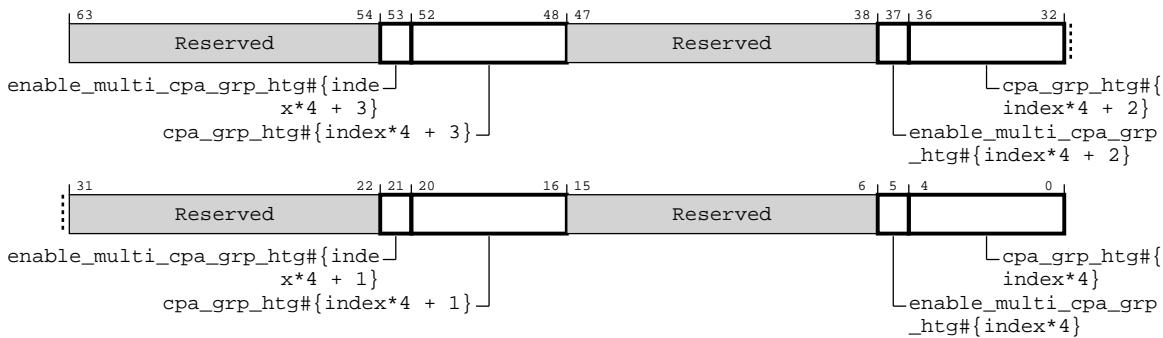


Table 4-637: hashed_target_grp_cpa_grp_reg1-7 attributes

Bits	Name	Description	Type	Reset
[63:54]	Reserved	Reserved	RO	-
[53]	enable_multi_cpa_grp_htg#{index*4 + 3}	Enables multiple CPA groups to be configured to HTG 1'b0 Default/Legacy mode: single CPA group ID is configured in cpa_grp_htg 1'b1 multi_cpag mode: multiple CPA group ID's are configured to HTG.	RW	1'b0
[52:48]	cpa_grp_htg#{index*4 + 3}	Specifies CCIX port aggregation group ID for Hashed Target Group #{index*4 + 3}	RW	5'h0
[47:38]	Reserved	Reserved	RO	-
[37]	enable_multi_cpa_grp_htg#{index*4 + 2}	Enables multiple CPA groups to be configured to HTG 1'b0 Default/Legacy mode: single CPA group ID is configured in cpa_grp_htg 1'b1 multi_cpag mode: multiple CPA group ID's are configured to HTG.	RW	1'b0
[36:32]	cpa_grp_htg#{index*4 + 2}	Specifies CCIX port aggregation group ID for Hashed target Group #{index*4 + 2}	RW	5'h0
[31:22]	Reserved	Reserved	RO	-
[21]	enable_multi_cpa_grp_htg#{index*4 + 1}	Enables multiple CPA groups to be configured to HTG 1'b0 Default/Legacy mode: single CPA group ID is configured in cpa_grp_htg 1'b1 multi_cpag mode: multiple CPA group ID's are configured to HTG.	RW	1'b0
[20:16]	cpa_grp_htg#{index*4 + 1}	Specifies CCIX port aggregation group ID for Hashed target Group #{index*4 + 1}	RW	5'h0
[15:6]	Reserved	Reserved	RO	-
[5]	enable_multi_cpa_grp_htg#{index*4}	Enables multiple CPA groups to be configured to HTG 1'b0 Default/Legacy mode: single CPA group ID is configured in cpa_grp_htg 1'b1 multi_cpag mode: multiple CPA group ID's are configured to HTG.	RW	1'b0

Bits	Name	Description	Type	Reset
[4:0]	cpa_grp_htg#{index*4}	Specifies CCIX port aggregation group ID for hashed target Group #{index*4}	RW	5'h0

4.3.16.32 hashed_target_grp_hnf_lcn_bound_cfg_reg0-1

There are 2 iterations of this register. The index ranges from 0 to 1. Configures cache lines routed to the HNF as LCN bound or Home bound 1'b0: cache lines routed to Home bound 1'b1: cache lines routed to LCN bound

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-3) : 16'h37C0 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-622: hashed_target_grp_hnf_lcn_bound_cfg_reg0-1

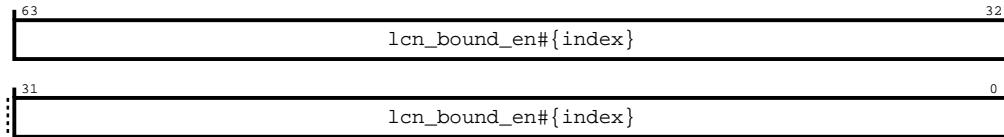


Table 4-638: hashed_target_grp_hnf_lcn_bound_cfg_reg0-1 attributes

Bits	Name	Description	Type	Reset
[63:0]	lcn_bound_en#{index}	Marks the Hashed HNF index as a LCN	RW	64'h0000000000000000

4.3.16.33 hashed_target_grp_hnf_target_type_override_cfg_reg0-1

There are 2 iterations of this register. The index ranges from 0 to 1. Configures the target type for each targetID, RNI/D uses this information to enable tunneling vs streaming. When POR_RNSAM_COMPACT_HN_TABLES_EN_PARAM == 1, this indication is derived from cpa_en 1'b0: HNF target 1'b1: CCG target

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-1) : 16'h37E0 + # {8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-623: hashed_target_grp_hnf_target_type_override_cfg_reg0-1

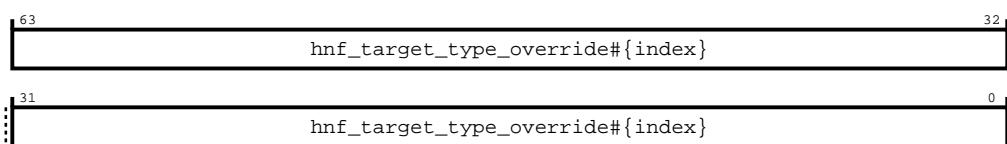


Table 4-639: hashed_target_grp_hnf_target_type_override_cfg_reg0-1 attributes

Bits	Name	Description	Type	Reset
[63:0]	hnf_target_type_override#{index}	Overrides the HNF target type with the CCG	RW	64'h0000000000000000

4.3.16.34 hashed_target_grp_compact_cpag_ctrl0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures the CPAG control for HTG#{index} valid only when POR_RNSAM_COMPACT_HN_TABLES_EN_PARAM == 1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h3A00 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-624: hashed_target_grp_compact_cpag_ctrl0-31

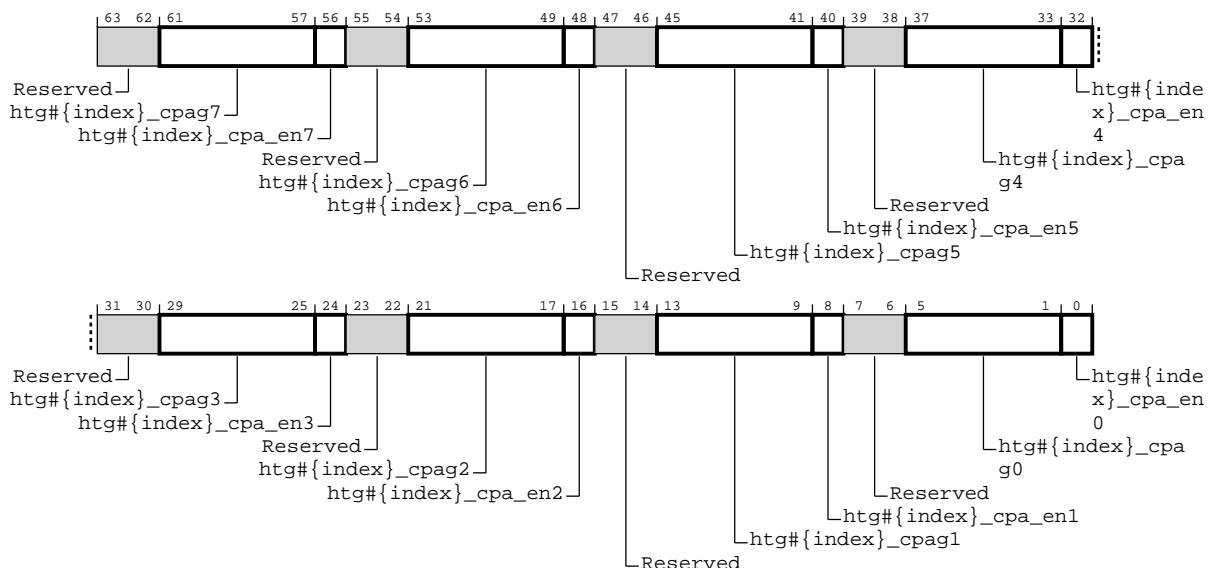


Table 4-640: hashed_target_grp_compact_cpag_ctrl0-31 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:57]	htg#{index}_cpag7	cpag id for index7	RW	5'b0
[56]	htg#{index}_cpa_en7	cpa enable for index7	RW	1'b0
[55:54]	Reserved	Reserved	RO	-
[53:49]	htg#{index}_cpag6	cpag id for index6	RW	5'b0
[48]	htg#{index}_cpa_en6	cpa enable for index6	RW	1'b0
[47:46]	Reserved	Reserved	RO	-
[45:41]	htg#{index}_cpag5	cpag id for index5	RW	5'b0
[40]	htg#{index}_cpa_en5	cpa enable for index5	RW	1'b0
[39:38]	Reserved	Reserved	RO	-
[37:33]	htg#{index}_cpag4	cpag id for index4	RW	5'b0
[32]	htg#{index}_cpa_en4	cpa enable for index4	RW	1'b0
[31:30]	Reserved	Reserved	RO	-
[29:25]	htg#{index}_cpag3	cpag id for index0	RW	5'b0
[24]	htg#{index}_cpa_en3	cpa enable for index3	RW	1'b0
[23:22]	Reserved	Reserved	RO	-
[21:17]	htg#{index}_cpag2	cpag id for index2	RW	5'b0
[16]	htg#{index}_cpa_en2	cpa enable for index2	RW	1'b0
[15:14]	Reserved	Reserved	RO	-
[13:9]	htg#{index}_cpag1	cpag id for index1	RW	5'b0
[8]	htg#{index}_cpa_en1	cpa enable for index1	RW	1'b0
[7:6]	Reserved	Reserved	RO	-
[5:1]	htg#{index}_cpag0	cpag id for index0	RW	5'b0
[0]	htg#{index}_cpa_en0	cpa enable for index0	RW	1'b0

4.3.16.35 hashed_target_grp_compact_hash_ctrl0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures the HNF hash selection and CPAG hash selection control information for HTG#{index} valid only when POR_RNSAM_COMPACT_HN_TABLES_EN_PARAM == 1

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h3B00 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-625: hashed_target_grp_compact_hash_ctrl0-31

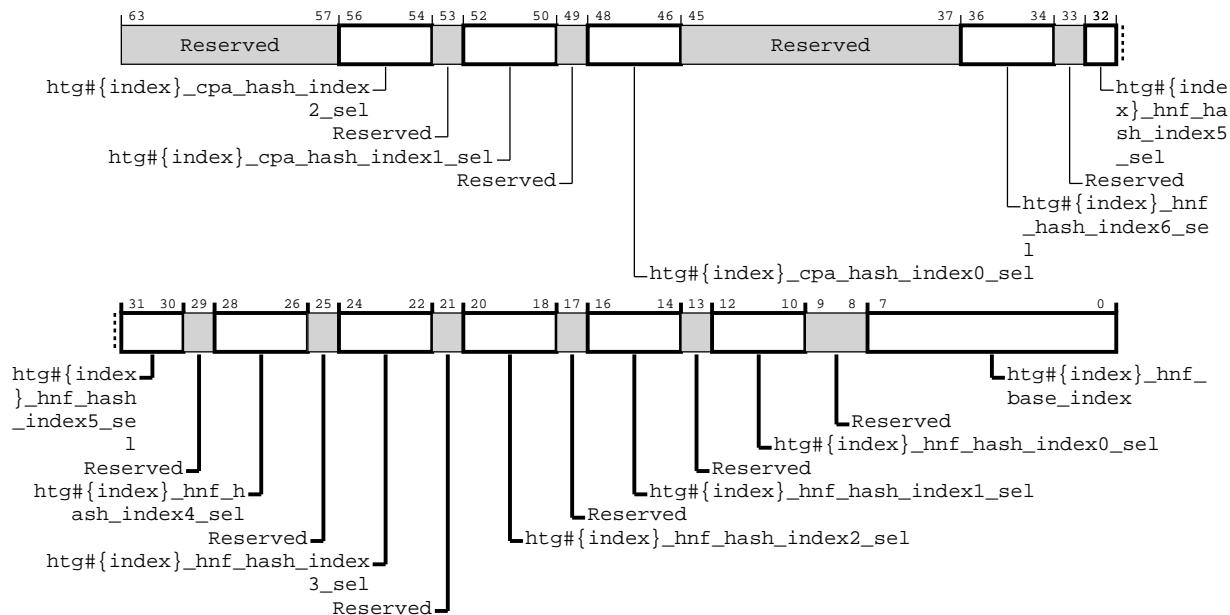


Table 4-641: hashed_target_grp_compact_hash_ctrl0-31 attributes

Bits	Name	Description	Type	Reset
[63:57]	Reserved	Reserved	RO	-
[56:54]	htg#[index]_cpa_hash_index2_sel	configures the CPAG hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index2. 3'b001 SMP hash index2 + 1. 3'b010 SMP hash index2 + 2. 3'b011 SMP hash index2 + 3. 3'b100 SMP hash index2 + 4. 3'b101 SMP hash index2 + 5 3'b110 SMP hash index2 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[53]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[52:50]	htg#[index]_cpa_hash_index1_sel	configures the CPAG hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index1. 3'b001 SMP hash index1 + 1. 3'b010 SMP hash index1 + 2. 3'b011 SMP hash index1 + 3. 3'b100 SMP hash index1 + 4. 3'b101 SMP hash index1 + 5 3'b110 SMP hash index1 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[49]	Reserved	Reserved	RO	-
[48:46]	htg#[index]_cpa_hash_index0_sel	configures the CPAG hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index0. 3'b001 SMP hash index0 + 1. 3'b010 SMP hash index0 + 2. 3'b011 SMP hash index0 + 3. 3'b100 SMP hash index0 + 4. 3'b101 SMP hash index0 + 5 3'b110 SMP hash index0 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[45:37]	Reserved	Reserved	RO	-
[36:34]	htg#[index]_hnf_hash_index6_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index6. 3'b001 SMP hash index6 + 1. 3'b010 SMP hash index6 + 2. 3'b011 SMP hash index6 + 3. 3'b100 SMP hash index6 + 4. 3'b101 SMP hash index6 + 5 3'b110 SMP hash index6 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[33]	Reserved	Reserved	RO	-
[32:30]	htg#[index]_hnf_hash_index5_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index5. 3'b001 SMP hash index5 + 1. 3'b010 SMP hash index5 + 2. 3'b011 SMP hash index5 + 3. 3'b100 SMP hash index5 + 4. 3'b101 SMP hash index5 + 5 3'b110 SMP hash index5 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[29]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[28:26]	htg#[index].hnf_hash_index4_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index4. 3'b001 SMP hash index4 + 1. 3'b010 SMP hash index4 + 2. 3'b011 SMP hash index4 + 3. 3'b100 SMP hash index4 + 4. 3'b101 SMP hash index4 + 5 3'b110 SMP hash index4 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[25]	Reserved	Reserved	RO	-
[24:22]	htg#[index].hnf_hash_index3_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index3. 3'b001 SMP hash index3 + 1. 3'b010 SMP hash index3 + 2. 3'b011 SMP hash index3 + 3. 3'b100 SMP hash index3 + 4. 3'b101 SMP hash index3 + 5 3'b110 SMP hash index3 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[21]	Reserved	Reserved	RO	-
[20:18]	htg#[index].hnf_hash_index2_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index2. 3'b001 SMP hash index2 + 1. 3'b010 SMP hash index2 + 2. 3'b011 SMP hash index2 + 3. 3'b100 SMP hash index2 + 4. 3'b101 SMP hash index2 + 5 3'b110 SMP hash index2 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[17]	Reserved	Reserved	RO	-
[16:14]	htg#[index].hnf_hash_index1_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index1. 3'b001 SMP hash index1 + 1. 3'b010 SMP hash index1 + 2. 3'b011 SMP hash index1 + 3. 3'b100 SMP hash index1 + 4. 3'b101 SMP hash index1 + 5 3'b110 SMP hash index1 + 6 3'b111 Hardcoded value (1'b0)	RW	3'b0
[13]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[12:10]	htg#[{index}]_hnf_hash_index0_sel	configures the local hnfs hash selection bits from the total hnfs hash across SMP. 3'b000 pass through from the SMP hnf_hash_index0. 3'b001 SMP hash index0 + 1. 3'b010 SMP hash index0 + 2. 3'b011 SMP hash index0 + 3. 3'b100 SMP hash index0 + 4. 3'b101 SMP hash index0 + 5. 3'b110 SMP hash index0 + 6. 3'b111 Hardcoded value (1'b0)	RW	3'b0
[9:8]	Reserved	Reserved	RO	-
[7:0]	htg#[{index}]_hnf_base_index	base index to the HNF target ID table	RW	8'b0

4.3.16.36 rnsam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE80

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-626: rnsam_hash_addr_mask_reg

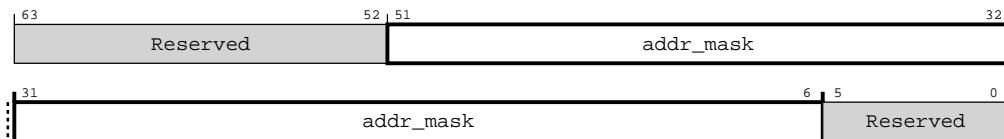


Table 4-642: rnsam_hash_addr_mask_reg attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:6]	addr_mask	Address mask applied before hashing	RW	46'h3FFFFFFFFF
[5:0]	Reserved	Reserved	RO	-

4.3.16.37 rnsam_hash_axi_id_mask_reg

Configures the AXI_ID mask that is applied before hashing the address bits.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE88

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-627: rnsam_hash_axi_id_mask_reg

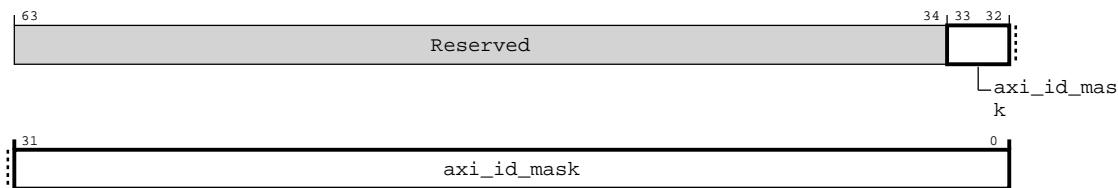


Table 4-643: rnsam_hash_axi_id_mask_reg attributes

Bits	Name	Description	Type	Reset
[63:34]	Reserved	Reserved	RO	-
[33:0]	axi_id_mask	AXI_ID mask applied before hashing	RW	34'h3FFFFFFF

4.3.16.38 rnsam_region_cmp_addr_mask_reg

Configures the address mask that is applied before region compare.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hE90

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-628: rnsam_region_cmp_addr_mask_reg

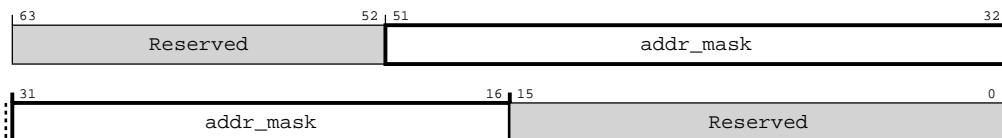


Table 4-644: rnsam_region_cmp_addr_mask_reg attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	addr_mask	Address mask applied before memory region compare	RW	36'hFFFFFF
[15:0]	Reserved	Reserved	RO	-

4.3.16.39 cml_port_aggr_grp0-31_add_mask

There are 32 iterations of this register. The index ranges from 0 to 31. Configures the CCIX port aggregation address mask for group #{index}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-5) : 16'h11C0 + #{8 * index}
index(6-37) : 16'h2B00 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-629: cml_port_aggr_grp0-31_add_mask

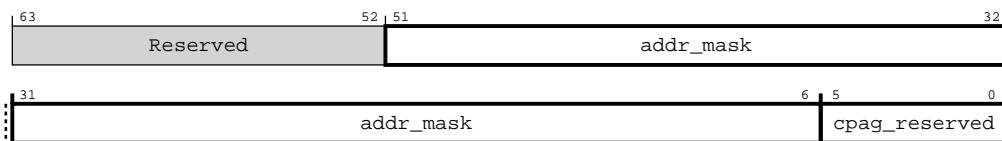


Table 4-645: cml_port_aggr_grp0-31_add_mask attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:6]	addr_mask	Address/AXID mask to be applied before hashing CONSTRAINT: ADDR MASK is [51:6] CONSTRAINT: AXID MASK is [31:0] = [37:6]	RW	46'h3FFFFFFFFF
[5:0]	cpag_reserved	reserved bits	RW	6'ho

4.3.16.40 cml_cpag_base_idx_grp0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Configures the CPAG base indexes.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-7) : 16'h2B00 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-630: cml_cpag_base_idx_grp0-3

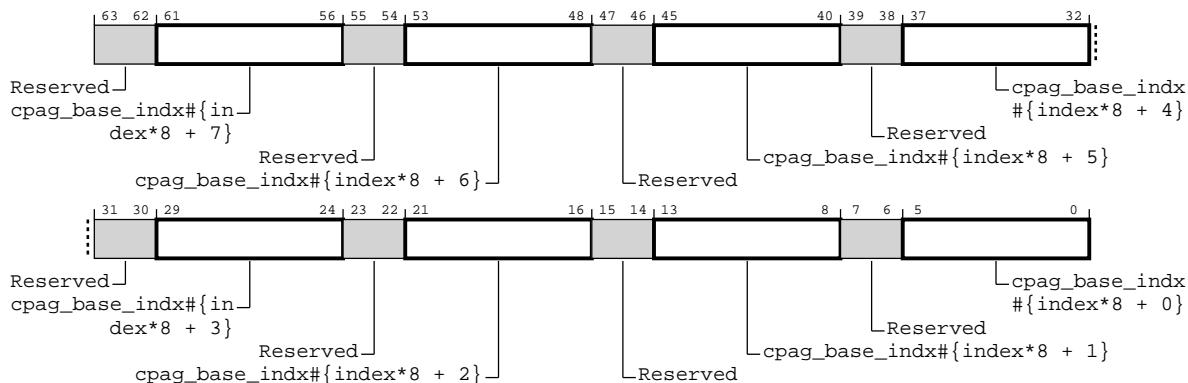


Table 4-646: cml_cpag_base_idx_grp0-3 attributes

Bits	Name	Description	Type	Reset
[63:62]	Reserved	Reserved	RO	-
[61:56]	cpag_base_idx#{index*8 + 7}	Configures the CPAG base index #{8*index + 7}	RW	6'h3F
[55:54]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[53:48]	cpag_base_idx#{index*8 + 6}	Configures the CPAG base index #{8*index + 6}	RW	6'h3F
[47:46]	Reserved	Reserved	RO	-
[45:40]	cpag_base_idx#{index*8 + 5}	Configures the CPAG base index #{8*index + 5}	RW	6'h3F
[39:38]	Reserved	Reserved	RO	-
[37:32]	cpag_base_idx#{index*8 + 4}	Configures the CPAG base index #{8*index + 4}	RW	6'h3F
[31:30]	Reserved	Reserved	RO	-
[29:24]	cpag_base_idx#{index*8 + 3}	Configures the CPAG base index #{8*index + 3}	RW	6'h3F
[23:22]	Reserved	Reserved	RO	-
[21:16]	cpag_base_idx#{index*8 + 2}	Configures the CPAG base index #{8*index + 2}	RW	6'h3F
[15:14]	Reserved	Reserved	RO	-
[13:8]	cpag_base_idx#{index*8 + 1}	Configures the CPAG base index #{8*index + 1}	RW	6'h3F
[7:6]	Reserved	Reserved	RO	-
[5:0]	cpag_base_idx#{index*8 + 0}	Configures the CPAG base index #{8*index + 0}	RW	6'h3F

4.3.16.41 cml_port_aggr_grp_reg0-12

There are 13 iterations of this register. The index ranges from 0 to 12. Configures the CCIX port aggregation port Node IDs

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-2) : 16'h11F0 + #{8 * index}
index(3-14) : 16'h2C00 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-631: cml_port_aggr_grp_reg0-12

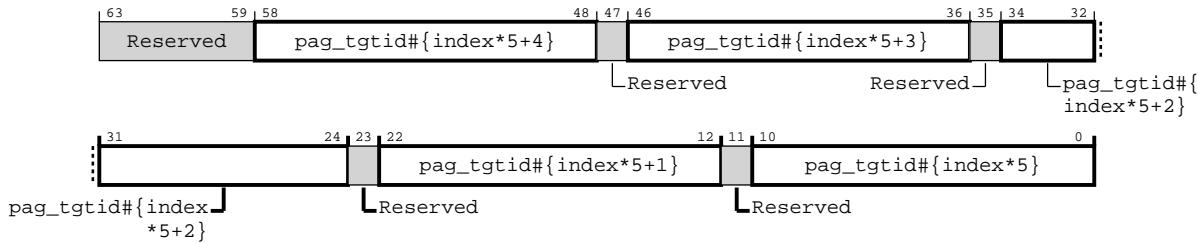


Table 4-647: cml_port_aggr_grp_reg0-12 attributes

Bits	Name	Description	Type	Reset
[63:59]	Reserved	Reserved	RO	-
[58:48]	pag_tgtid#[index*5+4]	Specifies target ID #{index*5+4} for CPAG	RW	11'b0
[47]	Reserved	Reserved	RO	-
[46:36]	pag_tgtid#[index*5+3]	Specifies target ID #{index*5+3} for CPAG	RW	11'b0
[35]	Reserved	Reserved	RO	-
[34:24]	pag_tgtid#[index*5+2]	Specifies target ID #{index*5+2} for CPAG	RW	11'b0
[23]	Reserved	Reserved	RO	-
[22:12]	pag_tgtid#[index*5+1]	Specifies target ID #{index*5+1} for CPAG	RW	11'b0
[11]	Reserved	Reserved	RO	-
[10:0]	pag_tgtid#[index*5]	Specifies target ID #{index*5} for CPAG	RW	11'b0

4.3.16.42 cml_port_aggr_ctrl_reg

Configures the CCIX port aggregation port IDs for group 2.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1208

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-632: cml_port_aggr_ctrl_reg

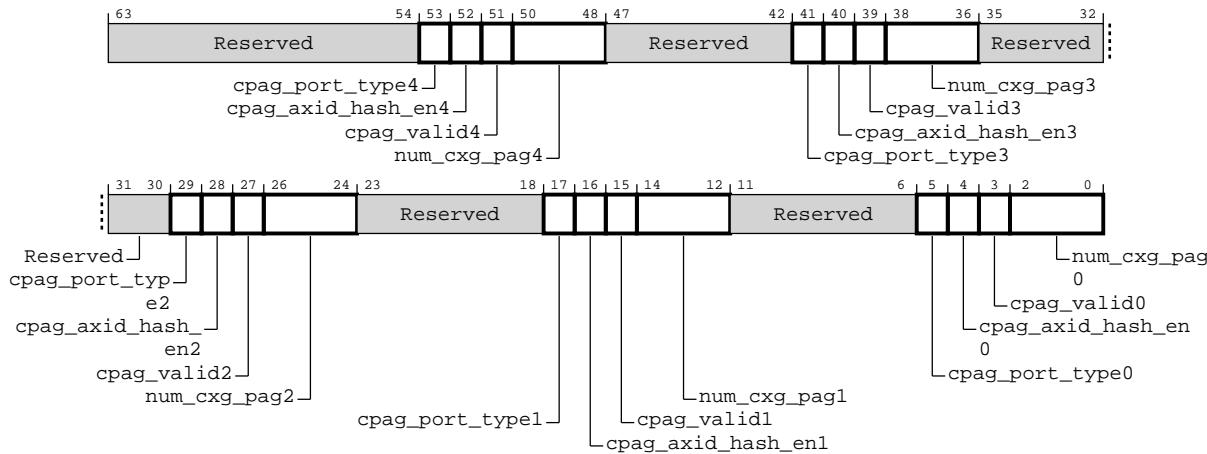


Table 4-648: cml_port_aggr_ctrl_reg attributes

Bits	Name	Description	Type	Reset
[63:54]	Reserved	Reserved	RO	-
[53]	cpag_port_type4	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0
[52]	cpag_axid_hash_en4	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[51]	cpag_valid4	Valid programming for CPAG4, Enabled by default (backward compatible)	RW	1'b1
[50:48]	num_cxg_pag4	Specifies the number of CXRAs in CPAG4 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[47:42]	Reserved	Reserved	RO	-
[41]	cpag_port_type3	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0

Bits	Name	Description	Type	Reset
[40]	cpag_axid_hash_en3	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[39]	cpag_valid3	Valid programming for CPAG + 3}, Enabled by default (backward compatible)	RW	1'b1
[38:36]	num_cxg_pag3	Specifies the number of CXRAs in CPAG3 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[35:30]	Reserved	Reserved	RO	-
[29]	cpag_port_type2	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0
[28]	cpag_axid_hash_en2	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[27]	cpag_valid2	Valid programming for CPAG + 2}, Enabled by default (backward compatible)	RW	1'b1
[26:24]	num_cxg_pag2	Specifies the number of CXRAs in CPAG2 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[23:18]	Reserved	Reserved	RO	-
[17]	cpag_port_type1	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0
[16]	cpag_axid_hash_en1	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[15]	cpag_valid1	Valid programming for CPAG + 1}, Enabled by default (backward compatible)	RW	1'b1
[14:12]	num_cxg_pag1	Specifies the number of CXRAs in CPAG1 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[11:6]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[5]	cpag_port_type0	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0
[4]	cpag_axid_hash_en0	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[3]	cpag_valid0	Valid programming for CPAG, Enabled by default (backward compatible)	RW	1'b1
[2:0]	num_cxg_pago	Specifies the number of CXRAs in CPAGO 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0

4.3.16.43 cml_port_aggr_ctrl_reg1-6

There are 6 iterations of this register. The index ranges from 1 to 6. Configures the CCIX port aggregation port IDs for group 2.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-15) : 16'h1208 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-633: cml_port_aggr_ctrl_reg1-6

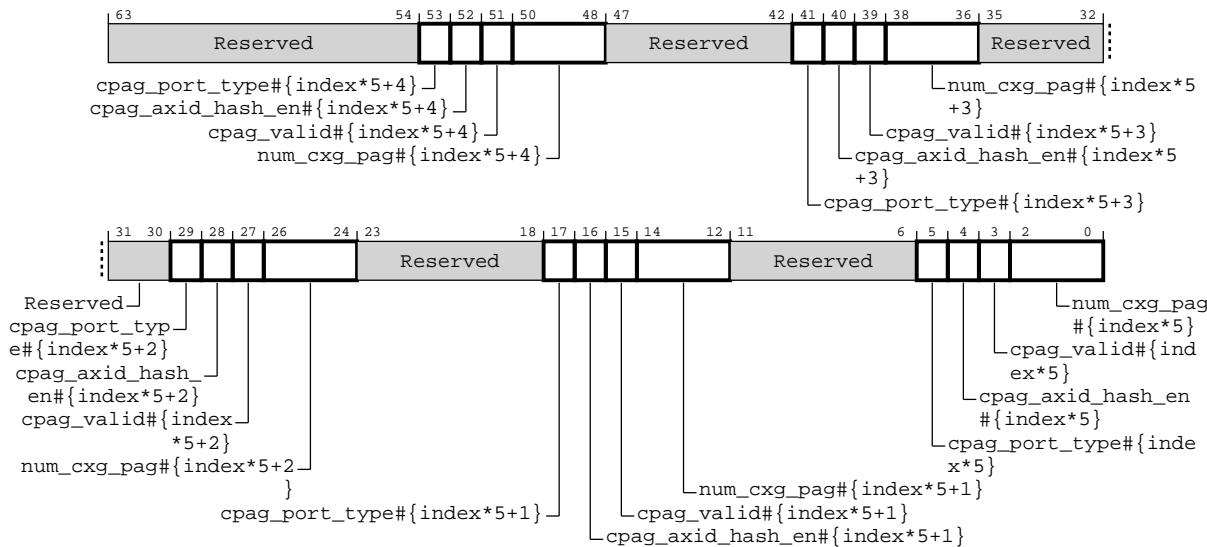


Table 4-649: cml_port_aggr_ctrl_reg1-6 attributes

Bits	Name	Description	Type	Reset
[63:54]	Reserved	Reserved	RO	-
[53]	cpag_port_type#{index*5+4}	Specifies the port type	RW	1'b0
	1'b0	CXL port		
	1'b1	CML SMP port		
[52]	cpag_axid_hash_en#{index*5+4}	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[51]	cpag_valid#{index*5+4}	Valid programming for CPAG #{index*5 + 4}, Enabled by default (backward compatible)	RW	1'b1
[50:48]	num_cxg_pag#{index*5+4}	Specifies the number of CXRAs in CPAG #{index*5 + 4}	RW	3'b0
	3'b000	1 port		
	3'b001	2 ports		
	3'b010	4 ports		
	3'b011	8 ports		
	3'b100	16 ports		
	3'b101	32 ports		
	3'b110	3 ports (MOD-3 hash)		
	3'b111	Reserved		
[47:42]	Reserved	Reserved	RO	-
[41]	cpag_port_type#{index*5+3}	Specifies the port type	RW	1'b0
	1'b0	CXL port		
	1'b1	CML SMP port		
[40]	cpag_axid_hash_en#{index*5+3}	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[39]	cpag_valid#{index*5+3}	Valid programming for CPAG #{index*5 + 3}, Enabled by default (backward compatible)	RW	1'b1

Bits	Name	Description	Type	Reset
[38:36]	num_cxg_pag#{index*5+3}	Specifies the number of CXRAs in CPAG #{index*5 + 3} 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[35:30]	Reserved	Reserved	RO	-
[29]	cpag_port_type#{index*5+2}	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0
[28]	cpag_axid_hash_en#{index*5+2}	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[27]	cpag_valid#{index*5+2}	Valid programming for CPAG #{index*5 + 2}, Enabled by default (backward compatible)	RW	1'b1
[26:24]	num_cxg_pag#{index*5+2}	Specifies the number of CXRAs in CPAG #{index*5 + 2} 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[23:18]	Reserved	Reserved	RO	-
[17]	cpag_port_type#{index*5+1}	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0
[16]	cpag_axid_hash_en#{index*5+1}	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[15]	cpag_valid#{index*5+1}	Valid programming for CPAG #{index*5 + 1}, Enabled by default (backward compatible)	RW	1'b1
[14:12]	num_cxg_pag#{index*5+1}	Specifies the number of CXRAs in CPAG #{index*5 + 1} 3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved	RW	3'b0
[11:6]	Reserved	Reserved	RO	-
[5]	cpag_port_type#{index*5}	Specifies the port type 1'b0 CXL port 1'b1 CML SMP port	RW	1'b0

Bits	Name	Description	Type	Reset
[4]	cpag_axid_hash_en#{index*5}	Enable AXID based port aggregation, by default address based hashing is enabled	RW	1'b0
[3]	cpag_valid#{index*5}	Valid programming for CPAG #{index*5}, Enabled by default (backward compatible)	RW	1'b1
[2:0]	num_cxg_pag#{index*5}	Specifies the number of CXRAs in CPAG #{index*5}	RW	3'b0
		3'b000 1 port 3'b001 2 ports 3'b010 4 ports 3'b011 8 ports 3'b100 16 ports 3'b101 32 ports 3'b110 3 ports (MOD-3 hash) 3'b111 Reserved		

4.3.16.44 sys_cache_grp_sn_attr

Configures attributes for SN node IDs for system cache groups.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEB0

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-634: sys_cache_grp_sn_attr

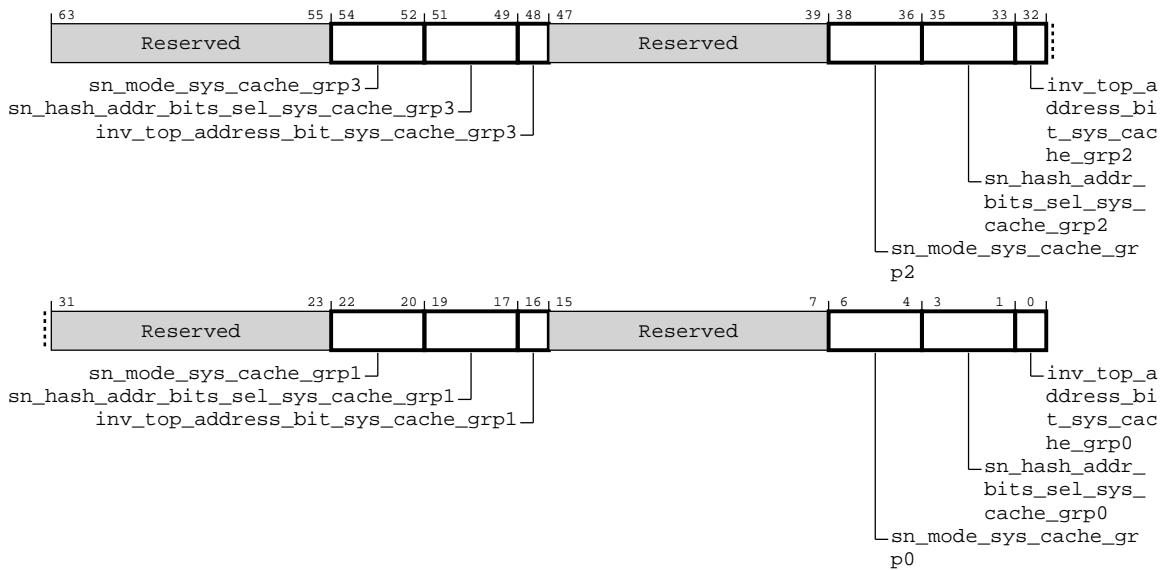


Table 4-650: sys_cache_grp_sn_attr attributes

Bits	Name	Description	Type	Reset
[63:55]	Reserved	Reserved	RO	-
[54:52]	sn_mode_sys_cache_grp3	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b0
[51:49]	sn_hash_addr_bits_sel_sys_cache_grp3	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[48]	inv_top_address_bit_sys_cache_grp3	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[47:39]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[38:36]	sn_mode_sys_cache_grp2	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b00
[35:33]	sn_hash_addr_bits_sel_sys_cache_grp2	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[32]	inv_top_address_bit_sys_cache_grp2	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[31:23]	Reserved	Reserved	RO	-
[22:20]	sn_mode_sys_cache_grp1	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b0
[19:17]	sn_hash_addr_bits_sel_sys_cache_grp1	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[16]	inv_top_address_bit_sys_cache_grp1	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[15:7]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[6:4]	sn_mode_sys_cache_grp0	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b0
[3:1]	sn_hash_addr_bits_sel_sys_cache_grp0	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[0]	inv_top_address_bit_sys_cache_grp0	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

4.3.16.45 sys_cache_grp_sn_attr1

Configures attributes for SN node IDs for system cache groups.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hEB8

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-635: sys_cache_grp_sn_attr1

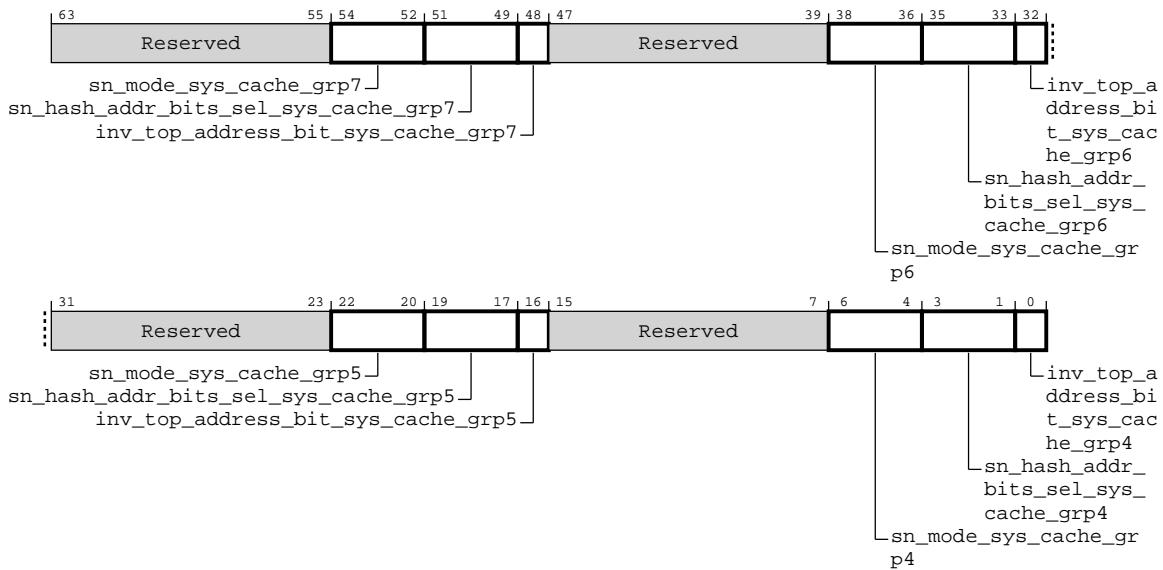


Table 4-651: sys_cache_grp_sn_attr1 attributes

Bits	Name	Description	Type	Reset
[63:55]	Reserved	Reserved	RO	-
[54:52]	sn_mode_sys_cache_grp7	SN selection mode	RW	3'b00
		3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved		
[51:49]	sn_hash_addr_bits_sel_sys_cache_grp7	SN hash address select(Valid for 3SN, 5SN, 6SN)	RW	3'h0
		3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved		
[48]	inv_top_address_bit_sys_cache_grp7	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[47:39]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[38:36]	sn_mode_sys_cache_grp6	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b00
[35:33]	sn_hash_addr_bits_sel_sys_cache_grp6	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[32]	inv_top_address_bit_sys_cache_grp6	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[31:23]	Reserved	Reserved	RO	-
[22:20]	sn_mode_sys_cache_grp5	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b0
[19:17]	sn_hash_addr_bits_sel_sys_cache_grp5	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[16]	inv_top_address_bit_sys_cache_grp5	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[15:7]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[6:4]	sn_mode_sys_cache_grp4	SN selection mode 3'b000 1-SN mode (SNO) 3'b001 3-SN mode (SNO, SN1, SN2) 3'b010 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100 2-SN mode (SNO, SN1) power of 2 hashing 3'b101 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing Others Reserved	RW	3'b0
[3:1]	sn_hash_addr_bits_sel_sys_cache_grp4	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[0]	inv_top_address_bit_sys_cache_grp4	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

4.3.16.46 sys_cache_grp_sn_sam_cfg0-3

There are 4 iterations of this register. The index ranges from 0 to 3. Configures top address bits for SN SAM system cache groups #{{index}*2} and #{{index}*2 + 1}. All top_address_bit fields must be between bits 47 and 28. top_address_bit2 > top_address_bit1 > top_address_bit0.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

```
index(0-7) : 16'h1140 + #{8 * index}
```

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-636: sys_cache_grp_sn_sam_cfg0-3

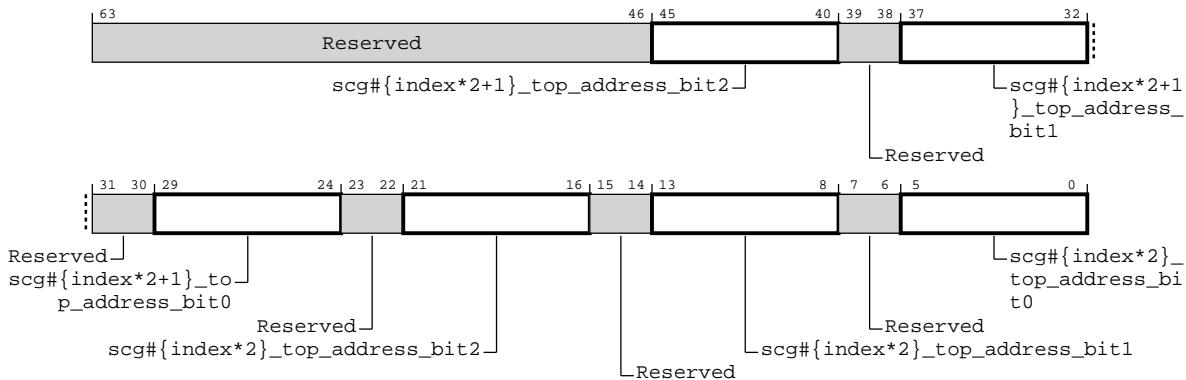


Table 4-652: sys_cache_grp_sn_sam_cfg0-3 attributes

Bits	Name	Description	Type	Reset
[63:46]	Reserved	Reserved	RO	-
[45:40]	<code>scg#{index*2+1}_top_address_bit2</code>	Top address bit 2 for system cache group # $\{index^*2+1\}$	RW	6'h00
[39:38]	Reserved	Reserved	RO	-
[37:32]	<code>scg#{index*2+1}_top_address_bit1</code>	Top address bit 1 for system cache group # $\{index^*2+1\}$	RW	6'h00
[31:30]	Reserved	Reserved	RO	-
[29:24]	<code>scg#{index*2+1}_top_address_bit0</code>	Top address bit 0 for system cache group # $\{index^*2+1\}$	RW	6'h00
[23:22]	Reserved	Reserved	RO	-
[21:16]	<code>scg#{index*2}_top_address_bit2</code>	Top address bit 2 for system cache group # $\{index^*2\}$	RW	6'h00
[15:14]	Reserved	Reserved	RO	-
[13:8]	<code>scg#{index*2}_top_address_bit1</code>	Top address bit 1 for system cache group # $\{index^*2\}$	RW	6'h00
[7:6]	Reserved	Reserved	RO	-
[5:0]	<code>scg#{index*2}_top_address_bit0</code>	Top address bit 0 for system cache group # $\{index^*2\}$	RW	6'h00

4.3.16.47 sam_qos_mem_region_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures the QoS value for memory region # $\{index\}$

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-15) : 16'h1280 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnsam_secure_register_groups_override.mem_range`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-637: sam_qos_mem_region_reg0-15

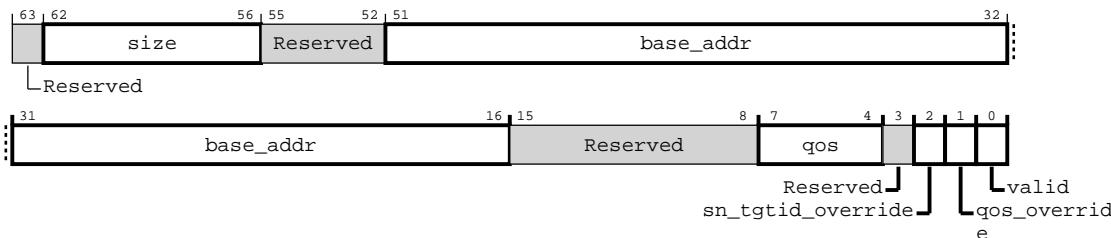


Table 4-653: sam_qos_mem_region_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
[55:52]	Reserved	Reserved	RO	-
[51:16]	base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	36'h0
[15:8]	Reserved	Reserved	RO	-
[7:4]	qos	Indicates the QoS value to be used for this region	RW	4'b0000
[3]	Reserved	Reserved	RO	-
[2]	sn_tgtid_override	Override the SN targetId for address contained in the region of this register	RW	1'b0
[1]	qos_override	QoS Memory region allow override 1'b0 Do not override the QoS value from the QoS regulator 1'b1 Override the QoS value with the programmed value in regionX_qos	RW	1'b0

Bits	Name	Description	Type	Reset
[0]	valid	<p>QoS Memory region valid</p> <p>1'b0 not valid</p> <p>1'b1 valid for memory region comparison</p>	RW	1'b0

4.3.16.48 sam_qos_mem_region_cfg2_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures the QOS memory region #{{index}}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-15) : 16'h1340 + #{{8 * index}}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-638: sam_qos_mem_region_cfg2_reg0-15

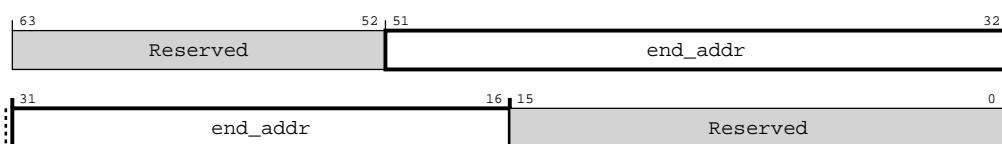


Table 4-654: sam_qos_mem_region_cfg2_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	end_addr	Bits [51:16] of end address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	36'h0
[15:0]	Reserved	Reserved	RO	-

4.3.16.49 sam_scg0-511/64_prefetch_nonhashed_ mem_region_cfg1_reg0-511%64

There are 512 iterations of this register. The index ranges from 0 to 511. Configures the prefetch nonhash memory region #{index}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-511) : 16'h4000 + # {8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-639: sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg1_reg0-511%64

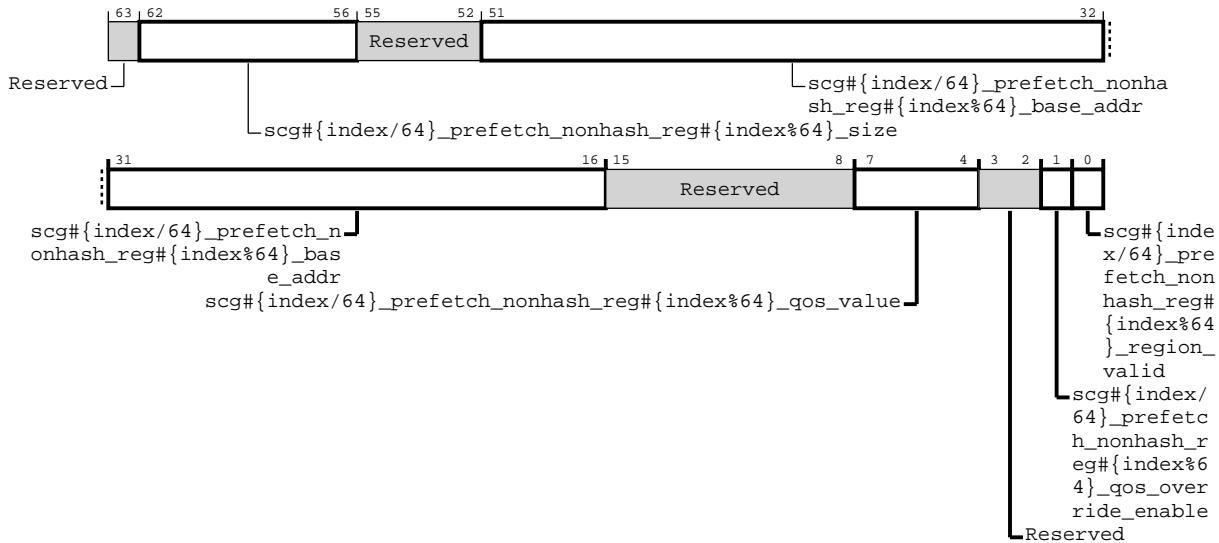


Table 4-655: sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg1_reg0-511%64 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	scg#[index/64]_prefetch_nonhash_reg#{index%64}_size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
[55:52]	Reserved	Reserved	RO	-
[51:16]	scg#[index/64]_prefetch_nonhash_reg#{index%64}_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	36'h0
[15:8]	Reserved	Reserved	RO	-
[7:4]	scg#[index/64]_prefetch_nonhash_reg#{index%64}_qos_value	Indicates the QoS value to be used for this region	RW	4'b0000
[3:2]	Reserved	Reserved	RO	-
[1]	scg#[index/64]_prefetch_nonhash_reg#{index%64}_qos_override_enable	Prefetch nonhash allow QOS override 1'b0 Do not override the QoS value from the QoS regulator 1'b1 Override the QoS value with the programmed value in regionX_qos	RW	1'b0
[0]	scg#[index/64]_prefetch_nonhash_reg#{index%64}_region_valid	Prefetch Nonhash region valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.50 sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg2_reg0-511%64

There are 512 iterations of this register. The index ranges from 0 to 511. Configures the Prefetch nonhash memory region #{index}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-511) : 16'h5000 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-640: sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg2_reg0-511%64

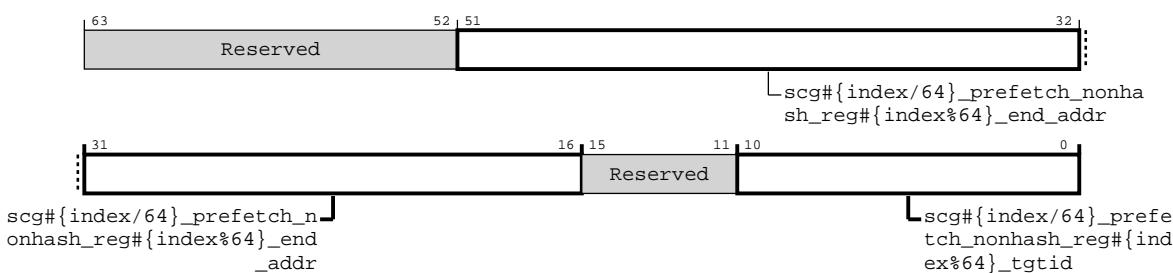


Table 4-656: sam_scg0-511/64_prefetch_nonhashed_mem_region_cfg2_reg0-511%64 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	scg#[index/64]_prefetch_nonhash_reg#[index%64]_end_addr	Bits [51:16] of end address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	36'h0

Bits	Name	Description	Type	Reset
[15:11]	Reserved	Reserved	RO	-
[10:0]	scg#{index/64}_prefetch_nonhash_reg#{index %64}_tgtid	SN TgtID for the non-hashed region	RW	11'h0

4.3.16.51 sam_scg0-63/8_prefetch_hashed_region_cfg1_reg0-63%8

There are 64 iterations of this register. The index ranges from 0 to 63. Configures the prefetch hashed memory region #{index}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-63) : 16'h6000 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-641: sam_scg0-63/8_prefetch_hashed_region_cfg1_reg0-63%8

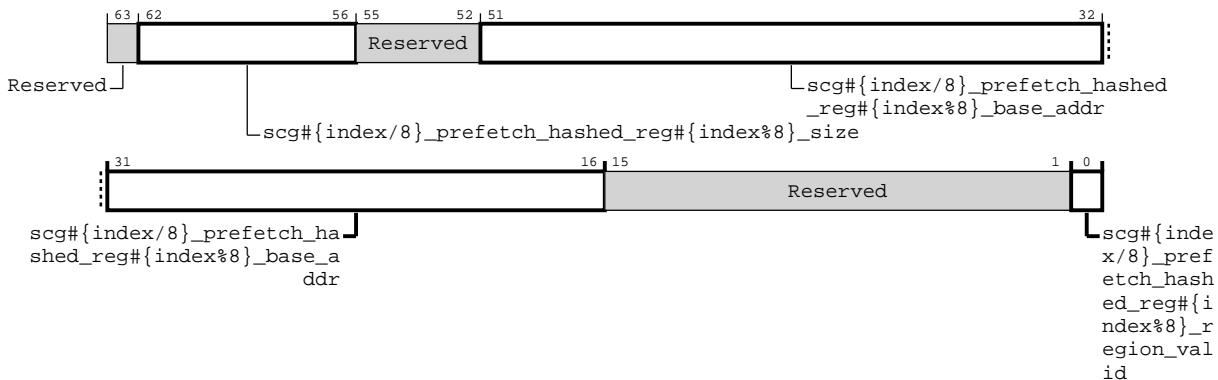


Table 4-657: sam_scg0-63/8_prefetch_hashed_region_cfg1_reg0-63%8 attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:56]	scg#[index/8]_prefetch_hashed_reg#[index%8]_size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size ($2^{\text{address width}}$).	RW	5'b00000
[55:52]	Reserved	Reserved	RO	-
[51:16]	scg#[index/8]_prefetch_hashed_reg#[index%8]_base_addr	Bits [51:16] of base address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	36'h0
[15:1]	Reserved	Reserved	RO	-
[0]	scg#[index/8]_prefetch_hashed_reg#[index%8]_region_valid	Prefetch Hashed region valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.52 sam_scg0-63/8_prefetch_hashed_region_cfg2_reg0-63%8

There are 64 iterations of this register. The index ranges from 0 to 63. Configures the Prefetch hashed memory region #{index}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-63) : 16'h6200 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-642: sam_scg0-63/8_prefetch_hashed_region_cfg2_reg0-63%8

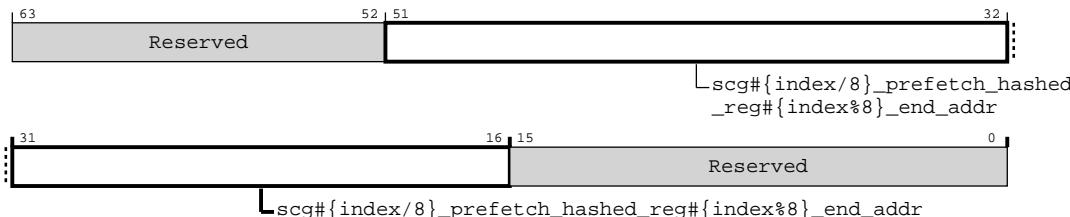


Table 4-658: sam_scg0-63/8_prefetch_hashed_region_cfg2_reg0-63%8 attributes

Bits	Name	Description	Type	Reset
[63:52]	Reserved	Reserved	RO	-
[51:16]	scg#{index/8}_prefetch_hashed_reg#{index%8}_end_addr	Bits [51:16] of end address of the range, LSB bit is defined by the parameter POR_HNSAM_RCOMP_LSB_PARAM	RW	36'h0
[15:0]	Reserved	Reserved	RO	-

4.3.16.53 sam_scg0-63/8_prefetch_hashed_region_cfg3_reg0-63%8

There are 64 iterations of this register. The index ranges from 0 to 63. Configures the Prefetch hashed memory region #{index}

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-63) : 16'h6400 + #{8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

`por_rnsam_secure_register_groups_override.mem_range`

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-643: sam_scg0-63/8_prefetch_hashed_region_cfg3_reg0-63%8

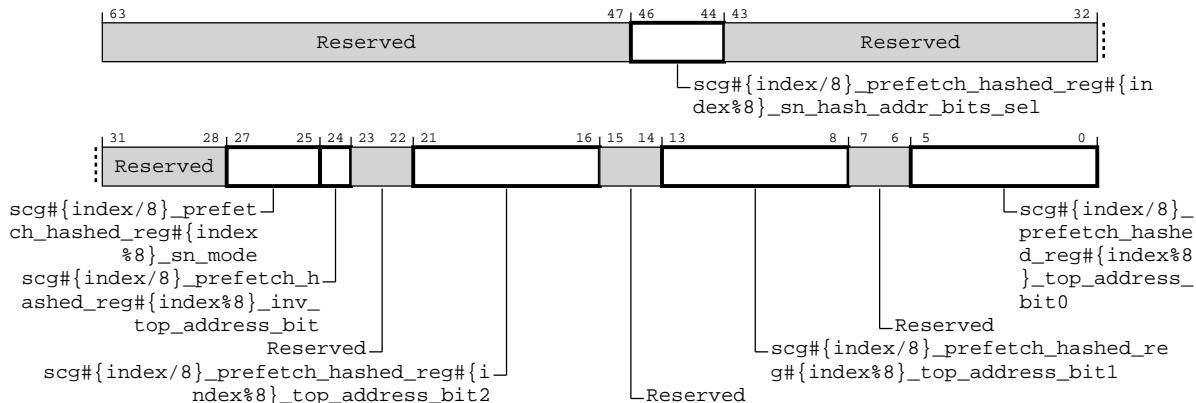


Table 4-659: sam_scg0-63/8_prefetch_hashed_region_cfg3_reg0-63%8 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[46:44]	scg#[index/8]_prefetch_hashed_reg#[index%8]_sn_hash_addr_bits_sel	SN hash address select(Valid for 3SN, 5SN, 6SN) 3'b000 [16:8] address bits (Default) 3'b001 [17:9] address bits 3'b010 [18:10] address bits 3'b011 [19:11] address bits 3'b100 [20:12] address bits 3'b101 [21:13] address bits Others Reserved	RW	3'h0
[43:28]	Reserved	Reserved	RO	-
[27:25]	scg#[index/8]_prefetch_hashed_reg#[index%8]_sn_mode	SN selection mode 3'b000: Reserved 3'b001: 3-SN mode (SNO, SN1, SN2) 3'b010: 6-SN mode (SNO, SN1, SN2, SN3, SN4, SN5) 3'b011: 5-SN mode (SNO, SN1, SN2, SN3, SN4) 3'b100: 2-SN mode (SNO, SN1) power of 2 hashing 3'b101: 4-SN mode (SNO, SN1, SN2, SN3) power of 2 hashing 3'b110: 8-SN mode (SNO, SN1, SN2, SN3, SN4, SN5, SN6, SN7) power of 2 hashing 3'b111: Reserved	RW	3'b0
[24]	scg#[index/8]_prefetch_hashed_reg#[index%8]_inv_top_address_bit	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
[23:22]	Reserved	Reserved	RO	-
[21:16]	scg#[index/8]_prefetch_hashed_reg#[index%8]_top_address_bit2	Top address bit 2	RW	6'h00
[15:14]	Reserved	Reserved	RO	-
[13:8]	scg#[index/8]_prefetch_hashed_reg#[index%8]_top_address_bit1	Top address bit 1	RW	6'h00
[7:6]	Reserved	Reserved	RO	-
[5:0]	scg#[index/8]_prefetch_hashed_reg#[index%8]_top_address_bit0	Top address bit 0	RW	6'h00

4.3.16.54 sys_cache_grp_sn_nodeid_reg0-31

There are 32 iterations of this register. The index ranges from 0 to 31. Configures hashed node IDs for system cache groups. Controls target SN node IDs #{{index}*4} to #{{index}*4 + 3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

`index(0-31) : 16'h1000 + #{8 * index}`

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-644: sys_cache_grp_sn_nodeid_reg0-31

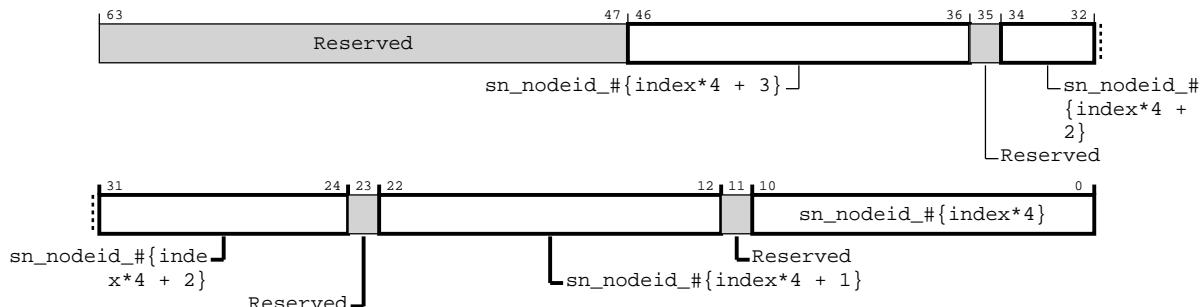


Table 4-660: sys_cache_grp_sn_nodeid_reg0-31 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:36]	<code>sn_nodeid_{index*4 + 3}</code>	Default Hashed target SN node ID <code>{index*4 + 3}</code>	RW	11'b000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	<code>sn_nodeid_{index*4 + 2}</code>	Default Hashed target SN node ID <code>{index*4 + 2}</code>	RW	11'b000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	<code>sn_nodeid_{index*4 + 1}</code>	Default Hashed target SN node ID <code>{index*4 + 1}</code>	RW	11'b000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	<code>sn_nodeid_{index*4}</code>	Default Hashed target SN node ID <code>{index*4}</code>	RW	11'b000000000000

4.3.16.55 sys_cache_grp_region0-63/32_sn_nodeid_reg0-63%32

There are 64 iterations of this register. Configures node IDs for SCG's Default hashed Region memory. Controls target SN node IDs #{{index}*4} to #{{index}*4+3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-63) : 16'h1400 + #{{8 * index}}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-645: sys_cache_grp_region0-63/32_sn_nodeid_reg0-63%32

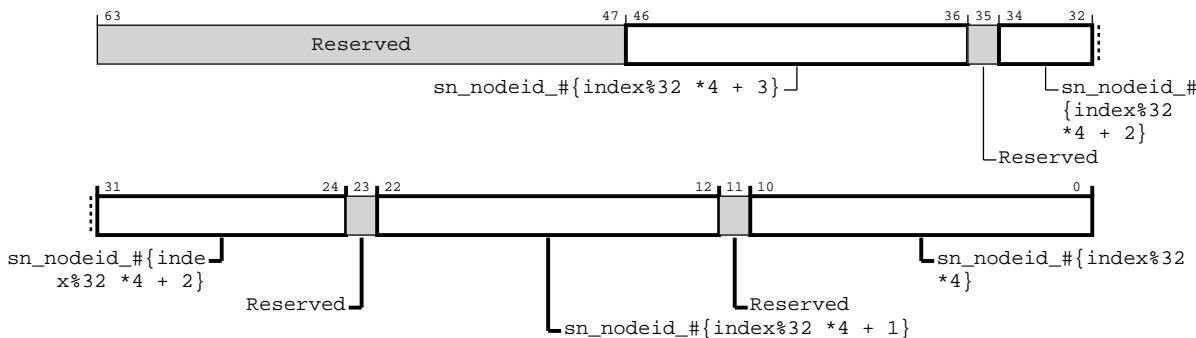


Table 4-661: sys_cache_grp_region0-63/32_sn_nodeid_reg0-63%32 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:36]	sn_nodeid_#{{index}%32 *4 + 3}	Hashed target SN node ID #{{index}%32 * 4 +3}	RW	11'b000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	sn_nodeid_#{{index}%32 *4 + 2}	Hashed target SN node ID #{{index}%32 * 4 +2}	RW	11'b000000000000

Bits	Name	Description	Type	Reset
[23]	Reserved	Reserved	RO	-
[22:12]	sn_nodeid_{index%32 *4 + 1}	Hashed target SN node ID #{index%32 * 4 +1}	RW	11'b000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	sn_nodeid_{index%32 *4}	Hashed target SN node ID #{index%32 * 4}	RW	11'b000000000000

4.3.16.56 sys_cache_grp_hashed_regions_sn_nodeid_reg0-15

There are 16 iterations of this register. The index ranges from 0 to 15. Configures SN node IDs for SCG's Hashed groups in the HNSAM . Controls target SN node IDs #{index*4} to #{index*4 + 3}.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-31) : 16'h6600 + # {8 * index}

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-646: sys_cache_grp_hashed_regions_sn_nodeid_reg0-15

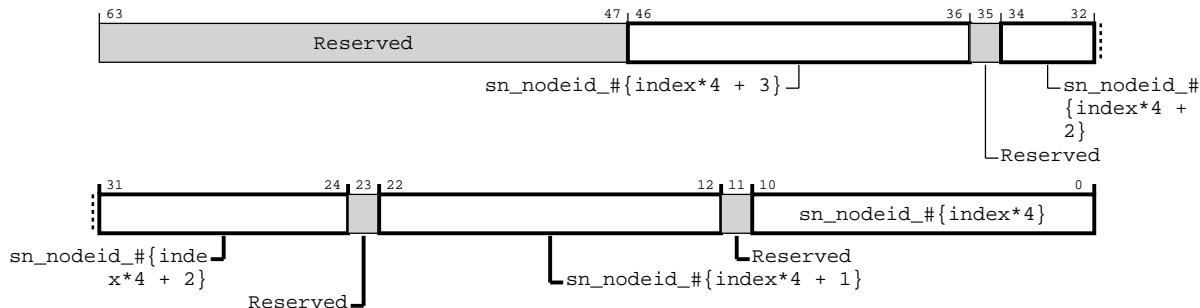


Table 4-662: sys_cache_grp_hashed_regions_sn_nodeid_reg0-15 attributes

Bits	Name	Description	Type	Reset
[63:47]	Reserved	Reserved	RO	-
[46:36]	sn_nodeid_{[index*4 + 3]}	Hashed target SN node ID #{index*4 + 3}	RW	11'b000000000000
[35]	Reserved	Reserved	RO	-
[34:24]	sn_nodeid_{[index*4 + 2]}	Hashed target SN node ID #{index*4 + 2}	RW	11'b000000000000
[23]	Reserved	Reserved	RO	-
[22:12]	sn_nodeid_{[index*4 + 1]}	Hashed target SN node ID #{index*4 + 1}	RW	11'b000000000000
[11]	Reserved	Reserved	RO	-
[10:0]	sn_nodeid_{[index*4]}	Hashed target SN node ID #{index*4}	RW	11'b000000000000

4.3.16.57 rnsam_status

Functions as the default and programming mode status register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1100

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-647: rnsam_status

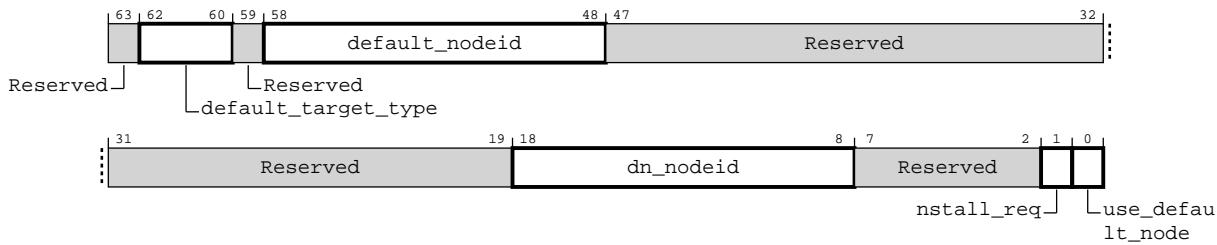


Table 4-663: rnsam_status attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:60]	default_target_type	<p>Indicates node type</p> <p>3'b000 HN-F</p> <p>3'b001 HN-I</p> <p>3'b010 CXRA</p> <p>3'b011 HN-P</p> <p>3'b100 PCI-CXRA</p> <p>3'b101 HN-S</p> <p>Others Reserved</p> <p>CONSTRAINT: Only applicable for RN-I</p>	RW	3'b001
[59]	Reserved	Reserved	RO	-
[58:48]	default_nodeid	Default Node ID	RW	Configuration dependent
[47:19]	Reserved	Reserved	RO	-
[18:8]	dn_nodeid	DN Node ID for DN operations	RW	11'b0
[7:2]	Reserved	Reserved	RO	-
[1]	nstall_req	<p>Indicates RN SAM is programmed and ready</p> <p>1'b0 STALL requests</p> <p>1'b1 UNSTALL requests</p>	RW	1'b0
[0]	use_default_node	<p>Indicates target ID selection mode</p> <p>1'b0 Enables RN SAM to hash address bits and generate target ID</p> <p>1'b1 Uses default target ID</p>	RW	1'b1

4.3.16.58 gic_mem_region_reg

Configures GIC memory region.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h1108

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-648: gic_mem_region_reg

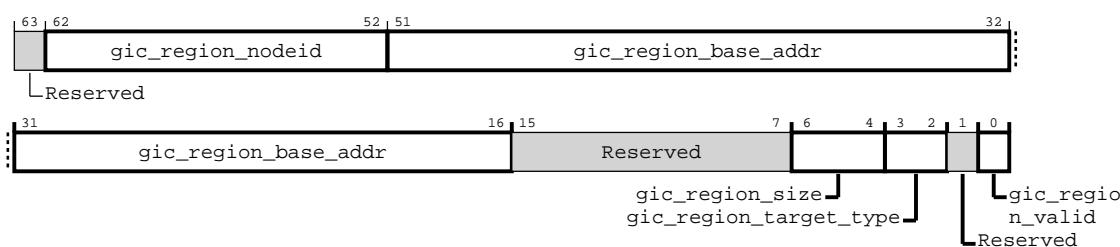


Table 4-664: gic_mem_region_reg attributes

Bits	Name	Description	Type	Reset
[63]	Reserved	Reserved	RO	-
[62:52]	gic_region_nodeid	GIC node ID	RW	11'b000000000000
[51:16]	gic_region_base_addr	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	36'h000000000
[15:7]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[6:4]	gic_region_size	GIC memory region size 3'b000 64KB 3'b001 128KB 3'b010 256KB 3'b011 512KB CONSTRAINT: Memory region must be a power of 2.	RW	3'b000
[3:2]	gic_region_target_type	Indicates node type 2'b00 HN-F 2'b01 HN-I 2'b10 CXRA 2'b11 HN-P CONSTRAINT: Only applicable for RN-I	RW	2'b00
[1]	Reserved	Reserved	RO	-
[0]	gic_region_valid	Memory region 1 valid 1'b0 not valid 1'b1 valid for memory region comparison	RW	1'b0

4.3.16.59 sam_generic_regs0-7

There are 8 iterations of this register. The index ranges from 0 to 7. Configuration register for the custom logic

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

index(0-7) : 16'h1600 + # {8 * index}

Type

RW

Reset value

See individual bit resets

Secure group override

por_rnsam_secure_register_groups_override.mem_range

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-649: sam_generic_regs0-7

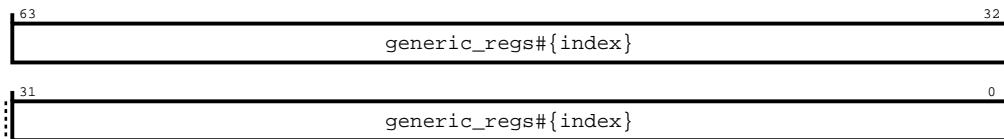


Table 4-665: sam_generic_regs0-7 attributes

Bits	Name	Description	Type	Reset
[63:0]	generic_regs#{index}	Configuration register for the custom logic	RW	64'h0

4.3.17 SBSX register descriptions

This section lists the SBSX registers.

4.3.17.1 por_sbsx_node_info

Provides component identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h0

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-650: por_sbsx_node_info

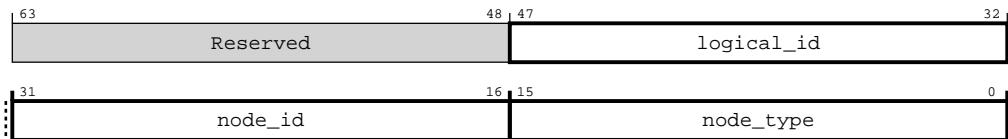


Table 4-666: por_sbsx_node_info attributes

Bits	Name	Description	Type	Reset
[63:48]	Reserved	Reserved	RO	-
[47:32]	logical_id	Component logical ID	RO	Configuration dependent
[31:16]	node_id	Component node ID	RO	Configuration dependent
[15:0]	node_type	CMN-700 node type identifier	RO	16'h0007

4.3.17.2 por_sbsx_child_info

Provides component child identification information.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h80

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-651: por_sbsx_child_info

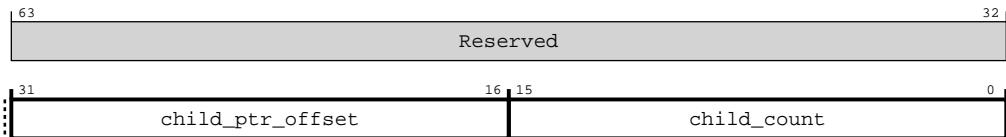


Table 4-667: por_sbsx_child_info attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31:16]	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
[15:0]	child_count	Number of child nodes; used in discovery process	RO	16'b0

4.3.17.3 por_sbsx_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h980

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-652: por_sbsx_secure_register_groups_override

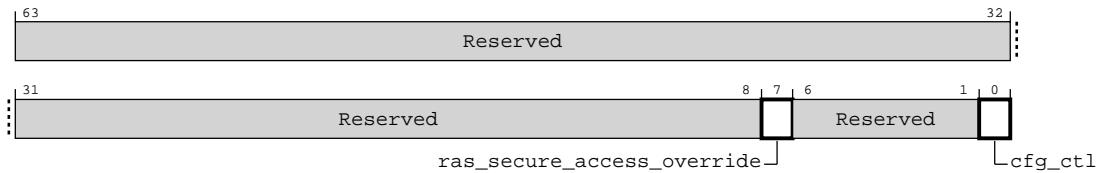


Table 4-668: por_sbsx_secure_register_groups_override attributes

Bits	Name	Description	Type	Reset
[63:8]	Reserved	Reserved	RO	-
[7]	ras_secure_access_override	Allow Non-secure access to Secure RAS registers	RW	1'b0
[6:1]	Reserved	Reserved	RO	-
[0]	cfg_ctl	Allows Non-secure access to Secure configuration control register (por_sbsx_cfg_ctl)	RW	1'b0

4.3.17.4 por_sbsx_unit_info

Provides component identification information for SBSX.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h900

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-653: por_sbsx_unit_info

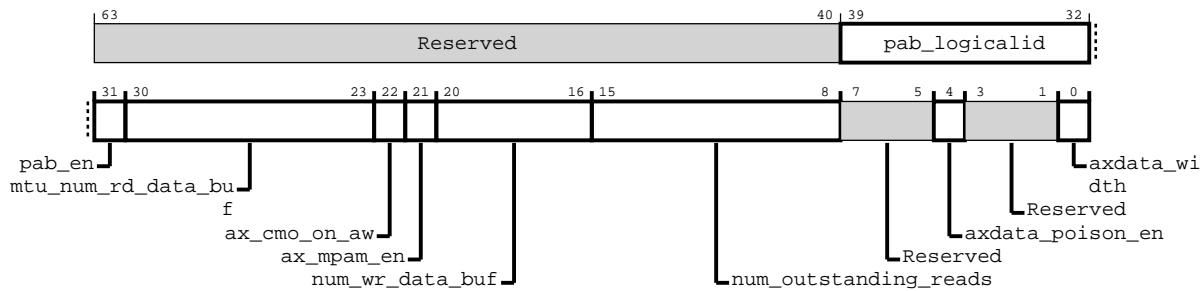


Table 4-669: por_sbsx_unit_info attributes

Bits	Name	Description	Type	Reset
[63:40]	Reserved	Reserved	RO	-
[39:32]	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
[31]	pab_en	PUB AUB bridge enable	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[30:23]	mtu_num_rd_data_buf	Number of mtu read data buffers in SBSX	RO	Configuration dependent
[22]	ax_cmo_on_aw	Write Channel CMOs enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[21]	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b1 Enabled 1'b0 Not enabled		
[20:16]	num_wr_data_buf	Number of write data buffers in SBSX	RO	Configuration dependent
[15:8]	num_outstanding_reads	Maximum number of outstanding AXI read requests from SBSX	RO	Configuration dependent
[7:5]	Reserved	Reserved	RO	-
[4]	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b0 Not supported 1'b1 Supported		
[3:1]	Reserved	Reserved	RO	-
[0]	axdata_width	Data width on ACE-Lite/AXI4 interface	RO	Configuration dependent
		1'b0 128 bits 1'b1 256 bits		

4.3.17.5 por_sbsx_cfg_ctl

Functions as the configuration control register for SBSX bridge.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA00

Type

RW

Reset value

See individual bit resets

Secure group override

por_sbsx_secure_register_groups_override.cfg_ctl

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-654: por_sbsx_cfg_ctl

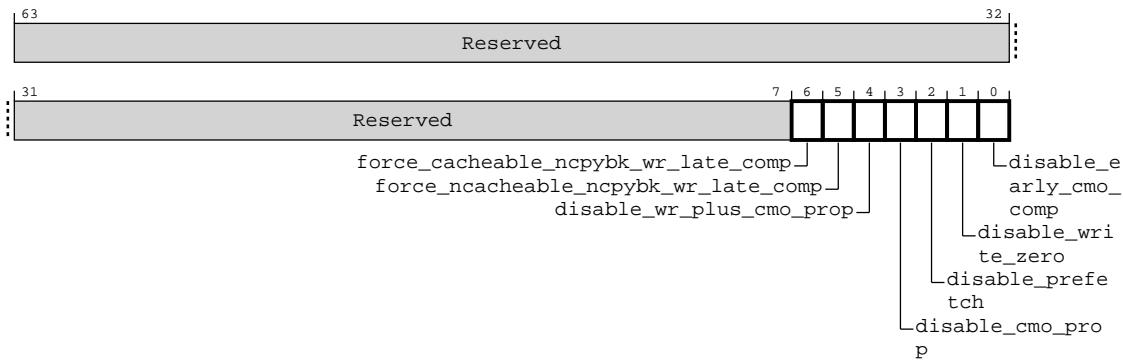


Table 4-670: por_sbsx_cfg_ctl attributes

Bits	Name	Description	Type	Reset
[63:7]	Reserved	Reserved	RO	-
[6]	force_cacheable_ncpybk_wr_late_comp	Late Comp for Cacheable Non-CopyBack Writes. Overrides EWA	RW	1'b0

Bits	Name	Description	Type	Reset
[5]	force_ncacheable_ncpybk_wr_late_comp	Late Comp for Non-cacheable Non-CopyBack Writes. Overrides EWA	RW	1'b0
[4]	disable_wr_plus_cmo_prop	Disables Write_plus_CMO propagation on ACE.	RW	1'b0
[3]	disable_cmo_prop	Disables CMO propagation on ACE.	RW	1'b0
[2]	disable_prefetch	Disables Prefetches on AXI.	RW	1'b0
[1]	disable_write_zero	Disables WriteZero Op on AXI.	RW	1'b0
[0]	disable_early_cmo_comp	Disables Early Comp for CMOs in SBSX to HNF.	RW	1'b0

4.3.17.6 por_sbsx_aux_ctl

Functions as the auxiliary control register for the SBSX bridge.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA08

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-655: por_sbsx_aux_ctl

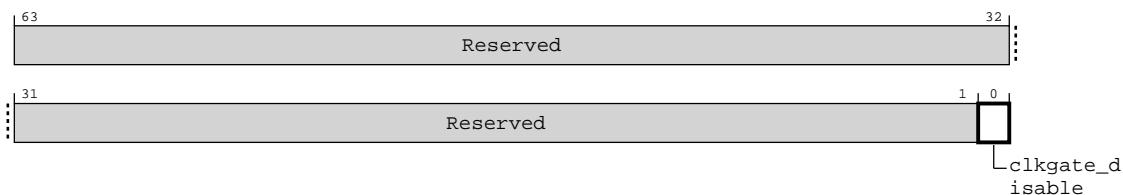


Table 4-671: por_sbsx_aux_ctl attributes

Bits	Name	Description	Type	Reset
[63:1]	Reserved	Reserved	RO	-
[0]	clkgate_disable	Disables internal clock gating in SBSX bridge	RW	1'b0

4.3.17.7 por_sbsx_cbusy_limit_ctl

Cbusy threshold limits for Request Tracker entries.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'hA18

Type

RW

Reset value

See individual bit resets

Usage constraints

Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-656: por_sbsx_cbusy_limit_ctl

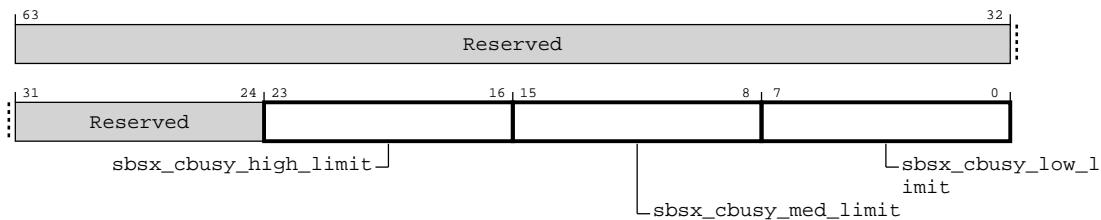


Table 4-672: por_sbsx_cbusy_limit_ctl attributes

Bits	Name	Description	Type	Reset
[63:24]	Reserved	Reserved	RO	-
[23:16]	sbsx_cbusy_high_limit	ReqTracker limit for CBusy High	RW	Configuration dependent

Bits	Name	Description	Type	Reset
[15:8]	sbsx_cbusy_med_limit	ReqTracker limit for CBusy Med	RW	Configuration dependent
[7:0]	sbsx_cbusy_low_limit	ReqTracker limit for CBusy Low	RW	Configuration dependent

4.3.17.8 por_sbsx_errfr

Functions as the error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3000

Type

RO

Reset value

See individual bit resets

Secure group override

por_sbsx_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-657: por_sbsx_errfr

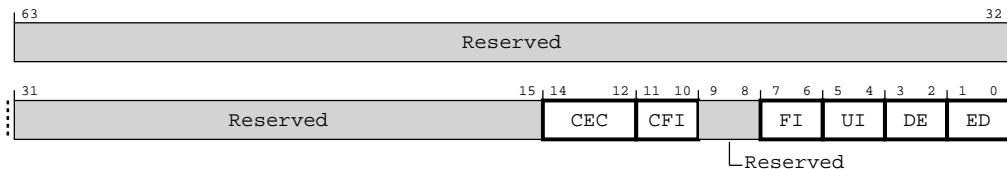


Table 4-673: por_sbsx_errfr attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000

Bits	Name	Description	Type	Reset
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors	RO	2'b00
[1:0]	ED	Error detection	RO	2'b01

4.3.17.9 por_sbsx_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferral are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3008

Type

RW

Reset value

See individual bit resets

Secure group override

por_sbsx_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-658: por_sbsx_errctlr

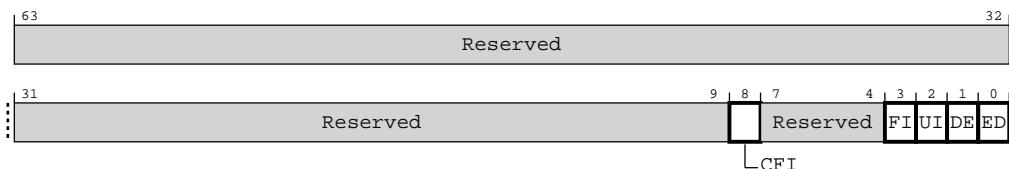


Table 4-674: por_sbsx_errctlr attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_sbsx_errfr.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_sbsx_errfr.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_sbsx_errfr.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_sbsx_errfr.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_sbsx_errfr.ED	RW	1'b0

4.3.17.10 por_sbsx_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3010

Type

W1C

Reset value

See individual bit resets

Secure group override

por_sbsx_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-659: por_sbsx_errstatus

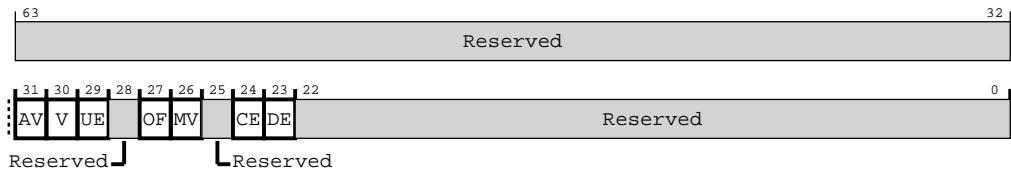


Table 4-675: por_sbsx_errstatus attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; por_sbsx_erraddr contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
[26]	MV	por_sbsx_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-

Bits	Name	Description	Type	Reset
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.17.11 por_sbsx_erraddr

Contains the error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3018

Type

RW

Reset value

See individual bit resets

Secure group override

por_sbsx_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-660: por_sbsx_erraddr

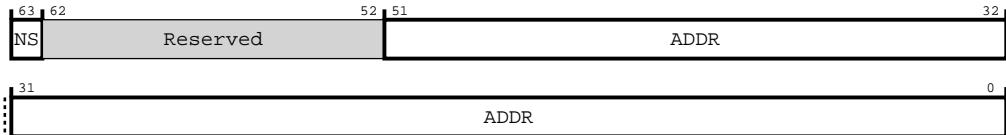


Table 4-676: por_sbsx_erraddr attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: por_sbsx_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.17.12 por_sbsx_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3020

Type

RW

Reset value

See individual bit resets

Secure group override

por_sbsx_secure_register_groups_override.ras_secure_access_override

Usage constraints

Only accessible by Secure accesses.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-661: por_sbsx_errmisc

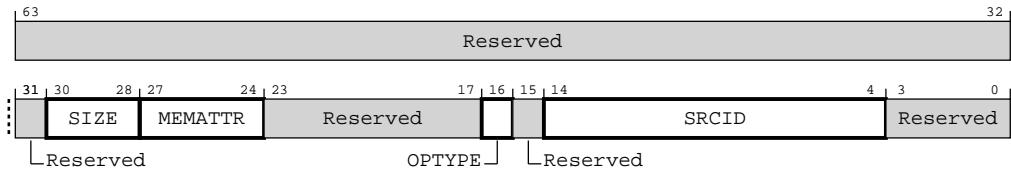


Table 4-677: por_sbsx_errmisc attributes

Bits	Name	Description	Type	Reset
[63:31]	Reserved	Reserved	RO	-
[30:28]	SIZE	Error transaction size	RW	3'b0
[27:24]	MEMATTR	Error memory attributes	RW	4'b0
[23:17]	Reserved	Reserved	RO	-
[16]	OPTYPE	Error opcode type	RW	1'b0
		1'b1 WR_NO_SNP_PTL (partial) 1'b0 WR_NO_SNP_FULL		
[15]	Reserved	Reserved	RO	-
[14:4]	SRCID	Error source ID	RW	11'b0
[3:0]	Reserved	Reserved	RO	-

4.3.17.13 por_sbsx_errfr_NS

Functions as the Non-secure error feature register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3100

Type

RO

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-662: por_sbsx_errfr_NS

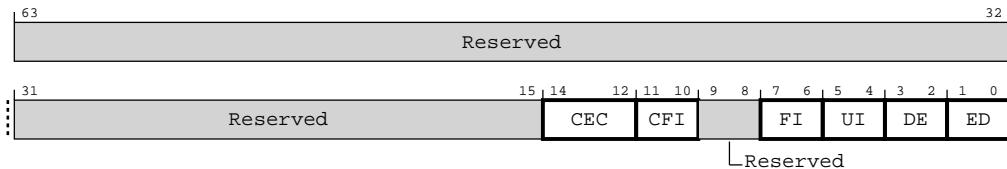


Table 4-678: por_sbsx_errfr_NS attributes

Bits	Name	Description	Type	Reset
[63:15]	Reserved	Reserved	RO	-
[14:12]	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
[11:10]	CFI	Corrected error interrupt	RO	2'b00
[9:8]	Reserved	Reserved	RO	-
[7:6]	FI	Fault handling interrupt	RO	2'b10
[5:4]	UI	Uncorrected error interrupt	RO	2'b10
[3:2]	DE	Deferred errors	RO	2'b00
[1:0]	ED	Error detection	RO	2'b01

4.3.17.14 por_sbsx_errctlr_NS

Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3108

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-663: por_sbsx_errctlr_NS

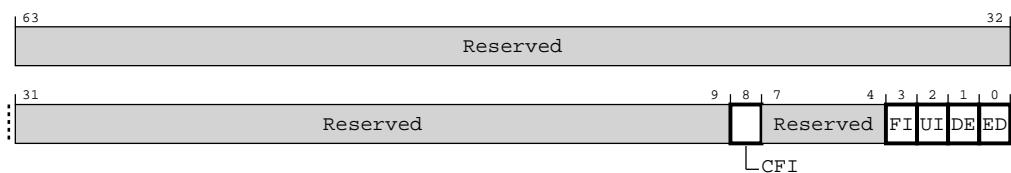


Table 4-679: por_sbsx_errctlr_NS attributes

Bits	Name	Description	Type	Reset
[63:9]	Reserved	Reserved	RO	-
[8]	CFI	Enables corrected error interrupt as specified in por_sbsx_errfr_NS.CFI	RW	1'b0
[7:4]	Reserved	Reserved	RO	-
[3]	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_sbsx_errfr_NS.FI	RW	1'b0
[2]	UI	Enables uncorrected error interrupt as specified in por_sbsx_errfr_NS.UI	RW	1'b0
[1]	DE	Enables error deferment as specified in por_sbsx_errfr_NS.DE	RW	1'b0
[0]	ED	Enables error detection as specified in por_sbsx_errfr_NS.ED	RW	1'b0

4.3.17.15 por_sbsx_errstatus_NS

Functions as the Non-secure error status register.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3110

Type

W1C

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-664: por_sbsx_errstatus_NS

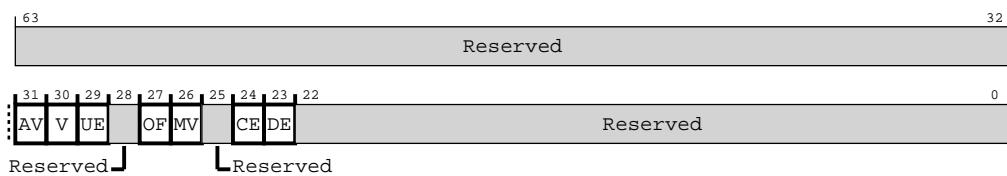


Table 4-680: por_sbsx_errstatus_NS attributes

Bits	Name	Description	Type	Reset
[63:32]	Reserved	Reserved	RO	-
[31]	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Address is valid; por_sbsx_erraddr_NS contains a physical address for that recorded error 1'b0 Address is not valid	W1C	1'b0
[30]	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error recorded; register is valid 1'b0 No errors recorded	W1C	1'b0
[29]	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error detected that is not corrected and is not deferred to a subordinate 1'b0 No uncorrected errors detected	W1C	1'b0
[28]	Reserved	Reserved	RO	-
[27]	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1 More than one error detected 1'b0 Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Bits	Name	Description	Type	Reset
[26]	MV	por_sbsx_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1 Miscellaneous registers are valid 1'b0 Miscellaneous registers are not valid	W1C	1'b0
[25]	Reserved	Reserved	RO	-
[24]	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one transient corrected error recorded 1'b0 No corrected errors recorded	W1C	1'b0
[23]	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1 At least one error is not corrected and is deferred 1'b0 No errors deferred	W1C	1'b0
[22:0]	Reserved	Reserved	RO	-

4.3.17.16 por_sbsx_erraddr_NS

Contains the Non-secure error record address.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3118

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-665: por_sbsx_erraddr_NS

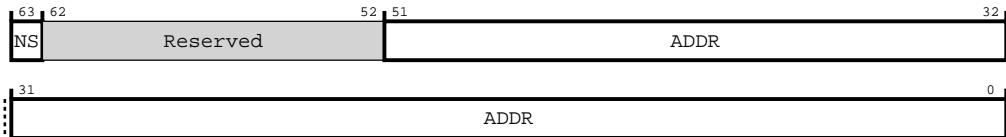


Table 4-681: por_sbsx_erraddr_NS attributes

Bits	Name	Description	Type	Reset
[63]	NS	Security status of transaction 1'b1 Non-secure transaction 1'b0 Secure transaction CONSTRAINT: por_sbsx_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
[62:52]	Reserved	Reserved	RO	-
[51:0]	ADDR	Transaction address	RW	52'b0

4.3.17.17 por_sbsx_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h3120

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-666: por_sbsx_errmisc_NS

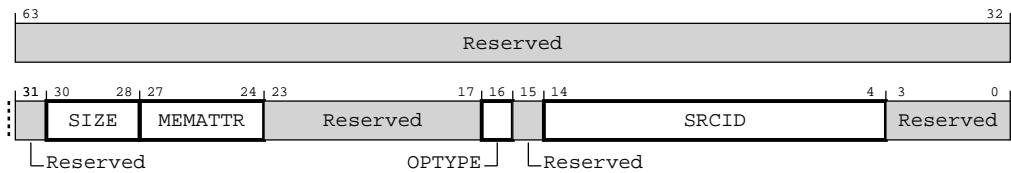


Table 4-682: por_sbsx_errmisc_NS attributes

Bits	Name	Description	Type	Reset
[63:31]	Reserved	Reserved	RO	-
[30:28]	SIZE	Error transaction size	RW	3'b0
[27:24]	MEMATTR	Error memory attributes	RW	4'b0
[23:17]	Reserved	Reserved	RO	-
[16]	OPTYPE	Error opcode type	RW	1'b0
		1'b1 WR_NO_SNP_PTL (partial) 1'b0 WR_NO_SNP_FULL		
[15]	Reserved	Reserved	RO	-
[14:4]	SRCID	Error source ID	RW	11'b0
[3:0]	Reserved	Reserved	RO	-

4.3.17.18 por_sbsx_pmu_event_sel

Specifies the PMU event to be counted.

Configurations

This register is available in all configurations.

Attributes

Width

64

Address offset

16'h2000

Type

RW

Reset value

See individual bit resets

Usage constraints

There are no usage constraints.

Bit descriptions

The following image shows the higher register bit assignments.

Figure 4-667: por_sbsx_pmu_event_sel

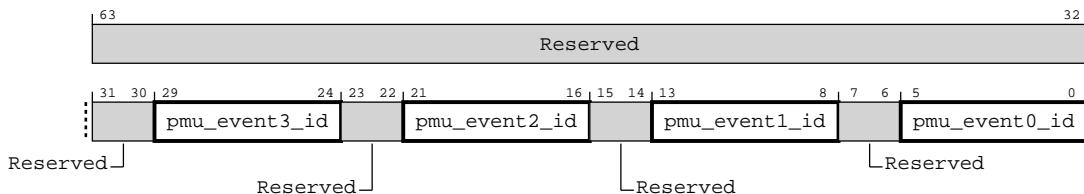


Table 4-683: por_sbsx_pmu_event_sel attributes

Bits	Name	Description	Type	Reset
[63:30]	Reserved	Reserved	RO	-
[29:24]	pmu_event3_id	SBSX PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
[23:22]	Reserved	Reserved	RO	-
[21:16]	pmu_event2_id	SBSX PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
[15:14]	Reserved	Reserved	RO	-
[13:8]	pmu_event1_id	SBSX PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0
[7:6]	Reserved	Reserved	RO	-
[5:0]	pmu_event0_id	SBSX PMU Event 0 select 6'h00 No event 6'h01 Read request 6'h02 Write request 6'h03 CMO request 6'h04 RETRYACK TXRSP flit sent 6'h05 TXDAT flit seen 6'h06 TXRSP flit seen 6'h11 Read request tracker occupancy count overflow 6'h12 Write request tracker occupancy count overflow 6'h13 CMO request tracker occupancy count overflow 6'h14 WDB occupancy count overflow 6'h15 Read AXI pending tracker occupancy count overflow 6'h16 CMO AXI pending tracker occupancy count overflow 6'h17 RDB occupancy count overflow. (Only when MTU is enabled) 6'h21 ARVALID set without ARREADY 6'h22 AWVALID set without AWREADY 6'h23 WVALID set without WREADY 6'h24 TXDAT stall (TXDAT valid but no link credit available) 6'h25 TXRSP stall (TXRSP valid but no link credit available)	RW	6'b0

NOTE: All other encodings are reserved.

4.4 CMN-700 programming

This section contains CMN-700 programming information.

4.4.1 Boot-time programming sequence

A specific boot-time programming sequence must be used to set up CMN-700 correctly. An example sequence is provided, which uses a *System Control Processor* (SCP) to perform the initial boot configuration.

After reset, the following configuration steps must happen before broad access to CMN-700 components is available:

1. CMN-700 uses a default configuration to access boot flash through the HN-D ACE-Lite manager interface and also the configuration registers.
2. An RN-F, or a manager that is connected to an RN-I, must then access the configuration registers to configure CMN-700. This boot-time configuration must happen before there is broader access to components such as HN-F or SN.



Note If booting from a device downstream of the HN-D node, in your final RN SAM

configuration the boot code region target must not change from the HN-D.

The following example provides more information on the boot process. It assumes an SCP is performing the CMN-700 configuration.

1. The SCP boots, either from local memory or through CMN-700 memory accesses targeting memory behind the HN-D:
 - All other managers are either held in reset or issue no requests to CMN-700 until the boot programming is complete.
 - The HN-D is identified through straps on the RN SAM.
2. If necessary, the SCP discovers the system.
3. The SCP determines the wanted address map and corresponding SAM register values.
4. If necessary, the SCP remaps the configuration register space by completing the following steps:
 - a. It drains all requests in flight by waiting for their responses.
 - b. It issues a single 64-bit store to a PERIPHBASE register behind the HN-D. This register would be in logic that is external to CMN-700 and an update would cause the signal values on the CFGM_PERIPHBASE input to change.
 - c. It waits for the response for that store.
5. If necessary, the SCP writes to the CMN-700 configuration registers to program the SAM for all RN-Fs.