Wajid Ali *Electrical Engineer*

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Lahore, Pakistan

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2003/05/19

Pakistani

Experience

2024/02 – present
Santa Clara, CA, USA

Mirabilis Design - Application Engineering Intern
Specialized in system modeling at Mirabilis Design, using VisualSim to create models for RISC-V BOOM core and ARM A720AE. Worked on Artries NoC and ARM CMN600, contributing to performance optimization and system integration. Additionally, I developed training content for Mirabilis Design's Seal-E learning program, creating computer architecture training sessions and hands-on experiments. I also worked on generating traces for different benchmarks, such as SPEC2006 and microbenchmarks, using tools like gem5, GPGPU-Sim, and NVBit, running these traces on VisualSim models to further deepen my understanding of system performance and architectural challenges.

2023/05 – present
Lahore, Punjab, Pakistan

MEDS Lab UET Lahore— Research Assistant
Developed and implemented verification tests for the privilege architecture of the CVA6 processor under the supervision of **Mr. Umer Shahid**. Successfully booted Linux on UET RV Pcore and currently focusing on floor planning, routing, and placement of UET RV Pcore using 22nm TSMC libraries with Cadence tools. Additionally, mentored new trainees in the lab, leading sessions on using the RISC-V toolchain and implementing single-cycle processors in RISC-V architecture.

2023/07 – 2024/02
Davis, CA, USA

Research Assistant of Phd student
Engaged in collaborative research on gem5 simulations with **Ayaz Akram,** a PhD scholar at UC Davis, contributing to the advancement of gem5 simulation techniques and gaining deep insights into computer architecture research. Worked on the project "Accelerating Computer Architecture Simulation through Machine Learning" which was published in CAMS (Computer Architecture Modelling and Simulation) 2023. This collaboration enriched my expertise in simulation methodologies and their intersection with machine learning.

2024/01 – 2024/05
Melbourne, Victoria, Australia

Escalo AI - Software Development Intern
Contributed to virtual reality project by developing an educational training VR model. Collaborated with the development team to design, implement, and optimize interactive VR experiences

2024/09 – present
Lahore, Punjab,, Pakistan

UET Lahore -Teaching Assistant (Microprocessor System EE-273L)
Assisting in the Microprocessor Systems Lab (EE-273L) under **Shehzeen Malik**, I guide students in using Tiva C microcontroller boards for embedded systems projects. My responsibilities include preparing lab manuals, supporting students during lab sessions, and assisting with evaluations.

2023/09 – 2024/01
Lahore, Punjab, Pakistan

UET Lahore -Teaching Assistant (Introduction To Computing And Data Science EE-132L)
Assisted **Dr. Muzamal Rafique** in delivering course content, facilitating lab sessions, and guiding students through programming fundamentals and data science principles. Developed instructional materials and provided individualized support to enhance student's understanding and application of course concepts.

2023/03 – 2023/07
Lahore, Punjab, Pakistan

UET Lahore -Teaching Assistant (Programming Fundamentals EE-133L)
Collaborated with **Dr. Suleman Sami Qazi** to facilitate course delivery, manage lab sessions, and assist students with programming assignments. Played a key role in creating supportive learning environments and enhancing students comprehension of fundamental programming concepts.

Education

2021/11 – present

Bs Electrical Engineering
University of Engineering and Technology, Lahore
GPA: 3.596/4.0
Courses: Microprocessor System (EE-273), Digital Systems (EE-272), Computer Architecture (EE-475), Introduction to Computing and Data Science (EE-132), Programming Fundamentals (EE-133), Data Structure and Algorithms (EE-234), Introduction to Machine Learning (EE-439), Discrete Mathematics (EE-233), Calculus (MA-123), Multivariate Calculus (MA-224), Ordinary differential equations (MA-229), Linear Algebra (MA-234), Applied Probability (EE-302).

2019/09 – 2021/07

Fsc Pre Engineering
Government College University , Lahore
Marks : 1050/1100

2009/01 – 2019/02

Matriculation
Allied School
Marks: 1050/1100

Research Work

"Accelerating Computer Architecture Simulation through Machine Learning", **Wajid Ali,** Ayaz Akram, The 1st Workshop on Computer Architecture Modeling and Simulation (CAMS 2023), associated with MICRO(one of the top Computer Architecture Conference), October 2023.

W. Ali, "Exploring Instruction Set Architectural Variations: x86, ARM, and RISC-V in Compute-Intensive Applications", Eng OA (Engineering Open Access), vol. 1, no. 3, pp. 157-162, Oct. 2023.

W. Ali, M. Zia, U. Kamal, and A. Azhar, "Virtual Memory Verification - SV32", IEEE ELEKTRON UET Lahore, 2023.

Projects

Accelerating Computer Architecture Simulation through Machine Learning
Led a project at the intersection of computer architecture and machine learning, aiming to accelerate simulation processes by integrating gem5 with predictive models. Achieved remarkable results in predicting application performance, particularly "instructions per cycle" (IPC), utilizing Random Forest algorithms and insightful feature analysis.

Backend Synthesis and Implementation of UETRV-PCORE
Led the backend synthesis and implementation of UETRV-PCORE, utilizing TSMC libraries designed for 22nm technology. Initially, simplified the flow on a 45nm general PDK, carefully removing all combinational loops. Currently, actively involved in optimizing floor planning, placement, and routing stages using Cadence tools, ensuring smooth integration and efficient utilization of the 22nm technology.

Privilege Architecture Verification of CVA6 (RISC-V)
Authored compliance tests for RISC-V SV32 virtual memory, ensuring accurate functionality and adherence to the RISC-V specification. Conducted a detailed comparison of the virtual memory implementation on the CVA6 core with the golden RISC-V model. Generated a comprehensive compliance report for the CVA6 RISC-V implementation.

RTL to GDS Flow
Worked on the RTL to GDS flow using OpenLane to produce a GDS from the RTL of the UETRV-PCore. This involved writing SDC and configuration files required for the OpenLane flow. Ensured proper optimization of the design for timing, power, and area, leading to successful layout.

UET-RV-PCore Linux Boot Project
Successfully booted Linux on the UETRV-PCORE using OpenSBI v0.9 as the first-level bootloader and Buildroot 2021.05 with Busybox 1.33 for the root file system. Utilized the GNU toolchain riscv32-unknown-linux-gnu and Linux kernel 6.1, integrated into OpenSBI. Achieved reliable OS image transfer via UART.

Linux Booting Automation for UET-RV-PCORE
Implemented a Makefile to automate the Linux booting process on the UET-RV-PCORE platform, enhancing the efficiency and accessibility of the system.

Integrated Pipelined Processor with UART and Privilege Support
Implemented a RISC-V base ISA processor in SystemVerilog, incorporating a pipelined architecture while managing data and control hazards. Added basic CSR support and integrated a UART transmitter and receiver, enabling communication through CSR interrupts. This design enhanced the processor's functionality and communication capabilities.

UART Transmitter
Designed a UART transmitter module using SystemVerilog, implementing the core functionalities of a UART communication protocol. The module efficiently handles data transmission, including start/stop bits and parity bit generation, following industry-standard UART communication practices. This project allowed me to enhance my hardware description language skills and grasp the fundamentals of serial communication protocols.

Spam classifier
Developed a spam classifier by applying various encoding methods to extract features from raw text. Explored different machine learning algorithms, including SVM, Logistic Regression, and Naive Bayes, for spam classification. Successfully implemented a model that achieved a validation accuracy of 99.4%.

Workload Prediction -using gem5 statistics
Developed a workload prediction model using machine learning techniques and gem5 simulation statistics. The objective was to classify workloads as either memory-intensive or computational-intensive based on collected performance metrics.

Created a gesture-controlled car using a TIVA board
Configured and interfaced the TIVA C Series microcontroller with the MPU6050 motion sensor over the I2C protocol to read sensor data. Added WiFi capability using the ESP01 module via UART, utilizing AT commands for communication. Additionally, assembled a model car featuring H-bridge-based independent PWM motor control, allowing precise motor operation and enhanced functionality.

Courses

Computer Architecture (David Wentzlaff)
Princeton University ,NJ

Supervised Machine learning (Andrew Ng)
Stanford University ,CA

Advance learning Algorithms (Andrew Ng)
Stanford University ,CA

Computer vision and Image processing
IBM

Languages

- Urdu
- English
- Chinese

Organizations

2023/07 – 2024/07
Lahore, Pakistan

IET UET Lahore
Head Research
As Head of Research at IET, I actively engage in cutting-edge research on computer architecture simulation, focusing on developing and enhancing the gem5 simulator.

Organized **gem5 Hackathon** at UET Lahore, pioneering a platform for cutting-edge research and development in gem5 technology. The event included participants working with RISC-V instruction set and RISC ISA files in gem5, significantly advancing computer architecture studies in Pakistan.

Organized a comprehensive **SoC design module** as part of IET UET Lahore's flagship event, "Electrokon," fostering practical learning and a deeper understanding of System-on-Chip (SoC) design principles among participants.

2023/08 – 2024/08
Lahore, Pakistan

IEEE UET LAHORE
Co-Chair CS chapter
Fostered technical learning and collaboration among peers by organizing events, workshops, and mentorship programs, enhancing members' academic and professional growth.

Organized and provided technical leadership for the **RISC-V International Hackathon** at UET Lahore, facilitating collaboration and innovation within the realm of open-source instruction set architectures.

Led and organized the **Logic Rumble programming competition**, where participants from all departments of the University of Engineering and Technology competed.

Skills

Programming Languages:
C, C++, Java, MATLAB, Python, Bash, Assembly Programming(x86, ARM, RISCV), Tcl Scripting

Tools:
Xilinx ISE, Xilinx Vivado, ModelSim, Keil, Proteus, Visual Studio, MentorGraphics EDA tools, Cadence (genus, innovus, tempus), OpenLane

Hardware Description Languages:
System Verilog ,Verilog HDL, VHDL

RISCV Verification Tools:
Spike, Sail, RISCOF

Data Science Tools:
TensorFlow, Scikit-learn, Keras, Jupyter Notebooks

Operating Systems:
Linux, Windows

Architectural Simulators and Emulators:
gem5, GPGPU Sim, Accel-Sim, NVBit, Multi2Sim, QEMU, Wireshark

PCB designing
Schematic Design and Capture, PCB Layout Design, Component Placement and Routing, Multi-layer PCB Design, Gerber File Generation

Benchmarks:
SPEC, NPB, GAPBS, MiBench

Libraries:
PyTorch, Pandas, NumPy, sklearn

Version Control & Collaboration Tools:
Git, GitHub

Documentation Tools:
Latex, Microsoft Word