1. Description

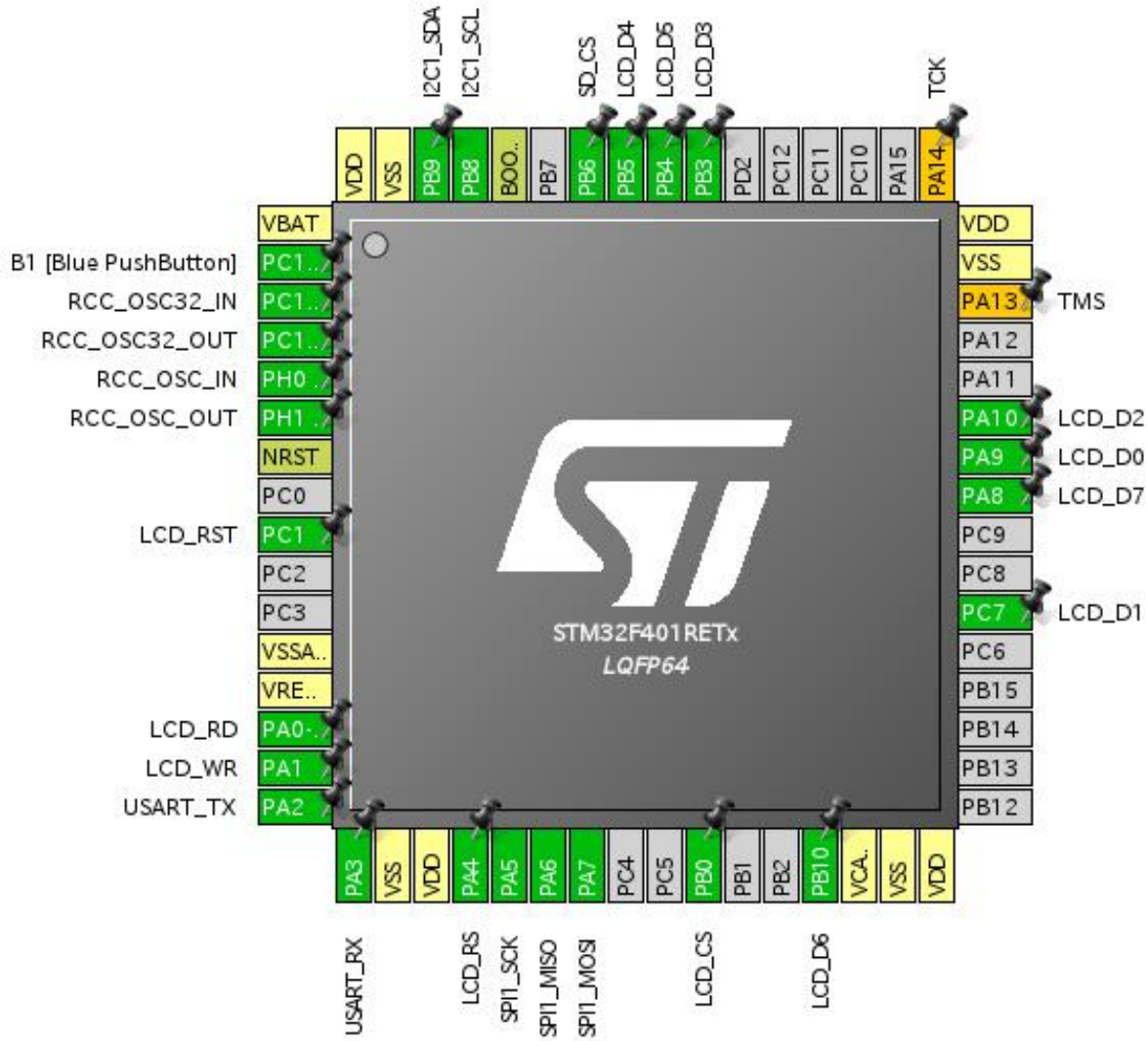
1.1. Project

Project Name	TFTClock_with_Temp
Board Name	NUCLEO-F401RE
Generated with:	STM32CubeMX 4.22.1
Date	11/04/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F401
MCU name	STM32F401RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

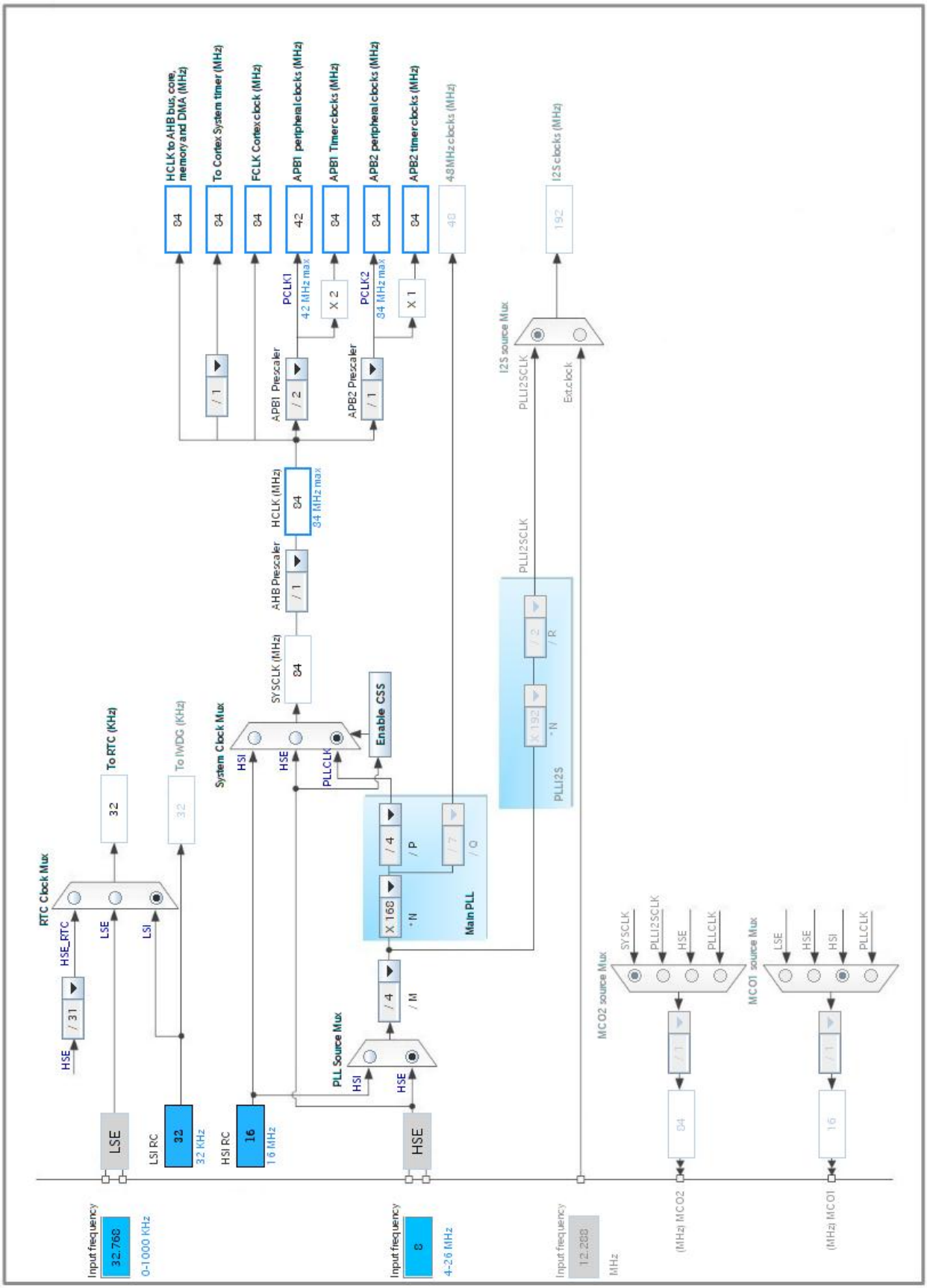
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
9	PC1 *	I/O	GPIO_Output	LCD_RST
12	VSSA/VREF-	Power		
13	VREF+	Power		
14	PA0-WKUP *	I/O	GPIO_Output	LCD_RD
15	PA1 *	I/O	GPIO_Output	LCD_WR
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	LCD_RS
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
26	PB0 *	I/O	GPIO_Output	LCD_CS
29	PB10 *	I/O	GPIO_Output	LCD_D6
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
38	PC7 *	I/O	GPIO_Output	LCD_D1
41	PA8 *	I/O	GPIO_Output	LCD_D7
42	PA9 *	I/O	GPIO_Output	LCD_D0
43	PA10 *	I/O	GPIO_Output	LCD_D2
46	PA13 **	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14 **	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 *	I/O	GPIO_Output	LCD_D3
56	PB4 *	I/O	GPIO_Output	LCD_D5
57	PB5 *	I/O	GPIO_Output	LCD_D4

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
58	PB6 *	I/O	GPIO_Output	SD_CS
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. I2C1

I2C: I2C

5.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	**Fast Mode ***
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : BYPASS Clock Source

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 2

5.3. RTC

mode: Activate Clock Source

mode: Activate Calendar

5.3.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	**17 ***

5.4. SPI1

Mode: Full-Duplex Master

5.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.5. SYS

Timebase Source: SysTick

5.6. TIM1

Clock Source : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	**Division by 4 ***
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.7. TIM2

Clock Source : Internal Clock

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	**Division by 4 ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.8. USART2

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	**No pull-up and no pull-down ***	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	**No pull-up and no pull-down ***	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	*	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	*	Low	USART_RX
Single Mapped Signals	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
GPIO	PC13-ANTI_TAMP	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_RST
	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_RD
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High**	LCD_WR

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_RS
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_CS
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D6
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D1
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D7
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D0
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D2
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D3
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D5
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	LCD_D4
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	SD_CS

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA2_Stream0	Peripheral To Memory	**High ***
SPI1_TX	DMA2_Stream3	Memory To Peripheral	**High ***
USART2_TX	DMA1_Stream6	Memory To Peripheral	**Medium ***
I2C1_RX	DMA1_Stream0	Peripheral To Memory	**Medium ***
I2C1_TX	DMA1_Stream7	Memory To Peripheral	**Medium ***

SPI1_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_RX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
I2C1 event interrupt	true	0	0
I2C1 error interrupt	true	0	0
SPI1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream3 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F401
MCU	STM32F401RETx
Datasheet	025644_Rev3

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	TFTClock_with_Temp
Project Folder	/home/evaota/STM32Cube/TFTClock_with_Temp
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No