TurboConcept

TC4200_enc WiMAX Low Density Parity Check Encoder v1.0
Datasheet
SoCLib

Revision 1
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TC4200 and TC4200_enc are products of TurboConcept SAS, 40 rue Joseph Fourier, 29280 PLOUZANE, FRANCE.

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DOCUMENT REVISION HISTORY

Date	Revision	Modifications
Oct 2008	1	Initial release

PRODUCT VERSIONS

Date	Version	Description
01/2008	v1.0	

BUG HISTORY

N°	Identified in version	Description	Fixed in version

Introduction

TurboConcept's TC4200_enc is a high speed Low Density Parity Check code (LDPC) encoder compliant with the IEEE 802.16e specifications used for WiMAX systems. The Core is a stand-alone module, with no external memory needs. It is available for mainstream FPGA or ASIC device targets. The Core covers the entire WiMAX LDPC specifications [1], in terms of block size and code rate. Block size and code rate can be switched on a block-by-block basis.

This document gives the functional and interfacing specifications. Actual device resource usages are provided in the device-dependant companion documentations.

1 General description

1.1 Functional overview

The Core is compliant with the LDPC code specification given in 802.16e documentation [1] section 8.4.9.2.5 ("Low Density Parity Check code (optional)").

The detailed specification of the encoding process can be found in this reference documentation and is not recalled here.

TC4200_enc performs the corresponding LDPC encoding. Figure 1 displays the functional block diagram of the Core.
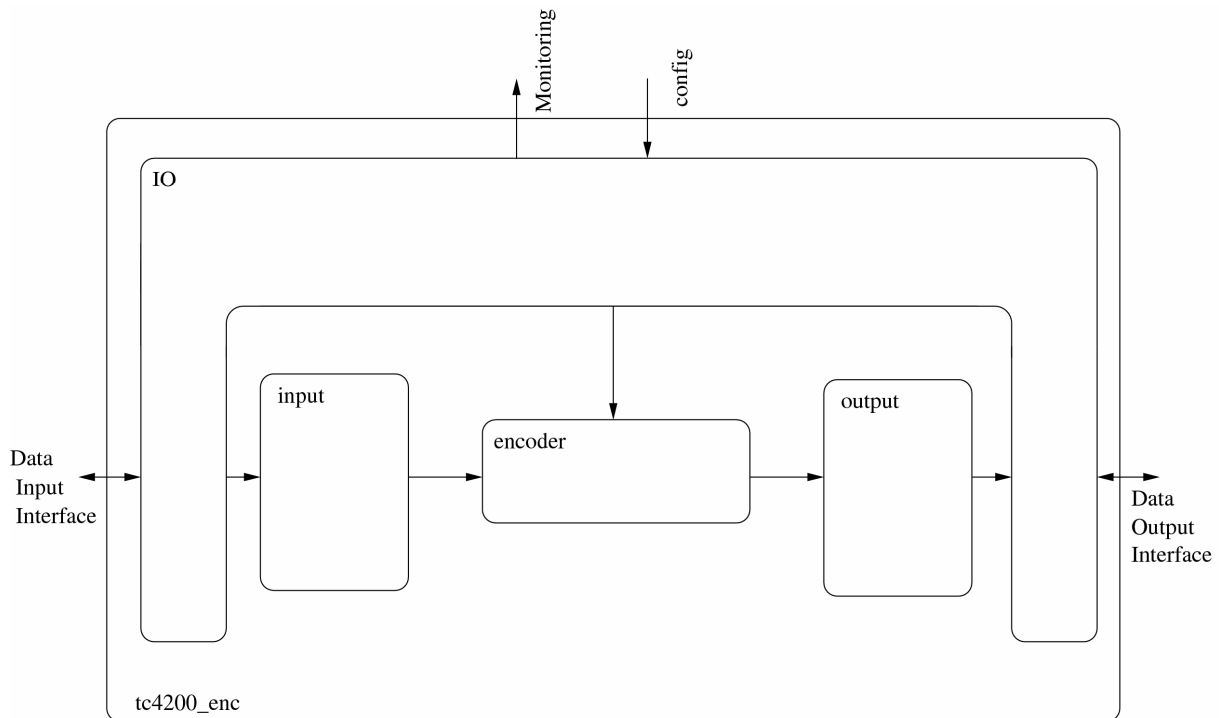
Figure 1: Functional block diagram

The Data Input Interface is used to give to the Core the k payload bits of the current frame to encode.

The Data Output Interface gives the encoding result, in the form of k systematic payload bits concatenated with n-k redundancy bits.

The Core is monitored and controlled through dedicated configuration pins.

The following Control facilities are available:
- WiMAX LDPC coding matrix
- Block size

These settings can be changed dynamically for each frame. TC4200_enc can therefore be easily implemented in an adaptive modulation and coding system.

The following Monitoring facility is available:
- An IDLE signal for the entire core. This signal can be used for power reduction management.

1.2 Codes supported

Table 1 gives the rates and block sizes supported. The Core covers the complete set of cases defined in [1]. Please refer to [1] for details on the "expansion factor".

Expansion factor	Coded Block size n (bits)	LDPC code rates
24	576	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
28	672	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
32	768	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
36	864	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
40	960	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
44	1056	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
48	1152	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
52	1248	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
56	1344	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
60	1440	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
64	1536	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
68	1632	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
72	1728	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
76	1824	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
80	1920	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
84	2016	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
88	2112	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
92	2208	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
96	2304	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6

Table 1: Frame size and code rate supported

2 Detailed description

2.1 Block Diagram
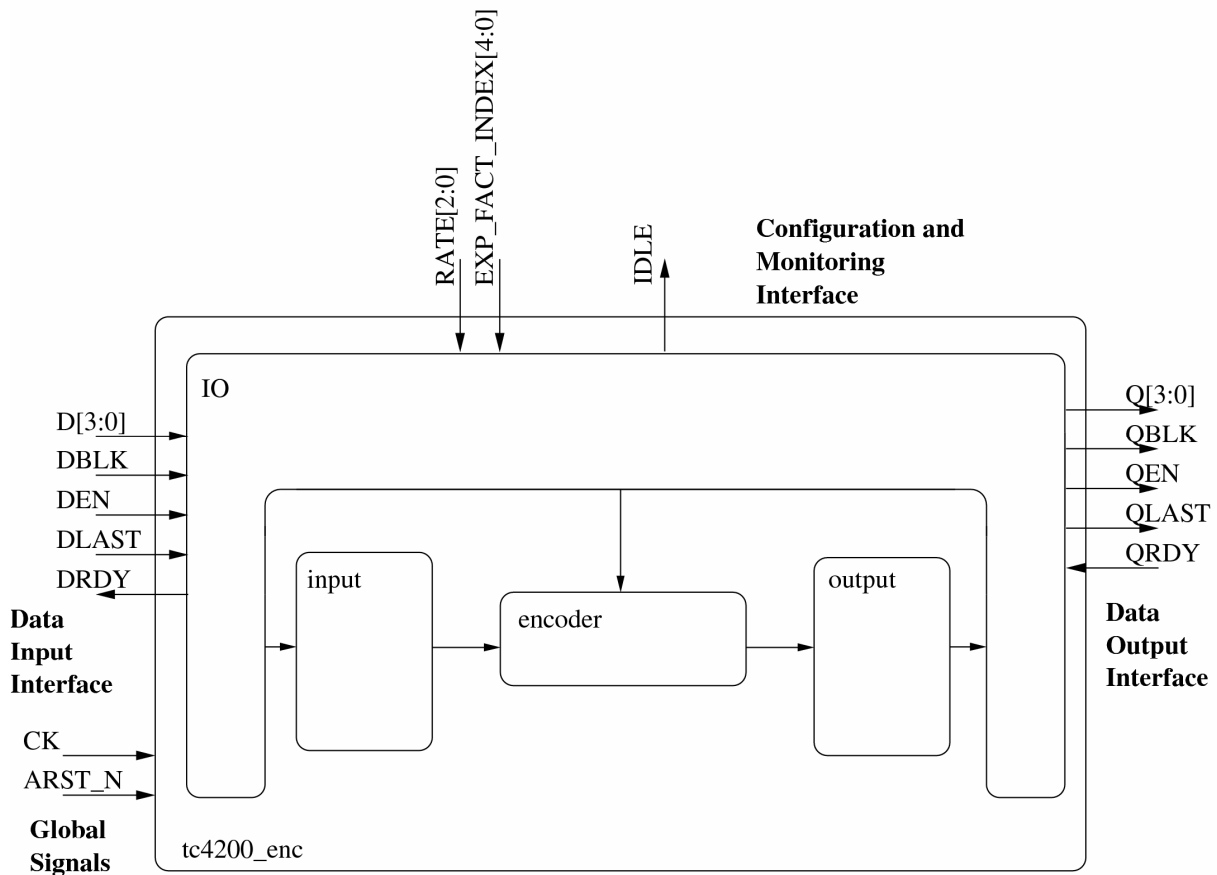
Figure 2: TC4200_enc block diagram

TC4200_enc is composed of the following modules:
- An input module handling the input interface using 4 systematic bits in parallel
- An encoder module
- An output module handling a 4 bit parallel output interface
- A I/O and configuration module, handling the configuration and interfacing the TC4200_enc core with the external world

2.2 Congestion control

Two signals are used to control the block processing and to avoid congestion:
- QRDY (Core input signal) asserted HIGH indicates to the Core that a block can be output from the Core.
- DRDY (Core output signal) asserted HIGH indicates that the Core is ready to receive a block.

The Core encodes frames on a block per block basis. Figure 3 shows the dependency between QRDY and DRDY assertions. DRDY is asserted HIGH once QRDY has been asserted HIGH (A). DRDY is asserted LOW during a frame encoding. DRDY will be asserted HIGH after QRDY is reasserted HIGH (B or C).

C

QRDY

DRDY

A

B

encoding   Blk$_0$ Blk$_1$

Figure 3: Congestion control

3 Interfaces and I/Os

This section details the I/Os pins and the interfaces protocols.

3.1 Global signals

Signal name	Type	Size	Function
CK	I	1	Core clock. Please refer to the applicable application note for maximum operating frequency
ARST_N	I	1	Asynchronous Hardware reset. Active LOW.

Table 2: Global signals

3.2 Data input interface

3.2.1 Signals

All signals are considered at rising edge of the clock CK.

Signal name	Type	Size	Function
D	I	4	Input bits (each sample carries 4 bits). Format is described in section 3.2.2
DBLK	I	1	Block start strobe. Active HIGH. Indicates a new block
DEN	I	1	Enable signal for symbols D Active HIGH
DLAST	I	1	Last data strobe: Active HIGH Activated synchronously with the current input block last data.
DRDY	O	1	Ready for block input start. Active HIGH. DRDY=HIGH indicates that the Core can accept a new block input. DBLK is ignored if DRDY=LOW. DRDY is asserted LOW two clock cycles after a valid strobe on DBLK. DRDY goes high a few clock cycles after a reset operation.

Table 3: Input interface signals

3.2.2 Data size and format

Let denote by c_i the emitted code word bits, with i in [0, n-1]. $c_0, …, c_{k-1}$ are the systematic part of the code word; $c_k, …, c_{n-1}$ are the redundancy part.
The input data signal D carries a set of 4 bits c_i i in [0, $k – 1$], according to the correspondence given Table 4.
The number of D-samples is denoted p.
p=k/4 (k is always an exact multiple of 4)

symbol index	D[3]	D[2]	D[1]	D[0]
0	c_0	c_1	c_2	c_3
1	c_4	c_5	c_6	c_7
..				
j	c_{4j}	c_{4j+1}	c_{4j+2}	c_{4j+3}
…				
p - 1	c_{k-4}	c_{k-3}	c_{k-2}	c_{k-1}

Table 4: Mapping of systematic bits c_j into signal D

3.2.3 Waveform examples

Figure 4 gives a waveform example of the input interface signals. The input samples are denoted D_0 to D_{p-1}.

The signal DRDY falls as indicated, two cycles after the strobe on DBLK. It rises again after the input data block has been encoded and provided by the Core as explain in section 2.2.
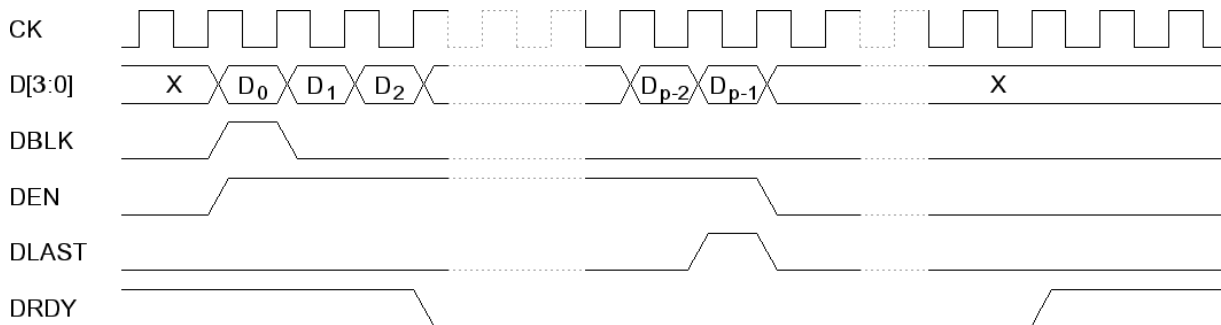

Figure 4: Input interface waveform example

Note that any pattern on DEN is accepted (only the trivial case where no idle cycle is shown in the figure for simplicity).
Any additional "high" value on signal DBLK occurring between the valid pulse and the following DRDY rising is ignored.

3.3 Data output interface

3.3.1 Signals

Signal name	Type	Size	Function
Q	O	4	Encoded bits – each sample carries 4 bits. Format is described in section 3.3.2
QBLK	O	1	Block synchronization signal. Active HIGH. QBLK is asserted HIGH synchronously with the first valid decoded data.
QEN	O	1	Enable for Q Active HIGH
QLAST	O	1	End of block synchronization signal. Active HIGH. QLAST is asserted HIGH synchronously with the last decoded data.
QRDY	I	1	Ready for output signal. Active HIGH. HIGH indicates that a data can be output. QRDY and DRDY are linked as described in section 2.2. Tie HIGH if not used.

Table 5: Output interface signals

3.3.2 Data size and format

The output data signal Q carries a set of 4 bits c_i , i in [0, n-1], according to the correspondence given in Table 6.
The number of Q-samples is denoted q.
q=n/4 (n is always an exact multiple of 4)

symbol index	Q[3]	Q[2]	Q[1]	Q[0]
0	c_0	c_1	c_2	c_3
1	c_4	c_5	c_6	c_7
..				
j	c_{4j}	c_{4j+1}	c_{4j+2}	c_{4j+3}
…				
p - 1	c_{k-4}	c_{k-3}	c_{k-2}	c_{k-1}
p	c_k	c_{k+1}	c_{k+2}	c_{k+3}
…				
q -1	c_{n-4}	c_{n-3}	c_{n-2}	c_{n-1}

Table 6: Output data order

Note that the first p samples on Q are equal to the p samples on D, the code being systematic.

3.3.3 Waveform examples

Figure 5 displays the general waveform for the output interface. Due to the dataflow mode, QEN will mimic the DEN signal after a latency of L_{sys} clock cycles for the systematic part. This means that any idle cycle on the input interface will be reproduced identically after L_{sys} cycles on the output.
The redundancy bits are output in a burst of q-p clock cycles with no idle cycle between first and last redundancy symbols.
Once an assertion to HIGH has been set to the QRDY signal, the Core is available for encoding a new frame as shown with the DRDY assertion to HIGH. A DBLK assertion to HIGH begins an encoding process: 2 clock cycles later, the DRDY signal falls to LOW and L_{sys} clock cycles later, a QBLK assertion to HIGH indicates a first systematic data.

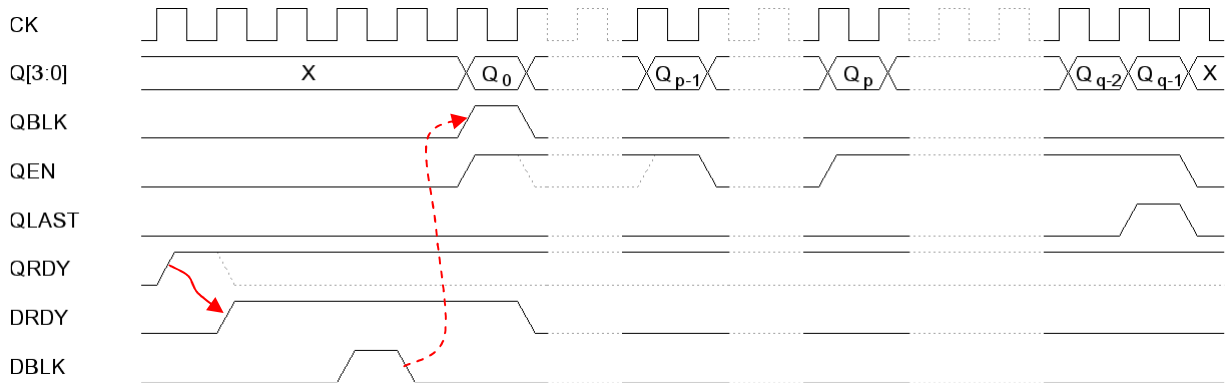QEN is LOW for L_{red} clock cycles before a first redundancy sample.

Figure 5: Output interface waveform example

3.4 Data Sequence

This section summarizes through an example what the input and output data sequences are.
Section 3.2.2 (resp. section 3.3.2) describes the data format for input (resp. output) interface. Notations used in these sections also apply in this section.

Example
Let us consider the LDPC code for the rate ¾ A code with an expansion factor equal to 60. 1440 coded bits are emitted and 1080 systematic bits are provided as input: 1080 bits are user payload bits, 360 bits are redundancy bits.

The input word is

$$c_0\ c_1\ \dots\ c_{1078}\ c_{1079}$$

Then, the input sequence shall be:
D: $D_0\ (c_0c_1c_2c_3)\ D_1\ (c_4c_5c_6c_7)\ \dots\ D_{269}\ (c_{1076}c_{1077}c_{1078}c_{1079})$
And the output sequence will be (user payload bits followed by redundancy bits):
Q: $Q_0\ (c_0c_1c_2c_3)$ $Q_1\ (c_4c_5c_6c_7)$ … $Q_{269}\ (c_{1076}c_{1077}c_{1078}c_{1079})$ $Q_{270}\ (c_{1080}c_{1081}c_{1082}c_{1083})$ … $Q_{359}\ (c_{1436}c_{1437}c_{1438}c_{1439})$

symbol index	D[3]	D[2]	D[1]	D[0]
0	c_0	c_1	c_2	c_3
1	c_4	c_5	c_6	c_7
..				
i	c_{4i+3}	c_{4i+2}	c_{4i+1}	c_{4i}
…				
269	c_{1076}	c_{1077}	c_{1078}	c_{1079}

Table 7: input sequence for rate ¾, 1440 coded bits

symbol index	Q[3]	Q[2]	Q[1]	Q[0]
0	c_0	c_1	c_2	c_3
1	c_4	c_5	c_6	c_7
..				
i	c_{4i+3}	c_{4i+2}	c_{4i+1}	c_{4i}
…				
269	c_{1076}	c_{1077}	c_{1078}	c_{1079}
…				
359	c_{1436}	c_{1437}	c_{1438}	c_{1439}

Table 8: output sequence for rate ¾, 1440 coded bits

3.5 Configuration and monitoring interface

The configuration and monitoring interface is made of 3 (2 for configurations, 1 for monitoring) dedicated signals.

3.5.1 Signals

Signal name	Type	Size	Function
RATE	I	3	Rate signal: "000" for rate = 1/2 "010" for rate = 2/3 A "011" for rate = 2/3 B "100" for rate = 3/4 A "101" for rate = 3/4 B "110" for rate = 5/6
EXP_FACT_INDEX	I	5	Index for expansion factor. Unsigned value Range from 0 to 18 The actual expansion factor is 24 + 4*EXP_FACT_INDEX

Table 9: Configuration interface signals

Signal name	Type	Size	Function
IDLE	O	1	Flag: - 1: the core is idle - 0: the core is busy This flag might be useful for power management

Table 10: Monitoring interface signals

Table 11 provides the actual correspondence between the EXP_FACT_INDEX configuration signal and the expansion factor and the coded block size in bits.

EXP_FACT_INDEX	Expansion factor	Coded block size n (bits)
0	24	576
1	28	672
2	32	768
3	36	864
4	40	960
5	44	1056
6	48	1152
7	52	1248
8	56	1344
9	60	1440
10	64	1536
11	68	1632
12	72	1728
13	76	1824
14	80	1920
15	84	2016
16	88	2112
17	92	2208
18	96	2304

Table 11: Expansion factor and index correspondence

3.5.2 Protocol

The configuration is registered synchronously with a valid DBLK flag. Figure 6 illustrates the configuration protocol. R_0, Ef_0 (resp. R_1, Ef_1) are linked to block #0 (resp. block #1)
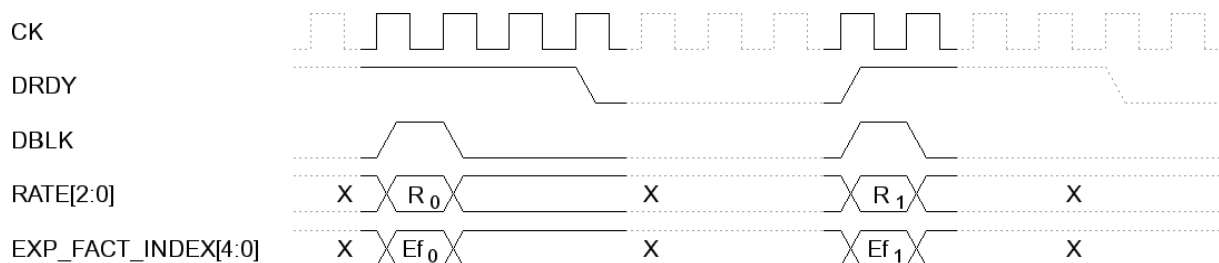

Figure 6: Configuration waveform

References

[1] IEEE Std 802.16e-2005 and IEEE std 802.16-2004/Cor1-2005 "PART 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems – Amendment 2: Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Bands – Corrigendum 1" IEEE Computer Society and IEEE Microwave Theory and Techniques Society, Feb.

[2] TC4200_enc_an1_Xilinx_implementations or TC4200_enc_an2_Altera_implementations

[3] TC4200_enc_an4_ASIC_implementation_figures