
STM32
CubeMX

02/01/2026

1. Description

1.1. Project

Project Name	Lora_RX_gemini
Board Name	custom
Generated with:	STM32CubeMX 6.16.1
Date	01/02/2026

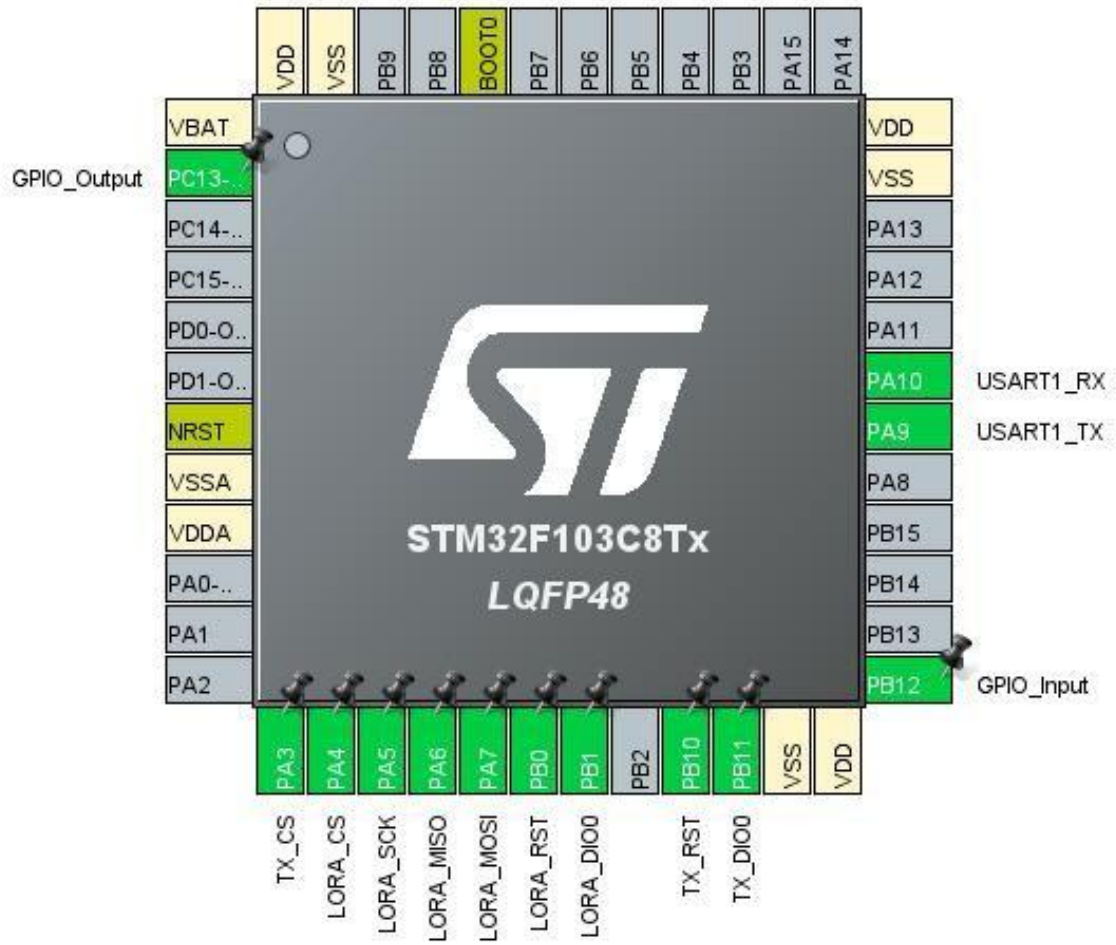
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration



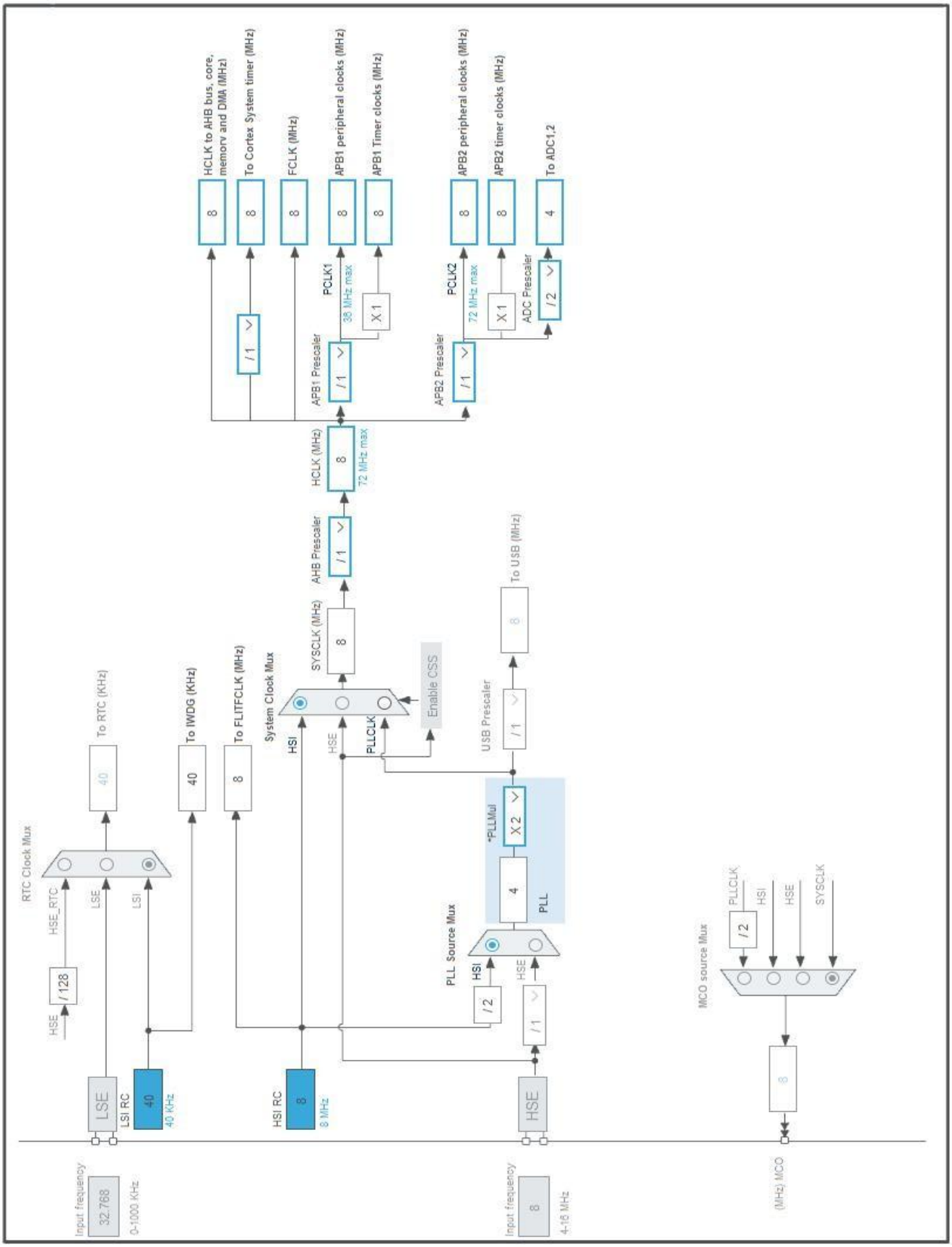
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
13	PA3 *	I/O	GPIO_Output	TX_CS
14	PA4 *	I/O	GPIO_Output	LORA_CS
15	PA5	I/O	SPI1_SCK	LORA_SCK
16	PA6	I/O	SPI1_MISO	LORA_MISO
17	PA7	I/O	SPI1_MOSI	LORA_MOSI
18	PB0 *	I/O	GPIO_Output	LORA_RST
19	PB1	I/O	GPIO_EXTI1	LORA_DIO0
21	PB10 *	I/O	GPIO_Output	TX_RST
22	PB11	I/O	GPIO_EXTI11	TX_DIO0
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Input	
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
35	VSS	Power		
36	VDD	Power		

44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	DS5319_Rev17

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

1.4. Sequence

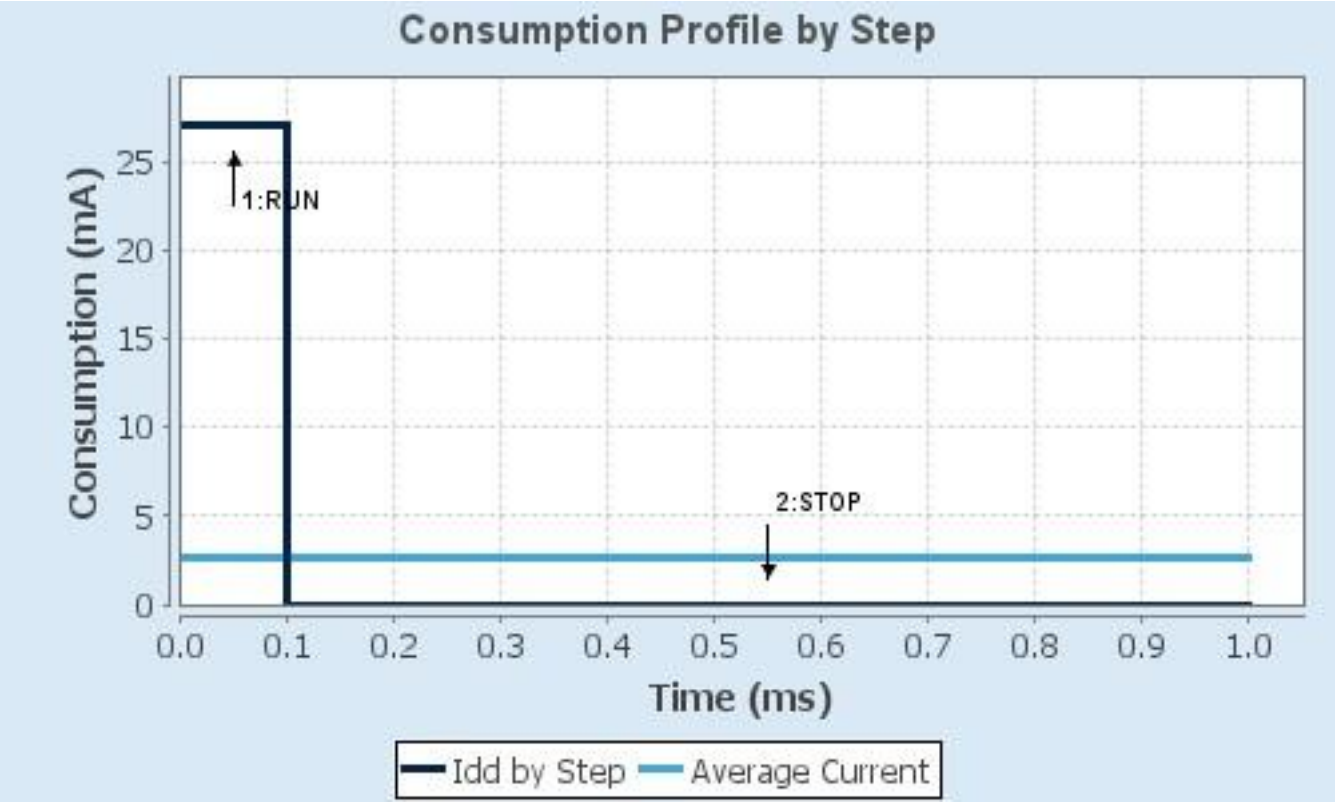
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale

Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days, 17 hours	Average DMIPS	61.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	Lora_RX_gemini
Project Folder	C:\Users\...\stm32\Lora_RX_gemini
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.6
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_SPI1_Init	SPI1
4	MX_USART1_UART_Init	USART1
5	MX_ADC1_Init	ADC1
6	MX_IWDG_Init	IWDG

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: Vrefint

Channel 3.1.1.

Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
____	Channel Vrefint
Channel	**239.5 Cycles ***
Sampling Time	
ADC_Injected_ConversionMode:	Disable
Enable Injected Conversions	
WatchDog:	false
Enable Analog WatchDog Mode	

3.2. IWDG

mode: Activated

3.2.1. Parameter Settings:

Clocking:	
IWDG counter clock prescaler	**64 ***
IWDG down-counter reload value	4095

3.3. RCC

3.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

3.4. SPI1

Mode: Full-Duplex Master

3.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**256 ***
Baud Rate	**31.25 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

3.5. SYS

Debug: No Debug

Timebase Source: SysTick

3.6. USART1

Mode: Asynchronous

3.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None

Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	n/a	**High ***	LORA_SCK
	PA6	SPI1_MISO	Input mode	No pull-up and no pull-down	**n/a**	LORA_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	n/a	**High ***	LORA_MOSI
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	TX_CS
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	LORA_CS
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_RST
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LORA_DIO0
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TX_RST
	PB11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	TX_DIO0
	PB12	GPIO_Input	Input mode	**Pull-up ***	n/a	

4.2. DMA configuration nothing

configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0

Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI line1 interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
EXTI line[15:10] interrupts	unused		

4.3.2. NVIC Code generation

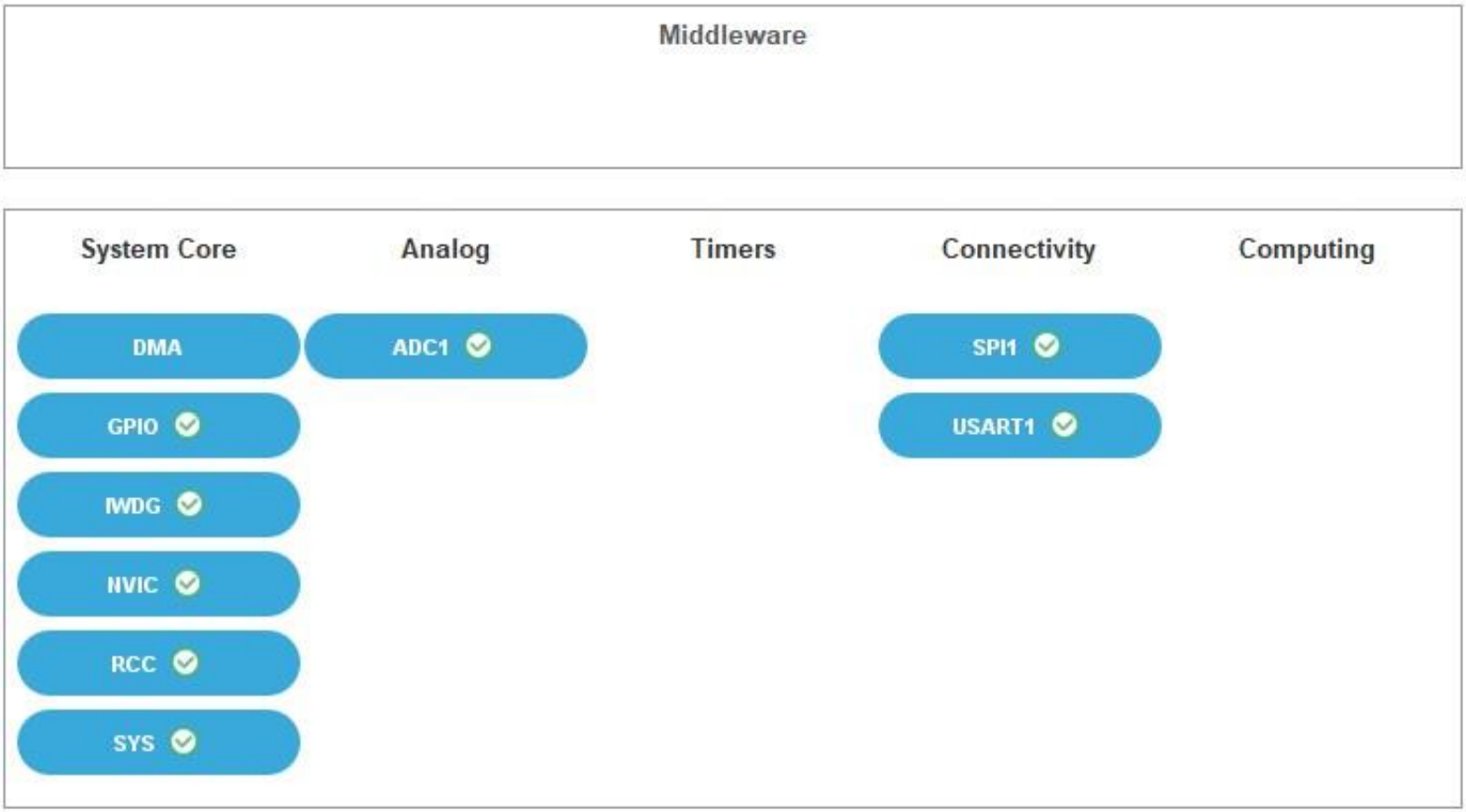
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line1 interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f1_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f1-ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f1_svd.zip
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