Logic Desing Lab I (BCD Counter)

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BCD Counter

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Introduction

In this lab, the objective was to design and implement a BCD (Binary Coded Decimal) counter from scratch using basic digital building blocks such as AND, OR, and NOT gates along with D flip-flops.

The counter should count from 0000 (0) to 1001 (9) and then reset back to 0000.

Tools

Software: Intel® Quartus® Prime (Lite Edition)

Target Device: Cyclone V Family — Device: 5CGXFC7C7F23C8

The Quartus tool was used to draw the schematic, simulate the design, and prepare it for FPGA implementation.

Design

Truth Table

Q3	Q2	Q1	Q0	Q3(T+1)	Q2(T+1)	Q1(T+1)	Q0(T+1)
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

D0 K-Map

Q3 Q2	0 0	0 1	1 1	1 0
Q1 Q0 0 0	1	1	X	1
0 1	0	0	X	0
1 1	0	0	X	X
1 0	1	1	X	X

Q0(T+1) = Q0'

D1 K-Map

Q3 Q2	0 0	0 1	1 1	1 0
Q1 Q0 0 0	0	0	X	0
0 1	1	1	X	0
1 1	0	0	X	X
1 0	1	1	X	X

Q1(T+1) = Q3' Q1' Q0 + Q1 Q0'

D2 K-Map

Q3 Q2	0 0	0 1	1 1	1 0
Q1 Q0 0 0	0	1	X	0
0 1	0	1	X	0
1 1	1	0	X	X
1 0	0	1	X	X

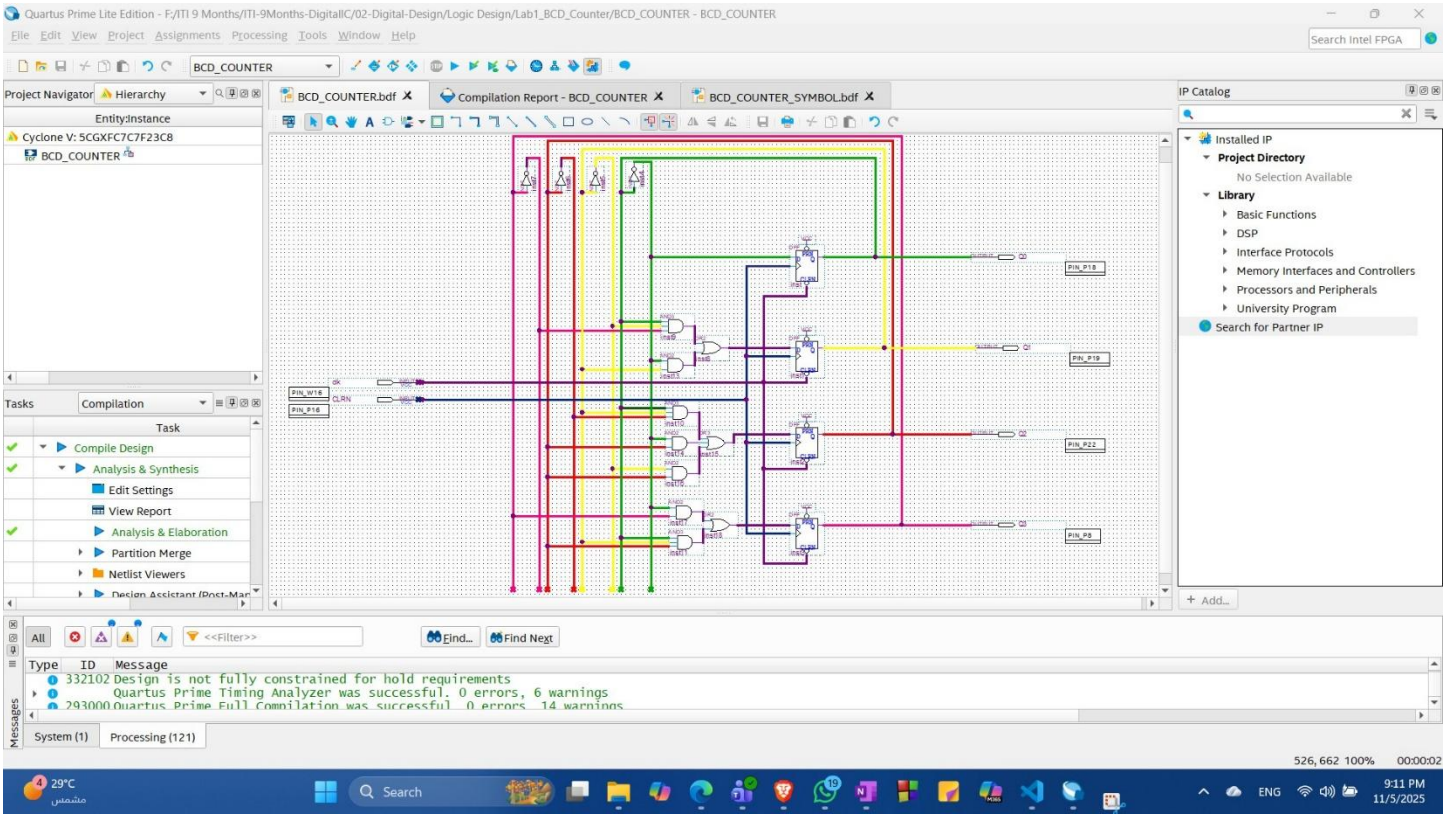
Q2(T+1) = Q2'Q1Q0 + Q2Q0' + Q2Q1'

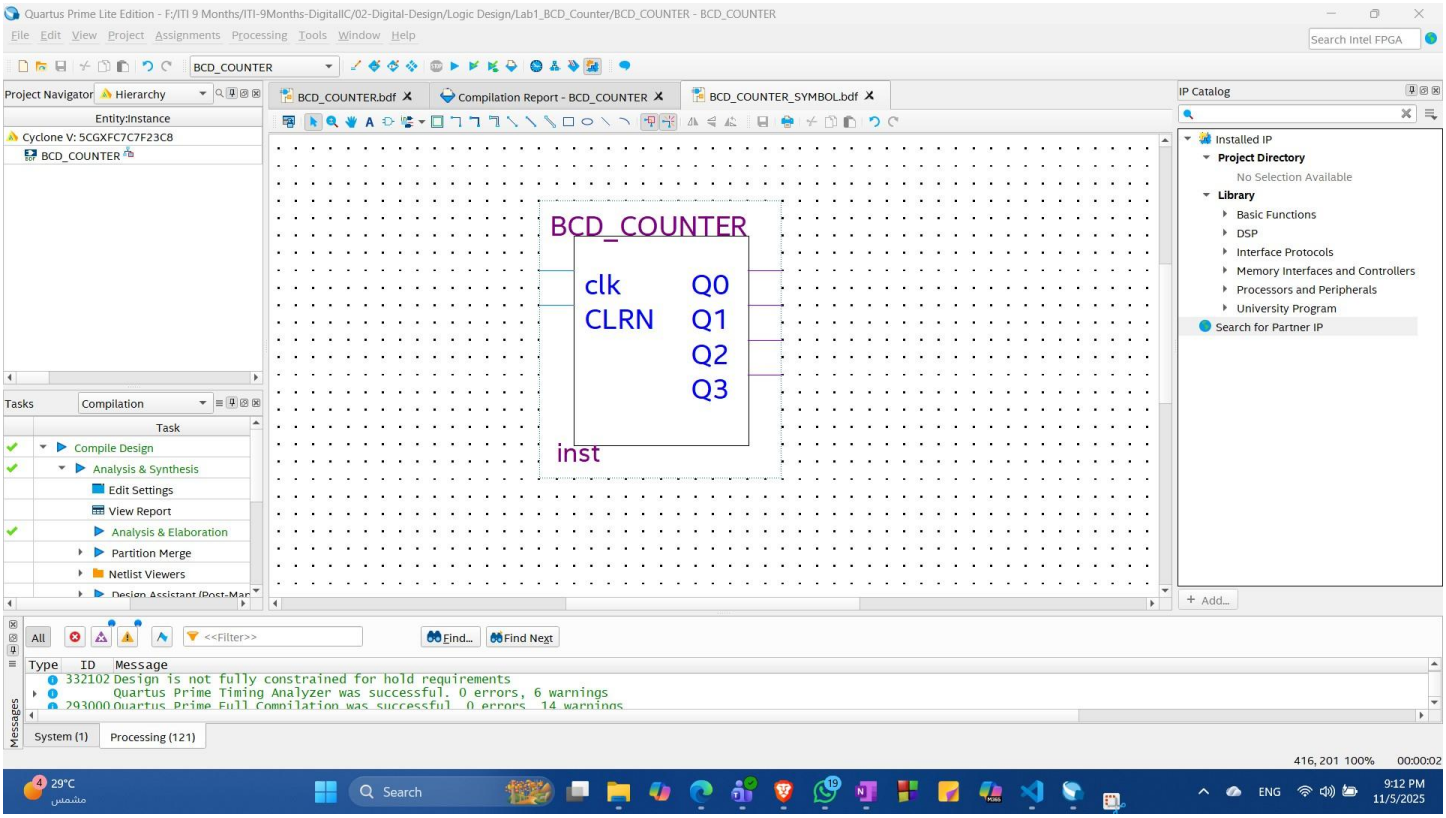
D3 K-Map

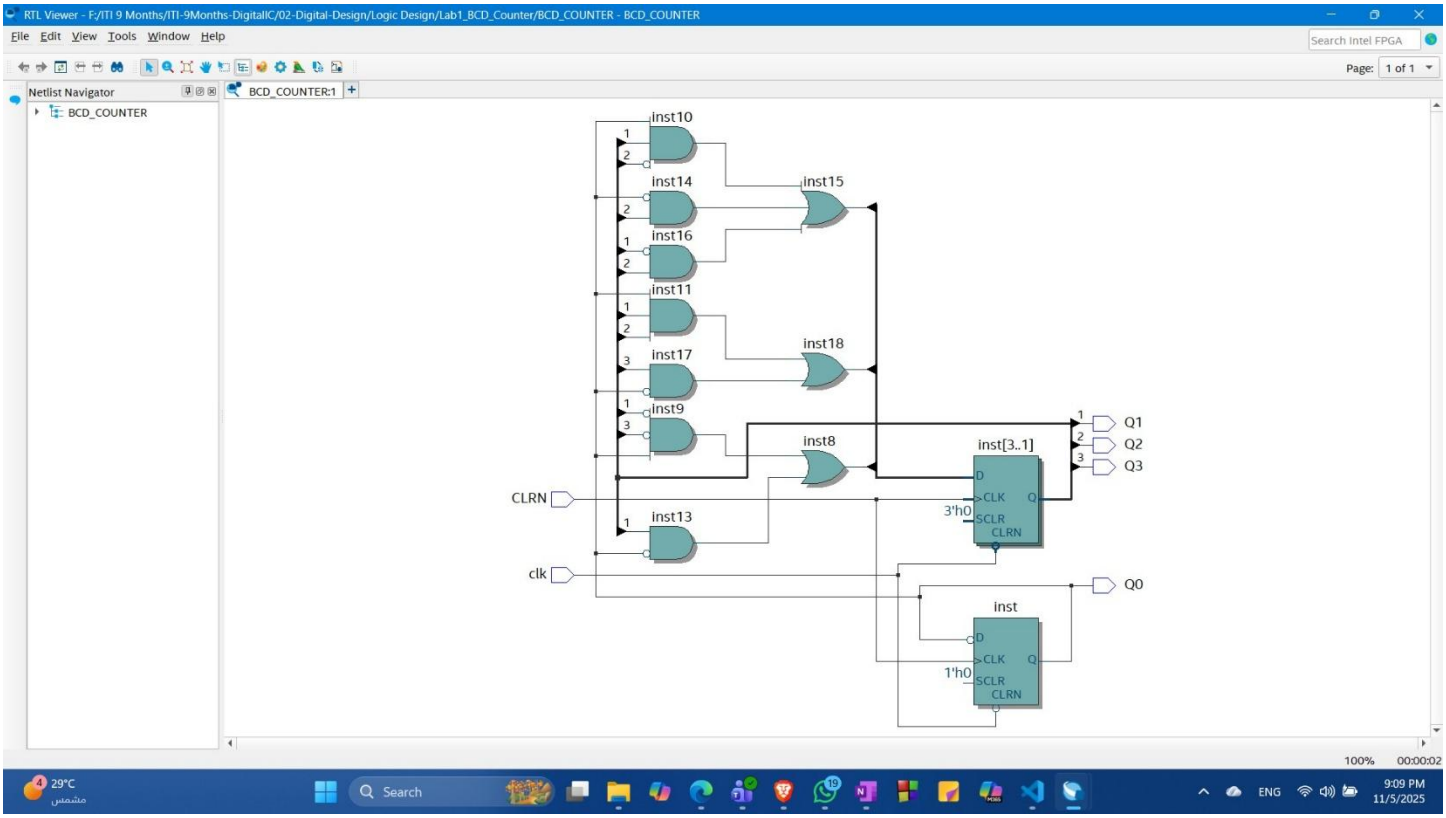
Q3 Q2	0 0	0 1	1 1	1 0
Q1 Q0 0 0	0	0	X	1
0 1	0	0	X	0
1 1	0	1	X	X
1 0	0	0	X	X

Q3(T+1) = Q3 Q0' + Q2Q1Q0

Implementation







Conclusion

The design has been implemented but not tested, next lab the design will be tested also.