

# Logic Desing Lab I (BCD Counter)

Waleed Emad Zakarya

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BCD Counter

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Dr. Hithem, Eng. El-Gemmal

# Introduction

In this lab, the objective was to design and implement a BCD (Binary Coded Decimal) counter from scratch using basic digital building blocks such as AND, OR, and NOT gates along with D flip-flops.

The counter should count from 0000 (0) to 1001 (9) and then reset back to 0000.

## Tools

Software: Intel® Quartus® Prime (Lite Edition)

Target Device: Cyclone V Family — Device: 5CGXFC7C7F23C8

The Quartus tool was used to draw the schematic, simulate the design, and prepare it for FPGA implementation.

## Design

Truth Table

| Q3 | Q2 | Q1 | Q0 | Q3(T+1) | Q2(T+1) | Q1(T+1) | Q0(T+1) |
|----|----|----|----|---------|---------|---------|---------|
| 0  | 0  | 0  | 0  | 0       | 0       | 0       | 1       |
| 0  | 0  | 0  | 1  | 0       | 0       | 1       | 0       |
| 0  | 0  | 1  | 0  | 0       | 0       | 1       | 1       |
| 0  | 0  | 1  | 1  | 0       | 1       | 0       | 0       |
| 0  | 1  | 0  | 0  | 0       | 1       | 0       | 1       |
| 0  | 1  | 0  | 1  | 0       | 1       | 1       | 0       |
| 0  | 1  | 1  | 0  | 0       | 1       | 1       | 1       |
| 0  | 1  | 1  | 1  | 1       | 0       | 0       | 0       |
| 1  | 0  | 0  | 0  | 1       | 0       | 0       | 1       |
| 1  | 0  | 0  | 1  | 0       | 0       | 0       | 0       |
| 1  | 0  | 1  | 0  | X       | X       | X       | X       |
| 1  | 0  | 1  | 1  | X       | X       | X       | X       |
| 1  | 1  | 0  | 0  | X       | X       | X       | X       |
| 1  | 1  | 0  | 1  | X       | X       | X       | X       |
| 1  | 1  | 1  | 0  | X       | X       | X       | X       |
| 1  | 1  | 1  | 1  | X       | X       | X       | X       |

D0 K-Map

| Q3 Q2     | 0 0 | 0 1 | 1 1 | 1 0 |
|-----------|-----|-----|-----|-----|
| Q1 Q0 0 0 | 1   | 1   | X   | 1   |
| 0 1       | 0   | 0   | X   | 0   |
| 1 1       | 0   | 0   | X   | X   |
| 1 0       | 1   | 1   | X   | X   |

$$Q0(T+1) = Q0'$$

D1 K-Map

| Q3 Q2     | 0 0 | 0 1 | 1 1 | 1 0 |
|-----------|-----|-----|-----|-----|
| Q1 Q0 0 0 | 0   | 0   | X   | 0   |
| 0 1       | 1   | 1   | X   | 0   |
| 1 1       | 0   | 0   | X   | X   |
| 1 0       | 1   | 1   | X   | X   |

$$Q1(T+1) = Q3' Q1' Q0 + Q1 Q0'$$

D2 K-Map

| Q3 Q2     | 0 0 | 0 1 | 1 1 | 1 0 |
|-----------|-----|-----|-----|-----|
| Q1 Q0 0 0 | 0   | 1   | X   | 0   |
| 0 1       | 0   | 1   | X   | 0   |
| 1 1       | 1   | 0   | X   | X   |
| 1 0       | 0   | 1   | X   | X   |

$$Q2(T+1) = Q2' Q1 Q0 + Q2 Q0' + Q2 Q1'$$

D3 K-Map

| Q3 Q2     | 0 0 | 0 1 | 1 1 | 1 0 |
|-----------|-----|-----|-----|-----|
| Q1 Q0 0 0 | 0   | 0   | X   | 1   |
| 0 1       | 0   | 0   | X   | 0   |
| 1 1       | 0   | 1   | X   | X   |
| 1 0       | 0   | 0   | X   | X   |

$$Q3(T+1) = Q3 Q0' + Q2 Q1 Q0$$

# Implementation

Quartus Prime Lite Edition - F:/ITI 9 Months/ITI-9Months-Digital/C02-Digital-Design/Logic Design/Lab1\_BCD\_Counter/BCD\_COUNTER - BCD\_COUNTER

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BCD\_COUNTER

Project Navigator Hierarchy

Entity/Instance

Cyclone V: 5CGXFC7C7F23C8

BCD\_COUNTER

Tasks

Compilation

Task

Compile Design

Analysis & Synthesis

Edit Settings

View Report

Analysis & Elaboration

Partition Merge

Netlist Viewers

Design Assistant / Post-Map

BCD\_COUNTER.bdf

Compilation Report - BCD\_COUNTER

BCD\_COUNTER\_SYMBOL.bdf

IP Catalog

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Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and Controllers

Processors and Peripherals

University Program

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293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings

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526,662 100% 00:00:02

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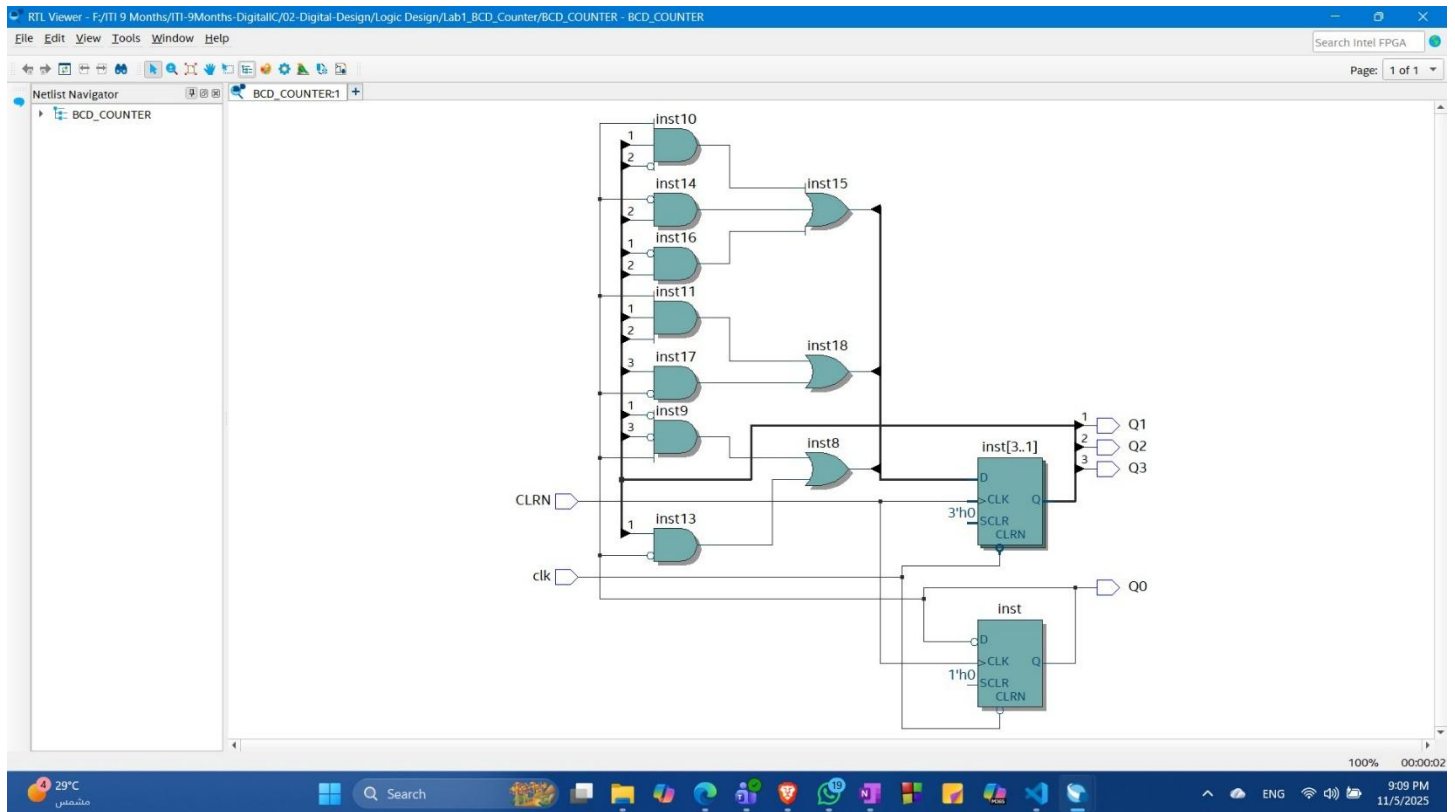
System (1) Processing (121)

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## Conclusion

The design has been implemented but not tested, next lab the design will be tested also.