



# Design of Transceiver Circuits for High-Speed Short-Reach Photonic Links in 65 nm CMOS Technology

By.

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## Thesis

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## Abstract

The need for high-speed data transmission is continuously increasing specially with the recent explosion in artificial intelligence technology, one of the ways to satisfy this need is transmitting data optically over optical fibers which have a very high bandwidth allowing high traffic at very high speeds with little losses and distortion to the data.

The electric data needs to be converted to light at the transmitting end which is done by laser, before the data is converted to light it needs to be conditioned for the conversion and the transmission.

At the receiving end the light needs to be converted to the electrical domain again using a photodiode.

The receiver is responsible for conditioning the weak noisy analog signal coming from the photo diode into a digital signal that can be sensed by following digital systems

This work discusses multiple designs for an analog frontend for optical receivers using different topologies and circuits and modulation techniques to be able to receive high data rates with low power dissipation and high sensitivity.

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## Abbreviations

TIA	Transimpedance Amplifier
NRZ	Non-Return to Zero
PAM-4	4 Level Pulse Amplitude Modulation
ISI	Inter-Symbol Interference
LPF	Low Pass Filter
HPF	High Pass Filter
PSD	Power Spectral Density
AWGN	Additive White Gaussian Noise
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-Channel MOSFET
PMOS	P-Channel MOSFET
CMOS	Complementary MOSFET
NPOLY	N-Polysilicon
P-Poly	P-Polysilicon
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal

# Chapter 1 Fundamentals and Basic Concepts

First, we need to discuss the optical communication system in general and discuss the parameters that affect the performance of the receiver.

## 1.1. Optical communication system

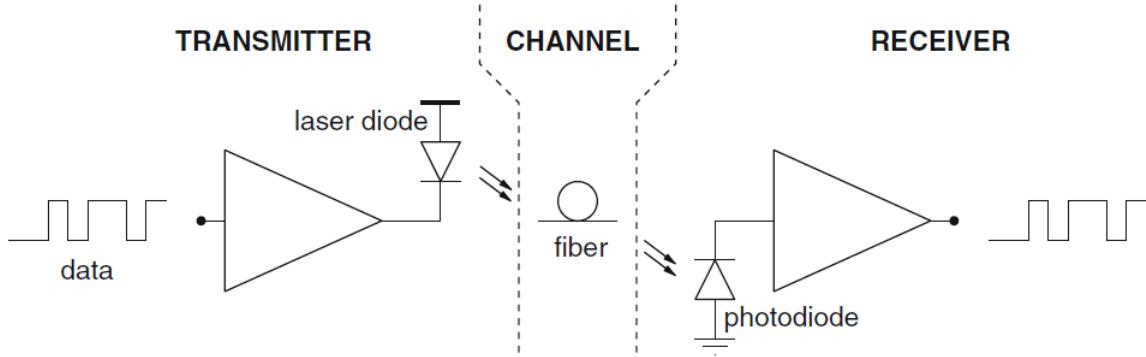


Figure 1.1. Optical communication system. [1]

The optical communication system, like any communication system, consists of a transmitter, channel and receiver.

The transmitter receives the data from the source and condition in it (serialization, modulation... etc.) for transmission.

The main difference in optical transmitter is that it terminated with a laser source which converts the data from electrical domain to light domain to be transmitted over the channel which in the case of optical communication system is an optical fiber which have various types.

Unlike wireline or wireless receiver, the optical receiver receives the signal as an optical signal which needs to be converted again to an electrical signal using a photodiode.

The photodiode is usually on a different chip from the rest of the receiver due to the poor optical properties of traditional silicon used in electronic circuits.

The signal received by the photodiode and then converted to an electrical signal is noisy and attenuated so it needs processing which is the first function of the receiver.

After the signal is processed the data needs to be extracted and clocked again before outputting it to other systems.

## 1.2. The Optical Receiver

There are two main issues with the received data:

1-The current produced by the photodiode has a very low magnitude sensed by any digital system

2-The data is transmitted without a clock hence it is not synchronized

The receiver is responsible for increasing the swing of the data to a sensible logic level and generate a clock proportional to the data and synchronize the data with it

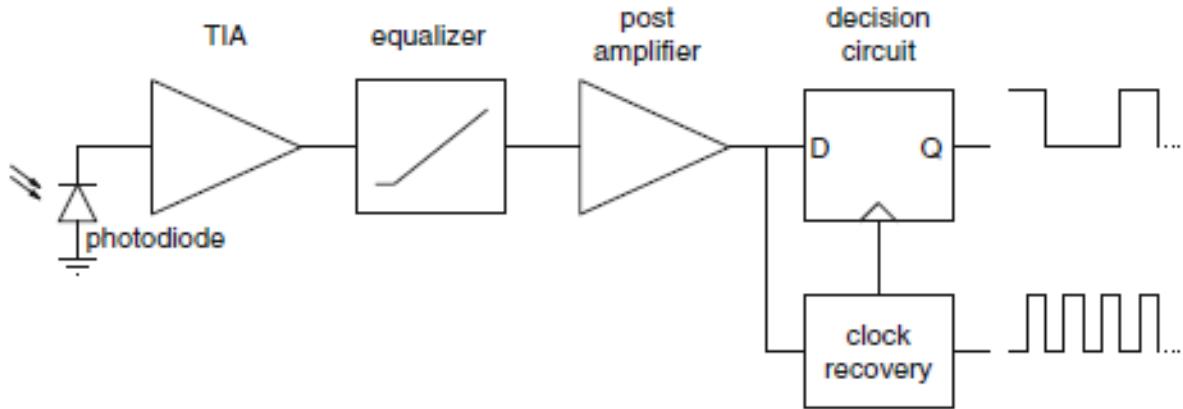


Figure 1.2. Optical receiver. [1]

### 1.2.1. The Photodiode

The photodiode is connected in reverse bias, and it generates a current proportional to the received optical signal.

As the photonic side of the system isn't the main interest of this work, we will suffice with modelling the photo diode with simple electrical elements.

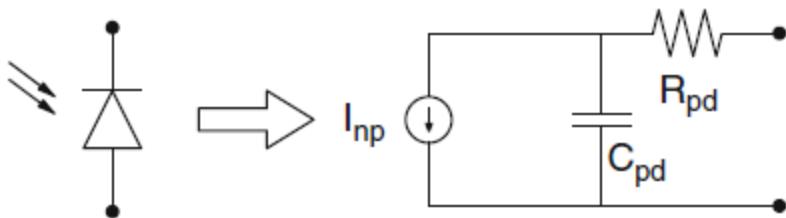


Figure 1.3. Photodiode symbol and its model, [1]

The photodiode can be modelled with a current source representing the current produced by the optical signal, a shunt capacitance representing the junction capacitance and a series resistance representing the ohmic resistance of the diode that can be neglected.

### 1.2.2. The Transimpedance Amplifier (TIA)

The first step needed in the receiver is converting the photodiode current to a voltage, this step is done using transimpedance amplifier which in addition to this function it provides initial amplification to the signal.

### 1.2.3. Equalizer

The high data rates require a proportionally high bandwidth which limits the gain of the total system.

The equalizer helps satisfy the required bandwidth with a sufficient gain to overcome the noise and to amplify the signal to a sensible level for the later digital circuits.

### 1.2.4. Limiting Amplifier

The TIA gain can't be high enough to produce a signal with enough amplitude without compromising the bandwidth.

Another amplification stage is needed to provide a sensible logical level and boost the signal swing

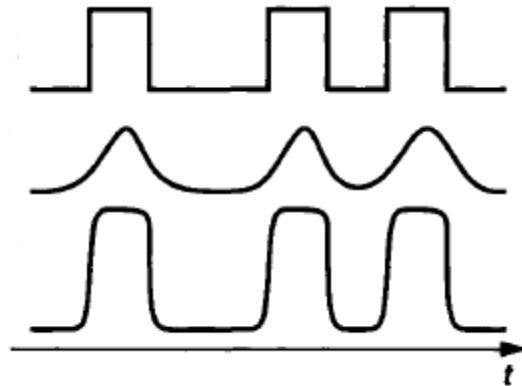


Figure 1.4 From top to bottom: The photodiode current, the usual TIA output voltage, and the desired limiting amplifier output. [2]

### 1.2.5. Decision Circuit and Clock Recovery

The output of the limiting amplifier needs to go through a decision circuit that compares it to a threshold to decide the logical levels.

The data needs a clock proportional to it to drive it which is generated by the clock recovery unit.

The clock recovery unit also clocks the decision circuit.

## 1.3. Optical Receiver Fundamentals

There are multiple parameters that decides the performance of optical receiver and there are multiple effects these parameters have on the output data.

### 1.3.1. Data Formats

The most basic data transmission format is unipolar non-return-to-zero (NRZ) format also known as on-off signaling, this format is the simplest as it works by switching the signal on and off to represent the ones and zeros but at the expense of power consumption as the signal has a dc component another disadvantage is having no power at the data rate making clock recovery challenging. [2]

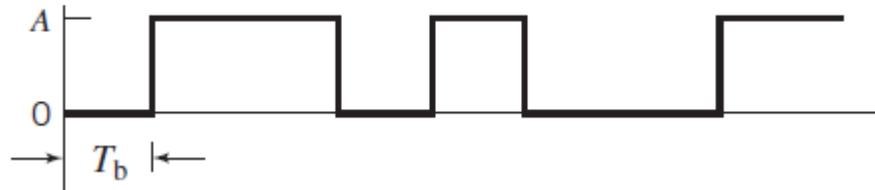


Figure 1.5. A unipolar non-return-to-zero waveform with amplitude A and bit period  $T_b$  [2]

A way for increasing the data rate at the same pulse rate (knowing as symbol or baud rate) is M-level pulse amplitude modulation (PAM), where there are M possible pulse amplitudes, and each pulse represents  $\log_2(M)$  bits

The previous formats were discussing 2-level PAM, currently the most popular transmission technique is 4-level PAM where there are 4 possible levels where each level represents a 2-bit sequence, this way the data rate doubles

### 1.3.2. Bandwidth, Inter-Symbol Interference and Baseline Wander

The bandwidth of a system trades off with the gain and power dissipation also increasing the bandwidth increases the total integrated noise.

Other than the clear tradeoffs, the limited bandwidth has other effects on random binary data.

When a signal passes through a low pass filter (LPF) it filters the high frequencies represented in the sharp changes between different bit levels smoothing these changes.

For a periodic signal changing between zero and one passing through a LPF, the output levels corresponding to zero and one doesn't change with time.

When there's a non-periodic bit sequence with different random bit runs, the output value depends on the consecutive number of zeros and ones, the longer the run the.

output will have more time to settle and to reach its final value making the values corresponding to zero and one continuously changing with time which can cause error when the output doesn't have enough time to pass the decision threshold value.

The past phenomenon is known as *inter-symbol interference* (ISI) and its effect relies on the system speed, the faster the system the less time the signal needs to reach its final value and the ISI effect is lower.

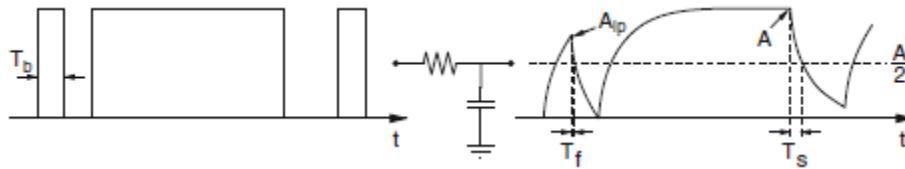


Figure 1.6 A bit stream with bit period  $T_b$  passing through a low pass filter, the output reaches a maximum value ' $A'$  and has settling time  $T_s$  and a decision threshold  $A/2$ . [1]

The other effect of the limited bandwidth on a signal is the high pass filtering effect, when a signal passes through a high pass filter (HPF) it filters the low frequency components represented in the long bit runs.

When a random bit sequence passes through a HPF the value of the long logical one runs starts to drop linearly because it lost the low frequency components a similar thing happen logical zero run as the start to increase linearly.

If the signal has enough time, it can reach the decision threshold when it shouldn't making an error.

The previous phenomenon is known as *baseline wander*.

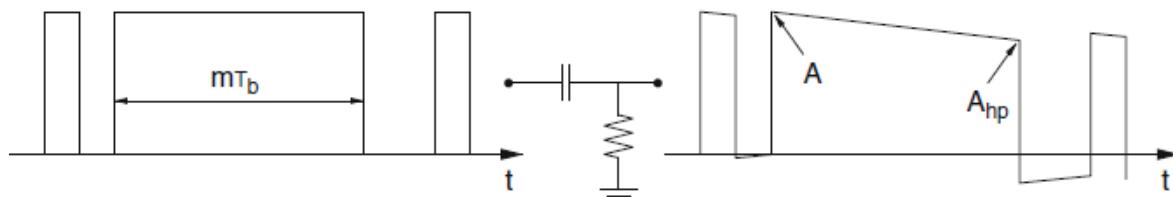


Figure 1.7 A bit stream with bit period  $T_b$  and  $m$  consecutive bits passing through a high pass filter, the output reaches a maximum value ' $A'$  and drops to value  $A_{hp}$  because of the baseline wander. [1]

### 1.3.3. Jitter

Jitter is the deviation of the zero crossing of a signal from its ideal position making different cycles taking different times.

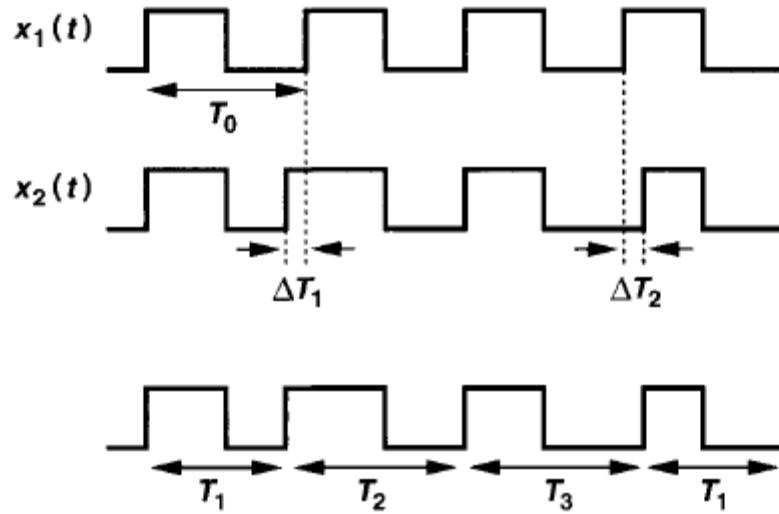


Figure 1.8.  $x_1(t)$  represents an ideal signal with no changing periods,  $x_2(t)$  represents a signal with jittering effect [2]

There are many ways of measuring jitter one of them is called absolute jitter which is measuring the time difference ( $\Delta T$ ) between the zero crossing of the waveform and that of another ideal reference wave form.

Since the deviation is random, we need to measure a lot of  $\Delta T$ 's to have a realistic realization and then determine the mean or root mean square value to able to quantify it.

Another type of jitter is cycle-to-cycle jitter which is measuring the absolute difference between the periods of two consecutive cycles then taking the mean or root mean square value of large number of these differences.

Another type is period jitter which measures the deviation of each cycle from the average value of the wave form.

#### 1.3.4. Eye Diagram

Since the system has different effects on different bit patterns a long sequence of bits have to be examined to have a realistic overview of the system.

A way of doing that is by plotting a diagram that has different bit patterns with a fixed interval (e.g. two or three bits wide) from various time intervals in the output waveform superimposed over each other..

Such a diagram is known as an eye diagram, for example let's take 4 2 bit intervals from a wave form representing all their possible states 00,01,10 and 11.

When looking at the output wave form it will look like the following figure.

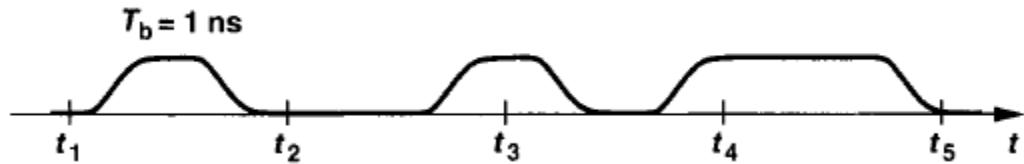


Figure 1.9 A bit sequence divided into 2-bit intervals. [2]

When taking each interval which is 2 ns alone and superimposing these intervals overreach other, we have an eye diagram.

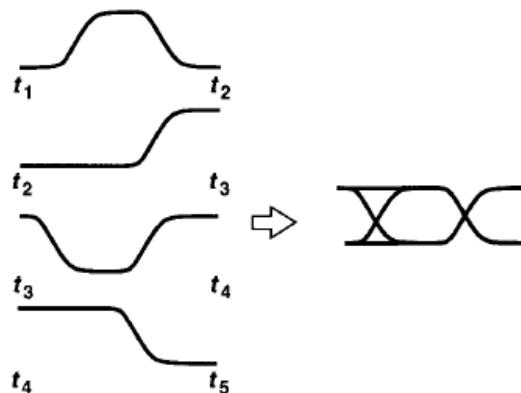


Figure 1.10 2-bit intervals sampled from a continuous sequence and reconstructed as an eye diagram. [2]

For a realistic eye diagram, the bit run must be longer and random, and many more intervals need to be taken like the following figure.

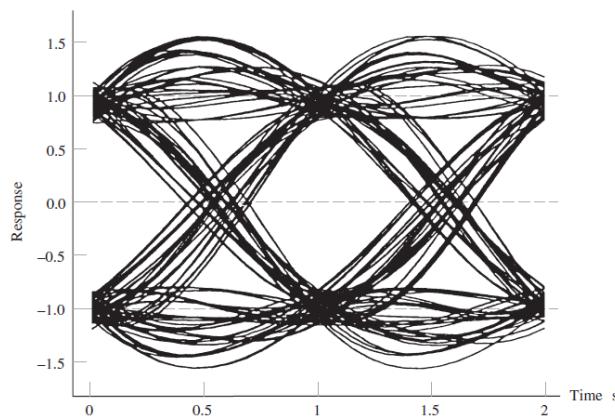


Figure 1.11 Eye diagram of random data sequence at the receiver. [3]

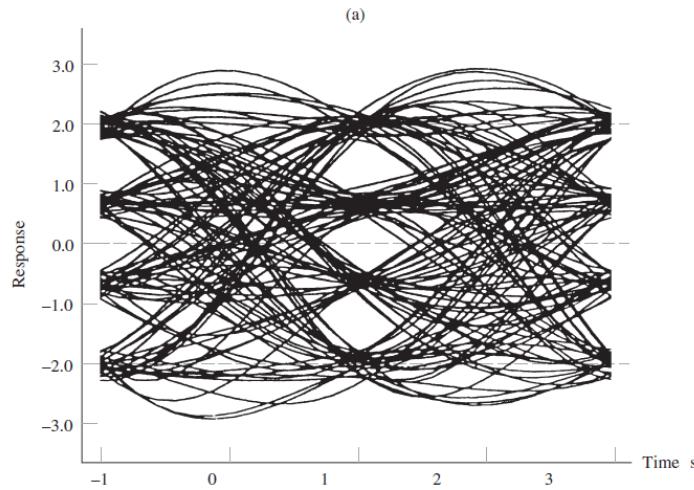


Figure 1.12 Eye diagram of random 4-level PAM data sequence at the receiver [3]

### 1.3.5. Noise

Noise is defined as any random unwanted effect on the signal.

The noise can be external noise induced by an external source like electromagnetic interference and internal noise that is generated by the internal components of the system.

As the noise is random it can't be expressed by an exact mathematical model or predicted its behavior with time so instead noise is expressed probabilistically in terms of power in frequency domain.

The relationship between any signal power and frequency is known as power spectral density (PSD).

There's a direct relationship between the noise generated by the receiver and the bit error ratio as well as the sensitivity.

The less the noise the less the bit error ratio and the higher the sensitivity reducing the transmission power needed.

Every component in the system generates additive noise, this noise could be white noise which means that it has the same power at all frequencies from dc.

White noise is mostly caused by thermal energy that causes a random movement of atoms and carriers, so it's also known as thermal noise, the probabilistic distribution of white noise is usually gaussian and in that case it's known as additive white gaussian noise (AWGN).

Another type of additive noise is pink noise which is caused by the device directly, this noise is inversely proportional to the frequency making it dominant only at low frequencies and making white noise more dominant in broadband applications.

The additive noise spectrum differs from one component to another, for a resistor.

$$\bar{V}_n^2 = 4KTR. \quad (1.1)$$

, where K is Boltzmann constant.

The pink noise mostly appears in MOSFETs and called flicker noise and it happens because of the imperfections between the oxide layer and the substrate traps and releases some of the carriers causing inconsistency in current flow.

The total power spectral density of the MOSFET is given by

$$\bar{V}_n^2 = \frac{4KT\gamma}{g_m} + \frac{K_T}{WLC_{ox}^2} \frac{1}{f}. \quad (1.2)$$

, where  $\gamma$  is fitting parameter to represent the channel effective resistance, it's equal to 1 for short channel devices.

$g_m$  is the transistor's transconductance, W and L are the transistor's width and length,  $C_{ox}$  is the gate oxide capacitance per unit area and  $K_T$  is fitting parameter.

The first term describes the thermal noise, where the second term is the flicker noise inversely proportional to the frequency.

The previous equation calculates the PSD of each component separately, to calculate the PSD at the output of a whole system we assume that all the devices are noiseless and model their noise with a source.

Using superposition theorem, the transfer function of each noise source is calculated separately, and the total PSD is the sum of all source values multiplied by their transfer function.

Describing the noise at the output isn't enough to intuitively judge a system behavior, for example a system with high output noise that have also a relatively high gain would have a high signal-to-noise ratio because the signal power at the output was large enough to overcome the noise while another system with small output noise but with a small gain could have a worse SNR although the noise is small, the gain didn't increase the signal power enough to overcome it.

To overcome this issue, the gain needs to be considered in noise calculation which is done by referring the noise to the input .

For any system with gain A the relationship between the output and input signals is the following.

$$x_{out} = Ax_{in}. \quad (1.3)$$

After calculating the noise, we consider the system to be noiseless and model the total noise as a signal at the output, hence we can apply relationship above to it.

$$\bar{X}_{n,out}^2 = A^2 \bar{X}_{n,in}^2. \quad (1.4)$$

From that we can assume that the noise at the input of the noiseless system.

$$\bar{X}_{n,in}^2 = \frac{\bar{X}_{n,out}^2}{A^2}. \quad (1.5)$$

Describing the noise at the input makes the SNR independent of the gain as both the signal and noise would be multiplied by the gain to refer them to the output.

This shows how much the input signal would be distorted by the system noise regardless of its gain allowing fair comparison between different systems.

The input referred noise is a fictitious quantity in that it cannot be *measured* at the input of the circuit [4]

This far we haven't included the system bandwidth in noise calculations.

Although the noise PSD is stretched from dc frequency to infinity there is only a limited amount integrated in the system because of its limited bandwidth.

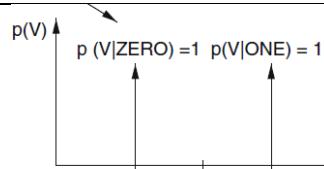


Figure 1.13. Probability density function of the received signal. [1, 1]

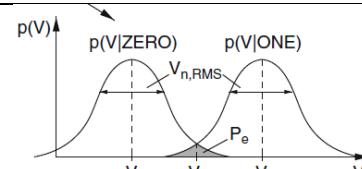


Figure 1.14. Probability density function of the received signal with AGWN introduced. [1]

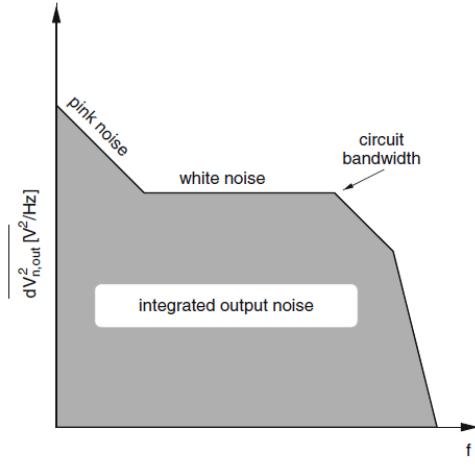


Figure 1.15 Noise power spectral density of noise after being shaped by a system bandwidth, the vertical access represent the mean of the squared noise voltage which is proportional to the noise power. [1]

Also, the calculations above determine only the spectral density of the noise, to be able to quantify the noise we have to find the total power in this spectrum, which is done by integrating the spectrum over the bandwidth if interest.

$$V_{n,rms}^2 = \int \bar{V}_n^2 df. \quad (1.6)$$

### 1.3.5. Bit error ratio

For a noiseless the probability of receiving a logical one when logical one is sent is 1 the same goes for zero.

When noise is introduced the probability of receiving a logical one or logical zero follows the noise probability around the voltage level corresponding to that level, for a gaussian noise the probability is gaussian.

The probability of receiving a zero or one curves intersect around the decision threshold causing error.

For a large number of received bits the error probability is equal for both zero and one, for a gaussian noise this probability can be calculated from the following formula.

$$P_e = Q\left(\frac{V_{ptp}}{2V_{n,rms}}\right). \quad (1.7)$$

, where  $Q(x)$  is called the *Q-function* and is the cumulative distribution function for the Gaussian distribution [1].

We can see that there's a direct relationship between the bit error ratio (BER) and the noise, also the peak-to-peak signal meaning that the noise directly affects the sensitivity of the receiver.

From this graph we see that to achieve a bit error ration of  $10^{-12}$  the sensitivity of the receiver is 14 times the noise which the transmitter power needs to adjust.

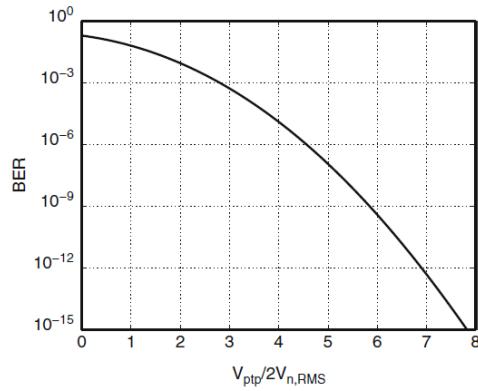


Figure 1.16. Bit error ratio against the signal to noise ratio. [1]

## Chapter 2 Literature Review

### 2.1. Transimpedance Amplifier

The transimpedance amplifier needs to have a bandwidth that's around 0.5 the baud rate to have a balance between the (ISI) and the generated noise.

The noise of the amplifier should be small enough to give a minimum bit error ratio.

It was previously discussed that the gain of the TIA isn't enough to amplify the received signal to logical levels, yet the gain has to be large enough to minimize the noise at the input.

#### 2.1.1. Single Resistor TIA

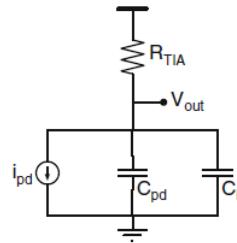


Figure 2.1. Single resistor TIA with current source  $i_{pd}$  and capacitance  $C_{pd}$  modelling the photodiode and load capacitance  $C_L$ . [1]

The simplest way to convert current to voltage is through a resistance in accordance with Ohm's law.

$$V = IR. \quad (2.1)$$

From equation (2.1) we can realize that the dc transimpedance gain

$$|Z_{dc}| = R_{TIA}. \quad (2.2)$$

Noticeably, there is a pole between the input and input which limits the bandwidth of the system; Since this is a single pole configuration this pole also represents the bandwidth (BW).

$$f_p = BW = \frac{1}{2\pi R_{TIA}(C_{PD} + C_L)}. \quad (2.3)$$

There's a clear tradeoff between the gain and bandwidth which can be quantified using the gain-bandwidth product (GBW) parameter.

$$GBW = \frac{1}{2\pi(C_{PD} + C_L)}. \quad (2.4)$$

The problem of the single-resistor TIA is the limited gain-bandwidth product which is governed only by the capacitance of the photodiode [1]

### 2.1.2. Common Gate TIA

The common gate TIA gain like the single resistor TIA gain only depends on a resistance value.

$$Z_{dc} = R_{TIA}. \quad (2.5)$$

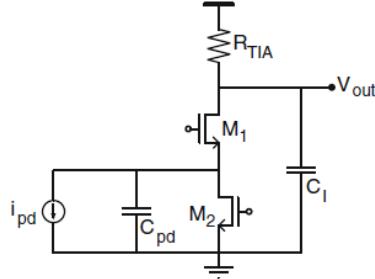


Figure 2.2. Common gate TIA. [1]

The common gate TIA separates the input and output introducing two poles .

$$f_{p1} = \frac{g_m}{2\pi C_{in}}. \quad (2.6)$$

$$f_{p2} = \frac{1}{2\pi R_{TIA} C_l}. \quad (2.7)$$

, where  $C_{in}$  is the combination of the transistor's capacitances and the photodiode capacitance.

Assuming the pole is the input is a dominant pole it will represent the bandwidth of the TIA making the gain-bandwidth product.

$$GBW = \frac{R_{TIA} g_m}{2\pi C_{in}}. \quad (2.8)$$

Here appears the advantage of this topology over single resistor TIA, the gain-bandwidth product is governed by the transistor's transconductance and the TIA resistance.

### 3.3.3 Regulated Cascode TIA

A way of increasing the transconductance of the common gate transistor without a significant increase in power consumption is introducing a local active feedback loop using a simple common source amplifier which boosts the transconductance. [1]

$$g_{m,boosted} = (1 + A)g_m. \quad (2.9)$$

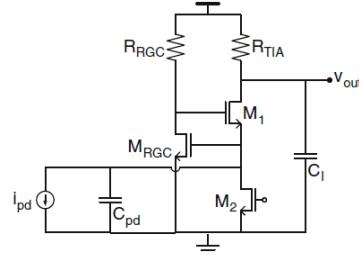


Figure 2.3. Regulated Cascode TIA. [1]

, where A is the gain of the common source amplifier and  $g_m$  is the transconductance of M1

The regulated cascode TIA have the same gain and bandwidth of the common gate except with boosted transconductance.

### 3.1.4. Shunt-Shunt Feedback Amplifier

Feedback has a lot of useful advantages over open loop topologies as it desensitizes the gain, extends the bandwidth over that of the amplifier used and for shunt-shunt topology decreases the input and output impedances. [4]

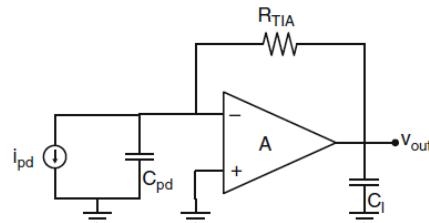


Figure 2.4. Shunt-shunt feedback TIA. [1]

The gain of the shunt-shunt feedback ideally equals to the feedback resistance but that only occurs in case that the gain of the voltage amplifier used is very high but for a relatively small gain which is the case in deep submicron devices the gain is

$$Z_{dc} = \frac{A}{1 + A} R_{TIA}. \quad (2.10)$$

, where A is the gain of the voltage amplifier.

This topology introduces two poles at the input and the output

$$f_{p1} = \frac{1}{2\pi \frac{R_{TIA}}{A} C_{in}}. \quad (2.11)$$

$$f_{p2} = \frac{1}{2\pi R_{TIA} C_l}. \quad (2.12)$$

Assuming that the input pole is the dominant pole that makes the gain-bandwidth product

$$GBW = \frac{A}{2\pi C_{in}}. \quad (2.13)$$

In this topology the gain-bandwidth product is governed by the design of the voltage amplifier.

An issue that appears in feedback topologies is the stability, unstable system will cause unwanted oscillation which will change the whole behavior of the system.

## 2.2. Main Amplifier

The TIA converts the photocurrent to voltage, this voltage produced by the TIA has a small swing, this small signal isn't sufficient for the operation of the following CDR circuits.

The main amplifier provides additional amplification and increase the signal swing to match the requirements of the CDR.

### 2.2.1 Limiting Amplifier and Automatic Gain Control Amplifier

Limiting amplifiers provide a fixed gain, making only a limited range of input swings can be amplified linearly. [1]

A signal with a large swing will introduce non-idealities like non-linearity and output clipping.

Automatic gain control (AGC) amplifiers modify their gain based on the input swing, decreasing the gain for large inputs and increasing the gain for small inputs ensuring linearity over a large range of inputs.

Although AGC amplifiers provide a higher linearity, they are more complex.

This complexity increases the power consumption and noise and limits the bandwidth.

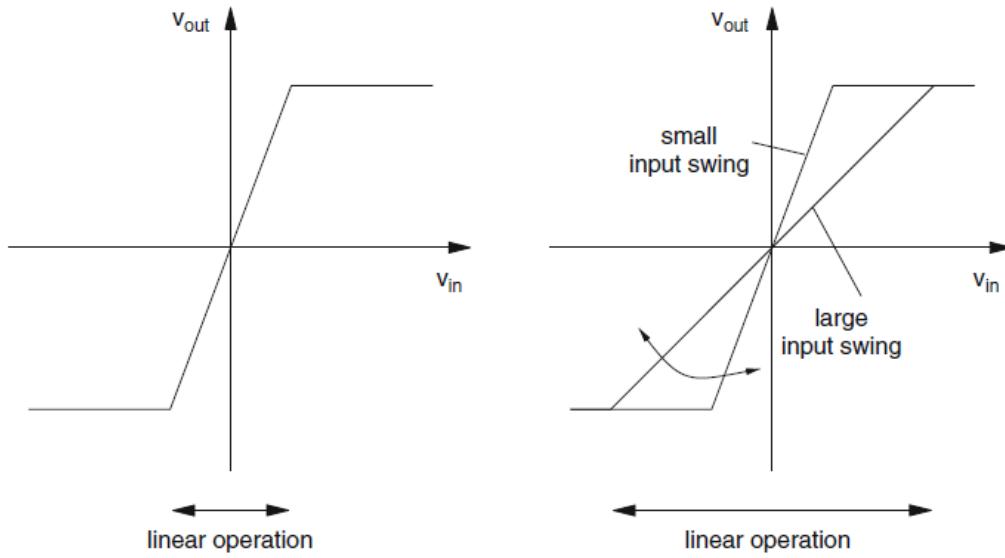


Figure 2.5. Input-output characteristics of limiting amplifier (left) and AGC (right). [1]

### 2.2.2. Cascade of Gain Stages

A first order gain stage with dc gain  $A_0$  and -3 dB frequency  $\omega_0$  has a transfer function

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}}. \quad (2.14)$$

When cascading  $n$  stages, the overall transfer function is

$$H(s) = \left( \frac{A_0}{1 + \frac{s}{\omega_0}} \right)^n. \quad (2.15)$$

This gives an overall gain of  $A_0^n$  and -3 dB frequency of  $\omega_0 \sqrt{n^2 - 1}$

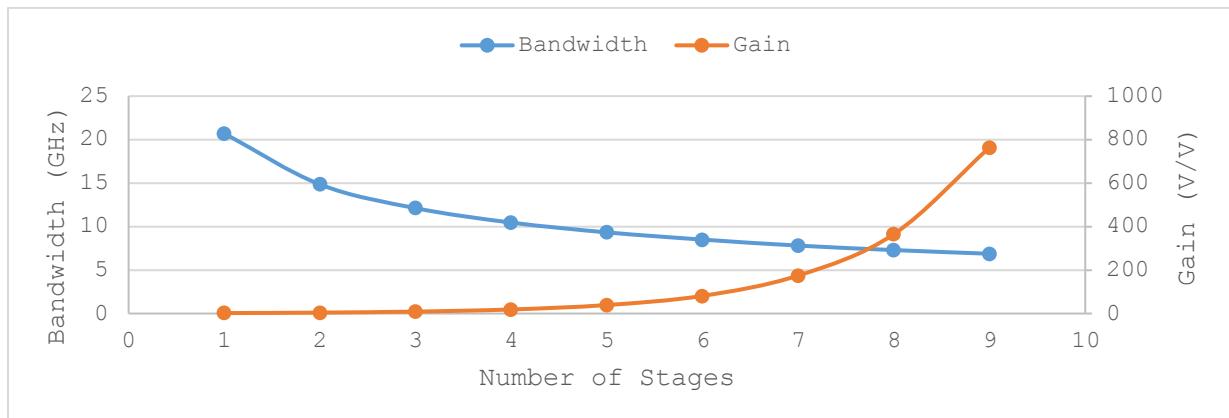


Figure 2.6. Gain and bandwidth of cascade of gain stage against the number of stages ( $A_0 \approx 2 \text{ V/V}$  and  $\omega_0 \approx 20 \text{ GHz}$ ).

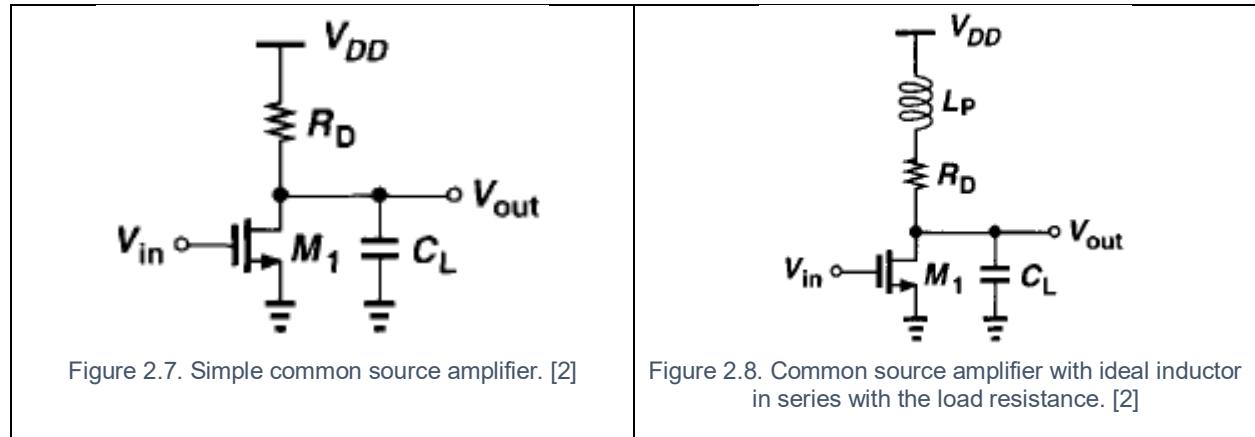
The term  $\sqrt{n/2} - 1$  is always less than one for any  $n > 1$ , making the total bandwidth always smaller than that of a single stage so to provide a high bandwidth the bandwidth of the single stage needs to be much higher than the required bandwidth (e.g. for 6 gain stages the bandwidth of each gain stage needs to be 2.86 times the total bandwidth) which isn't feasible for very-high speed applications which needs different broadband circuit techniques [2]

### 2.2.2. Inductive peaking

The gain of a simple common-source amplifier with resistive load and a relatively large capacitance at the output can be calculated as the product of the transistor's transconductance  $g_m$  and the circuit's output impedance  $Z_{out}$ .

$$Z_{out} = R_D // \frac{1}{sC_L}. \quad (2.16)$$

$$A(s) = g_m \frac{R_D}{sC_L R_D + 1}. \quad (2.17)$$



Which gives a single pole response with a dc gain  $g_m R_L$  of and bandwidth of  $\frac{1}{C_L R_L}$

Adding an ideal inductor in series with the load resistance changes the output impedance and hence changing the gain as follows

$$Z_{out} = (R_D + sL_P) // \frac{1}{sC_L}. \quad (2.18)$$

$$A(s) = g_m \frac{(R_D + sL_P)}{s^2 + s \frac{R_D}{L_P} + \frac{1}{C_L L_P}}. \quad (2.19)$$

With the inductor the circuit maintains the same dc operating point and the same dc gain, but the inductor introduces a zero that increases the impedance with frequency compensating for the decrease that was caused by the loading capacitor. [5]

The -3dB bandwidth can be calculated as follows [2]

$$\omega_{-3dB} = \left[ \frac{1}{4\zeta^2} + 1 - 2\zeta^2 + \sqrt{\left(\frac{1}{4\zeta^2} + 1 - 2\zeta^2\right)^2 + 1} \right] \omega_n^2 . \quad (2.20)$$

, where  $\zeta = \frac{R_D}{2} \sqrt{\frac{C_L}{L_P}}$  and  $\omega_n^2 = \frac{1}{L_P C_L} = \frac{4\zeta^2}{R_D^2 C_L^2}$

Substituting  $\zeta = \frac{1}{\sqrt{2}}$  yields a bandwidth of  $\frac{1.84}{R_D C_L}$ , which 84% bandwidth extension when compared to the common source amplifier without the inductor, this comes with 1.5 dB peaking.

Because of the zero the maximally flat response is achieved with  $\zeta = -\frac{1}{2} + \frac{1}{\sqrt{2}}$  which yields a bandwidth extension of 72%

The circuit exhibits an overshoot in the step response because of the zero, this overshoot trades off with the bandwidth extension. [2]

The issue with inductive peaking is the integration of monolithic inductors on chip, the integration of monolithic inductors is possible but it takes a very large chip area. [2]

Another issue with monolithic inductors on chip are the complex modelling and low quality factor at high frequencies because of the parasitics

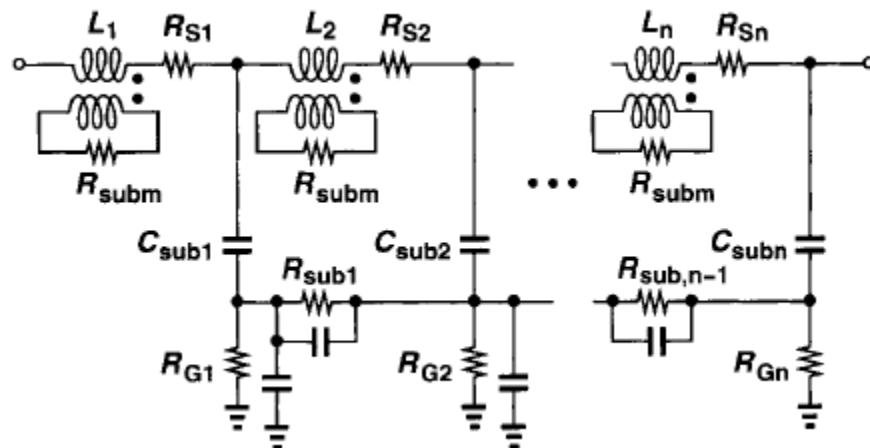
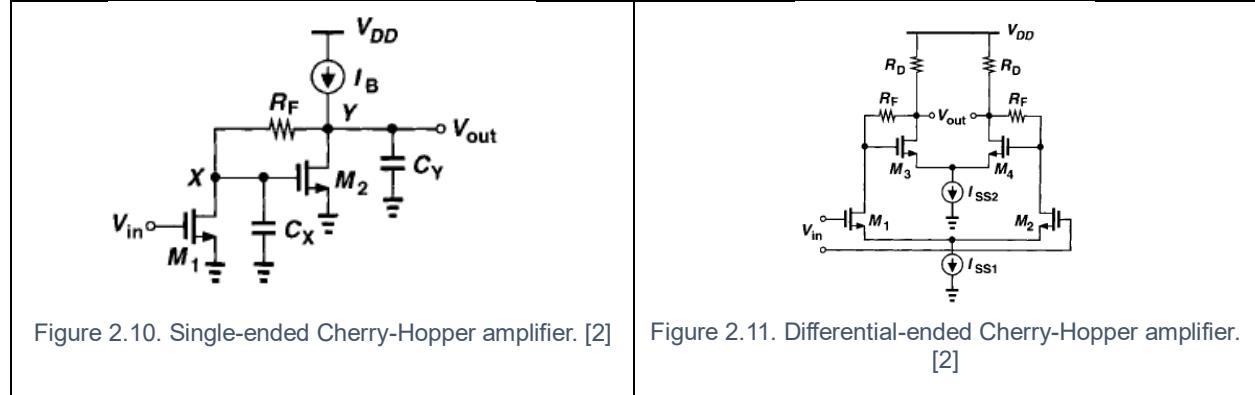


Figure 2.9. Inductor model including magnetic coupling to the substrate. [2]

### 2.2.3. Cherry Hopper amplifier

A single Cherry-Hopper amplifier stage is constructed by cascading one transconductance stage with a shunt-shunt feedback transimpedance stage

The local feedback makes the small signal resistance in the intermediate and output nodes  $g_{m2}$  approximately [2]



This approximation is only valid for low frequency as at high frequencies  $C_X$  and  $C_Y$  shunt their respective nodes increasing the impedances seen at these nodes

Assuming the system configuration has to equal poles

$$\omega_{p1} = \omega_{p2} = \frac{2g_{m2}}{C_X + C_Y + g_{m2}R_F C_{GD2}}. \quad (2.21)$$

Although the pole values are higher than the original approximation  $\frac{g_{m2}}{C_X}$  and  $\frac{g_{m2}}{C_Y}$  it still yields a high value

Differential Cherry-Hopper amplifiers suffer from difficulties at low supply voltages

ISS1 should flow through RF while ISS1+ISS2 should flow through RD making the minimum supply voltage

$$V_{DD,min} = \frac{I_{SS1} + I_{SS2}}{2} R_D + \frac{I_{SS1}}{2} R_F + V_{GS\ 3,4} + V_{ISS2}. \quad (2.21)$$

The circuit can be modified to overcome the supply voltage issues

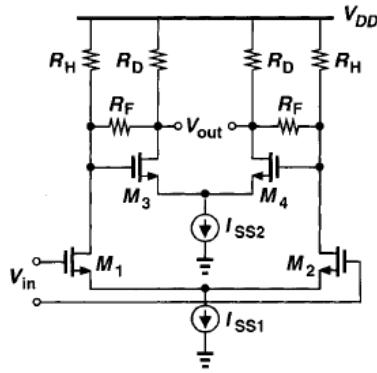


Figure 2.12. Modified differential-ended Cherry-Hopper amplifier. [2]

The resistance  $R_H$  provides bias current to the input stage;  $R_H$  must be much larger than the input resistance of the second stage to avoid gain degradation

#### 2.2.4. Second Order Gain Stage with Active Feedback

Cherry-Hopper amplifier employs a second order gain stage with passive feedback, the issue with passive feedback is it resistively loads the two stages of the amplifier which causes a reduction in gain.

The use of active feedback fixes the loading issue as well as increasing the bandwidth over that of the passive feedback. [6]

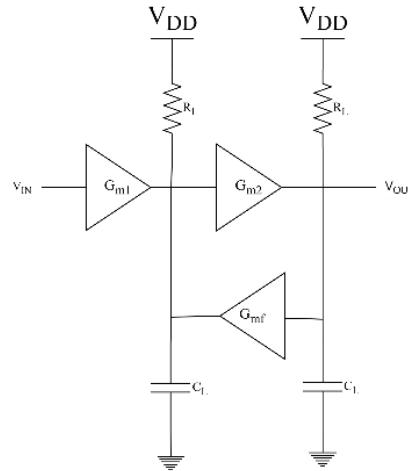


Figure 2.13. Second order stage with active feedback.

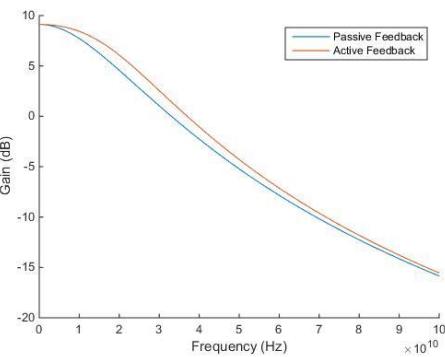


Figure 2.14. Second order stage with active and passive feedback without the resistive feedback loading effect.

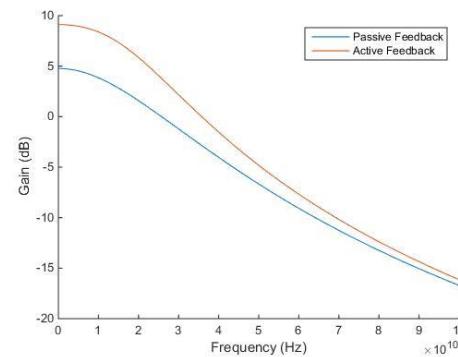


Figure 2.15. Second order stage with active and passive feedback with the resistive feedback loading effect.

Without taking the resistive loading effect of the passive feedback, the active feedback still outperforms it as it extends the bandwidth at the same gain.

When taking the resistive loading effect into account the gain is highly degenerated, and the use of active feedback give a gain and bandwidth advantage.

The overall transfer function of second order stage with active feedback

$$A(s) = \frac{G_{m1}(s)G_{m2}(s)}{1 + G_{m2}(s)G_{mf}(s)}. \quad (2.23)$$

The transconductance stages can be implemented by a resistive load differential pair, assuming these pairs have a dominant pole at the output the transfer function of the transconductance stages can be written as

$$G_{m1}(s) = G_{m2}(s) = \frac{g_m R_L}{1 + s R_L C_L}. \quad (2.24)$$

$$G_{mf}(s) = \frac{g_{mf} R_L}{1 + s R_L C_L}. \quad (2.25)$$

The overall transfer function can be written as

$$A(s) = \frac{g_m^2 R_L^2}{(1 + s R_L C_L)^2 + g_m g_{mf} R_L^2}. \quad (2.26)$$

$$A(s) = \frac{A_0^2}{\left(1 + \frac{s}{\omega_0}\right)^2 + A_0 \beta}. \quad (2.27)$$

By solving for -3dB frequency at maximally flat response we can find that the gain-bandwidth product is [6]

$$GBW = f_T \frac{f_T}{f_{-3dB}}. \quad (2.28)$$

Which reveals that the gain bandwidth product of the second order active feedback increases the gain bandwidth product over the technology  $f_T$  [6, 6]

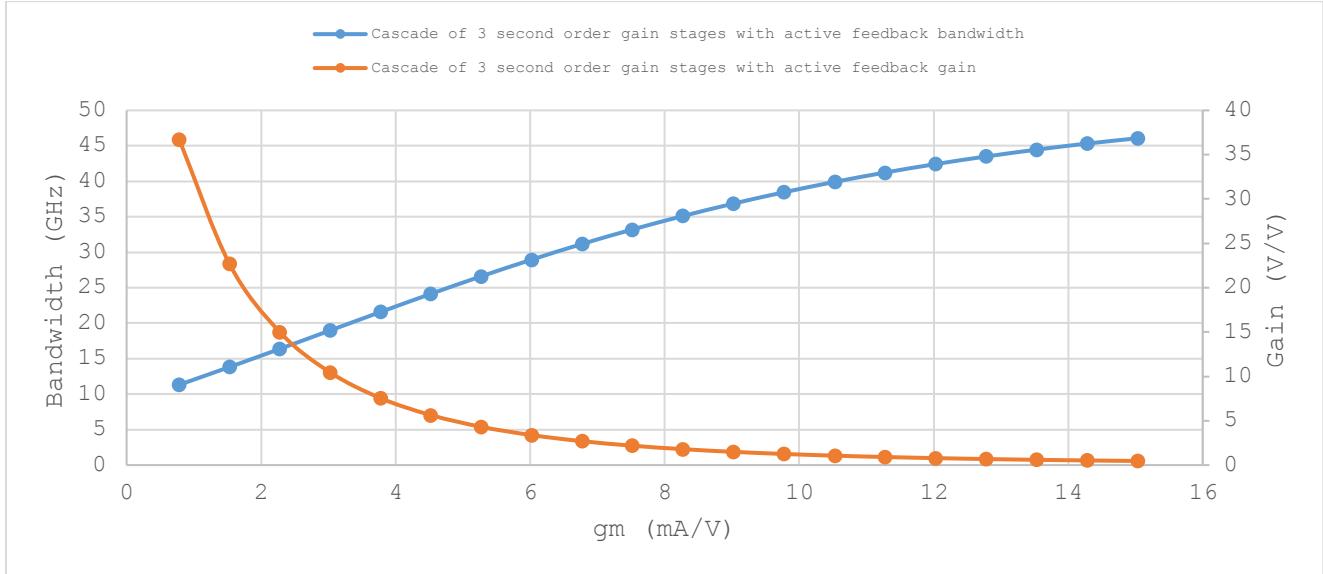


Figure 2.16. Gain and bandwidth of cascade 3 second order gain stage with active against feedback stage transconductance ( $A_0 \approx 2 \text{ V/V}$  and  $\omega_0 \approx 20 \text{ GHz}$ ).

## 2.2.5. Third Order Gain Stage with Active Feedback

The use of third order gain stage with active feedback increases the gain-bandwidth product further. [7]

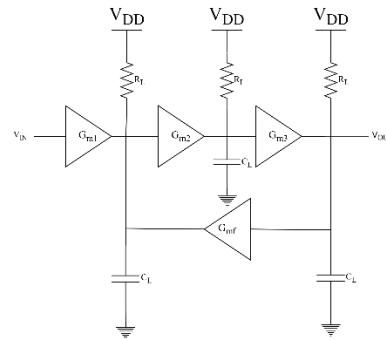


Figure 2.17. Third order stage with active feedback.

The overall transfer function for a third order stage with active feedback can be written similar to the equation 2.27 as

$$A(s) = \frac{A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3 + A_0^2\beta}. \quad (2.29)$$

The system has a dc gain  $\frac{A_0^3}{1+A_0^2\beta}$  and has 1 real pole  $-\omega_0(1+A_0^2\beta)^{\frac{1}{3}}$  and a pair of conjugate imaginary poles  $-\omega_0(1 - \frac{1}{2}(A_0^2\beta)^{\frac{1}{3}} \pm j \frac{\sqrt{3}}{2}(A_0^2\beta)^{\frac{1}{3}})$

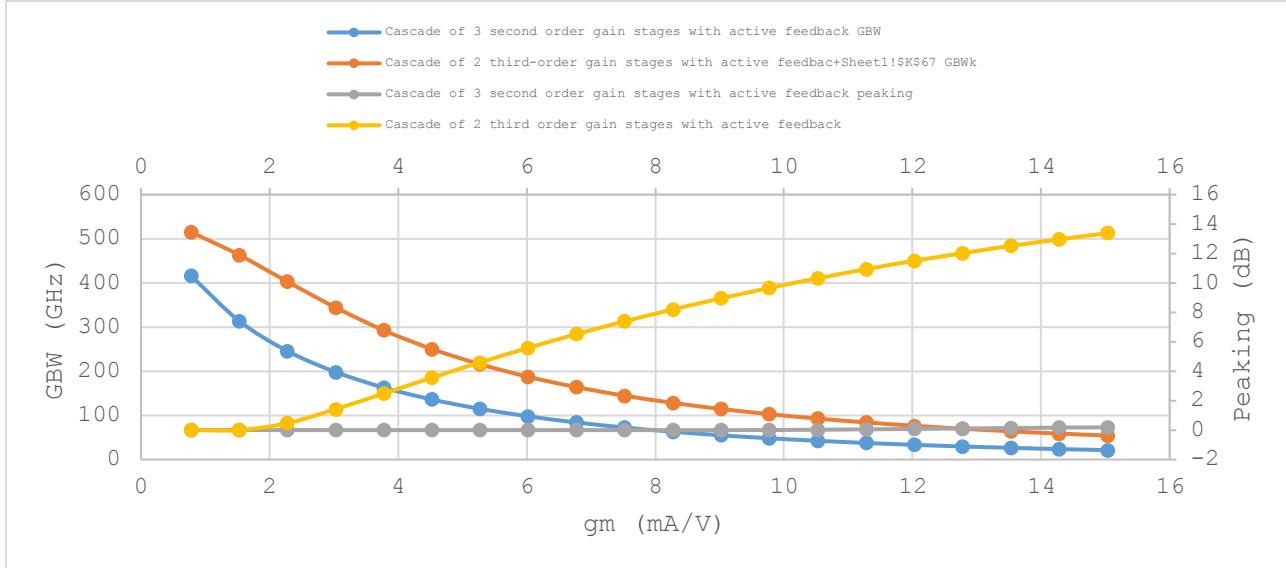


Figure 2.18. Gain-bandwidth product and peaking of cascade of 3 second order stages and 2 third order stages with active feedback against the feedback transconductance.

Although the third order stage increase the gain bandwidth product by around 100 GHz, it suffers from a very high peaking.

To overcome this issue interleaving feedback between two stages in a cascade of third order stages can be used, this technique cause pole splitting which reduces the peaking [7]

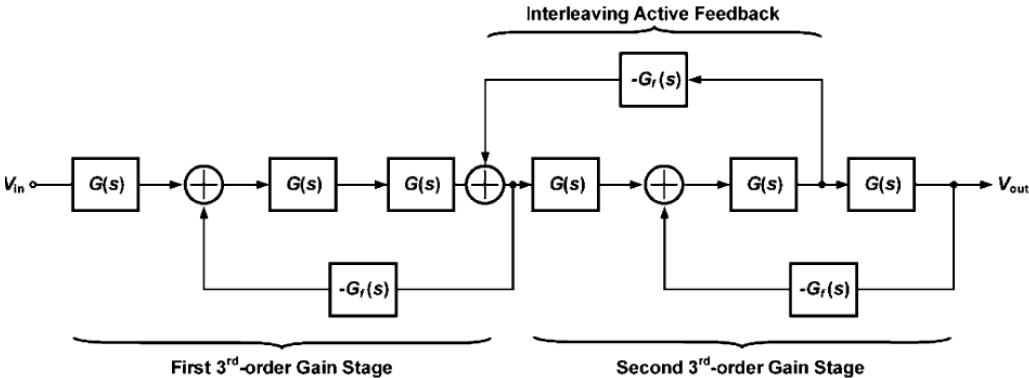


Figure 2.19. Block diagram of cascade of 2 third order stages with active interleaving feedback. [7]

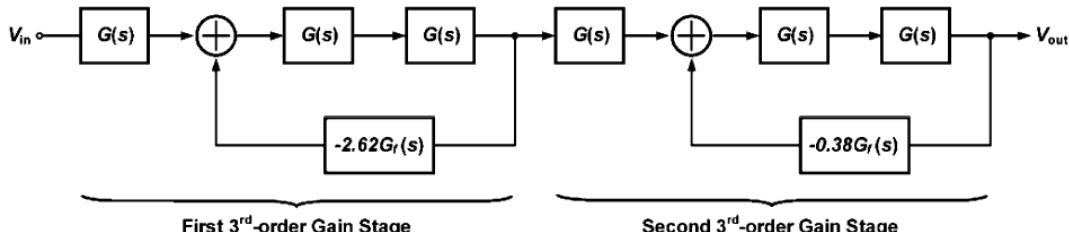


Figure 2.20. Equivalent block diagram of cascade of 2 third order stages with active interleaving feedback. [7]

By introducing the interleaving feedback between the two stages the transfer function can be expressed as

$$H(s) = \frac{G^6(s)}{1 + 3G^2(s)G_f(s) + G^4(s)G_f^2(s)} = H_A(s) \times H_B(s). \quad (2.30)$$

Which can be expressed as two transfer functions A1(s) and A2(s) where

$$H_A(s) = \frac{G^3(s)}{1 + 2.62G^2(s)G_f(s)}. \quad (2.31) \text{ and } H_B(s) = \frac{G^3(s)}{1 + 0.38G^2(s)G_f(s)}. \quad (2.32)$$

The system with interleaving feedback is equivalent to a cascade of two stages with different feedback factor, one stage with high feedback factor having an overdamped response and the other with a small feedback factor having an underdamped response which results in an overall response with reduced peaking

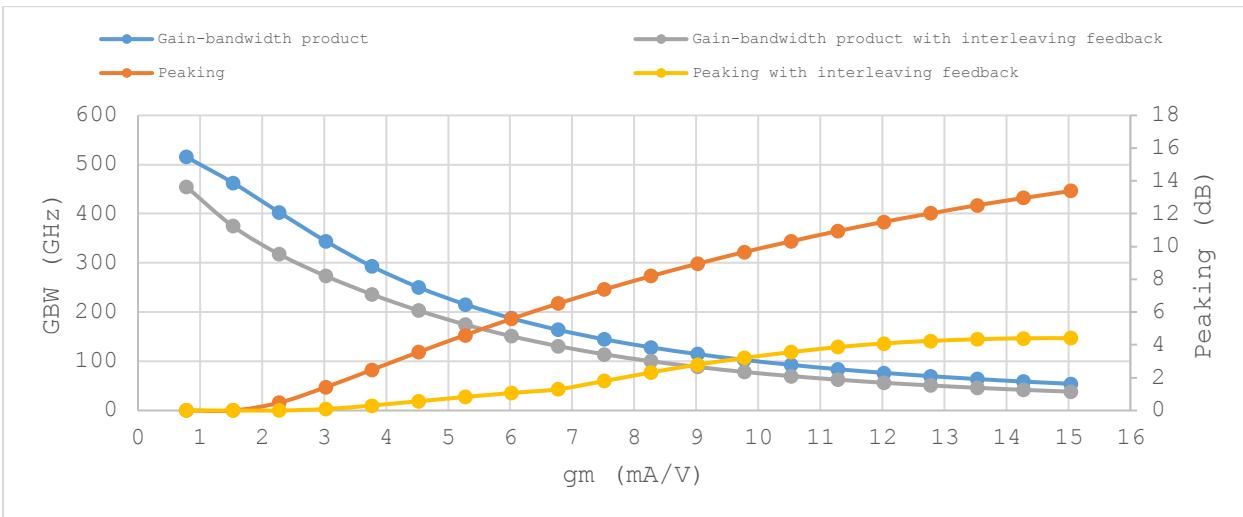
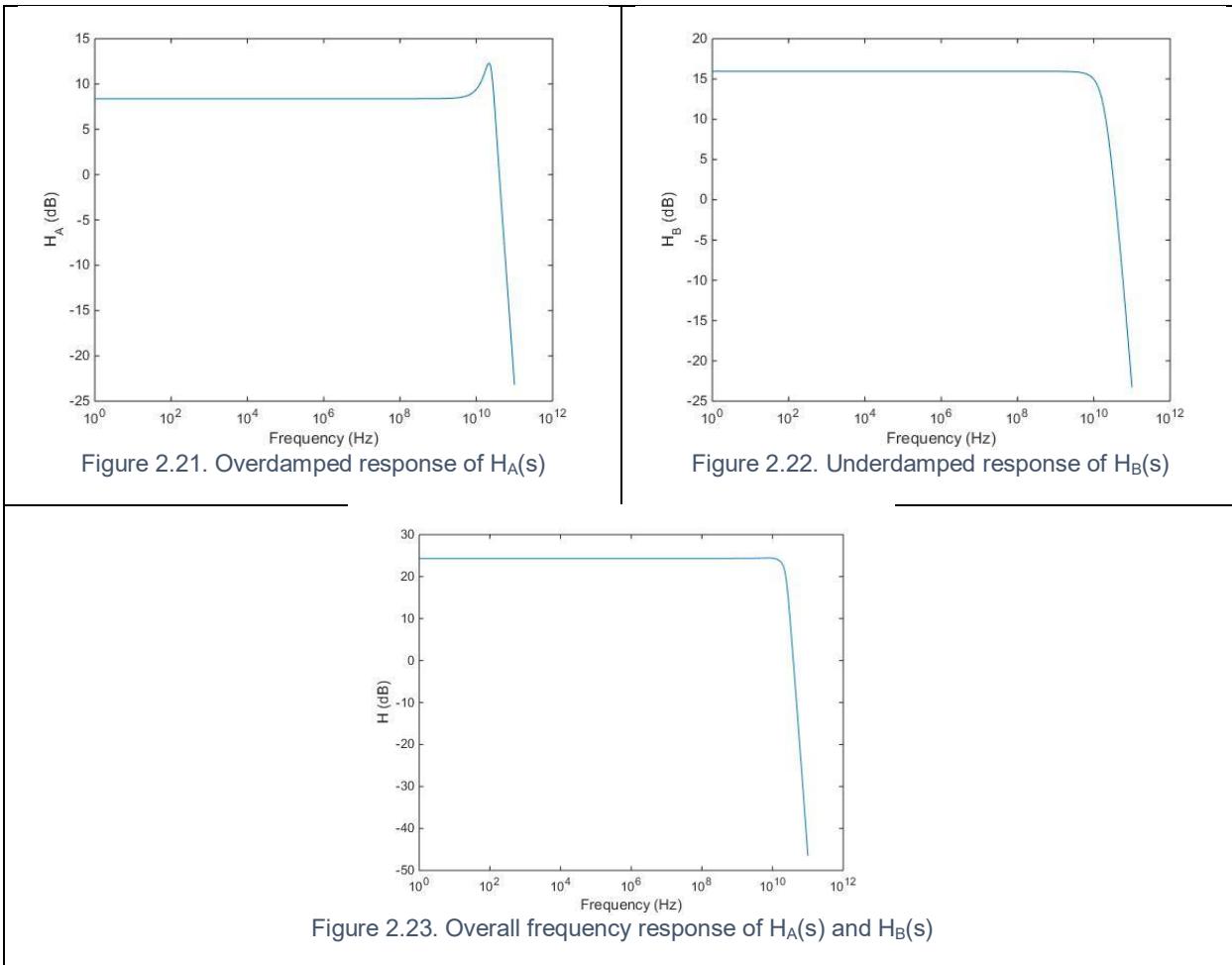


Figure 2.24. Gain-bandwidth product and peaking of cascade of 2 third order stages with active feedback with and without interleaving feedback against the feedback transconductance

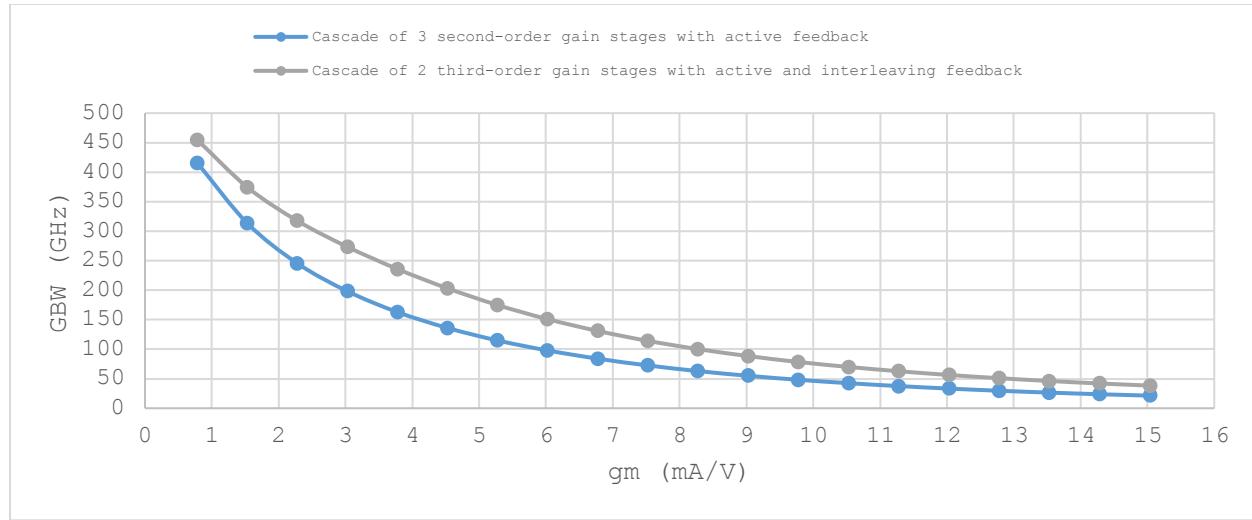


Figure 2.25. Gain-bandwidth product and peaking of cascade of 3 second order stages with active interleaving feedback and 2 third order stages with active feedback against the feedback transconductance

Although the use of interleaving feedback reduces the gain-bandwidth product, it still achieves a higher gain-bandwidth product than the second order stages with active feedback

### 2.3. Equalizer

Receiver's TIA can be intentionally designed with a low bandwidth such that the circuit suffers from severe ISI to increase the gain while reducing the integrated input referred noise, required gain stage and power consumption, the resultant ISI then is reduced using equalizers. [8]

In such topologies the midband input referred gain of the TIA can't be considered the actual gain of the circuit, it can be only used if the bandwidth is large enough such that no ISI is introduced, the actual gain which is lower needs to be calculated from the transient response of the system

There are three main classes of equalizers; continuous time linear equalizer (CTLE), decision feedback equalized (DFE), and feedforward equalizers (FFE)

CTLE works by extending the overall bandwidth of previous stages, CTLE is common when using electrical channel to extend its bandwidth which is mostly low for high-speed applications on the other hand in optical systems the channel has a very high bandwidth in order of 100's of GHz so in our system it's used to compensate for the intentionally low bandwidth TIA

CTLE works by providing a response that cancels the decay in the system and extends its bandwidth up to the desired frequency

Such a behavior can be realized by providing a zero at the bandwidth of the system that cancels the decay of the system, practically the equalizer will also provide poles, these poles should be placed such that it do not cause the response of the system to decay before the required frequency

DFE eliminates the ISI partially by subtracting the time extension of the symbol caused by the limited bandwidth following the maximum the symbol reached from the next symbol which interferes with current symbol

The maximum value the pulse reaches is known as main cursor while the extension following and preceding it are known as postcursor and precursor respectively

FFE eliminates the ISI partially by subtracting the precursor of the current symbol from the next symbol which it interferes with

It's common to combine FFE and DFE in the transmitter to eliminate the precursor and postcursor ISI to transmit clean symbols for the receiver

### 2.3.1 Source Degeneration Continuous Time Linear Equalizer

When an amplifier is degenerated by a capacitor that decrease the gain at low frequencies that starts to increase with frequency because of the zero that was introduced, the gain then starts flattening and decrease by the circuit poles

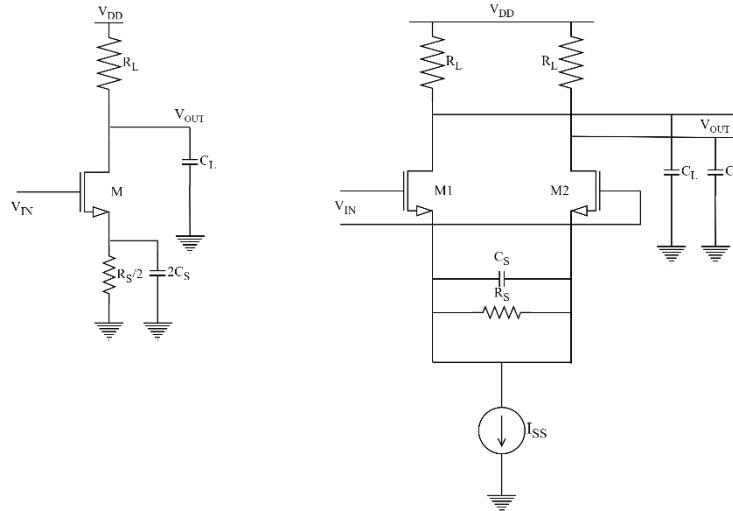


Figure 2.26. differential source degeneration CTLE and its half circuit equivalent

The circuit has a low frequency zero  $\frac{1}{R_S C_S}$  and low frequency gain  $\frac{g_m R_D}{1 + \frac{g_m R_S}{2}}$

The circuit provides two poles one at the output  $\frac{1}{R_D C_L}$  and another caused by the degeneration  $\frac{1+g_m R_S}{R_S C_S}$ , the high frequency gain is the same as a simple common source amplifier  $g_m R_D$

### 2.3.2 Additive Inverter-Based Continuous Time Linear Equalizer

Inverter based analog design has been very popular lately as conventional analog topologies don't take full advantage of technology scaling while inverters directly scale with process, are easy to operate at low supply voltages, and have good linearity and when biasing properly can work as power efficient transconductance stages. [9]

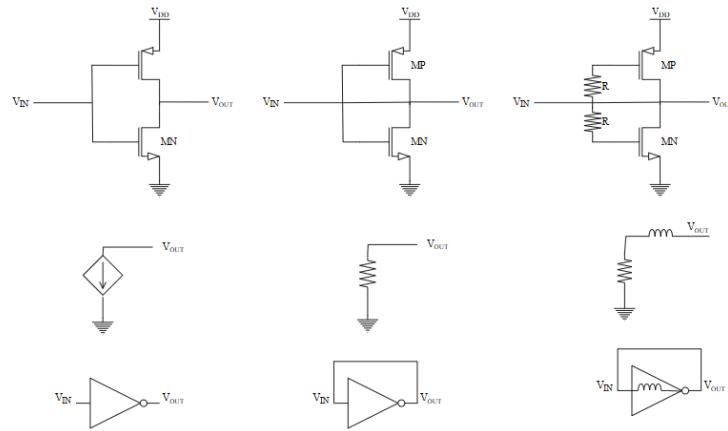


Figure 2.27. CMOS inverter different configurations and their equivalent component.

Additive two path CTLE is better option for inverter-based circuits as source degeneration requires source node network that affect the biasing. [9]

Inverters can work as different linear circuit elements in different configurations, a diode connected can behave as a self-biased resistance  $\frac{1}{g_m}$  while an active inductor can be realized by adding two resistors between the output and the gate of the inverter's transistors.

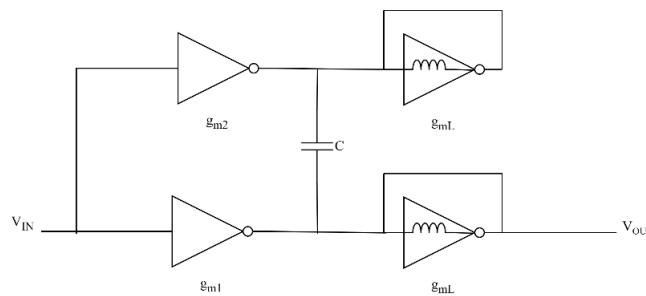


Figure 2.28. Additive inverter-based CTLE.

The circuit has a low frequency gain  $\frac{g_{m1}}{g_{mL}}$  and high frequency gain  $\frac{g_{m1}+g_{m2}}{2g_{mL}}$

This configuration provides a low frequency zero  $\frac{g_{m1}}{g_{m1}+g_{m2}} \frac{g_{mL}}{C}$  and a high frequency pole  $\frac{g_{mL}}{2C}$  making the overall transfer function of the circuit.

$$A(s) = -\frac{g_{m1}}{g_{mL}} \frac{1 + s \frac{g_{m1} + g_{m2}}{g_{m1}} \frac{C}{g_{mL}}}{1 + s \frac{g_{mL}}{C}} \times P(S). \quad (2.33)$$

$P(s)$  is added from the use of active inductors which increase the peaking and extends the bandwidth.

## 2.4. DC Offset Cancellation

Due to process variations and mismatch in differential circuits an offset in the common mode level appears.

The dc offset increases along a chain of amplifiers causing a significant offset at final stages which causes the amplifiers to saturate.

To minimize this offset a network to incorporate a high pass filtering characteristics is added to suppress the dc.

The simplest implementation of that is a low pass filter to extract the output dc level followed by an amplifier to detect the error and subtract it from input.

The high pass filtering effect causes baseline wander which in order to be minimized the low cutoff frequency needs to be minimized too.

For optical communication system the overall gain of the system is transimpedance gain  $Z$ , for that a transconductance stage needs to be used to detect the output voltage error and convert it to a current to be subtracted from the input offset current.

The low cutoff frequency can be calculated as

$$f_{cLF} = \frac{\frac{Z_{TIA} A G_{MFB}}{2} + 1}{2\pi R_{LPF} C_{LPF}}. \quad (2.34)$$

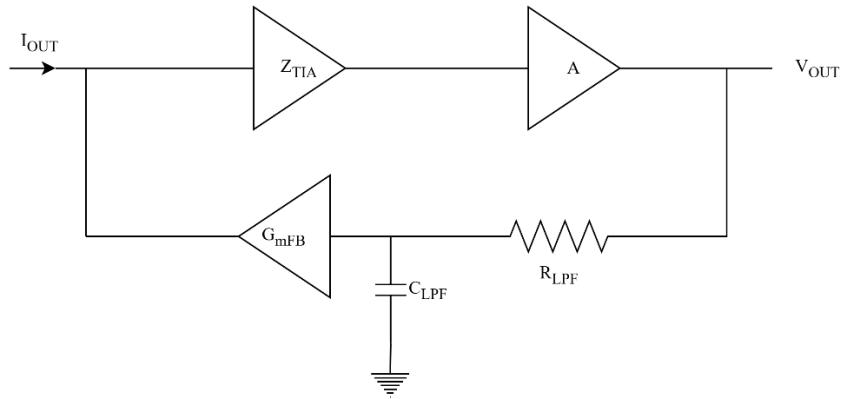


Figure 2.29. Analog frontend with TIA, main amplifier and offset compensation loop

Another function of the offset compensation loop which even used in single ended circuits comes from the unipolar nature of the photodiode.

The photodiode produce a current when illuminated and the dark current when it's not illuminated is close to zero making the input current have a dc level which needs to be suppressed to provide a proper biasing.

## Chapter 3 28 Gb/s Single-Ended Receiver Front-End in 65 nm CMOS Technology for NRZ Data Communication

Inverters take full advantage of technology downsizing. The same advantages can also be taken for the TIA by using inverter base shunt-shunt feedback TIA. [9] [10]

The TIA will be followed by 3 stages inverter based cherry hopper amplifier to increase the total gain of the AFE while providing sufficient bandwidth.

### 3.1. Amplifier Transistor sizing

To maximize the transconductance the PMOS and NMOS widths needs to be equal [11], this can be verified by the following method.

The widths of the NMOS and PMOS will be set as  $\alpha * W$  and  $(1-\alpha) * W$ , where  $W$  is the total width of the NMOS and PMOS ( $W=W_n+W_p$ ) and  $\alpha$  is a factor larger than 0 and smaller than 1 representing the width difference between the NMOS and PMOS ( $\alpha=0.5$  means the NMOS and PMOS have similar width).

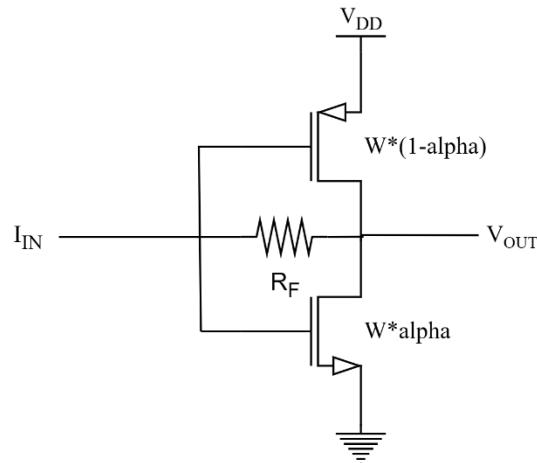


Figure 3.1. Inverter-based shunt-shunt feedback TIA

By sweeping the values of  $\alpha$  and testing for different  $W$  while fixing the value of the feedback resistance.

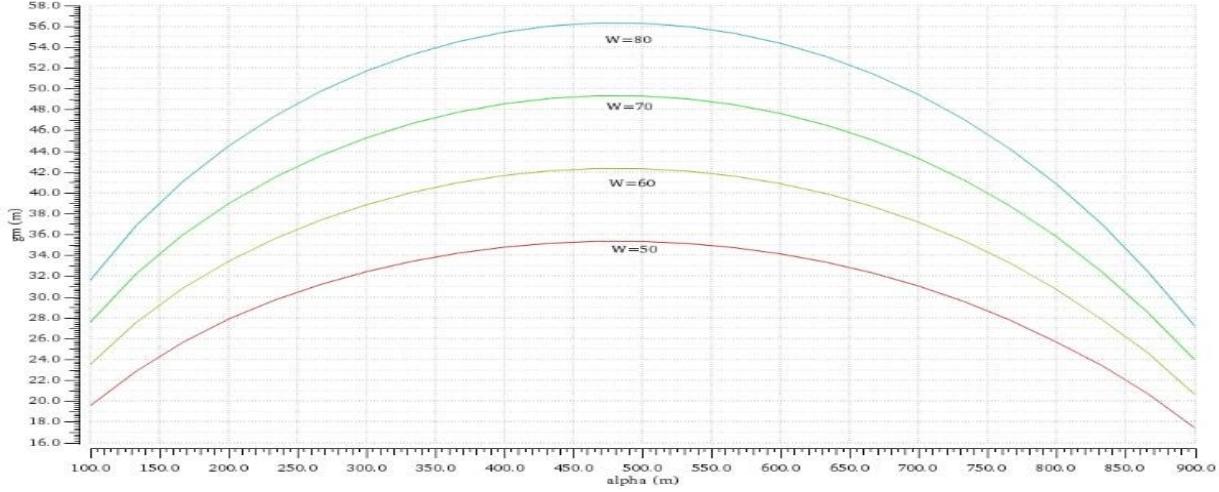


Figure 3.2. Inverter Transconductance VS. The Ratio Between NMOS and PMOS Widths at various total Width

We can notice that the maximum point isn't constant in all curves, but all curves have a nearly flat region between 0.45 and 0.55 so the maximum transconductance can be nearly taken at  $W_n=W_p$ .

The bandwidth of the TIA is usually between 0.35 to 0.5 the baud rate.

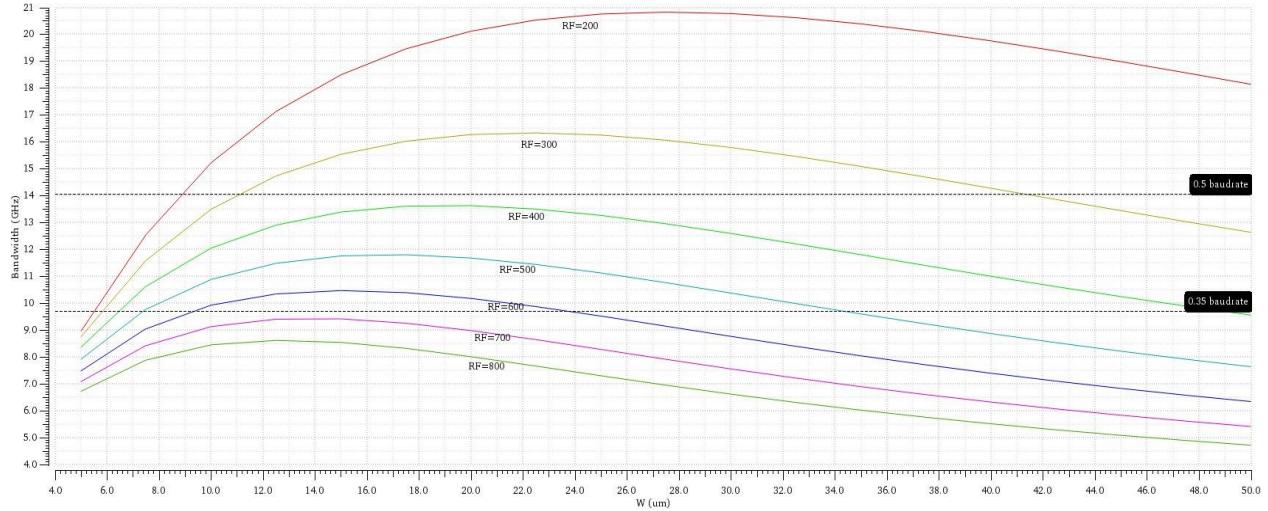


Figure 3.3. TIA Bandwidth VS. Transistor Width ( $W_N=W_P$ ) at Different Feedback Resistances with Load Capacitance of 50 fF.

This range is achieved with feedback resistance between nearly  $400\Omega$  and  $600$  ohm..

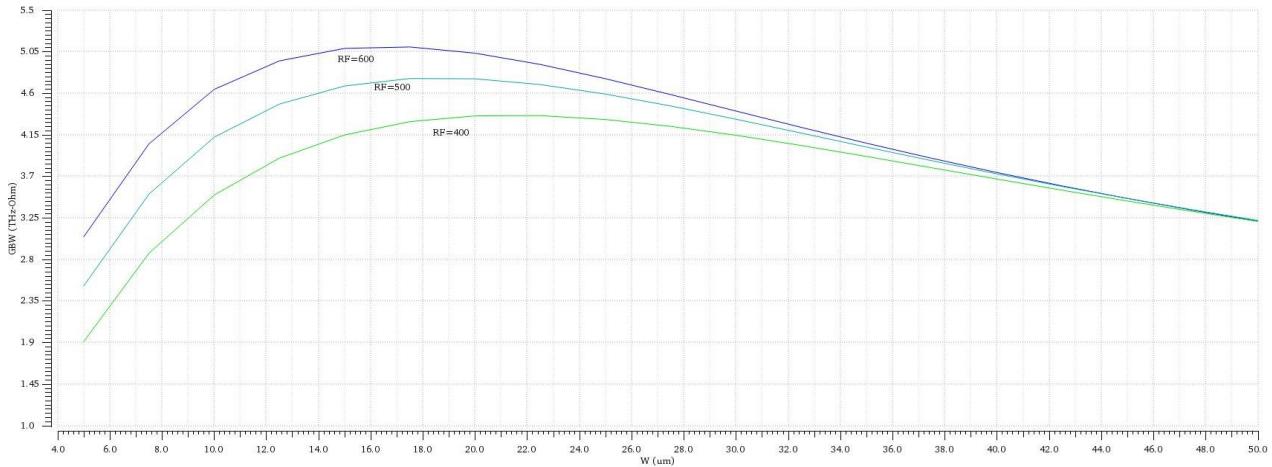


Figure 3.4. TIA Gain-Bandwidth VS. Transistor Width (WN=WP) at Different Feedback Resistances with Load Capacitance of 50 fF

For feedback resistances 500 and 600 ohms the gain-bandwidth product maximizes around a width of 17.5 um, for the 400 ohms feedback resistance the gain-bandwidth product maximizes around 22.5 um but it maintains a nearly flat response between a width of 15 um and 25 um for that a width of 17.5 um will be suitable for the TIA.

Since the limiting amplifier drives a load comparable to the input capacitance there's no need to increase the size of the main amplifier than that of the TIA so a width of 17.5 um will also be suitable for all the limiting amplifier stages. [2]

The length of each transistor is set to the minimum to maximize the speed and take full advantage of the technology..

### 3.2. TIA's Optimal Bandwidth

The bandwidth tradeoff between the total integrated noise, jitter and intersymbol interference (ISI), the required bandwidth has to have the maximum signal to noise ratio (SNR) with minimum ISI

By sweeping the feedback resistance at constant width to change the bandwidth and measuring the total integrated noise at the output and the peak-to-peak output signal from the eye diagram at 30  $\mu$ A peak to peak random bit stream input

The following graph shows that the signal to noise ratio is nearly flat between a bandwidth of 0.44 and 0.3 the baud rate, therefore a bandwidth of 0.44 the baudrate will

be chose for the design to minimize ISI

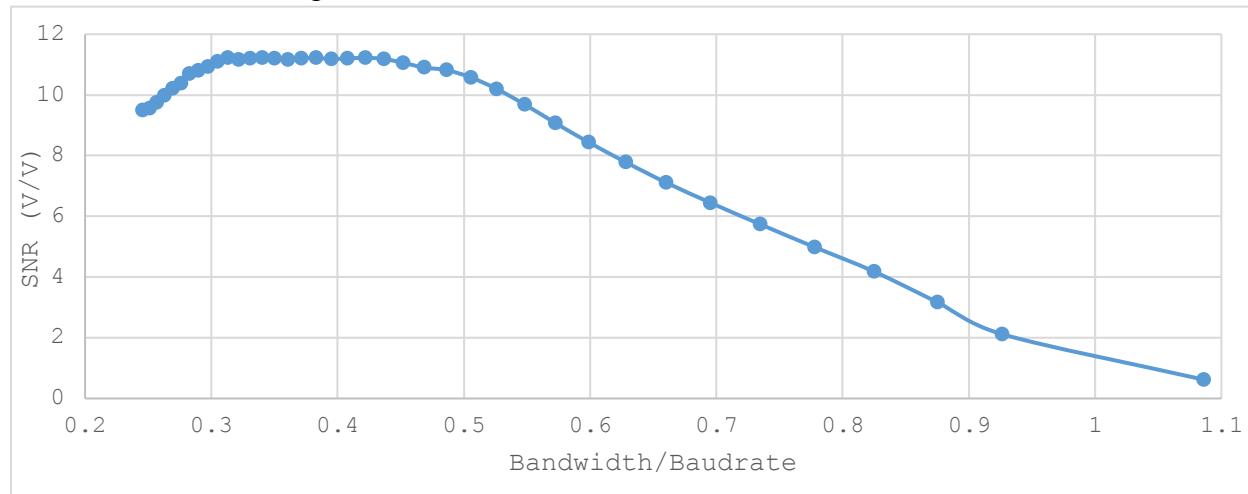


Figure 3.5. TIA Output Signal-to-Noise Ratio VS. The Bandwidth Normalized to The Baudrate at Total Inverter Width of 35  $\mu\text{m}$  and Load Capacitance 50fF

The bandwidth of the limiting amplifier (LA) should be large enough, so the total bandwidth of the system be as close as possible to the optimal bandwidth of the TIA

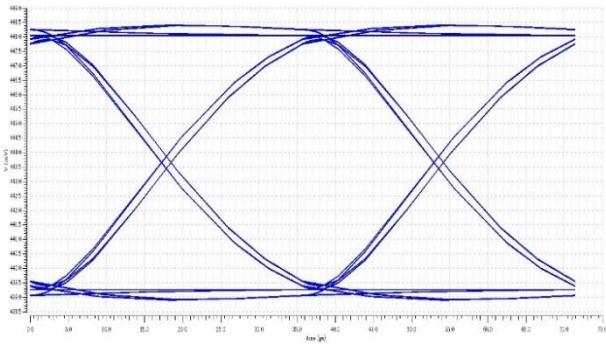


Figure 3.6. TIA Output Eye Diagram at Bandwidth=0.5 Baud Rate

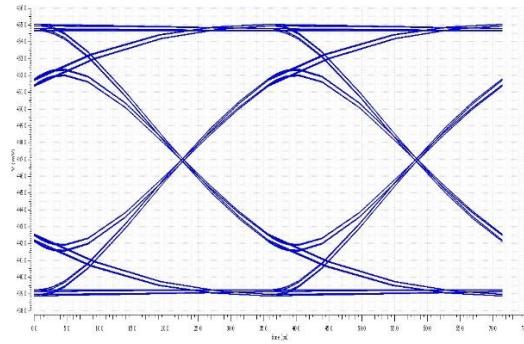


Figure 3.7 TIA Output Eye Diagram at Bandwidth=0.4 Baud Rate

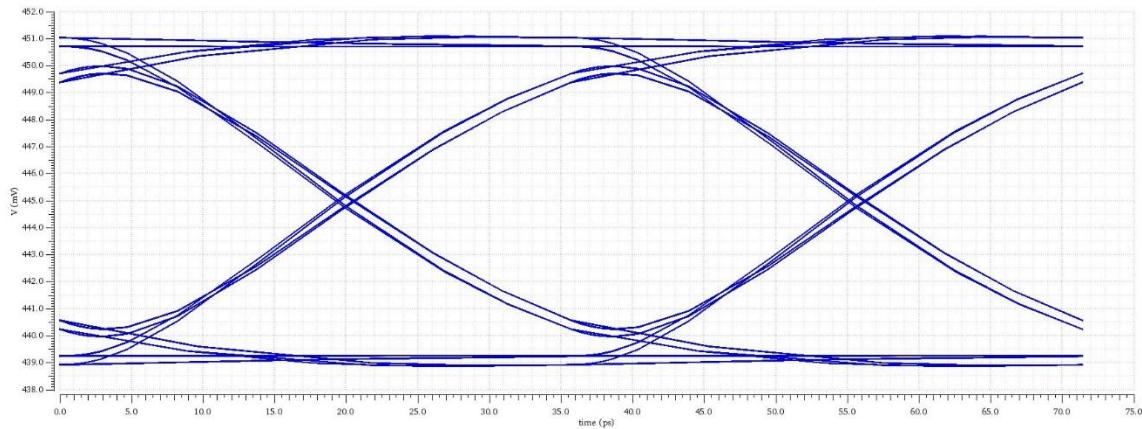


Figure 3.8. TIA Output Eye Diagram at Bandwidth=0.44 Baud Rate

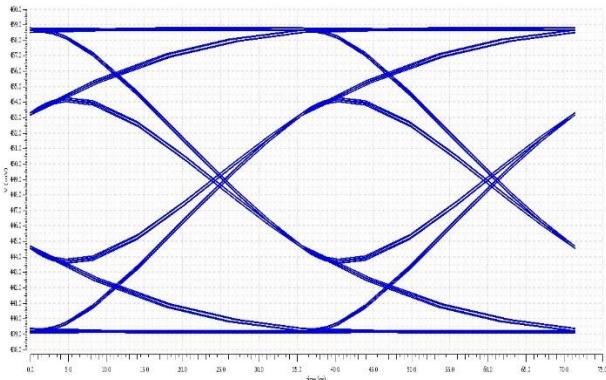


Figure 3.9. TIA Output Eye Diagram at Bandwidth=0.3 Baud Rate

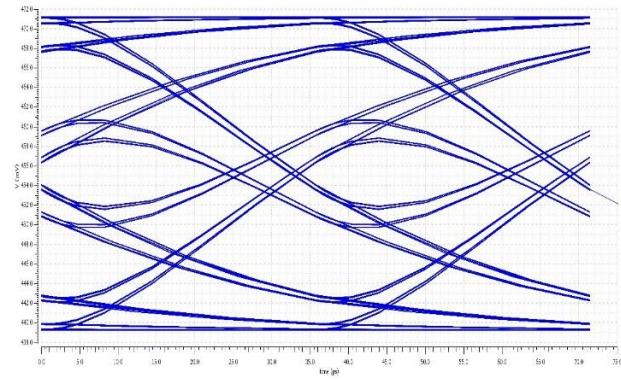


Figure 3.10. TIA Output Eye Diagram at Bandwidth=0.2 Baud Rate

### 3.3. Single-Ended Analog Frontend

Low threshold voltage transistors were used to accommodate the high bandwidth requirements, for feedback resistors N-Poly resistors with silicide were used as they provide good voltage and temperature coefficients with low parasitic and the use of silicide allows high accuracy

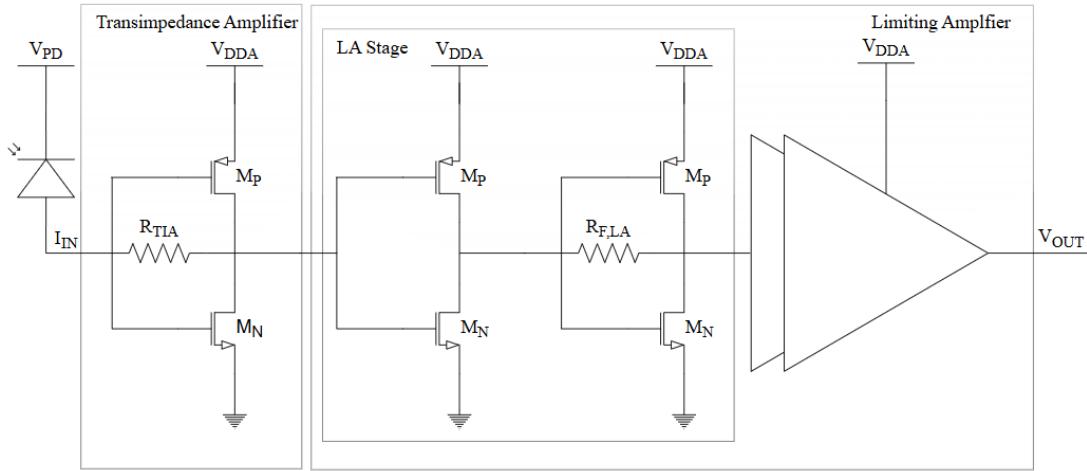


Figure 3.11. Inverter-Based Analog Front-End Architecture Without Offset Compensation

### Design Specifications

<i>Supply Voltage</i>	1V
<i>Baude rate</i>	28 Gbps
<i>TIA bandwidth</i>	12.3 GHz
<i>Overall bandwidth</i>	~12.3 GHz

### Circuit Parameters

<i>W/L (Wn=Wp)</i>	$17.5\mu\text{m}/0.06\mu\text{m}$
<i>TIA Feedback Resistance (R<sub>F</sub>)</i>	$480 \Omega$
<i>TIA Cherry Hopper Amplifier Resistance (R<sub>F</sub>)</i>	$200 \Omega$
<i>Photodiode capacitance (C<sub>PD</sub>)</i>	$100 fF$
<i>Load capacitance (C<sub>L</sub>)</i>	$50 fF$

### Results

<i>Total Small Signal Gain</i>	$75.747 \text{ dB}\Omega$
<i>Total Transient Gain</i>	$73.12 \text{ dB}\Omega$
<i>Overall Bandwidth</i>	11.71 GHz

<i>Output Referred Noise</i>	7.716 mV
<i>Input Referred Noise</i>	1.7 $\mu$ A
<i>Input Sensitivity (for BER = 10<sup>-12</sup>)</i>	23.8 $\mu$ A
<i>Power Dissipation</i>	11.73 mW
<i>Energy Efficiency</i>	0.419 pJ/bit
<i>TIA Gain</i>	51.53 dB $\Omega$
<i>TIA Bandwidth</i>	12.36 GHz
<i>Limiting Amplifier Gain</i>	24.22 dB
<i>Limiting Amplifier Bandwidth</i>	24.5 GHz

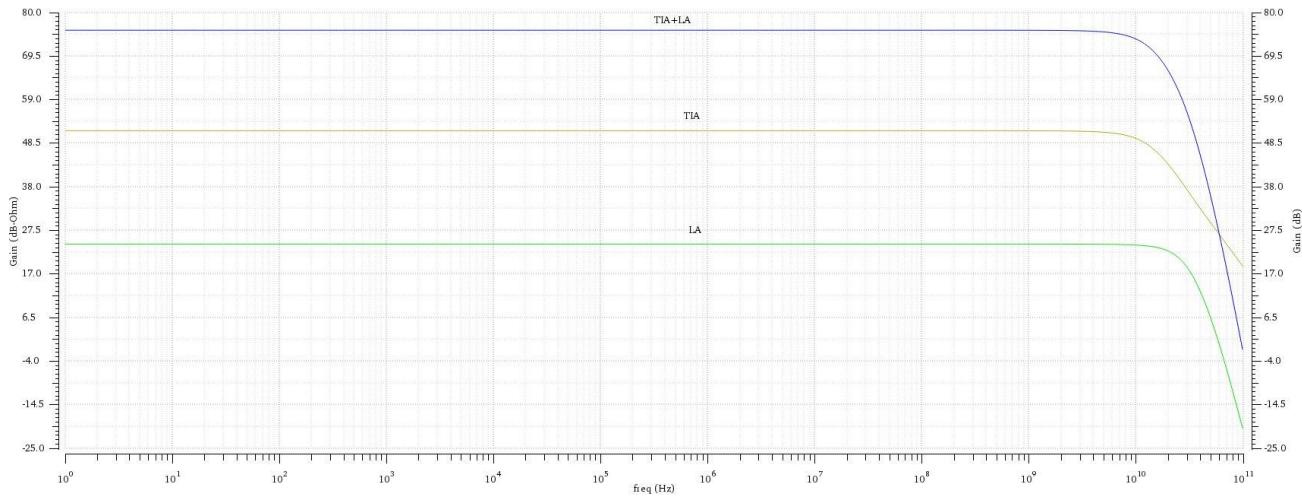


Figure 3.12. Design 3.3 TIA, LA and Overall Frequency Responses

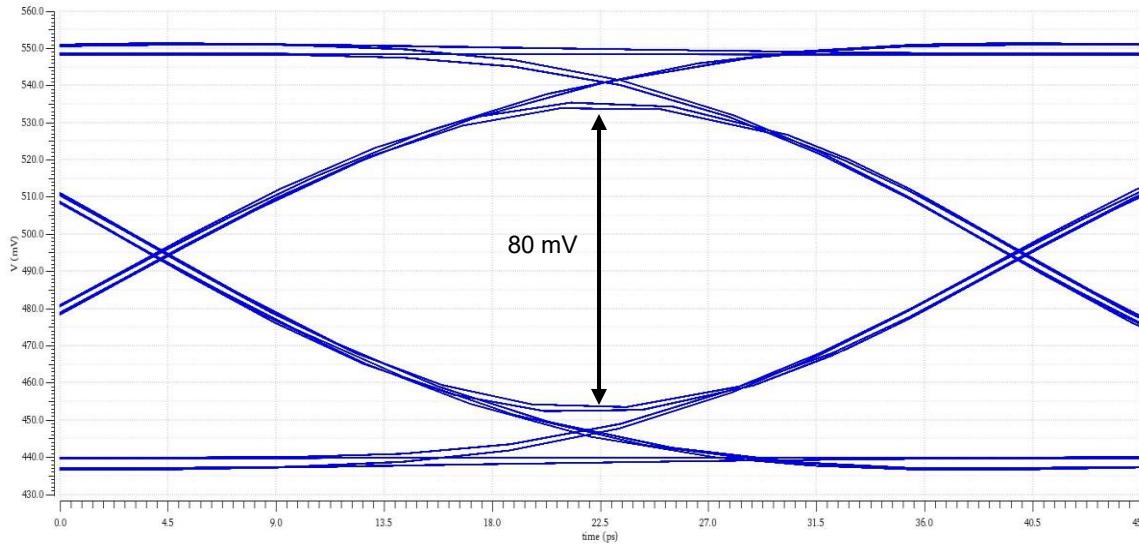


Figure 3.13. Output Eye Diagram of design 3.3 at the input sensitivity level with 80 mV vertical eye opening

The transient gain is 73.12 dB $\Omega$  which is around 3.4% drop from the small signal gain

### 3.4. Single-Ended Analog Frontend with Offset Compensation

The offset compensation is done by adding feedback with a low pass filter and transconductance amplifier, the low pass filter is a miller low pass filter to decrease the cutoff frequency and increase the loop gain to avoid unstably and reduce baseline wander

For the offset compensation loop nominal threshold voltage transistors were used as they are incorporated in a low frequency path, for the same reason devices had a length more than the minimum length as they are incorporated in a low frequency path to minimize their noise contribution

A MIM capacitor was used as it have a higher capacitance per unit area, P-Poly resistance without silicide were used as it has the highest sheet resistance in the process

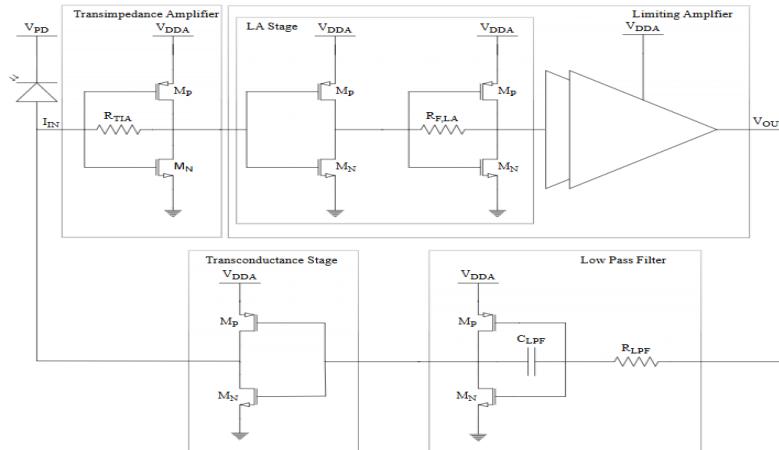


Figure 3.14. Inverter-Based Analog Front-End Architecture Without Offset Compensation

The low pass filter and transconductance stage were designed such the low cut-off frequency is below 100 kHz to limit the baseline wander

#### Circuit Parameters

W/L (Main Path)	17.5μm/0.06μm
TIA Feedback Resistance ( $R_f$ )	470 Ω
TIA Cherry Hopper Amplifier Resistance ( $R_f$ )	200 Ω
W/L (Low Pass Filter)	10μm/0.24μm
Low Pass Filter Resistance	2 M Ω
Low Pass Filter Capacitance	1 pF
W/L (Transconductance Stage)	0.48μm/0.24μm

#### Results

Total Small Signal Gain	75.725 dBΩ
Total Transient Gain	71.83 dBΩ
Overall Bandwidth	11.67 GHz
Output Referred Noise	7.745 mV
Input Referred Noise	1.98 μA
Input Sensitivity (for BER = $10^{-12}$ )	27.72 μA
Power Consumption	11.91 mW
Energy Efficiency	0.425 pJ/bit
TIA Gain	51.51 dBΩ
TIA Bandwidth	12.31 GHz
Limiting Amplifier Gain	24.2 dB
Limiting Amplifier Bandwidth	24.54 GHz

The gain and the bandwidth didn't differ from the previous design, but the frequency response behavior changed as it has another low cut off frequency of 75.42 kHz

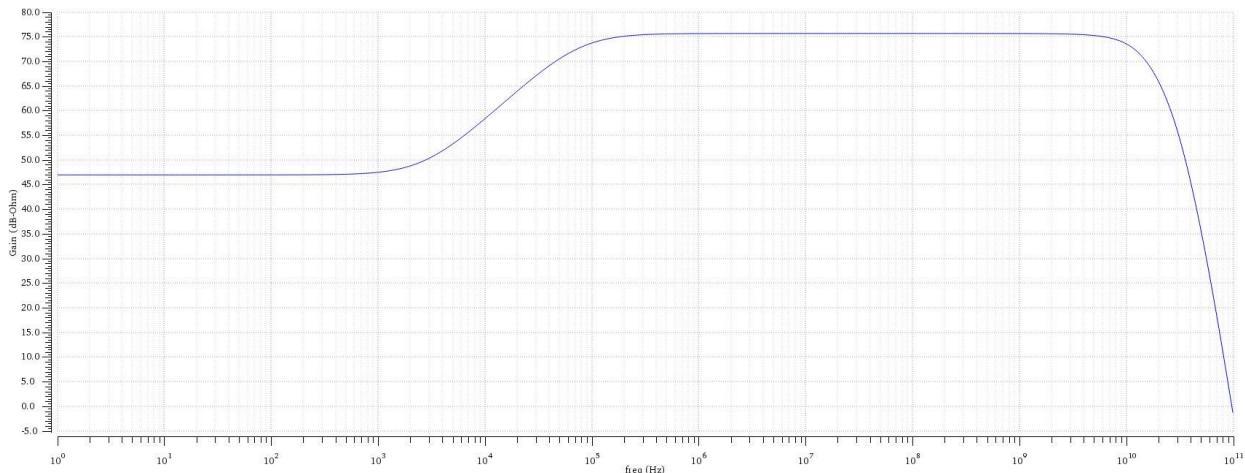


Figure 3.15. Design 3.4 Overall Frequency Responses with 75.42 KHz low cutoff frequency

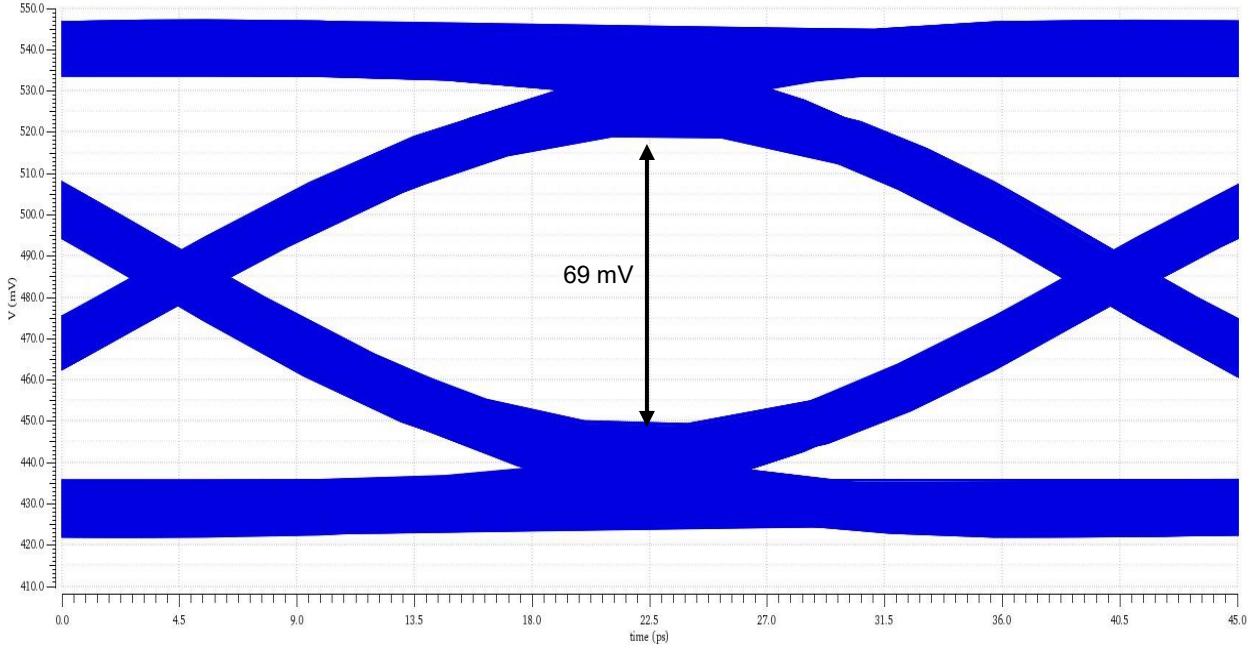


Figure 3.16. Desing 3.4 Output Eye Diagram at input sensitivity level with 69 mV vertical eye opening

The output has a maximum swing of around 125 mV at the input sensitivity level, the eye opening is around 69mV making the transient gain 71.83 dB which is around 5% lower than the small signal gain which 68% higher than the drop of the design without the offset compensation loop

### 3.5. Single-Ended Analog Frontend with Equalizer

The design works by increasing the gain of the TIA and reducing the number of main amplifier stages which both should reflect on the noise performance.

The increase in TIA gain causes a drop in the total bandwidth which then is compensated with the CTLE

The TIA gain is increased such that the bandwidth is half of the design in 3.3, for the CTLE to be able to properly compensate for the bandwidth it needs a difference between the maximum high frequency gain and low frequency of 6 dB

As the CTLE needs to have high frequency pole low threshold voltage devices are used and their length is set to minimum, the width of the CTLE is chosen as the minimum width that can drive the load and the limiting amplifier can drive

The equalizer capacitor has a relatively small capacitance, so a MOM capacitor is used as it has good performance and is less susceptible to process variations compared to MIM capacitors

The low pass filter and transconductance stage were added for dc offset compensation, a low pass filter with miller capacitance causes a instability so a simple RC LPF with MIM capacitor and P-poly resistor is used

To limit the baseline wander a low cutoff frequency of less than 100 kHz is needed

The offset compensation loop reduced the low frequency losses of the CTLE so the gain of the limiting amplifier is reduced compared to that in section 3.5 to reach an overall gain of 75 dB

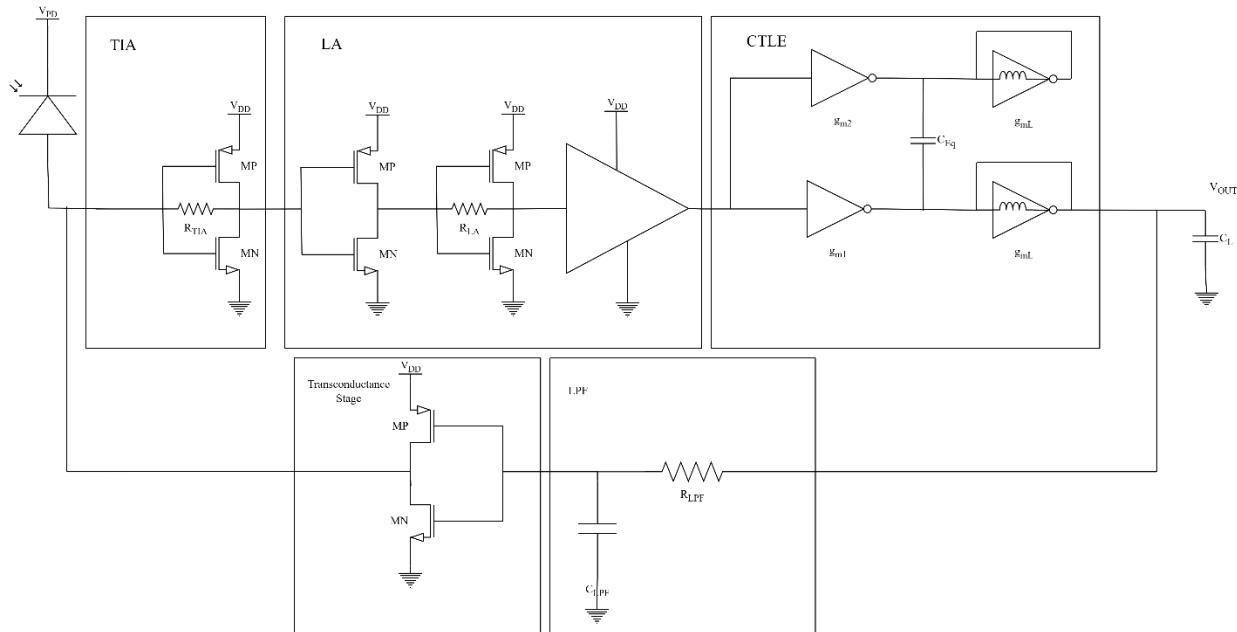


Figure 3.17. Single-ended analog front-end with CTLE and offset compensation loop

## Design Specifications

Supply Voltage	1V
Baude rate	28 GBps
TIA bandwidth	6.15 GHz
Overall bandwidth	$\sim$ 12.3 GHz
CTLE peaking	6 dB
Overall Gain	75 dB

## Circuit Parameters

W/L (TIA & LA)	17.5μm/0.06μm
TIA feedback resistance ( $R_{TIA}$ )	1100 Ω
LA feedback resistance ( $R_{LA}$ )	230 Ω
W/L ( $g_{m1}$ & $g_{mL}$ )	4.5μm/0.06μm
W/L ( $g_{m2}$ )	13.5μm/0.06μm
CTLE $g_{mL}$ stages resistance	5000 Ω
CTLE capacitance ( $C_{EQ}$ )	46 fF
Low Pass Filter Resistance	3 M Ω
Low Pass Filter Capacitance	1 pF
Photodiode capacitance ( $C_{PD}$ )	100 fF
Load capacitance ( $C_L$ )	50fF

## Results

Total Small Signal Gain	76.66 dBΩ
Total Transient Gain	73.2 dBΩ
Overall Bandwidth	11.58 GHz
Output Referred Noise	5.666 mV
Input Referred Noise	1.24 μA
Input Sensitivity (for BER = $10^{-12}$ )	17.36 μA
Power Consumption	10.74 mW
Energy Efficiency	0.385 pJ/bit
TIA Gain	59.35 dBΩ
TIA Bandwidth	6.14 GHz
Limiting Amplifier Gain	19.16 dB
Limiting Amplifier Bandwidth	24.74 GHz
CTLE Peaking	5.83 dB

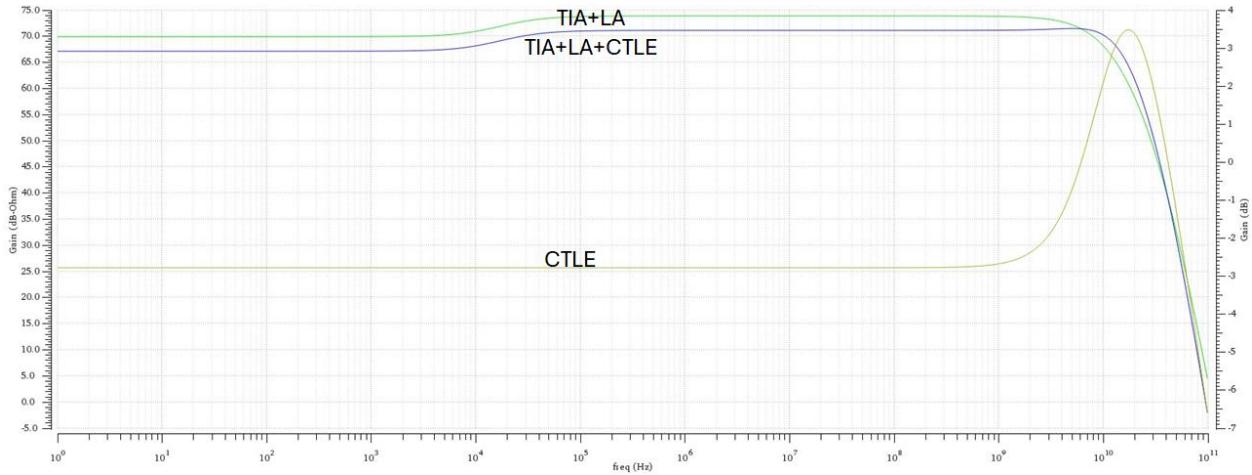


Figure 3.18. Frequency response of design 3.5 with 88 kHz low cutoff frequency for the overall response

The CLTE had a low frequency gain of around 3 dB causing an drop in the TIA and LA gain, despite that drop it still maintained a higher transient gain when compared to the design without CTLE

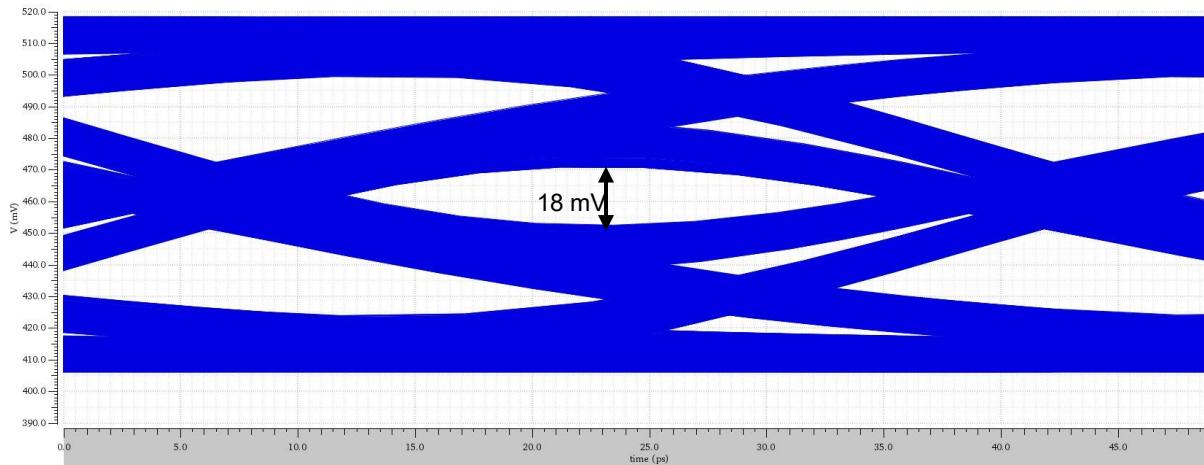


Figure 3.19. Pre-equalizer eye diagram of design 3.5 at 20  $\mu$ A input current

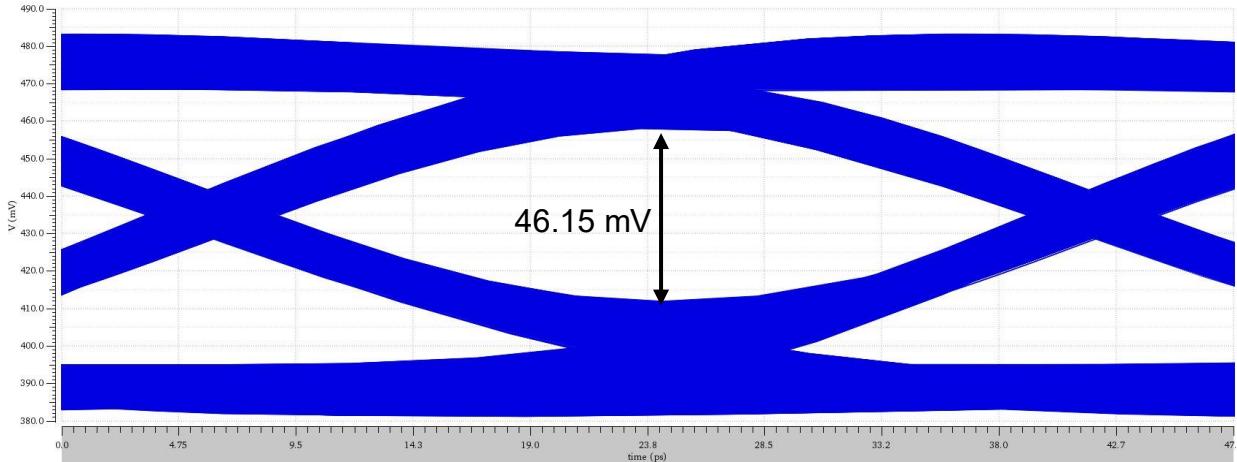


Figure 3.20. Post-equalizer eye diagram of design 3.5 at 20  $\mu\text{A}$  input current

The eye opening increased from 18 mV to 46.15 mV despite the gain reduction

To compare between the different designs, this figure of merit is used

$$FoM = \frac{\text{Transient Gain} \times \text{Bandwidth}}{\text{Power Dissipation} \times \text{Input Referred Noise}}. \quad (3.1)$$

	Design in section 3.4	Design in section 3.5
Architecture	TIA + 3 LA stages + Offset compensation loop	TIA+ 2 LA stages + CTLE + Offset compensation loop
Transient Gain ( $\text{dB}\Omega$ )	71.83	73.2
Bandwidth (GHz)	11.67	11.58
Input referred noise ( $\mu\text{A}$ )	1.98	1.24
Power dissipation (mW)	11.91	10.78
FoM (GHz.k $\Omega$ /mW. $\mu\text{A}$ )	1.93	3.96

The use of equalizer enhanced the response of the circuit, decreasing the power consumption and input referred noise and limit the effect of ISI

## Chapter 4 56 Gb/s 4-PAM Single-Ended Optical Receiver Front-End in 65 nm CMOS Technology

The maximum data rate that can be reached is limited by the technology, many circuit solutions are used to reach that limit but it can't exceed it

to increase the data rate further beyond technology a different approach needs to be taken, one approach is to modify the data format such that each pulse represents more than one bit

PAM-4 system sends data over 4 levels, each level carrying 2 bits which doubles the data rate at the same symbol rate and the same system

Although the symbol rate is the same, the amplitude difference between each two levels is reduced making the data more susceptible to ISI hence the data needed to be transmitted over a higher bandwidth

### 4.1. Amplifier Transistor sizing

As in chapter 3 the minimum length will be used to take full advantage of the technology, and the main path has the same size.

The PAM-4 data needs higher bandwidth, from 3.1 we established that the bandwidth of the TIA predominantly increases with the decrease of the feedback, at lower feedback resistances the gain-bandwidth product maximizes in a certain range of transistor widths, a  $22.5 \mu\text{m}$  will be suitable as it's covered in that range for feedback resistances between  $200\Omega$  and  $400\Omega$

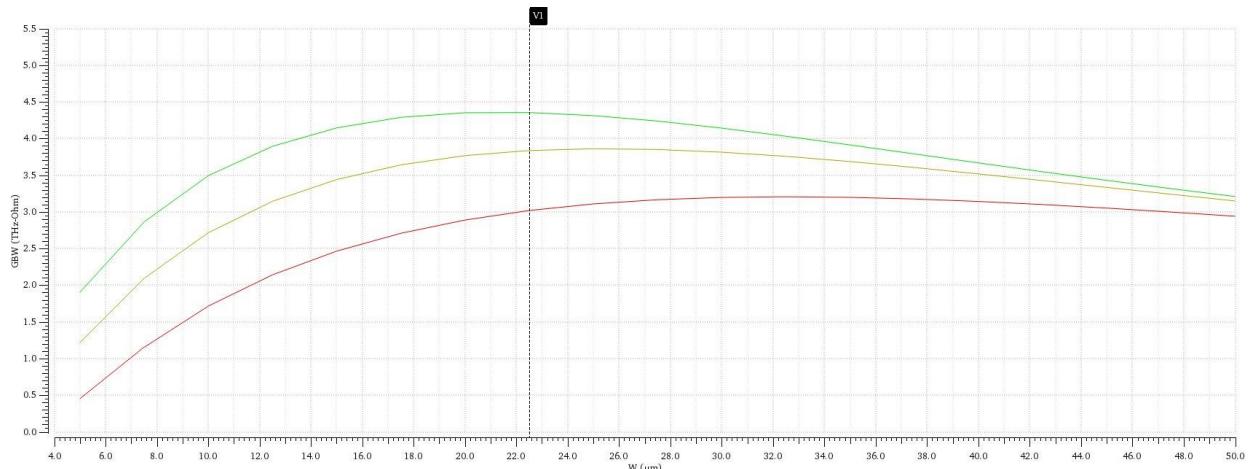


Figure 4.1. TIA Gain-Bandwidth VS. Transistor Width ( $WN=WP$ ) at Different Feedback Resistances with Load Capacitance of  $50 \text{ fF}$

## 4.2. TIA's Optimal Bandwidth

To find the optimal bandwidth the process in 3.2 was repeated for PAM-4 data to find the bandwidth that balances between the signal to noise ratio and ISI

The SNR was calculated as the ratio between the -1/3 to 1/3 eye opening amplitude and the total integrated noise at the output

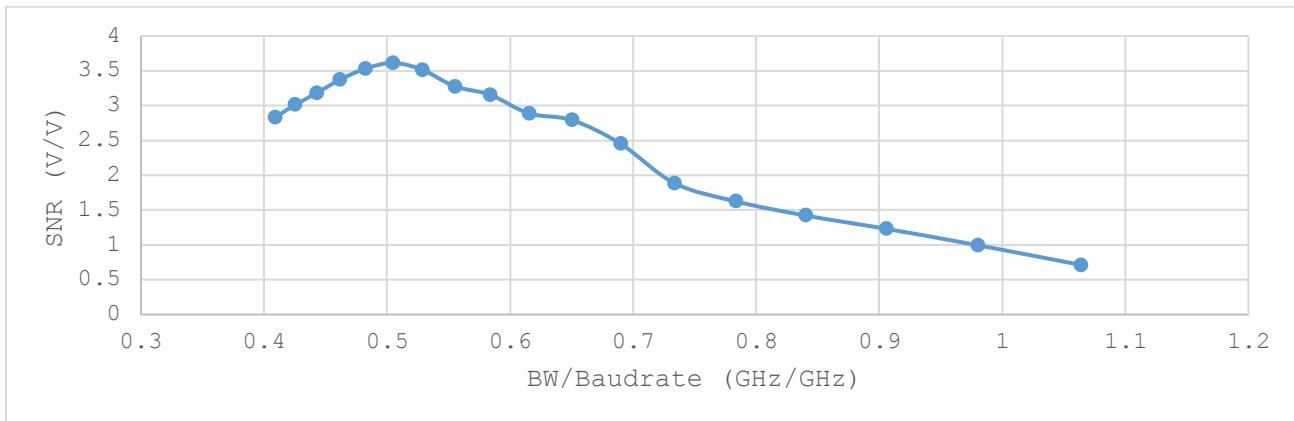


Figure 4.2. TIA Output Signal-to-Noise Ratio VS. The Bandwidth Normalized to The Baudrate at Total Inverter Width of 45  $\mu$ m and Load Capacitance 50fF

The optimal bandwidth at which the SNR maximizes at bandwidth of 0.5 Baud rate, the bandwidth only increased 13.36% on the expense of the bitrate increasing 100% maintaining a good spectral efficiency

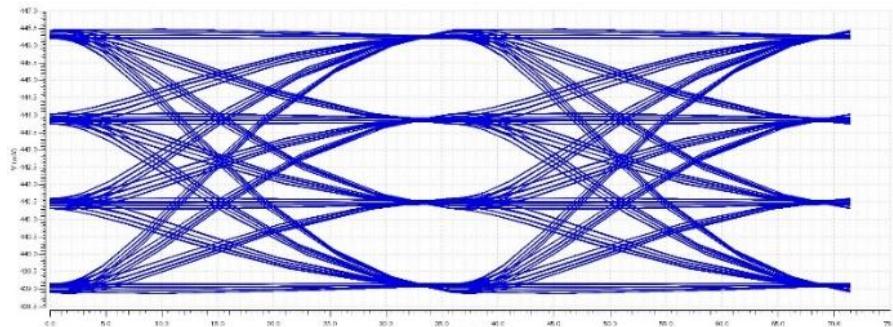


Figure 4.3. TIA Output Eye Diagram @Bandwidth=0.6 Baud Rate

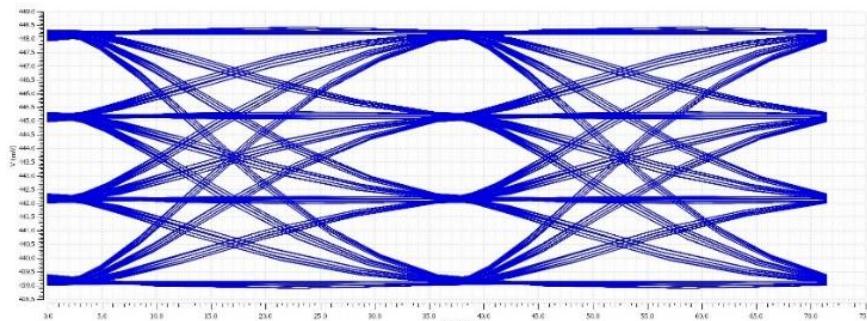


Figure 4.4. TIA Output Eye Diagram @Bandwidth=0.5 Baud Rate

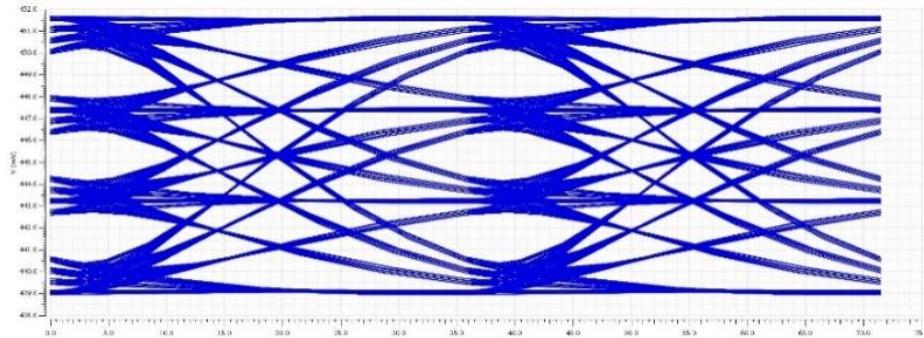


Figure 4.5. TIA Output Eye Diagram @Bandwidth=0.4 Baud Rate

### 4.3. Single-Ended Analog Frontend for PAM-4 Data

The system have the same architecture of figure 3.15 with adjustments to the sizing and components values

The low pass filter and transconductance stage were designed such the low cut-off frequency is below 50 kHz to limit the baseline wander,

#### Circuit Parameters

W/L (Main Path)	22.5μm/0.06μm
TIA Feedback Resistance ( $R_F$ )	370 Ω
TIA Cherry Hopper Amplifier Resistance ( $R_F$ )	165 Ω

W/L (Low Pass Filter)	10μm/0.24μm
Low Pass Filter Resistance	5 MΩ
Low Pass Filter Capacitance	1 pF
W/L (Transconductance Stage)	0.48μm/0.24μm

## Results

Total Gain	75.64 dBΩ
Overall Bandwidth	13.1 GHz
Input Referred Noise	1.282 μA
Power Consumption	15.25 mW
Energy Efficiency	0.272 pJ/bit
TIA Gain	49.44 dBΩ
TIA Bandwidth	14.08 GHz
Limiting Amplifier Gain	26.2 dB
Limiting Amplifier Bandwidth	24.38 GHz

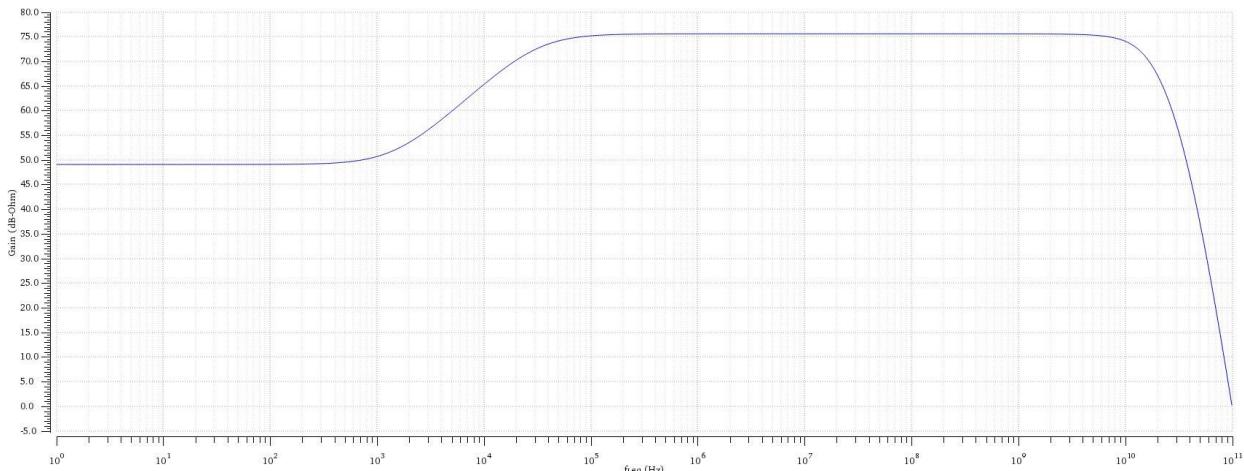


Figure 4.6. Design 4.3 Overall Frequency Response with 31.4 kHz low cutoff frequency

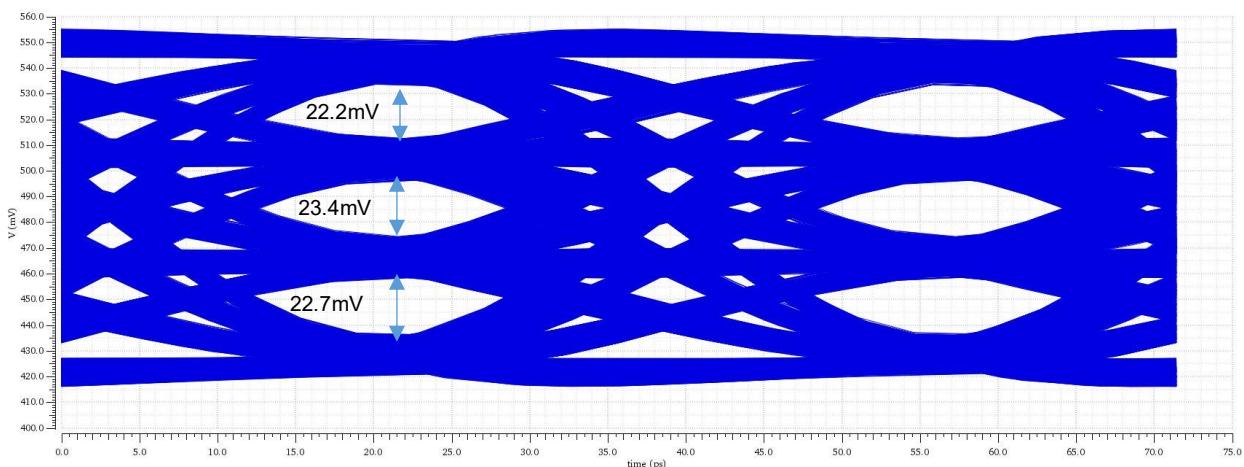


Figure 4.7. Design 4.3 Output Eye Diagram @ An Input Current of 20 μA

The eye diagram show good linearity as the ratio between the widest vertical opening and the narrowest one 0.95

## Chapter 5 28 Gbaud/s NRZ and PAM4 Differential Analog Front End

Differential circuits have larger chip area, dissipate more power and generate more internal noise when compared to their single-ended counterparts, although differential circuits are more vulnerable to external disturbance and power supply variations on the condition that the two sides of the circuit are well matched.

### 5.1. Biasing Circuit

Differential pairs sides are coupled together through a current source; this current source is realized by a transistor biased by an external circuits.

In order to have a well-defined biasing and robust performance the biasing circuit needs to be vulnerable to PVT variations.

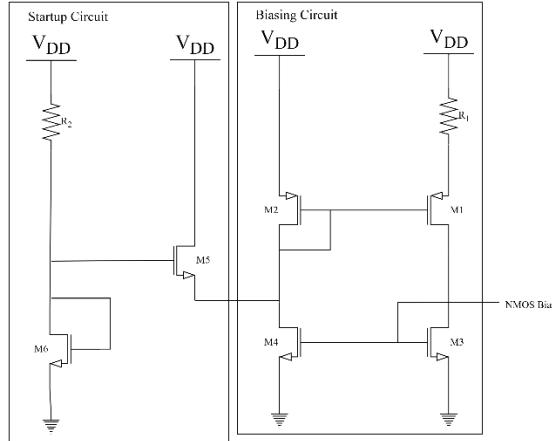


Figure 5.1. Biasing Circuit

The circuit in figure 5.1 is self-biased and its biasing doesn't depend on any external circuits or supply voltage; it only depends on the transistors sizing and the resistance  $R_1$  value making it very vulnerable to PVT variations.

The circuit have many balanced operating points, so the startup circuit is added to force it to the desired operating point.

The circuit uses nominal threshold voltage devices and NPoly resistors without silicide to reduce the area

#### Circuit Parameters

W/L (M1)	17 $\mu\text{m}$ /0.24 $\mu\text{m}$
----------	--------------------------------------

W/L (M2)	5 $\mu\text{m}$ /0.24 $\mu\text{m}$
W/L (M3-M4)	1.66 $\mu\text{m}$ /0.24 $\mu\text{m}$
W/L (M5)	3.3 $\mu\text{m}$ /0.06 $\mu\text{m}$
W/L (M6)	1.66 $\mu\text{m}$ /0.24 $\mu\text{m}$
R <sub>1</sub>	2 k $\Omega$
R <sub>2</sub>	10 k $\Omega$

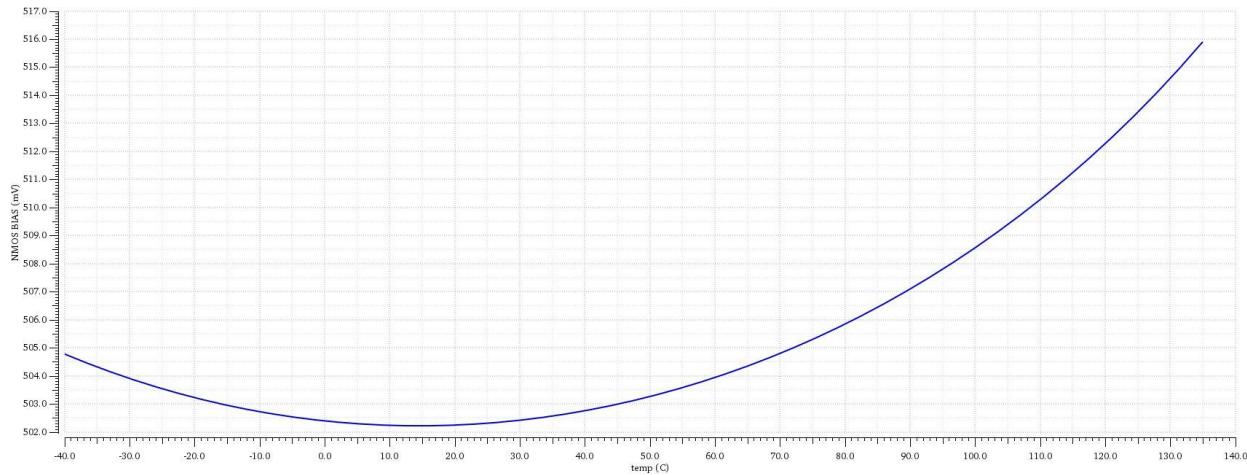


Figure 5.2. Biassing voltage against temperature at constant supply voltage of 1V (nominal value 502.2 mV at 27 °C temperature)

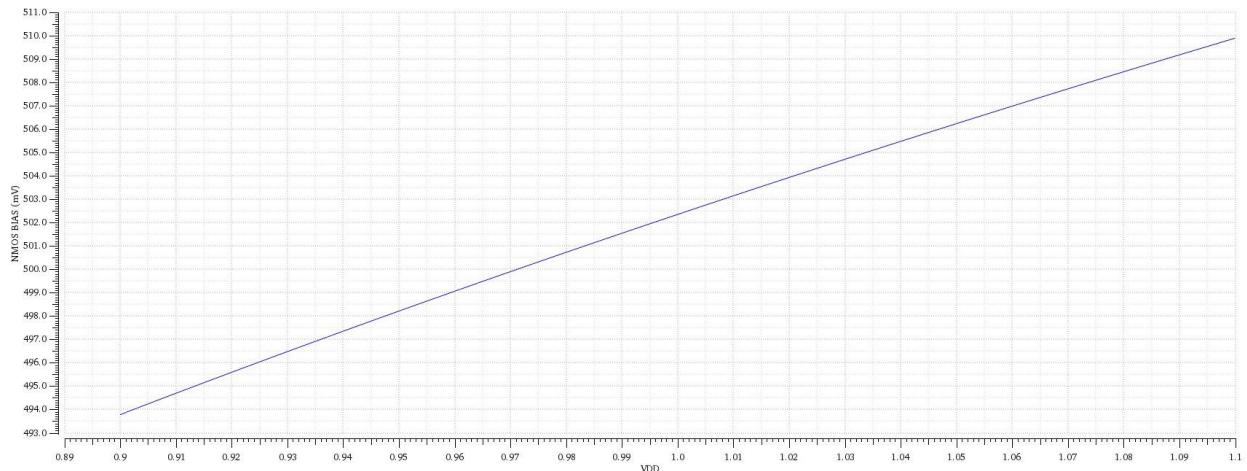


Figure 5.3.Biassing voltage against supply voltage at a constant temperature of 27 °C (nominal value 502.2 mV at 1 V supply voltage)

The circuit output voltage used for biasing has maximum variation of nearly 14 mV from the nominal temperature reached at a temperature of 135 °C, also it has a maximum variation of nearly 8 mV from the nominal supply voltage reached at a supply voltage value of 0.9 V.

The circuit has a power dissipation of around 0.1 mW

## 5.2. 28 Gb/s NRZ Differential Analog Front End

The circuit consists of pseudo-differential inverter-based shunt-shunt feedback TIA, one is connected to the input photodiode and the other is connected to a dummy for biasing, followed by 2 third order gain stages with active interleaving feedback.

A output dc level of the inverter-based TIA is nearly half the supply voltage, a truly differential pair with NMOS input has a dc input level close to the supply rail and PMOS is close to ground rail

The traditional solution to overcome this dc level variation is using voltage level shifter, the issue with that it dissipates more power and limit the bandwidth.

Instead, a pseudo-differential stage is used as the first stage of the limiting amplifier to do the voltage level shifting operation and be a part of the amplifier.

As previously the main path amplifiers use low threshold voltage devices and NPoly resistor with silicide for the load

The feedback path uses nominal threshold voltage devices and MIM capacitor and PPoly resistor without silicide for the LPF

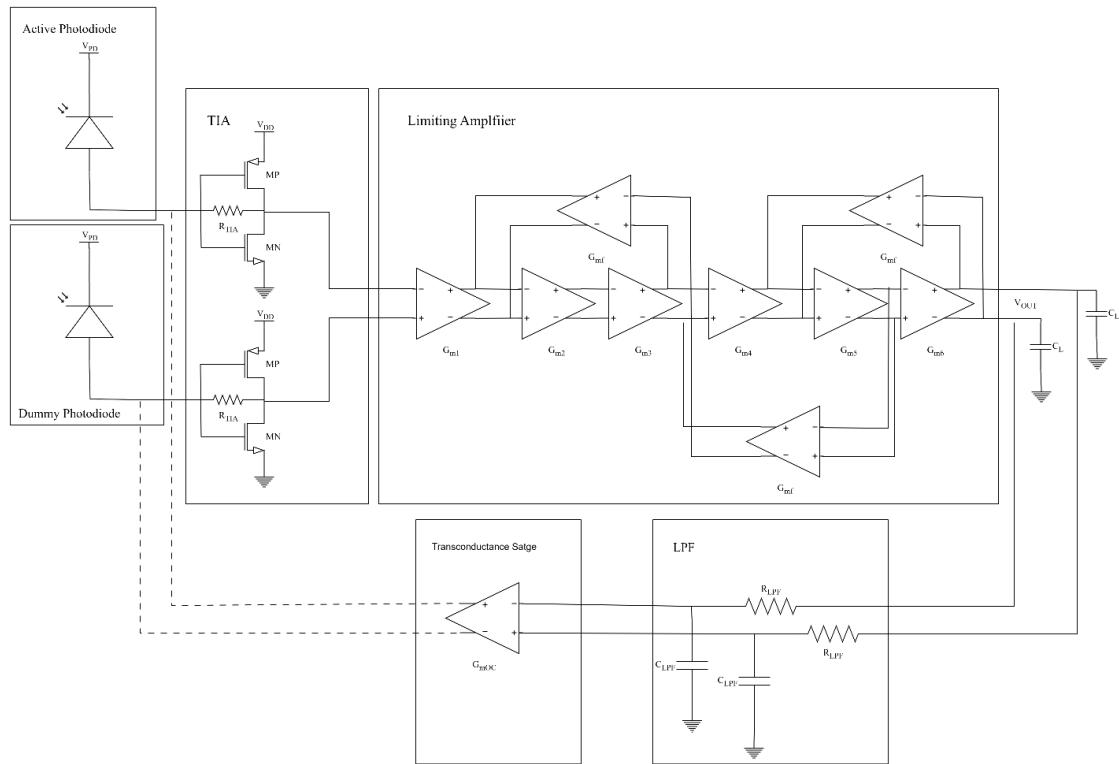


Figure 5.4. Differential analog front-end architecture

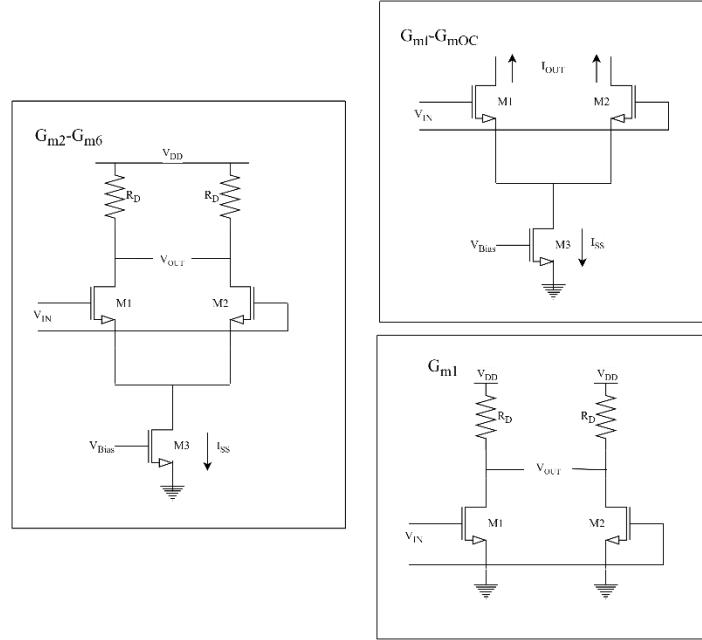


Figure 5.5. Differential analog front-end stages topologies

The amplifiers are using resistive load not active load to have a well-defined output dc level and reduce the system complexity as there's no need for common-mode feedback

Also, active loads tends to have higher parasitics which all add up to the output node reducing the speed and since resistors are linear devices the overall linearity of the system is better with resistive load

### Design Goals

Supply Voltage	1V
Baude rate	28 Gbaud/s
TIA bandwidth	12.3 GHz
Overall bandwidth	Approx. 12.3 GHz

### Circuit Parameters

W/L (TIA)	17.5 $\mu\text{m}$ /0.06 $\mu\text{m}$
TIA Feedback Resistance ( $R_F$ )	470 $\Omega$
W/L ( $G_{m1}$ )	12 $\mu\text{m}$ /0.06 $\mu\text{m}$
W/L ( $G_{m2}$ - $G_{m6}$ ) (M1-M2)	25.8 $\mu\text{m}$ /0.06 $\mu\text{m}$
$R_D$ ( $G_{m1}$ - $G_{m3}$ - $G_{m4}$ )	145 $\Omega$
$R_D$ ( $G_{m1}$ - $G_{m3}$ - $G_{m4}$ )	167 $\Omega$

W/L ( $G_{m2}$ - $G_{m6}$ ) (M3)	25.8 $\mu\text{m}/0.06 \mu\text{m}$
$I_{SS}$ ( $G_{m2}$ - $G_{m6}$ )	3 mA
W/L ( $G_{mf}$ ) (M1-M2)	2.5 $\mu\text{m}/0.06 \mu\text{m}$
W/L ( $G_{mf}$ ) (M3)	13.3 $\mu\text{m}/0.24 \mu\text{m}$
$I_{SS}$ ( $G_{mf}$ )	0.375 mA
$R_{LPF}$	3 M $\Omega$
$C_{LPF}$	1.5 pF
W/L ( $G_{mOC}$ ) (M1-M2-M3)	2 $\mu\text{m}/0.24 \mu\text{m}$
W/L ( $G_{mOC}$ ) (M3)	2.5 $\mu\text{m}/0.24 \mu\text{m}$
Load Capacitance ( $C_L$ )	50 fF
Photodiode Capacitance ( $C_{PD}$ )	100 fF

## Results

Total Small Signal Gain	72.1 dB $\Omega$
Total Transient Gain	69 dB $\Omega$
Total Bandwidth	11.5 GHz
Output Referred Noise	7.868 mV
Input Referred Noise	2.8 $\mu\text{A}$
Input Sensitivity (for BER = $10^{-12}$ )	39.2 $\mu\text{A}$
Power Consumption	22.98 mW
Energy Efficiency	0.821 pJ/bit
TIA Bandwidth	11.87 GHz
Limiting Amplifier Bandwidth	27.87 GHz

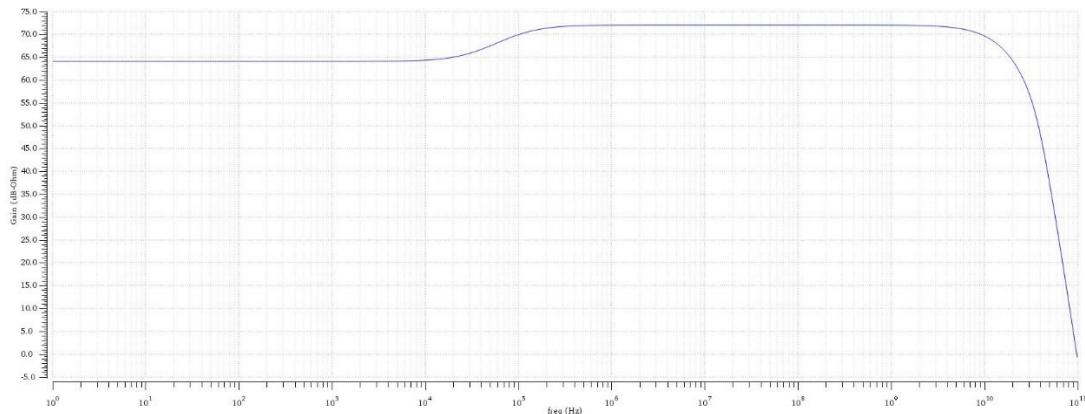


Figure 5.6. Design 5.2 overall frequency response with 76 kHz low cutoff frequency

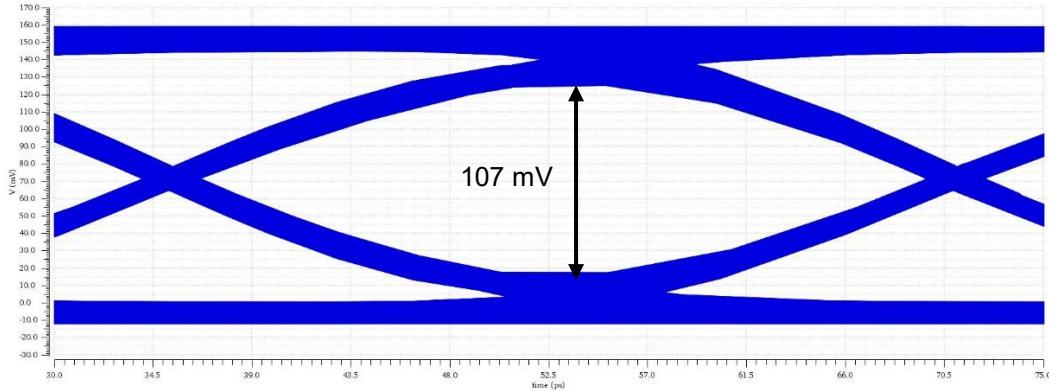


Figure 5.7. Design 5.2 Output eye diagram at input sensitivity level with 107 mV vertical opening

	Design in section 3.4	Design in section 3.5	Design in section 5.2
Architecture	Single ended w	Single ended with CTIE	Differential ended
Transient Gain ( $dB\Omega$ )	71.83	73.2	69
Bandwidth (GHz)	11.67	11.58	11.5
Input referred noise ( $\mu A$ )	1.98	1.24	2.8
Power dissipation (mW)	11.91	10.78	22.98
FoM (GHz.k $\Omega$ /mW. $\mu A$ )	1.93	3.96	0.5

The gain of differential is lower as the increase in sensitivity makes the input larger which requires less amplification

It appears that the differential system has a much worse performance, but the differential circuit is more immune to external disturbances and power supply variations

### 5.3. 56 Gb/s PAM-4 Differential Analog Front End

The system uses the same architecture in figure 5.4 with modification two the TIA and feedback path to accommodate the bandwidth requirements for PAM-4

Design Goals

Supply Voltage	1V
Baude rate	28 Gbaud/s
TIA bandwidth	14 GHz
Overall bandwidth	Approx. 14 GHz

Circuit Parameters

W/L (TIA)	22.5 $\mu m$ /0.06 $\mu m$
-----------	----------------------------

TIA Feedback Resistance ( $R_F$ )	365 $\Omega$
W/L ( $G_{m1}$ )	12 $\mu\text{m}/0.06 \mu\text{m}$
W/L ( $G_{m2}$ - $G_{m6}$ ) (M1-M2)	25.8 $\mu\text{m}/0.06 \mu\text{m}$
$R_D$ ( $G_{m1}$ - $G_{m3}$ - $G_{m4}$ )	145 $\Omega$
$R_D$ ( $G_{m1}$ - $G_{m3}$ - $G_{m4}$ )	167 $\Omega$
W/L ( $G_{m2}$ - $G_{m6}$ ) (M3)	25.8 $\mu\text{m}/0.06 \mu\text{m}$
$I_{SS}$ ( $G_{m2}$ - $G_{m6}$ )	3 mA
W/L ( $G_{mf}$ ) (M1-M2)	2.5 $\mu\text{m}/0.06 \mu\text{m}$
W/L ( $G_{mf}$ ) (M3)	13.3 $\mu\text{m}/0.24 \mu\text{m}$
$I_{SS}$ ( $G_{mf}$ )	0.375 mA
$R_{LPF}$	3 M $\Omega$
$C_{LPF}$	2 pF
W/L ( $G_{mOC}$ ) (M1-M2-M3)	2 $\mu\text{m}/0.24 \mu\text{m}$
W/L ( $G_{mOC}$ ) (M3)	2.5 $\mu\text{m}/0.24 \mu\text{m}$
Load Capacitance ( $C_L$ )	50 fF
Photodiode Capacitance ( $C_{PD}$ )	100 fF

## Results

Total Small Signal Gain	69.51 dB $\Omega$
Total Bandwidth	13.16 GHz
Output Referred Noise	6.858 mV
Power Consumption	23.84 mW
Energy Efficiency	0.425 pJ/bit
TIA Bandwidth	13.86 GHz
Limiting Amplifier Bandwidth	27.8 GHz

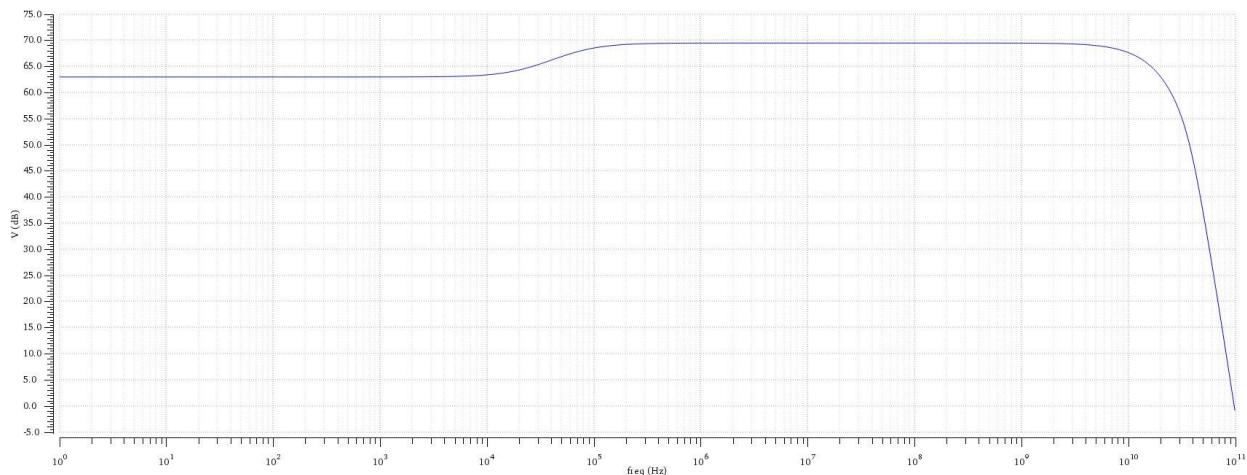


Figure 5.8. Design 5.3 overall frequency response with 44 kHz low cutoff frequency

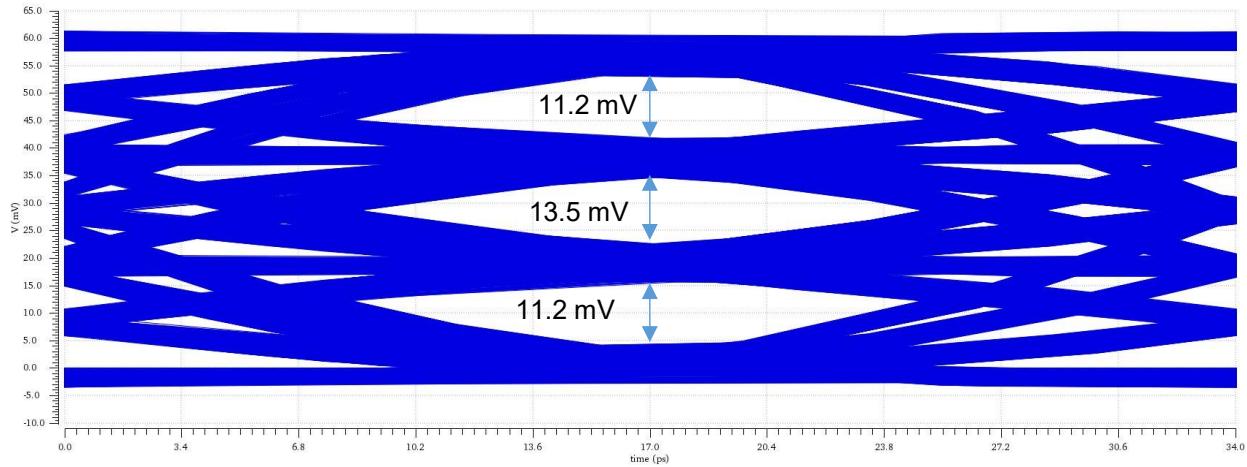


Figure 5.9. Design 5.3 Output eye diagram at  $20 \mu\text{A}$  input current

The PAM-4 system has nearly half the energy per bit when compared to NRZ system, when compared to single-ended system it has a worse performance but as discussed in 5.2 it has better immunity to external disturbances and power supply variations.

## Appendix A

### MOSFET Small Signal Model

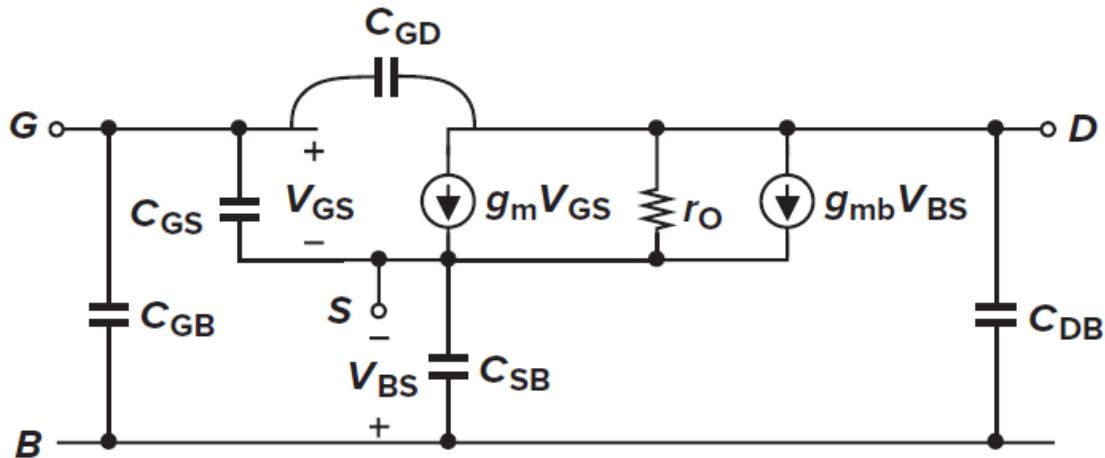


Figure A.1. Complete MOSFET small signal model with body effect

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$r_0 = \frac{\partial V_{DS}}{\partial I_D}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}}$$

## Appendix B.

# Differential Circuits and Signaling

True Differential Amplifiers are constructed by two basic amplifier stages coupled by a current source to have a well-defined common mode level

A single ended signal is a signal that is measured in respect to a fixed potential in the system.

$$x_{SE} = x_{sig} - x_{ref}$$

A differential signal is a signal measured between two nodes having equal potential with equal magnitude and opposite polarities

$$x_{DE} = x_+ - x_-.$$

Where,  $x_+ = -x_- = \frac{1}{2}x_{sig}$

The average potential of differential signals is known as common mode level.

$$x_{CM} = \frac{x_+ + x_-}{2}.$$

$$x_+ = \frac{x_{sig}}{2} + x_{CM}.$$

$$x_- = \frac{-x_{sig}}{2} + x_{CM}.$$

Differential amplifiers consume more power and take more area compared to single-ended amplifiers, but they have a great immunity to external noise.

Unlike internal noise that affect every device differently external noise coming from the power supply or EMI affect adjacent circuits similarly.

Since the effect is the same this noise disrupts the two nodes of the differential signal with equal amounts, so this distribution appears in the common mode level

$$x_{CM} = \frac{x_+ + x_-}{2} + x_n.$$

So, when the differential signal is measuring the common mode noise at each node of the signal cancels each other and it's called common mode noise rejection

There are two parameters that characterize a differential amplifier quality of common mode noise rejection, common mode rejection ratio (CMRR) and power rejection ratio (PSSR)

CMRR is defined as the gain of the differential signal ( $A_d$ ) by the gain of the common mode signal ( $A_{CM}$ )

$$CMMR = 20 \log \left( \frac{A_d}{A_{CM}} \right). \quad (27)$$

Ideally  $A_{CM}$  is supposed to be zero making the ratio tends to infinity but in order for that the circuit has to be perfectly symmetrical, so it has the same effect in common mode signal in both nodes, practically the circuits have slight mismatch because of fabrication issues that cause a small common mode gain

PSSR characterizes how the amplifier rejects the noise specifically coming from the powers supply and is defined as the ratio between the gain from the input to the output and the gain from the power supply to the output

## Appendix C

### Verilog-A Code for NRZ Pseudo-Random Bits Generation

```

`include "discipline.h"
`include "constants.h"

(* instrument_module *)
module rand_bit_stream (vout);

output vout;
electrical vout;
parameter real tperiod = 1 from (0:inf);
parameter integer seed = 21;
parameter real vlogic_high = 5;
parameter real vlogic_low = 0 ;
parameter real tdel=0 from [0:inf];
parameter real trise=1n;
parameter real tfall=1n;
real next;
integer bit;
real vout_val;
integer iseed;
analog begin
@ ( initial_step ) begin
next = $abstime + tperiod;
bit = 0;
iseed = seed;
vout_val = vlogic_low;
end
$bound_step(tperiod);
bit = abs($random(iseed)) & 1;
@ ( timer( next ) ) begin
vout_val = (vlogic_high - vlogic_low) * bit + vlogic_low;
next = next + tperiod;
end
V(vout) <+ transition(vout_val,tdel,trise,tfall);
end

endmodule

```

## Appendix D

### Verilog-A Code for PAM-4 Pseudo-Random Symbol Generation

```

`include "discipline.h"
`include "constants.h"

(* instrument_module *)
module rand_pam4_stream(vout);

output vout;
electrical vout;
parameter real tperiod = 1 from (0:inf);
parameter integer seed = 42;
parameter real level_00 = -3.0;
parameter real level_01 = -1.0;
parameter real level_10 = 1.0;
parameter real level_11 = 3.0;
parameter real tdel=0 from [0:inf];
parameter real trise=1n;
parameter real tfall=1n;
real next_time;
real pam4_val;
integer rand_val;
integer iseed;
analog begin
@(initial_step) begin
next_time = $abstime + tperiod;
iseed = seed;
pam4_val = level_00; // start at some valid level
end
$bound_step(tperiod);
rand_val = abs($random(iseed)) % 4;
@(timer(next_time)) begin
case (rand_val)
0: pam4_val = level_00;
1: pam4_val = level_01;
2: pam4_val = level_10;
3: pam4_val = level_11;
default: pam4_val = 0.0;
endcase
next_time = next_time + tperiod;
end
V(vout) <+ transition(pam4_val, tdel, trise, tfall);
end

endmodule

```

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