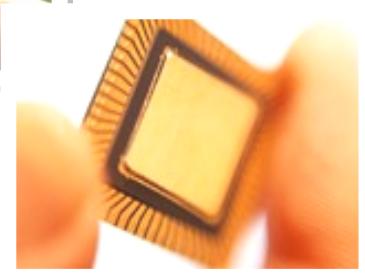
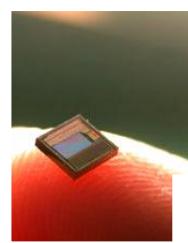
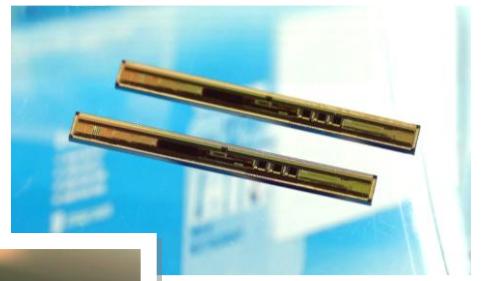


瑞鼎科技股份有限公司
Raydium Semiconductor Corporation

RM69310 User Guide

Single Chip Driver
with 16.7M color
for 240RGBx240 AMOLED



Revision : 0.2

Date : Sep. 09, 2016

On/Revision History

Version	Date	Prepared By	Checked By	Description	page
V0.1	2016/07/29	CL Huang		First Release	
V0.2	2016/9/07	CL Huang			

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1. Manufacture Command Set (MCS)

1.1 Command Control (FE00h): CMD Mode Switch

FE00H		CMD Mode Switch																											
Instruction	R/W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
CMD Mode Switch	W	FEh	FE00h	00h	0	0	0	0	CMD_Page[3:0]			00																	
Description	This command is used to switch the Manufacture Command Pages and User Commands sets.																												
	<table border="1"> <thead> <tr> <th>CMD_Page[3:0]</th><th>Hex Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000</td><td>00h (default)</td><td>User Command Set (UCS = CMD1)</td></tr> <tr> <td>0001</td><td>01h</td><td>Manufacture Command Set Page0 (CMD2 P0)</td></tr> <tr> <td>0010</td><td>02h</td><td>Manufacture Command Set Page1 (CMD2 P1)</td></tr> <tr> <td>0011</td><td>03h</td><td>Manufacture Command Set Page2 (CMD2 P2)</td></tr> <tr> <td>0100</td><td>04h</td><td>Manufacture Command Set Page3 (CMD2 P3)</td></tr> </tbody> </table>												CMD_Page[3:0]	Hex Value	Description	0000	00h (default)	User Command Set (UCS = CMD1)	0001	01h	Manufacture Command Set Page0 (CMD2 P0)	0010	02h	Manufacture Command Set Page1 (CMD2 P1)	0011	03h	Manufacture Command Set Page2 (CMD2 P2)	0100	04h
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Sleep In	Yes																												

Default	Status	Default Value
		FEh / FE00h
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

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(FF00h): Read CMD Status

FF00H		RD CMD Status																													
Instruction	R/W	Address		Parameter																											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
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Sleep In	Yes																														
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S/W Reset	00h																														
H/W Reset	00h																														

1.2 MTP Program Flow

1.2.1 CMD2 Program Flow

CMD2 MTP Summary Table Programmed by Customer

CMD2 Page0: Display Option, Power etc.

Reg 0x0440h ~ 0xE740h

Total Program Count = **2**

1st Enable Program => **CMD2 Page0 Reg 0xF040h, D[5]=OTP_cmd2_P0_PGM_EN**
1st Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[5]=CMD2_P0_1st_Done**

2nd Enable Program => **CMD2 Page0 Reg 0xF040h, D[5]=OTP_cmd2_P0_PGM_EN**
2nd Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[6]=CMD2_P0_2nd_Done**

CMD2 Page1: Gamma1 etc.

Reg 0x0050h ~ 0x9B50h

Total Program Count = **2**

1st Enable Program => **CMD2 Page0 Reg 0xF040h, D[4]=OTP_cmd2_P1_PGM_EN**
1st Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[4]=CMD2_P1_1st_Done**

2nd Enable Program => **CMD2 Page0 Reg 0xF040h, D[4]=OTP_cmd2_P1_PGM_EN**
2nd Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[3]=CMD2_P1_2nd_Done**

CMD2 Page2: Gamma2 etc.

Reg 0x0060h ~ 0x9B60h

Total Program Count = **2**

1st Enable Program => **CMD2 Page0 Reg 0xF040h, D[3]=OTP_cmd2_P2_PGM_EN**
1st Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[2]=CMD2_P2_1st_Done**

2nd Enable Program => **CMD2 Page0 Reg 0xF040h, D[3]=OTP_cmd2_P2_PGM_EN**
2nd Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[1]=CMD2_P2_2nd_Done**

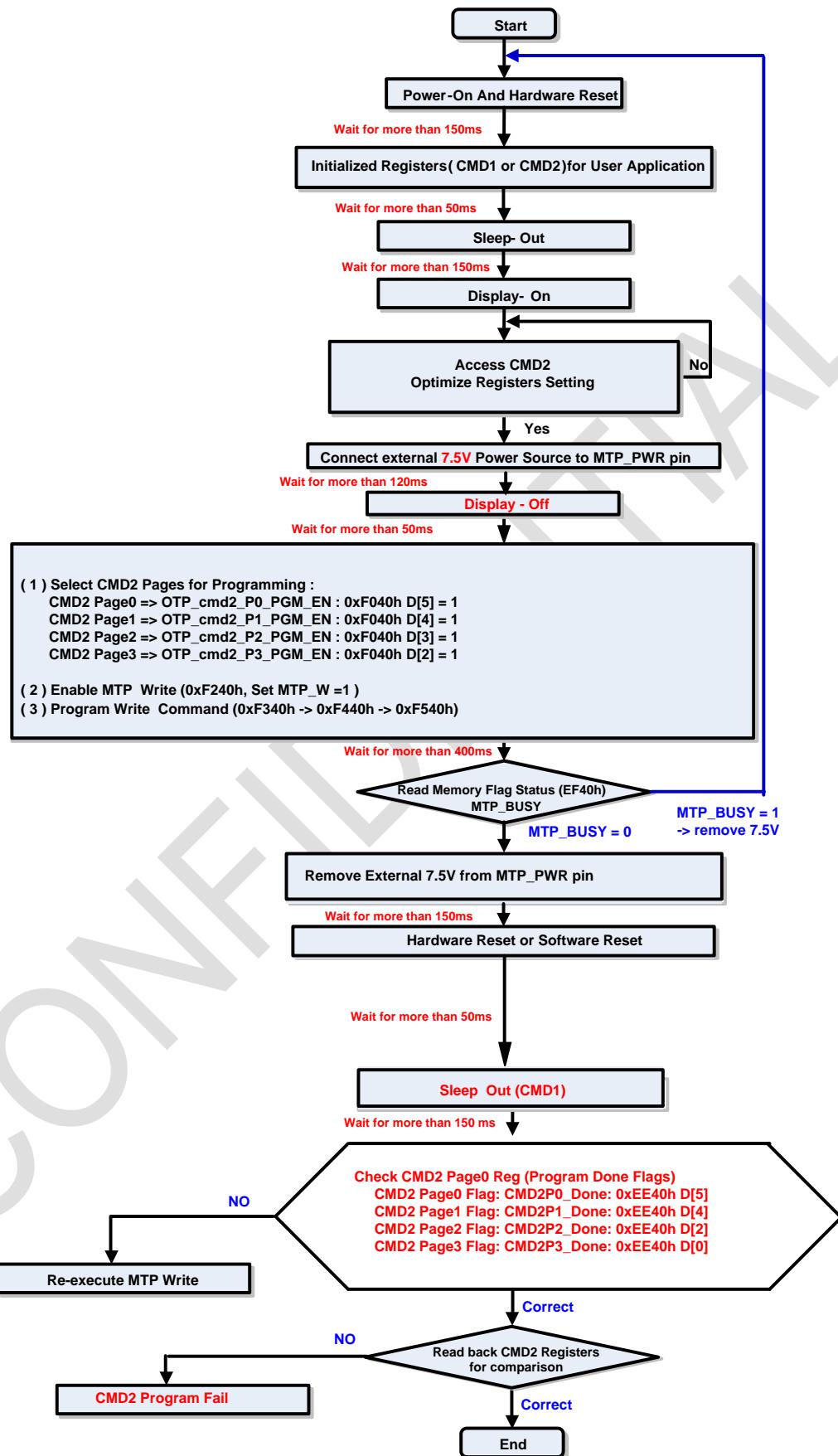
CMD2 Page3: VSR

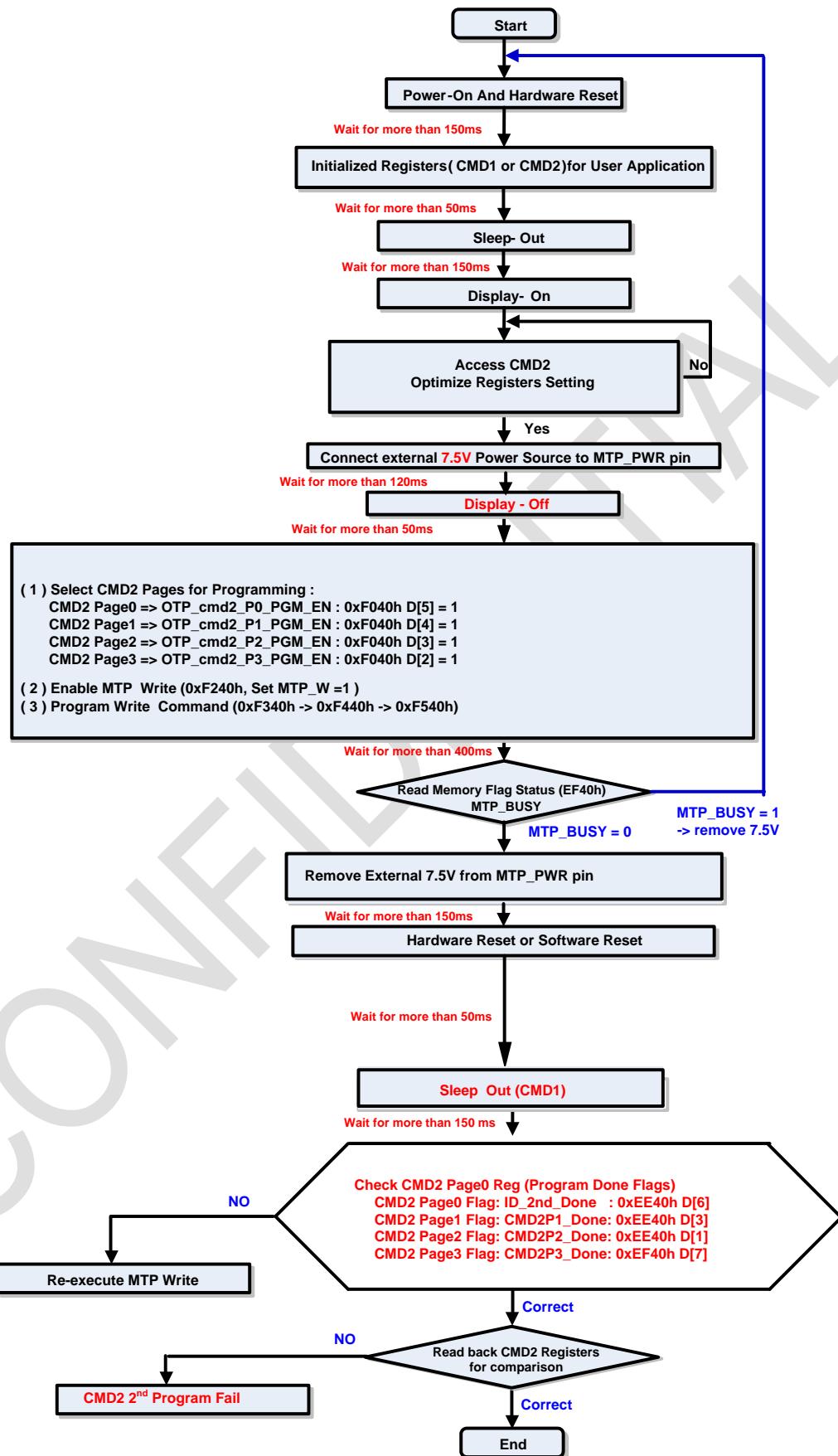
Reg 0x0070h ~ 0x6F70h

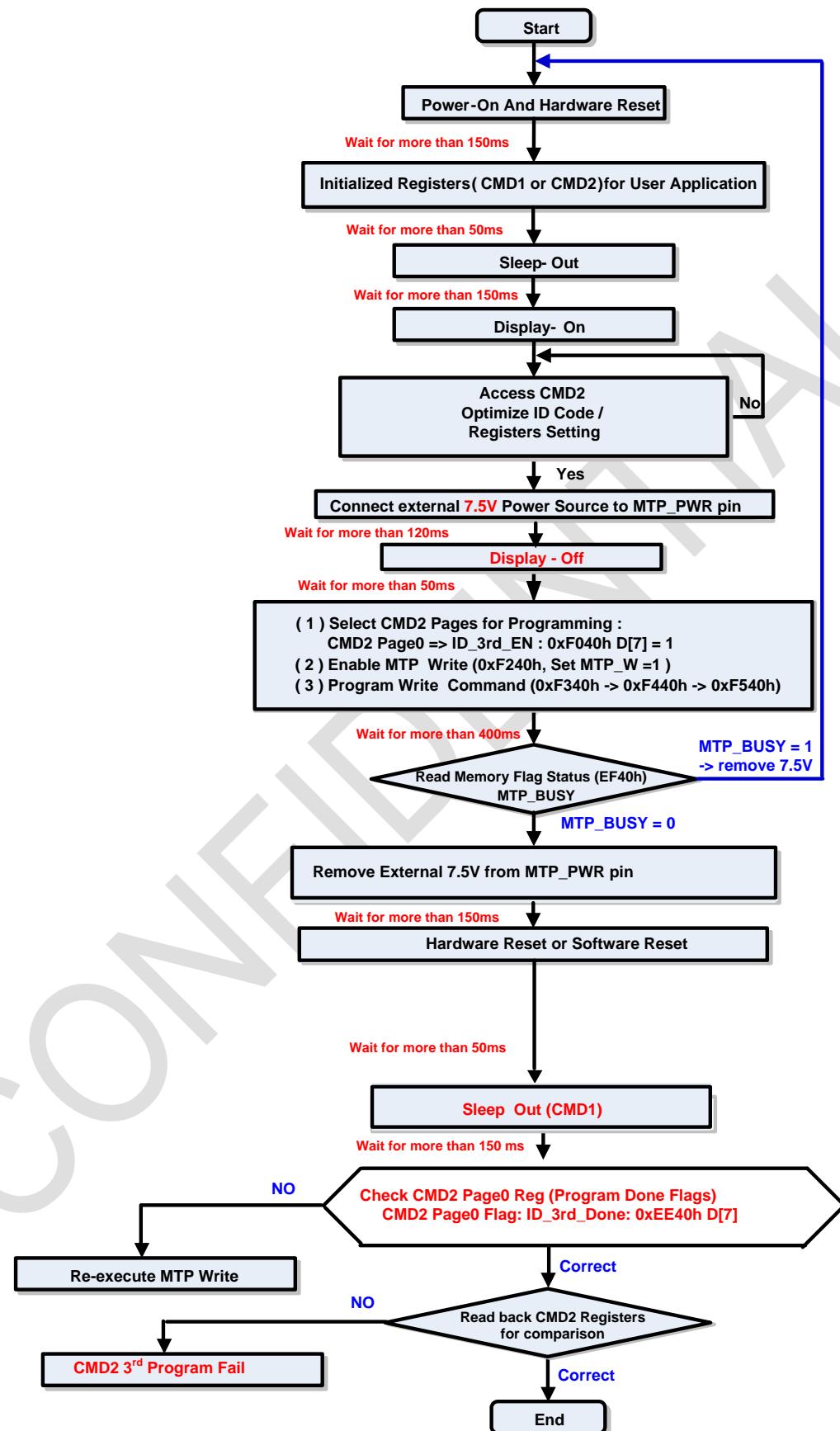
Total Program Count = **2**

1st Enable Program => **CMD2 Page0 Reg 0xF040h, D[2]=OTP_cmd2_P3_PGM_EN**
1st Program Done Flag => **CMD2 Page0 Reg 0xEE40h, D[0]=CMD2_P3_1st_Done**

2nd Enable Program => **CMD2 Page0 Reg 0xF040h, D[2]=OTP_cmd2_P3_PGM_EN**
2nd Program Done Flag => **CMD2 Page0 Reg 0xEF40h, D[7]=CMD2_P3_2nd_Done**







1.3 MCS: CMD2 Page0 = Display Options + Power

Manufacture Command Set (CMD2 Page0 Display+Power)																			
Instruction	R/W	Address		Parameter									Function						
		MIPi	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0							
SPIWRAM	R/W	0x04h	0x0440h	0	SPI_WRA M	-	-	-	-	-	-	-	SPI Write SRAM						
CGMCTR	R/W	0x05h	0x0540h	0	-	CGM[2:0]			CTB	CRL[1:0]		CREV	Display Resolution Panel Option						
DPRSLCTR	R/W	0x06h	0x0640h	0	NL[7:0]									Display Resolution Panel Option					
TE1CTR	R/W	0x07h	0x0740h	0	TE1_POSE_SEL[7:0]									TE1 Output Setting					
TE1CTR	R/W	0x08h	0x0840h	0	TE1_period[7:0]									TE1 Output Setting					
TE1CTR	R/W	0x09h	0x0940h	0	TE1_POSE_SEL[9: 8]	TE1_period[9:8]		TE1_po I	TE1_EN	-	-	-	TE1 Output Setting						
HSIFOPCTR Control	R/W	0x0Ah	0x0A40h	0	DSITE	DIS_EoT p_HS	DSIG	N565	DSIM	-	-	-	MIPI Control						
HSIFOPCTR Control	R/W	0x0Bh	0x0B40h	0	Iptx_freq_sel[1:0]	Iptx_TAGETD_s el[1:0]	Iptx_TAGOD_sel [1:0]	-	-	-	-	-	MIPI Control						
HSIFOPCTR Control	R/W	0x0Ch	0x0C40h	0	-	-	tato_en	Iptxto_ en	hsrxto_ en	-	vcid[1:0]	-	MIPI Control						
BT1CTR	R/W	0x0Eh	0x0E40h	0	DC1A[2:0]			VDHA[4:0]					AVDD Charge Pump Control Normal Mode						
BT1CTRIDM	R/W	0x0Fh	0x0F40h	0	DC1B[2:0]			VDHB[4:0]					AVDD Charge Pump Control Idle Mode						
BT1BT3REGEN	R/W	0x10h	0x1040h	0	-	BT_DHA	BT_DH B	EN_PU MP_VC LREG	-	-	-	EN_PUM P_DDWD HREG	AVDD/VCL Regulator Enable						
BT3CTR	R/W	0x11h	0x1140h	0	DC3A[2:0]			BT_VC LA	-	-	-	DVCLA[1:0]	VCL Charge Pump Control Normal Mode						
BT3CTRIDM	R/W	0x12h	0x1240h	0	DC3B[2:0]			BT_VC LB	-	-	-	DVCLB[1:0]	VCL Charge Pump Control Idle Mode						
BT4CTR	R/W	0x13h	0x1340h	0	DC4A[2:0]			-	-	-	-	BT_VGHA[1:0]	VGH Charge Pump Clock						
BT4CTRIDM	R/W	0x14h	0x1440h	0	DC4B[2:0]			-	-	-	-	BT_VGHB[1:0]	VGH Charge Pump Control Idle Mode						
BT5CTR	R/W	0x15h	0x1540h	0	DC5A[2:0]			-	-	-	-	BT_VGLA[1:0]	VGL Charge Pump Clock						
BT5CTRIDM	R/W	0x16h	0x1640h	0	DC5B[2:0]			-	-	-	-	BT_VGLB[1:0]	VGL Charge Pump Clock Idle Mode						
SETVGHR	R/W	0x18h	0x1840h	0	VGHREGB[3:0]				VGHREGA[3:0]				VGHR Control						
SETVGLR	R/W	0x19h	0x1940h	0	VGLREGB[3:0]				VGLREGA[3:0]				VGHL Control						
SWEQCTR	R/W	0x1Dh	0x1D40h	0	-	-	GREQ_SW[5:0]						SW EQ Control						
SWEQCTR	R/W	0x1Eh	0x1E40h	0	-	-	GFEQ_SW[5:0]						SW EQ Control						
VSREQCTR	R/W	0x1Fh	0x1F40h	0	-	-	GREQ_VSR[5:0]						VSR EQ Control						
VSREQCTR	R/W	0x20h	0x2040h	0	-	-	GFEQ_VSR[5:0]						VSR EQ Control						
LFRCTR1	R/W	0x25h	0x2540h	0	GMA2_E N_A	VFPDA[8]	D_CM_A[1:0]	PSEL_A[1:0]	T1A[9:8]			Low Frame Rate Control Normal Mode							
LFRCTR2	R/W	0x26h	0x2640h	0	T1A[7:0]									Low Frame Rate Control Normal Mode					

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Manufacture Command Set (CMD2 Page0 Display+Power)																		
Instruction	R/W	Address		Parameter								Function						
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1							
LFRCTR3	R/W	0x27h	0x2740h	0	VBPDA[7:0]								Low Frame Rate Control Normal Mode					
LFRCTR4	R/W	0x28h	0x2840h	0	VFPDA[7:0]								Low Frame Rate Control Normal Mode					
LFRCTRIDM1	R/W	0x2Ah	0x2A40h	0	GMA2_E_N_B	VFPDB[8]	D_CM_B[1:0]	PSELB[1:0]	T1B[9:8]			Low Frame Rate Control IDLE Mode						
LFRCTRIDM2	R/W	0x2Bh	0x2B40h	0	T1B[7:0]								Low Frame Rate Control IDLE Mode					
LFRCTRIDM3	R/W	0x2Dh	0x2D40h	0	VBPDB[7:0]								Low Frame Rate Control IDLE Mode					
LFRCTRIDM4	R/W	0x2Fh	0x2F40h	0	VFPDB[7:0]								Low Frame Rate Control IDLE Mode					
SGOPCTR	R/W	0x36h	0x3640h	0	-	AP_A[2:0]		PTD	AP_B[2:0]			Source Bias Current						
SWTIMCTR1	R/W	0x3Ah	0x3A40h	0	T1_sd[7:0]								Switch Timing					
SWTIMCTR2	R/W	0x3Bh	0x3B40h	0	Tp_sd[7:0]								Switch Timing					
SWTIMCTR3	R/W	0x3Dh	0x3D40h	0	Th_sd[7:0]								Switch Timing					
SWTIMCTR4	R/W	0x3Fh	0x3F40h	0	Tsw_sd[7:0]								Switch Timing					
SWTIMCTR5	R/W	0x40h	0x4040h	0	Thsw_sd[7:0]								Switch Timing					
SWTIMCTR6	R/W	0x41h	0x4140h	0	Thsd_sd[7:0]								Switch Timing					
SWSELCTR1	R/W	0x42h	0x4240h	0	SW_step1_of_ol[3:0]				SW_step1_of_el[3:0]			Switch Selection						
SWSELCTR2	R/W	0x43h	0x4340h	0	SW_step2_of_ol[3:0]				SW_step2_of_el[3:0]			Switch Selection						
SWSELCTR3	R/W	0x44h	0x4440h	0	SW_step3_of_ol[3:0]				SW_step3_of_el[3:0]			Switch Selection						
SWSELCTR4	R/W	0x45h	0x4540h	0	SW_step4_of_ol[3:0]				SW_step4_of_el[3:0]			Switch Selection						
SWSELCTR5	R/W	0x46h	0x4640h	0	SW_step5_of_ol[3:0]				SW_step5_of_el[3:0]			Switch Selection						
SWSELCTR6	R/W	0x47h	0x4740h	0	SW_step6_of_ol[3:0]				SW_step6_of_el[3:0]			Switch Selection						
SWSELCTR7	R/W	0x48h	0x4840h	0	SW_step1_ef_ol[3:0]				SW_step1_ef_el[3:0]			Switch Selection						
SWSELCTR8	R/W	0x49h	0x4940h	0	SW_step2_ef_ol[3:0]				SW_step2_ef_el[3:0]			Switch Selection						
SWSELCTR9	R/W	0x4Ah	0x4A40h	0	SW_step3_ef_ol[3:0]				SW_step3_ef_el[3:0]			Switch Selection						
SWSELCTR10	R/W	0x4Bh	0x4B40h	0	SW_step4_ef_ol[3:0]				SW_step4_ef_el[3:0]			Switch Selection						
SWSELCTR11	R/W	0x4Ch	0x4C40h	0	SW_step5_ef_ol[3:0]				SW_step5_ef_el[3:0]			Switch Selection						
SWSELCTR12	R/W	0x4Dh	0x4D40h	0	SW_step6_ef_ol[3:0]				SW_step6_ef_el[3:0]			Switch Selection						
SWSELCTR13	R/W	0x4Eh	0x4E40h	0	SD_step1_of_ol[3:0]				SD_step1_of_el[3:0]			Switch Selection						
SWSELCTR14	R/W	0x4Fh	0x4F40h	0	SD_step2_of_ol[3:0]				SD_step2_of_el[3:0]			Switch Selection						
SWSELCTR15	R/W	0x50h	0x5040h	0	SD_step3_of_ol[3:0]				SD_step3_of_el[3:0]			Switch Selection						

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Manufacture Command Set (CMD2 Page0 Display+Power)																		
Instruction	R/W	Address		Parameter									Function					
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0						
SWSELCTR16	R/W	0x51h	0x5140h	0	SD_step4_of_ol[3:0]					SD_step4_of_el[3:0]			Switch Selection					
SWSELCTR17	R/W	0x52h	0x5240h	0	SD_step5_of_ol[3:0]					SD_step5_of_el[3:0]			Switch Selection					
SWSELCTR18	R/W	0x53h	0x5340h	0	SD_step6_of_ol[3:0]					SD_step6_of_el[3:0]			Switch Selection					
SWSELCTR19	R/W	0x54h	0x5440h	0	SD_step1_ef_ol[3:0]					SD_step1_ef_el[3:0]			Switch Selection					
SWSELCTR20	R/W	0x55h	0x5540h	0	SD_step2_ef_ol[3:0]					SD_step2_ef_el[3:0]			Switch Selection					
SDSELCTR1	R/W	0x56h	0x5640h	0	SD_step3_ef_ol[3:0]					SD_step3_ef_el[3:0]			Source Data Selection					
SDSELCTR1	R/W	0x57h	0x5740h	0	SD_step4_ef_ol[3:0]					SD_step4_ef_el[3:0]								
SDSELCTR2	R/W	0x58h	0x5840h	0	SD_step5_ef_ol[3:0]					SD_step5_ef_el[3:0]			Source Data Selection					
SDSELCTR3	R/W	0x59h	0x5940h	0	SD_step6_ef_ol[3:0]					SD_step6_ef_el[3:0]			Source Data Selection					
SDSELCTR5	R/W	0x5Bh	0x5B40h	0	-	-	-	VREFN5 EN	-	-	-	VREFP5 EN	Source Data Selection					
SDSELCTR8	R/W	0x5Eh	0x5E40h	0	-	-	-	VP5REGA[5:0]					Source Data Selection					
SDSELCTR9	R/W	0x5Fh	0x5F40h	0	-	-	-	VP5REGB[5:0]					Source Data Selection					
SDSELCTR10	R/W	0x62h	0x6240h	0	-	-	-	VN5REGA[5:0]					Source Data Selection					
SDSELCTR11	R/W	0x63h	0x6340h	0	-	-	-	VN5REGB[5:0]					Source Data Selection					
SDSELCTR15	R/W	0x69h	0x6940h	0	-	swire_0 ff	-	-	-	-	-	-	Source Data Selection					
OVSSCTR	R/W	0x73h	0x7340h	0	-	-	-	OVSS_REG[5:0]					OVSS Control					
VGMPTR	R/W	0x89h	0x8940h	0	VGMPTR[7:0]								VGMP Control					
VGSPTR	R/W	0x8Ah	0x8A40h	0	VGS PTR[7:0]								VGSP Control					
VGMSPTR	R/W	0x8Bh	0x8B40h	0	-	-	-	VGSPT R[8]	-	-	-	VGMPT R[8]	VGMSP Control					
VGMPTR	R/W	0x8Ch	0x8C40h	0	VGMPTR2[7:0]								VGMP Control					
VGS PTR	R/W	0x8Dh	0x8D40h	0	VGS PTR2[7:0]								VGSP Control					
VGMSPTR	R/W	0x8Eh	0x8E40h	0	-	-	-	VGSPT R2[8]	-	-	-	VGMPT R2[8]	VGMSP Control					
RDICID	R	0xDEh	0xDE40h	0	ID41[7:0]									IC Chip Code				
RDICID	R	0xDFh	0xDF40h	0	ID42[7:0]									IC Chip Code				
RDICVERCODE	R	0xE0h	0xE040h	0	IC_VERSION_Customer[7:0]									IC Version Code Information				
WRDDB	R/W	0xE1h	0xE140h	0	SID[15:8]									IC ID Code Information				
WRDDB	R/W	0xE2h	0xE240h	0	SID[7:0]									IC ID Code Information				
WRDDB	R/W	0xE3h	0xE340h	0	MID[15:8]									IC ID Code Information				
WRDDB	R/W	0xE4h	0xE440h	0	MID[7:0]									IC ID Code Information				

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Manufacture Command Set (CMD2 Page0 Display+Power)															
Instruction	R/W	Address		Parameter									Function		
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0			
WRDID	R/W	0xE5h	0xE540h	0	ID1[7:0]									ID1 code	
WRDID	R/W	0xE6h	0xE640h	0	ID2[7:0]									ID2 code	
WRDID	R/W	0xE7h	0xE740h	0	ID3[7:0]									ID3 code	
RDMTPCMP1	R	0xECCh	0xED40h	0	-	-	-	-	-	-	-	-	cmp_ck_sum		
RDMTPFLG1	R	0xEEh	0xEE40h	0	CMD2P0_3rd_Done	CMD2P0_2nd_Done	CMD2P0_1st_Done	CMD2P1_1st_Done	CMD2P1_2nd_Done	CMD2P2_1st_Done	CMD2P2_2nd_Done	CMD2P3_1st_Done	MTP Flag Check		
RDMTPFLG2	R	0xEFh	0xEF40h	0	CMD2P3_2nd_Done	-	-	-	-	-	MTP_B_USY	-	MTP Flag Check		
MTPCTR	R/W	0xF0h	0xF040h	0	OTP_cmd2_P0_PGM_M_3rdEN	-	OTP_cmd2_P0_PGM_EN	OTP_cmd2_P1_PGM_EN	OTP_cmd2_P2_PGM_EN	OTP_cm2_P3_PGM_EN	-	-	MTP Control		
MTPW	R/W	0xF2h	0xF240h	0	-	-	-	-	-	-	1	MTP_W	MTP Control		
MTPW1	W	0xF3h	0xF340h	0	MTP_KEY1[7:0]									MTP Control	
MTPW2	W	0xF4h	0xF440h	0	MTP_KEY2[7:0]									MTP Control	
MTPW3	W	0xF5h	0xF540h	0	MTP_KEY3[7:0]									MTP Control	
CMD Mode Switch	R/W	0xFEh	0xFE40h	0	-	-	-	-	-	CMD_Page_Selection[3:0]		CMD Mode Switch			
RD CMD Status	R	0xFFh	0xFF40h	0	-	-	-	-	-	Current_CMD_Page[3:0]		RD CMD Status			

(0440h) SPI Write SRAM

		SPIWRAM																								
Instruction	R/W	Address		Parameter																						
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
SPIWRAM	R/W	0x04h	0x0440h	00h	SPI_WRAM	-	1	-	-	-	-	-	0x20h													
Description	This command is used in SPI/SPINK interfaces. Making sure to set SPI_WRAM equal to 1 before host writes SRAM via SPI/SPINK interfaces.																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
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(0540h) Display Resolution Panel Option

		CGMCTR																																																																											
Instruction	R/ W	Address		Parameter																																																																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																
CGMCTR	R/ W	0x05 h	0x0540h	00h	-	CGM[2:0]			CTB	CRL[1:0]		CREV	0x50h																																																																
Description	This command is used as below,																																																																												
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CREV	<table border="1"> <tr> <td colspan="3">Display data reversed selection for NB/NW panel type. This bit is XOR operation with INVON/OFF commands.</td><td colspan="10"> <table border="1"> <tr> <th>CREV</th> <th>INVON</th> <th>Display Data</th> </tr> <tr> <td>0</td> <td>0</td> <td>No reversion (NW)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reversion (NB)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reversion (NB)</td> </tr> <tr> <td>1</td> <td>1</td> <td>No reversion (NW)</td> </tr> </table> </td></tr> </table>	Display data reversed selection for NB/NW panel type. This bit is XOR operation with INVON/OFF commands.			<table border="1"> <tr> <th>CREV</th> <th>INVON</th> <th>Display Data</th> </tr> <tr> <td>0</td> <td>0</td> <td>No reversion (NW)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reversion (NB)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reversion (NB)</td> </tr> <tr> <td>1</td> <td>1</td> <td>No reversion (NW)</td> </tr> </table>										CREV	INVON	Display Data	0	0	No reversion (NW)	0	1	Reversion (NB)	1	0	Reversion (NB)	1	1	No reversion (NW)																																																
Display data reversed selection for NB/NW panel type. This bit is XOR operation with INVON/OFF commands.			<table border="1"> <tr> <th>CREV</th> <th>INVON</th> <th>Display Data</th> </tr> <tr> <td>0</td> <td>0</td> <td>No reversion (NW)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reversion (NB)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reversion (NB)</td> </tr> <tr> <td>1</td> <td>1</td> <td>No reversion (NW)</td> </tr> </table>										CREV	INVON	Display Data	0	0	No reversion (NW)	0	1	Reversion (NB)	1	0	Reversion (NB)	1	1	No reversion (NW)																																																		
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Restriction

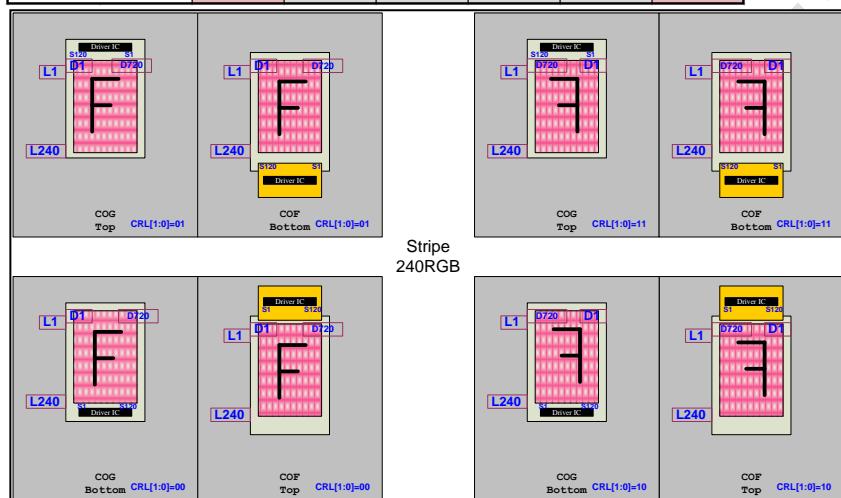
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

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	Sleep In	Yes
Default	Status Power On Sequence S/W Reset H/W Reset	Default Value 0x05h / 0x0540h 0x50h 0x50h 0x50h

CH	Left side			Right side		
	120~89	88~75	74~61	60~45	44~33	32~1
CGM						
101 is 240RGB	1	1	1	1	1	1
110 is 180RGB	1	1	0	0	1	1
111 is 128RGB	1	0	0	0	0	1



(0640h) Display Resolution Panel Option

	DPRSLCTR																																				
Instruction	R/W	Address		Parameter																																	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
DPRSLCTR	R/W	0x06h	0x0640h	00h	NL[7:0]						0x3Ch																										
Description	This command is used to vertical scan line for Display.																																				
	<table border="1"> <thead> <tr> <th>Bit</th><th colspan="2">Value</th><th colspan="2">Display Scan Line Number</th></tr> </thead> <tbody> <tr> <td rowspan="6">NL[7:0]</td><td>00h</td><td>Reserved</td><td colspan="2">Reserved</td></tr> <tr> <td>01h</td><td>1</td><td colspan="2">4 lines</td></tr> <tr> <td>02h</td><td>2</td><td colspan="2">8 lines</td></tr> <tr> <td>:</td><td>:</td><td colspan="2">$= 4 * NL[7:0]$</td></tr> <tr> <td>3Ch</td><td>60</td><td colspan="2" rowspan="4">240 lines</td></tr> </tbody> </table>												Bit	Value		Display Scan Line Number		NL[7:0]	00h	Reserved	Reserved		01h	1	4 lines		02h	2	8 lines		:	:	$= 4 * NL[7:0]$		3Ch	60	240 lines
Bit	Value		Display Scan Line Number																																		
NL[7:0]	00h	Reserved	Reserved																																		
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	:	:	$= 4 * NL[7:0]$																																		
	3Ch	60	240 lines																																		
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Status	Availability																																				
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Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td colspan="2">0x06h / 0x0640h</td></tr> <tr> <td>Power On Sequence</td><td>0x64h</td></tr> <tr> <td>S/W Reset</td><td>0x64h</td></tr> <tr> <td>H/W Reset</td><td>0x64h</td></tr> </tbody> </table>												Status	Default Value	0x06h / 0x0640h		Power On Sequence	0x64h	S/W Reset	0x64h	H/W Reset	0x64h															
Status	Default Value																																				
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Power On Sequence	0x64h																																				
S/W Reset	0x64h																																				
H/W Reset	0x64h																																				

(0740h) TE1 Output Setting

		TE1CTR																						
Instruction	R/W	Address		Parameter																				
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
TE1CTR	R/W	0x07h	0x0740h	00h	TE1_POSE_SEL[7:0]										0x00h									
		This command is to select the transient edge of TE1 signal. The timing reference start point is internal Hsync, and 1 clock period is 50ns.																						
Description				Bit		Value		Description																
				STB_POSE_SEL[9:0]	0	000h	0 Clocks																	
					1	001h	1 Clock = 50ns																	
					:	:	50 ns / Clock																	
					Reserved		Reserved																	
		TE1_POSE_SEL + TE1_period < T1A TE1_POSE_SEL + TE1_period < T1B																						
				Status		Availability																		
				Normal Mode On, Idle Mode Off, Sleep Out		Yes																		
				Normal Mode On, Idle Mode On, Sleep Out		Yes																		
				Partial Mode On, Idle Mode Off, Sleep Out		Yes																		
				Partial Mode On, Idle Mode On, Sleep Out		Yes																		
				Sleep In		Yes																		
Default				Status		Default Value																		
				0x07h / 0x0740h																				
				Power On Sequence		0x00h																		
				S/W Reset		0x00h																		
				H/W Reset		0x00h																		

(0840h) TE1 Output Setting

		TE1CTR																																																																																																
Instruction	R/W	Address		Parameter																																																																																														
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																					
TE1CTR	R/W	0x08h	0x0840h	00h	TE1_period[7:0]																																																																																													
Description	This command is to select the period of TE1 signal. The timing reference start point is TE1 transient edge, and 1 clock period is 50ns.																																																																																																	
	<table border="1"> <thead> <tr> <th colspan="2">Bit</th><th colspan="2">Value</th><th colspan="8">Description</th></tr> </thead> <tbody> <tr> <td colspan="2" rowspan="4">STB_period[9:0]</td><td>0</td><td>000h</td><td colspan="8">0 Clocks</td></tr> <tr> <td>1</td><td>001h</td><td colspan="8">1 Clock = 50ns</td></tr> <tr> <td>:</td><td>:</td><td colspan="8">50 ns / Clock</td></tr> <tr> <td colspan="2" rowspan="2">Reserved</td><td colspan="8" rowspan="3">Reserved</td></tr> </tbody> </table>													Bit		Value		Description								STB_period[9:0]		0	000h	0 Clocks								1	001h	1 Clock = 50ns								:	:	50 ns / Clock								Reserved		Reserved																																						
Bit		Value		Description																																																																																														
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		1	001h	1 Clock = 50ns																																																																																														
		:	:	50 ns / Clock																																																																																														
		Reserved		Reserved																																																																																														
TE1_POSE_SEL + TE1_period < T1A TE1_POSE_SEL + TE1_period < T1B																																																																																																		
Register Availability	<table border="1"> <thead> <tr> <th colspan="5">Status</th><th colspan="9">Availability</th></tr> </thead> <tbody> <tr> <td colspan="5">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="9">Yes</td></tr> <tr> <td colspan="5">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="9">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="9">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="9">Yes</td></tr> <tr> <td colspan="5">Sleep In</td><td colspan="9" rowspan="6">Yes</td></tr> </tbody> </table>														Status					Availability									Normal Mode On, Idle Mode Off, Sleep Out					Yes									Normal Mode On, Idle Mode On, Sleep Out					Yes									Partial Mode On, Idle Mode Off, Sleep Out					Yes									Partial Mode On, Idle Mode On, Sleep Out					Yes									Sleep In					Yes								
	Status					Availability																																																																																												
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																																																																																												
	Normal Mode On, Idle Mode On, Sleep Out					Yes																																																																																												
	Partial Mode On, Idle Mode Off, Sleep Out					Yes																																																																																												
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	Sleep In					Yes																																																																																												
Default	<table border="1"> <thead> <tr> <th colspan="3">Status</th><th colspan="11">Default Value</th></tr> </thead> <tbody> <tr> <td colspan="3">Power On Sequence</td><td colspan="11">0x08h / 0x0840h</td></tr> <tr> <td colspan="3">S/W Reset</td><td colspan="11">0x00h</td></tr> <tr> <td colspan="3">H/W Reset</td><td colspan="11">0x00h</td></tr> </tbody> </table>														Status			Default Value											Power On Sequence			0x08h / 0x0840h											S/W Reset			0x00h											H/W Reset			0x00h																																						
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	S/W Reset			0x00h																																																																																														
	H/W Reset			0x00h																																																																																														

(0940h) TE1 Output Setting

		TE1CTR																							
Instruction	R/ W	Address		Parameter																					
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
TE1CTR	R/ W	0x09h	0x0940h	00h	TE1_POSE_S EL[9:8]	TE1_period[9: 8]	TE1_p ol	TE1_E N	-	-	-	-	0x00h												
Description	This command is used to set TE1 enable and polarity.																								
	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>TE1_pol</td><td>TE1 Output Polarity</td><td>0: Low Active 1: Hi Active</td></tr> <tr> <td>TE1_EN</td><td>TE1 Output Control</td><td>0: Disable FTE1 Output 1: Enable FTE1 Output</td></tr> </tbody> </table>												Bit	Description	Value	TE1_pol	TE1 Output Polarity	0: Low Active 1: Hi Active	TE1_EN	TE1 Output Control	0: Disable FTE1 Output 1: Enable FTE1 Output				
Bit	Description	Value																							
TE1_pol	TE1 Output Polarity	0: Low Active 1: Hi Active																							
TE1_EN	TE1 Output Control	0: Disable FTE1 Output 1: Enable FTE1 Output																							
Restriction																									
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
	0x09h / 0x0940h																								
Power On Sequence	0x00h																								
S/W Reset	0x00h																								
H/W Reset	0x00h																								

(0A40h) MIPI Control

		HSIFOPCTR Control																		
Instruction	R/W	Address		Parameter																
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
HSIFOPCTR Control	R/W	0x0Ah	0x0A40h	00h	DSITE	DIS_EoT_p_HS	DSIG	N565	DSIM	-	-	-	0xF8h							
Description	This command is used to setup MIPI options for customer's application.																			
	Bit	Description					Data													
	DSITE	TE line enable/disable					0: Disable 1: Enable													
	DSIG	Generic read/write data type enable/disable for MIPI DSI					0: Generic read/write disable 1: Generic read/write enable													
	DSIM	Video mode data type enable/disable for MIPI DSI					0: Disable 1: Enable													
	DIS_EoTP_HS	“DSI Protocol Violation” error reporting enable/disable control					0: Enable report function 1: Disable report function													
	N565	16-bit/pixel format (MSB to LSB) selection in MIPI command mode					“0”: G[2:0]+R[4:0] & B[4:0]+G[5:3] “1”: R[4:0]+G[5:3] & G[2:0]+B[4:0]													
Restriction																				
		Status				Availability														
	Normal Mode On, Idle Mode Off, Sleep Out				Yes															
	Normal Mode On, Idle Mode On, Sleep Out				Yes															
	Partial Mode On, Idle Mode Off, Sleep Out				Yes															
	Partial Mode On, Idle Mode On, Sleep Out				Yes															
	Sleep In				Yes															
Default		Status		Default Value																
	Power On Sequence		0xF8h																	
	S/W Reset		0xF8h																	
	H/W Reset		0xF8h																	

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(0B40h) MIPI Control

		HSIFOPCTR Control																					
Instruction	R/W	Address		Parameter																			
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
HSIFOPCTR Control	R/W	0x0Bh	0x0B40h	00h	Iptx_freq_sel[1:0]	Iptx_TAGSOD_sel[1:0]	Iptx_TAGSOD_sel[1:0]	-	-	0x00h													
		This command is used to setup MIPI options for customer's application.																					
Description		<table border="1"> <thead> <tr> <th>Iptx_freq_sel[1:0]</th> <th>LP-TX Frequency</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>7.37 MHz</td> </tr> <tr> <td>01h</td> <td>3.68 MHz</td> </tr> <tr> <td>02h</td> <td>1.84 MHz</td> </tr> <tr> <td>03h</td> <td>0.92 MHz</td> </tr> </tbody> </table>		Iptx_freq_sel[1:0]	LP-TX Frequency	00h	7.37 MHz	01h	3.68 MHz	02h	1.84 MHz	03h	0.92 MHz										
Iptx_freq_sel[1:0]	LP-TX Frequency																						
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<table border="1"> <thead> <tr> <th>Iptx_TAGSOD_sel[1:0]</th> <th>Periods</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>5*T_{LPX}</td> </tr> <tr> <td>01h</td> <td>4*T_{LPX}</td> </tr> <tr> <td>02h</td> <td>6*T_{LPX}</td> </tr> <tr> <td>03h</td> <td>7*T_{LPX}</td> </tr> </tbody> </table>		Iptx_TAGSOD_sel[1:0]	Periods	00h	5*T _{LPX}	01h	4*T _{LPX}	02h	6*T _{LPX}	03h	7*T _{LPX}												
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Iptx_TAGSOD_sel[1:0]	Periods																						
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Restriction																							
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Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						

	Sleep In	Yes
Default	Status	Default Value
		0x0Bh / 0x0B40h
	Power On Sequence	0x00h
	S/W Reset	0x00h
	H/W Reset	0x00h

(0C40h) MIPI Control

Instruction	R/W	HSIFOPCTR Control																							
		Address		Parameter																					
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
HSIFOPCTR Control	R/W	0x0C h	0x0C40h	00h	-	-	tato_en	lptxo_en	hsrxto_en	-	vcid[1:0]		0x38h												
Description	This command is used to setup MIPI options for customer's application.																								
	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>tato_en</td><td>Enable TA timer</td></tr> <tr> <td>lptxo_en</td><td>Enable LPDT Timer</td></tr> <tr> <td>hsrxto_en</td><td>Enable HSRX Timer</td></tr> </tbody> </table>												Bit	Description	tato_en	Enable TA timer	lptxo_en	Enable LPDT Timer	hsrxto_en	Enable HSRX Timer					
Bit	Description																								
tato_en	Enable TA timer																								
lptxo_en	Enable LPDT Timer																								
hsrxto_en	Enable HSRX Timer																								
This command is used to setup virtual channel for customer's application.																									
<table border="1"> <thead> <tr> <th>vcid[1:0]</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>Virtual Channel = 00h</td></tr> <tr> <td>01h</td><td>Virtual Channel = 01h</td></tr> <tr> <td>02h</td><td>Virtual Channel = 02h</td></tr> <tr> <td>03h</td><td>Virtual Channel = 03h</td></tr> </tbody> </table>												vcid[1:0]	Description	00h	Virtual Channel = 00h	01h	Virtual Channel = 01h	02h	Virtual Channel = 02h	03h	Virtual Channel = 03h				
vcid[1:0]	Description																								
00h	Virtual Channel = 00h																								
01h	Virtual Channel = 01h																								
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03h	Virtual Channel = 03h																								
Please don't trim or change vcid[1:0] if only one display driver is used.																									
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(0E40h) AVDD Charge Pump Control Normal Mode

		BT1CTR																																														
Instruction	R/W	Address		Parameter																																												
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0																																				
BT1CTR	R/W	0x0Eh	0x0E40h	00h	DC1A[2:0]			VDHA[4:0]				0xA5h																																				
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Default	Status
	Default Value
	0x0Eh / 0x0E40h
	Power On Sequence
	0xA5h
	S/W Reset
	0xA5h
	H/W Reset
	0xA5h

(0F40h) AVDD Charge Pump Control Idle Mode

		BT1CTRIDM																																														
Instruction	R/W	Address		Parameter																																												
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0																																				
BT1CTRIDM	R/W	0x0Fh	0x0F40h	00h	DC1B[2:0]			VDHB[4:0]			0xA5h																																					
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Restriction	If BT_DHB (0x1040) is equal to 1, the output range of AVDD is from 6.5v to (2*VCI – 0.6).																																															
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Default	Status
	Default Value
	0x0Fh / 0x0F40h
	Power On Sequence
	0xA5h
	S/W Reset
	0xA5h
	H/W Reset
	0xA5h

(1040h) AVDD/VCL Regulator Enable

	BT1BT3REGEN																							
Instruction	R/ W	Address		Parameter																				
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
BT1BT3REGEN	R/ W	0x10h	0x1040h	00h	-	BT_D HA	BT_D HB	EN_P UMP_ VCLR EG	-	-	-	EN_P UMP_ DDVD HREG	0x11h											
		This command is used to set AVDD step up factor and output voltage level in normal mode/idle mode.																						
Description	<table border="1"> <tr> <td>BT_DHA BT_DHB</td><td>AVDD</td></tr> <tr> <td>0</td><td>VCI x 2.0</td></tr> <tr> <td>1</td><td>VCI x 3.0</td></tr> </table>												BT_DHA BT_DHB	AVDD	0	VCI x 2.0	1	VCI x 3.0						
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Power On Sequence	0x11h																							
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(1140h) VCL Charge Pump Control Normal Mode

	BT3CTR																												
Instruction	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BT3CTR	R/ W	0x11h	0x1140h	00h	DC3A[2:0]			BT_V CLA	-	-	DVCLA[1:0]	0xA2h																	
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Power On Sequence	0xA2h										
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(1240h) VCL Charge Pump Control Idle Mode

	BT3CTRIDM																												
Instruction	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BT3CTRIDM	R/ W	0x12h	0x1240h	00h	DC3B[2:0]			BT_V CLB	-	-	DVCLB[1:0]	0xA2h																	
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(1340h) VGH Charge Pump Control Normal Mode

Instruction	BT4CTR																												
	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BT4CTR	R/ W	0x13h	0x1340h	00h	DC4A[2:0]			-	-	-	BT_VGHA[1:0]	0x80h																	
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S/W Reset	0x80h										
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(1440h) VGH Charge Pump Control Idle Mode

	BT4CTRIDM																												
Instruction	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BT4CTRIDM	R/ W	0x14h	0x1440h	00h	DC4B[2:0]			-	-	-	BT_VGHB[1:0]	0x80h																	
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Power On Sequence	0x80h										
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(1540h) VGL Charge Pump Control Normal Mode

Instruction	BT5CTR																												
	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BT5CTR	R/ W	0x15h	0x1540h	00h	DC5A[2:0]			-	-	-	BT_VGLA[1:0]	0x81h																	
Description	This command is used to control the Charge Pump clock in normal mode.																												
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(1640h) VGL Charge Pump Control Idle Mode

	BT5CTRIDM																												
Instruction	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BT5CTRIDM	R/ W	0x16h	0x1640h	00h	DC5B[2:0]			-	-	-	BT_VGLB[1:0]	0x81h																	
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(1840h) VGHR Control

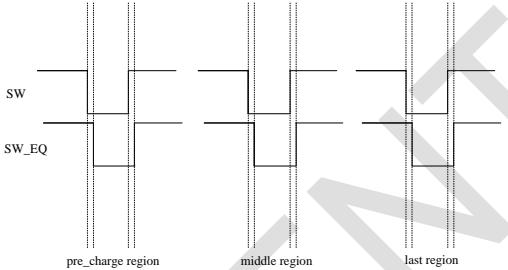
	SETVGHR																																												
Instruction	R/W	Address		Parameter																																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																
SETVGHR	R/W	0x18h	0x1840h	00h	VGHREGB[3:0]				VGHREGA[3:0]			0x44h																																	
Description	This command is used to select VGHR output level in normal mode and idle mode.																																												
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Power On Sequence	0x44h																																												
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H/W Reset	0x44h																																												

(1940h) VGLR Control

	SETVGLR																																												
Instruction	R/W	Address		Parameter																																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																
SETVGLR	R/W	0x19h	0x1940h	00h	VGLREGB[3:0]				VGLREGA[3:0]			0x33h																																	
Description	This command is to select VGLR regulator output level in normal mode and idle mode.																																												
	<table border="1"> <thead> <tr> <th>VGLREGA[3:0] VGLREGB[3:0]</th> <th>VGLR (V)</th> </tr> </thead> <tbody> <tr><td>0000</td><td>-2</td></tr> <tr><td>0001</td><td>-3</td></tr> <tr><td>0010</td><td>-4</td></tr> <tr><td>0011</td><td>-5</td></tr> <tr><td>0100</td><td>-6</td></tr> <tr><td>0101</td><td>-7</td></tr> <tr><td>0110</td><td>-8</td></tr> <tr><td>0111</td><td>-9</td></tr> <tr><td>1000</td><td>reserved</td></tr> <tr><td>1001</td><td>reserved</td></tr> <tr><td>1010</td><td>reserved</td></tr> <tr><td>1011</td><td>reserved</td></tr> <tr><td>1100</td><td>reserved</td></tr> <tr><td>1101</td><td>reserved</td></tr> <tr><td>1110</td><td>reserved</td></tr> <tr><td>1111</td><td>reserved</td></tr> </tbody> </table>												VGLREGA[3:0] VGLREGB[3:0]	VGLR (V)	0000	-2	0001	-3	0010	-4	0011	-5	0100	-6	0101	-7	0110	-8	0111	-9	1000	reserved	1001	reserved	1010	reserved	1011	reserved	1100	reserved	1101	reserved	1110	reserved	1111
VGLREGA[3:0] VGLREGB[3:0]	VGLR (V)																																												
0000	-2																																												
0001	-3																																												
0010	-4																																												
0011	-5																																												
0100	-6																																												
0101	-7																																												
0110	-8																																												
0111	-9																																												
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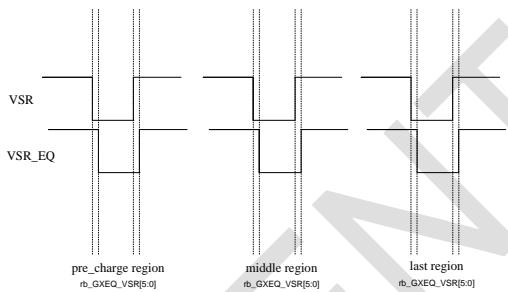
(1D40h/1E40h) SWITCH EQ Control

Instruction	R/W	EQCTR																													
		Address		Parameter																											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
SWEQCTR	R/W	0x1Dh	0x1D40h	00h	-	-	GREQ_SW[5:0]					0x00h																			
SWEQCTR	R/W	0x1Eh	0x1E40h	00h	-	-	GFEQ_SW[5:0]					0x00h																			
Description	<p>This command is used to control the EQ function for gate signals SW.</p> <p>rb_GREQ_SW_XX[5:0]: time setting of EQ step for rising edge.</p> <p>rb_GFEQ_SW_XX[5:0]: time setting of EQ step for falling edge.</p>  <table border="1"> <thead> <tr> <th>rb_GREQ_SW_xxx[5:0]/rb_GREQ_SW_xxx[5:0]</th> <th>NO. of PCLK</th> <th>SW EQ time (us)</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0</td> <td>0</td> </tr> <tr> <td>01h</td> <td>1</td> <td>0.045</td> </tr> <tr> <td>02h</td> <td>2</td> <td>0.091</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>3Fh</td> <td>63</td> <td>2.863</td> </tr> </tbody> </table> <p>Note: PCLK frequency is 22MHz.</p>													rb_GREQ_SW_xxx[5:0]/rb_GREQ_SW_xxx[5:0]	NO. of PCLK	SW EQ time (us)	00h	0	0	01h	1	0.045	02h	2	0.091	:	:	:	3Fh	63	2.863
rb_GREQ_SW_xxx[5:0]/rb_GREQ_SW_xxx[5:0]	NO. of PCLK	SW EQ time (us)																													
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01h	1	0.045																													
02h	2	0.091																													
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Power On Sequence			
S/W Reset		0x1D40h	0x00h
H/W Reset		0x1E40h	0x00h

CONFIDENTIAL

(1F40h/2040h) VSR EQ Control

Instruction	R/W	EQCTR																		
		Address		Parameter																
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
VSREQCTR	R/W	0x1Fh	0x1F40h	00h	-	-	GREQ_VSR[5:0]					0x00h								
VSREQCTR	R/W	0x20h	0x2040h	00h	-	-	GFEQ_VSR[5:0]					0x00h								
Description	<p>This command is used to control the EQ function for gate signals VSR.</p> <p>rb_GREQ_VSR_XX[5:0]: time setting of EQ step for rising edge.</p> <p>rb_GFEQ_VSR_XX[5:0]: time setting of EQ step for falling edge.</p>  <table border="1"> <thead> <tr> <th>rb_GREQ_VSR_xxx[5:0]/ rb_GREQ_VSR_xxx[5:0]</th> <th>NO. of PCLK</th> <th>SW EQ time (us)</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0</td> <td>0</td> </tr> <tr> <td>01h</td> <td>1</td> <td>0.045</td> </tr> <tr> <td>02h</td> <td>2</td> <td>0.091</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>3Fh</td> <td>63</td> <td>2.863</td> </tr> </tbody> </table> <p>Note: PCLK frequency is 22MHz.</p>		rb_GREQ_VSR_xxx[5:0]/ rb_GREQ_VSR_xxx[5:0]	NO. of PCLK	SW EQ time (us)	00h	0	0	01h	1	0.045	02h	2	0.091	:	:	:	3Fh	63	2.863
rb_GREQ_VSR_xxx[5:0]/ rb_GREQ_VSR_xxx[5:0]	NO. of PCLK	SW EQ time (us)																		
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Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default																				

	Status	Default Value	
		0x1Fh / 0x1F40h	0x20h / 0x2040h
	Power On Sequence		
	S/W Reset	0x1F40h	0x00h
	H/W Reset	0x2040h	0x00h

CONFIDENTIAL

(2540h~2840h) Low Frame Rate Control Normal Mode

Instruction	R/W	LFRCTR																																									
		Address		Parameter																																							
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																														
LFRCTR1	R/W	0x25h	0x2540h	00h	GMA2_EN_A	VFPD A[8]	D_CM_A[1:0]	PSEL_A[1:0]	T1A[9:8]				0x06h																														
LFRCTR2	R/W	0x26h	0x2640h	00h					T1A[7:0]				0x58h																														
LFRCTR3	R/W	0x27h	0x2740h	00h					VBPDA[7:0]				0x12h																														
LFRCTR4	R/W	0x28h	0x2840h	00h					VFPDA[7:0]				0x12h																														
Description	GMA2_EN_A: 0, select Gamma1 setting under the normal mode 1, select Gamma2 setting under the normal mode This command is used to set display color mode in normal mode. <table border="1"> <tr> <th>D_CM_A[1:0]</th> <th>Display color bit</th> </tr> <tr> <td>00</td> <td>24 bit</td> </tr> <tr> <td>01</td> <td>12 bit</td> </tr> <tr> <td>10</td> <td>3 bit (8 color)</td> </tr> <tr> <td>11</td> <td>reserved</td> </tr> </table> This command is used to select pixel clock frequency in normal mode. <table border="1"> <tr> <th>PSEL_A[1:0]</th> <th>Divisor</th> </tr> <tr> <td>00</td> <td>1</td> </tr> <tr> <td>01</td> <td>2</td> </tr> <tr> <td>10</td> <td>4</td> </tr> <tr> <td>11</td> <td>8</td> </tr> </table> This command is used to set display time of one scan line in normal mode. <table border="1"> <tr> <th>T1A[9:0]</th> <th>Number of clock</th> </tr> <tr> <td>0h~FFh</td> <td>0~255</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>3FEh</td> <td>1022</td> </tr> <tr> <td>3FFh</td> <td>1023</td> </tr> </table>													D_CM_A[1:0]	Display color bit	00	24 bit	01	12 bit	10	3 bit (8 color)	11	reserved	PSEL_A[1:0]	Divisor	00	1	01	2	10	4	11	8	T1A[9:0]	Number of clock	0h~FFh	0~255	3FEh	1022	3FFh	1023
D_CM_A[1:0]	Display color bit																																										
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PSEL_A[1:0]	Divisor																																										
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0h~FFh	0~255																																										
...	...																																										
3FEh	1022																																										
3FFh	1023																																										

This command is used to set vertical back porch lines in normal mode.

VBPDA[7:0]	Number of line
0h~7h	reserved
8h	8
9h	9
...	...
12h	18
...	...
FEh	254
FFh	255

This command is used to set vertical front porch lines in normal mode.

VFPDA[8:0]	Number of line
0h~7h	reserved
8h	8
9h	9
...	...
12h	18
...	...
1FEh	510
1FFh	511

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence		
S/W Reset	0x2540h	0x06h

H/W Reset

0x2640h	0x58h
0x2740h	0x12h
0x2840h	0x12h

CONFIDENTIAL

(2A40h~2F40h) Low Frame Rate Control Idle Mode

Instruction	R/W	LFRCTRIDM																																									
		Address		Parameter																																							
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																														
LFRCTRIDM1	R/W	0x2Ah	0x2A40h	00h	GMA2_EN_B	VFPD B[8]	D_CM_B[1:0]	PSELB[1:0]	T1B[9:8]				0x26h																														
LFRCTRIDM2	R/W	0x2Bh	0x2B40h	00h									0x58h																														
LFRCTRIDM3	R/W	0x2Dh	0x2D40h	00h									0x12h																														
LFRCTRIDM4	R/W	0x2Fh	0x2F40h	00h									0x12h																														
Description	<p>GMA2_EN_B: 0, select Gamma1 setting under the idle mode 1, select Gamma2 setting under the idle mode</p> <p>This command is used to set display color mode in idle mode.</p> <table border="1"> <tr> <th>D_CM_B[1:0]</th> <th>Display color bit</th> </tr> <tr> <td>00</td> <td>24 bit</td> </tr> <tr> <td>01</td> <td>12 bit</td> </tr> <tr> <td>10</td> <td>3 bit (8 color)</td> </tr> <tr> <td>11</td> <td>reserved</td> </tr> </table> <p>This command is used to select pixel clock frequency in idle mode.</p> <table border="1"> <tr> <th>PSEL_B[1:0]</th> <th>Divisor</th> </tr> <tr> <td>00</td> <td>1</td> </tr> <tr> <td>01</td> <td>2</td> </tr> <tr> <td>10</td> <td>4</td> </tr> <tr> <td>11</td> <td>8</td> </tr> </table> <p>This command is used to set display time of one scan line in idle mode.</p> <table border="1"> <tr> <th>T1B[9:0]</th> <th>Number of clock</th> </tr> <tr> <td>0h~FFh</td> <td>0~255</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>3FEh</td> <td>1022</td> </tr> <tr> <td>3FFh</td> <td>1023</td> </tr> </table>													D_CM_B[1:0]	Display color bit	00	24 bit	01	12 bit	10	3 bit (8 color)	11	reserved	PSEL_B[1:0]	Divisor	00	1	01	2	10	4	11	8	T1B[9:0]	Number of clock	0h~FFh	0~255	3FEh	1022	3FFh	1023
D_CM_B[1:0]	Display color bit																																										
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3FFh	1023																																										

This command is used to set vertical back porch lines in idle mode.

VBpdb[7:0]	Number of line
0h~7h	reserved
8h	8
9h	9
...	...
12h	18
...	...
FEh	254
FFh	255

This command is used to set vertical front porch lines in idle mode.

Vfpdb[8:0]	Number of line
0h~7h	reserved
8h	8
9h	9
...	...
12h	18
...	...
1FEh	510
1FFh	511

Restriction**Register Availability**

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence		
S/W Reset	0x2A40h	0x26h

H/W Reset

0x2B40h	0x58h
0x2D40h	0x12h
0x2F40h	0x12h

CONFIDENTIAL

(3640h) Source Bias Current Control

	SGOPCTR																												
Instruction	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
SGOPCTR	R/ W	0x36h	0x3640h	00h	-	AP_A[2:0]	PTD	AP_B[2:0]					0x44h																
Description	This command is used to set non-display area of partial display.																												
	<table border="1"> <thead> <tr> <th>PTD</th> <th>Non-display area</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Black</td> </tr> <tr> <td>1</td> <td>White</td> </tr> </tbody> </table>												PTD	Non-display area	0	Black	1	White											
PTD	Non-display area																												
0	Black																												
1	White																												
This command is used to set source driver driving condition in normal/idle mode.																													
<table border="1"> <thead> <tr> <th>AP_A[2:0] AP_B[2:0]</th> <th>OPAMP power consumption</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>-50%</td> </tr> <tr> <td>001</td> <td>-37.5%</td> </tr> <tr> <td>010</td> <td>-25%</td> </tr> <tr> <td>011</td> <td>-12.5%</td> </tr> <tr> <td>100</td> <td>default</td> </tr> <tr> <td>101</td> <td>+12.5%</td> </tr> <tr> <td>110</td> <td>+25%</td> </tr> <tr> <td>111</td> <td>+37.5%</td> </tr> </tbody> </table>												AP_A[2:0] AP_B[2:0]	OPAMP power consumption	000	-50%	001	-37.5%	010	-25%	011	-12.5%	100	default	101	+12.5%	110	+25%	111	+37.5%
AP_A[2:0] AP_B[2:0]	OPAMP power consumption																												
000	-50%																												
001	-37.5%																												
010	-25%																												
011	-12.5%																												
100	default																												
101	+12.5%																												
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Restriction																													
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	0x36h / 0x3640h																												
Power On Sequence	0x44h																												
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(3A40h~4140h) Switch Timing Control

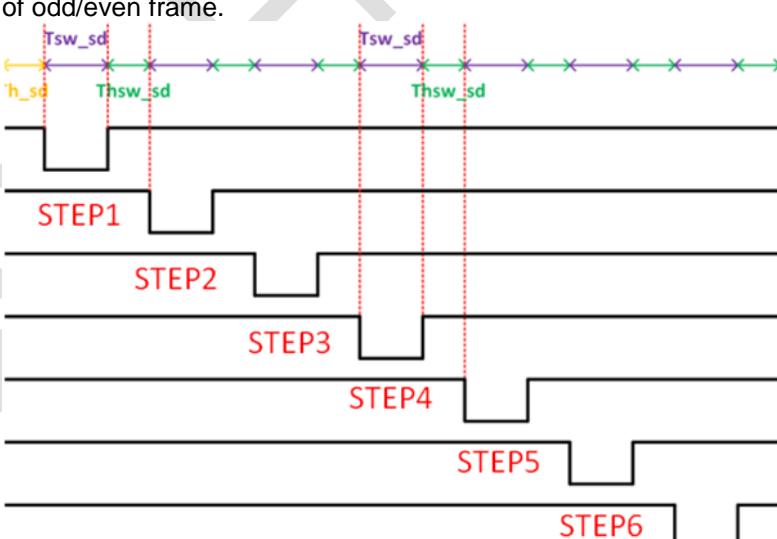
Instruction	R/W	SWTIMCTR																																														
		Address	Parameter										HEX																																			
	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0																																					
SWTIMCTR1	R/W	0x3Ah	0x3A40h	00h	T1_sd[7:0]										0x17h																																	
SWTIMCTR2	R/W	0x3Bh	0x3B40h	00h	Tp_sd[7:0]										0x00h																																	
SWTIMCTR3	R/W	0x3Dh	0x3D40h	00h	Th_sd[7:0]										0x17h																																	
SWTIMCTR4	R/W	0x3Fh	0x3F40h	00h	Tsw_sd[7:0]										0x44h																																	
SWTIMCTR5	R/W	0x40h	0x4040h	00h	Thsw_sd[7:0]										0x17h																																	
SWTIMCTR6	R/W	0x41	0x4140h	00h	Thsd_sd[7:0]										0x0Dh																																	
Description	This command is used to set all kinds of pulse width for switch.																																															
	<table border="1"> <thead> <tr> <th>Name</th> <th>Description</th> <th>Unit</th> <th>Range (DEC)</th> <th>Default (DEC)</th> </tr> </thead> <tbody> <tr> <td>T1_sd</td> <td>Time delay from Hsync to pre-charge start</td> <td>Dclk</td> <td>0 ~ 255</td> <td>0</td> </tr> <tr> <td>Tp_sd</td> <td>Pulse width of pre-charge</td> <td>Dclk</td> <td>0 ~ 255</td> <td>0</td> </tr> <tr> <td>Th_sd</td> <td>Time delay from pre-charge stop to SW1 start</td> <td>Dclk</td> <td>0 ~ 255</td> <td>23</td> </tr> <tr> <td>Tsw_sd</td> <td>Pulse width of SW(n)</td> <td>Dclk</td> <td>0 ~ 255</td> <td>69</td> </tr> <tr> <td>Thsw_sd</td> <td>Non overlap period between SW(n) to SW(n+1)</td> <td>Dclk</td> <td>0 ~ 255</td> <td>23</td> </tr> <tr> <td>Thsd_sd</td> <td>Source data output hold time</td> <td>Dclk</td> <td>0 ~ 255</td> <td>13</td> </tr> </tbody> </table>														Name	Description	Unit	Range (DEC)	Default (DEC)	T1_sd	Time delay from Hsync to pre-charge start	Dclk	0 ~ 255	0	Tp_sd	Pulse width of pre-charge	Dclk	0 ~ 255	0	Th_sd	Time delay from pre-charge stop to SW1 start	Dclk	0 ~ 255	23	Tsw_sd	Pulse width of SW(n)	Dclk	0 ~ 255	69	Thsw_sd	Non overlap period between SW(n) to SW(n+1)	Dclk	0 ~ 255	23	Thsd_sd	Source data output hold time	Dclk	0 ~ 255
Name	Description	Unit	Range (DEC)	Default (DEC)																																												
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Th_sd	Time delay from pre-charge stop to SW1 start	Dclk	0 ~ 255	23																																												
Tsw_sd	Pulse width of SW(n)	Dclk	0 ~ 255	69																																												
Thsw_sd	Non overlap period between SW(n) to SW(n+1)	Dclk	0 ~ 255	23																																												
Thsd_sd	Source data output hold time	Dclk	0 ~ 255	13																																												
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Register																																																

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Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	

Default	Status	Default Value	
	Power On Sequence	0x3A40h 0x17h 0x3B40h 0x00h 0x3D40h 0x17h 0x3F40h 0x44h 0x4040h 0x17h 0x4140h 0x0Dh	
	S/W Reset		
	H/W Reset		

(4240h~5540h) Switch Output Selection

Instruction	R/ W	SWSELCTR											
		Address		Parameter									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWSELCTR1	R/ W	0x42h	0x4240h	00h	SW_step1_of_ol[3:0]	SW_step1_of_el[3:0]							0x11h
SWSELCTR2	R/ W	0x43h	0x4340h	00h	SW_step2_of_ol[3:0]	SW_step2_of_el[3:0]							0x22h
SWSELCTR3	R/ W	0x44h	0x4440h	00h	SW_step3_of_ol[3:0]	SW_step3_of_el[3:0]							0x33h
SWSELCTR4	R/ W	0x45h	0x4540h	00h	SW_step4_of_ol[3:0]	SW_step4_of_el[3:0]							0x44h
SWSELCTR5	R/ W	0x46h	0x4640h	00h	SW_step5_of_ol[3:0]	SW_step5_of_el[3:0]							0x55h
SWSELCTR6	R/ W	0x47h	0x4740h	00h	SW_step6_of_ol[3:0]	SW_step6_of_el[3:0]							0x66h
SWSELCTR7	R/ W	0x48h	0x4840h	00h	SW_step1_ef_ol[3:0]	SW_step1_ef_el[3:0]							0x11h
SWSELCTR8	R/ W	0x49h	0x4940h	00h	SW_step2_ef_ol[3:0]	SW_step2_ef_el[3:0]							0x22h
SWSELCTR9	R/ W	0x4Ah	0x4A40h	00h	SW_step3_ef_ol[3:0]	SW_step3_ef_el[3:0]							0x33h
SWSELCTR10	R/ W	0x4Bh	0x4B40h	00h	SW_step4_ef_ol[3:0]	SW_step4_ef_el[3:0]							0x44h
SWSELCTR11	R/ W	0x4Ch	0x4C40h	00h	SW_step5_ef_ol[3:0]	SW_step5_ef_el[3:0]							0x55h
SWSELCTR12	R/ W	0x4Dh	0x4D40h	00h	SW_step6_ef_ol[3:0]	SW_step6_ef_el[3:0]							0x66h
Description	This command is used to assign step1 ~ step6 to which SWITCH PAD at odd/even line of odd/even frame. 												

Ex : SW_step3_*[3:0] = 5h means that assign STEP3 to SW_L/R[5] and so on.

SW_step*_of_ol : SW output mapping at odd line of odd frame

SW_step*_ef_ol : SW output mapping at even line of odd frame

SW_step*_ef_el : SW output mapping at odd line of even frame

SW_step*_of_el : SW output mapping at even line of even frame

Restriction**Register Availability**

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

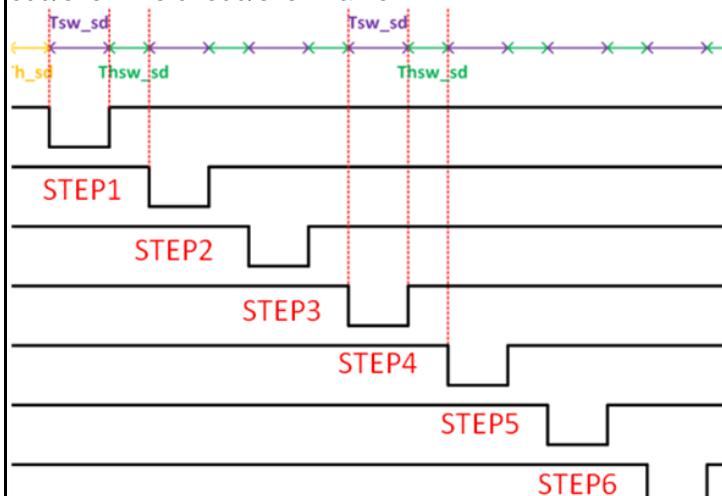
Default

Status	Default Value		
	0x4240h	0x11h	
Power On Sequence	0x4340h	0x22h	
	0x4440h	0x33h	
	0x4540h	0x44h	
	0x4640h	0x55h	
	0x4740h	0x66h	
	0x4840h	0x11h	
	0x4940h	0x22h	
	0x4A40h	0x33h	
	0x4B40h	0x44h	
	0x4C40h	0x55h	
	0x4D40h	0x66h	
H/W Reset			

(4E40h~5940h) Source Data Output Selection

Instruction	R/ W	SDSELCTR											
		Address		Parameter									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SDSELCTR1	R/ W	0x4Eh	0x4E40h	00h	SD_step1_of_oI[3:0]			SD_step1_of_eI[3:0]			0x11h		
SDSELCTR2	R/ W	0x4Fh	0x4F40h	00h	SD_step2_of_oI[3:0]			SD_step2_of_eI[3:0]			0x22h		
SDSELCTR3	R/ W	0x50h	0x5040h	00h	SD_step3_of_oI[3:0]			SD_step3_of_eI[3:0]			0x33h		
SDSELCTR4	R/ W	0x51h	0x5140h	00h	SD_step4_of_oI[3:0]			SD_step4_of_eI[3:0]			0x44h		
SDSELCTR5	R/ W	0x52h	0x5240h	00h	SD_step5_of_oI[3:0]			SD_step5_of_eI[3:0]			0x55h		
SDSELCTR6	R/ W	0x54h	0x5340h	00h	SD_step6_of_oI[3:0]			SD_step6_of_eI[3:0]			0x66h		
SDSELCTR7	R/ W	0x54h	0x5440h	00h	SD_step1_ef_oI[3:0]			SD_step1_ef_eI[3:0]			0x11h		
SDSELCTR8	R/ W	0x55h	0x5540h	00h	SD_step2_ef_oI[3:0]			SD_step2_ef_eI[3:0]			0x22h		
SDSELCTR9	R/ W	0x56h	0x5640h	00h	SD_step3_ef_oI[3:0]			SD_step3_ef_eI[3:0]			0x33h		
SDSELCTR10	R/ W	0x57h	0x5740h	00h	SD_step4_ef_oI[3:0]			SD_step4_ef_eI[3:0]			0x44h		
SDSELCTR11	R/ W	0x58h	0x5840h	00h	SD_step5_ef_oI[3:0]			SD_step5_ef_eI[3:0]			0x55h		
SDSELCTR12	R/ W	0x59h	0x5940h	00h	SD_step6_ef_oI[3:0]			SD_step6_ef_eI[3:0]			0x66h		

This command is used to assign source dot data corresponding to step1~step6 at odd/even line of odd/even frame.



The relationship between source dot data and source pad is as below,

SW tag	1	2	3	4	5	6
Pixel Order(1,3,⋯Odd line)	R1	G1	B1	R2	G2	B2
Pixel Order(2,4,⋯Even line)	R1	G1	B1	R2	G2	B2

Description

SW order setting		
SW tag	Register Setting(Decimal)	
1	SD_step1_*_ol=1	SD_step1_*_el=1
2	SD_step2_*_ol=2	SD_step2_*_el=2
3	SD_step3_*_ol=3	SD_step3_*_el=3
4	SD_step4_*_ol=4	SD_step4_*_el=4
5	SD_step5_*_ol=5	SD_step5_*_el=5
6	SD_step6_*_ol=6	SD_step6_*_el=6

SD_step*_of_ol : SD output mapping at odd line of odd frame
 SD_step*_of_el : SD output mapping at even line of odd frame
 SD_step*_ef_ol : SD output mapping at odd line of even frame
 SD_step*_ef_el : SD output mapping at even line of even frame

Restriction			
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
Default	Sleep In	Yes	
	Status	Default Value	
	Power On Sequence	0x4E40h	0x11h
		0x4F40h	0x22h
		0x5040h	0x33h
	S/W Reset	0x5140h	0x44h
		0x5240h	0x55h
		0x5340h	0x66h
	H/W Reset	0x5440h	0x11h
		0x5540h	0x22h
		0x5640h	0x33h
		0x5740h	0x44h
		0x5840h	0x55h
		0x5940h	0x66h

(5B40h) VREFPN5 ENABLE

		SETVREFPN5EN																		
Instruction	R/W	Address		Parameter																
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
SETVREFPN5 EN	R/W	0x5Bh	0x5B40h	00h	-	-	-	VREF N5EN	-	-	-	VREF P5EN	0x01h							
Description	Bit		Description				Data													
	VREFP5EN		VREFP5 regulator on/off				0=regulator off, output is GND 1=regulator on													
Restriction																				
	Register Availability	Status						Availability												
Default		Normal Mode On, Idle Mode Off, Sleep Out						Yes												
		Normal Mode On, Idle Mode On, Sleep Out						Yes												
		Partial Mode On, Idle Mode Off, Sleep Out						Yes												
		Partial Mode On, Idle Mode On, Sleep Out						Yes												
		Sleep In						Yes												
		Status						Default Value												
						0x5Bh / 0x5B40h														
						0x01h														
						0x01h														
						0x01h														

(5E40h/5F40h) VREFP5

		SETVREFP5																																								
Instruction	R/W	Address		Parameter																																						
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
SETVREFP5	R/W	0x5Eh	0x5E40h	00h	-	-	VP5REGA[5:0]				0x0Dh																															
SETVREFP5	R/W	0x5Fh	0x5F40h	00h	-	-	VP5REGB[5:0]				0x0Dh																															
Description	This command is to select VREFP5 regulator output level in normal mode and idle mode.																																									
	<table border="1"> <thead> <tr> <th>VP5REGA[5:0] VP5RGB[5:0]</th> <th>VREFP5 (V)</th> </tr> </thead> <tbody> <tr><td>000000~000010</td><td>Reserved</td></tr> <tr><td>000011</td><td>0.5</td></tr> <tr><td>000100</td><td>0.6</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>001101</td><td>1.5</td></tr> <tr><td>:</td><td>0.1V / Step</td></tr> <tr><td>010010</td><td>2.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>011100</td><td>3.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>100110</td><td>4.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>110000</td><td>5.0</td></tr> <tr><td>110001~111111</td><td>Reserved</td></tr> </tbody> </table>													VP5REGA[5:0] VP5RGB[5:0]	VREFP5 (V)	000000~000010	Reserved	000011	0.5	000100	0.6	:	:	001101	1.5	:	0.1V / Step	010010	2.0	:	:	011100	3.0	:	:	100110	4.0	:	:	110000	5.0	110001~111111
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Status	Default Value																																									
Power On Sequence	0x5E40h																																									
	0x0Dh																																									

	S/W Reset	0x5F40h	0x0Dh	
	H/W Reset			

CONFIDENTIAL

(6240h/6340h) VREFN5

	SETVREFN5																																												
Instruction	R/W	Address		Parameter																																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																
SETVREFN5	R/W	0x62h	0x6240h	00h	-		VN5REGA[5:0]					0x05h																																	
SETVREFN5	R/W	0x63h	0x6340h	00h	-		VN5REGB[5:0]					0x05h																																	
Description	<p>This command is to select VREFN5 regulator output level in normal mode and idle mode.</p> <table border="1"> <thead> <tr> <th>VN5REGA[5:0] VN5REGB[5:0]</th> <th>VREFN5 (V)</th> </tr> </thead> <tbody> <tr><td>000000</td><td>-0.5</td></tr> <tr><td>000001</td><td>-0.6</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>000101</td><td>-1.0</td></tr> <tr><td>:</td><td>-0.1V / Step</td></tr> <tr><td>001010</td><td>-1.5</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>001111</td><td>-2.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>011001</td><td>-3.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>100011</td><td>-4.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>101000</td><td>-4.5</td></tr> <tr><td>101001~111111</td><td>Reserved</td></tr> </tbody> </table>													VN5REGA[5:0] VN5REGB[5:0]	VREFN5 (V)	000000	-0.5	000001	-0.6	:	:	000101	-1.0	:	-0.1V / Step	001010	-1.5	:	:	001111	-2.0	:	:	011001	-3.0	:	:	100011	-4.0	:	:	101000	-4.5	101001~111111	Reserved
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Power On Sequence			
S/W Reset		0x6240h	0x05h
H/W Reset		0x6340h	0x05h

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(6A40h) OVSS Control

		OVSSDEF																																																																																		
Instruction	R/W	Address		Parameter																																																																																
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0																																																																								
OVSSDEF		0x6Ah	0x6A40h	00h	ovss_def[7:0]									0x00h																																																																						
Description	This command is used for setting OVSS default pulse number																																																																																			
Restriction																																																																																				
Register Availability	<table border="1"> <thead> <tr> <th colspan="5">Status</th><th colspan="7">Availability</th></tr> </thead> <tbody> <tr> <td colspan="5">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="5">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="5">Sleep In</td><td colspan="7" rowspan="7">Yes</td></tr> </tbody> </table>												Status					Availability							Normal Mode On, Idle Mode Off, Sleep Out					Yes							Normal Mode On, Idle Mode On, Sleep Out					Yes							Partial Mode On, Idle Mode Off, Sleep Out					Yes							Partial Mode On, Idle Mode On, Sleep Out					Yes							Sleep In					Yes						
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H/W Reset			0x00h																																																																																	

(8940h) VGMP Control

	SETVGMP														
Instruction	R/W	Address		Parameter											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
SETVGMP	R/W	0x89h	0x8940h	00h	VGMPTR[7:0]										0x50h
Description	This command is for VGMP output level selection.												VGMPTR[8:0]		
Restriction															
Register Availability															
Default															

(8A40h) VGSP Control

		SETVGSP											
Instruction	R/W	Address		Parameter									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	
SETVGSP	R/W	0x8Ah	0x8A40h	00h	VGSPTR[7:0]								
Description	This command is for VGSP output level selection.											VGSPTR[8:0]	
Restriction													
Register Availability													
Default													

(8B40h) VGMP / VGSP control

Instruction	R/W	SETVGMSPI																													
		Address		Parameter																											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
SETVGMSPI	R/W	0x8Bh	0x8B40h	00h	-	-	-	VGSP TR[8]	-	-	-	VGMP TR[8]	0x00h																		
Description	This command is for VGMP/VGSP Output level control. Please refer to CMD2 Page0 Reg 0x8940h~0x8B40h.																														
Restriction																															
Register Availability	<table border="1"> <thead> <tr> <th colspan="2">Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Partial Mode On, Idle Mode Off, Sleep Out		Yes	Partial Mode On, Idle Mode On, Sleep Out		Yes	Sleep In		Yes
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	Status		Default Value																												
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	Power On Sequence		0x00h																												
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	H/W Reset		0x00h																												

(8C40h) VGMP Control

	SETVGMP																																
Instruction	R/W	Address		Parameter																													
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
SETVGMP	R/W	0x8Ch	0x8C40h	00h	VGMPTR2[7:0]										0x00h																		
Description	This command is for VGMP output level selection.																																
													<table border="1"> <thead> <tr> <th>Bit</th> <th>Value</th> <th>VGMP Output level</th> </tr> </thead> <tbody> <tr> <td>VGMPTR2[8:0]</td> <td>000h</td> <td>2.0000V</td> </tr> <tr> <td></td> <td>001h</td> <td>2.0125V</td> </tr> <tr> <td>:</td> <td></td> <td>0.0125V / Step</td> </tr> <tr> <td></td> <td>028h</td> <td>2.5000V</td> </tr> <tr> <td>:</td> <td></td> <td>0.0125V / Step</td> </tr> <tr> <td></td> <td>050h</td> <td>3.0000V</td> </tr> <tr> <td>:</td> <td></td> <td>0.0125V / Step</td> </tr> <tr> <td></td> <td>157h</td> <td>6.2875V</td> </tr> <tr> <td></td> <td>158h</td> <td>6.3000V</td> </tr> <tr> <td></td> <td>159h~1FFh</td> <td>Reserved</td> </tr> </tbody> </table>	Bit	Value	VGMP Output level	VGMPTR2[8:0]	000h	2.0000V		001h	2.0125V	:		0.0125V / Step		028h	2.5000V	:		0.0125V / Step		050h
Bit	Value	VGMP Output level																															
VGMPTR2[8:0]	000h	2.0000V																															
	001h	2.0125V																															
:		0.0125V / Step																															
	028h	2.5000V																															
:		0.0125V / Step																															
	050h	3.0000V																															
:		0.0125V / Step																															
	157h	6.2875V																															
	158h	6.3000V																															
	159h~1FFh	Reserved																															
Restriction																																	
												Register Availability																					
												Default																					

(8D40h) VGSP Control

		SETVGSP																			
Instruction	R/W	Address		Parameter																	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0									
SETVGSP	R/W	0x8Dh	0x8D40h	00h	VGSPTR2[7:0]																
Description	This command is for VGSP output level selection.																				
	VGSPTR2[8:0]	Bit	Value	VGSP Output level																	
			000h	0.0000V																	
			001h	0.2125V																	
		:		0.0125V / Step																	
			005h	0.2625V																	
		:		0.0125V / Step																	
			018h	0.5000V																	
		:		0.0125V / Step																	
			158h	4.5000V																	
Restriction																					
Register Availability																					
Default																					

(8E40h) VGMP / VGSP control

Instruction	R/W	SETVGMSPI											
		Address		Parameter									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SETVGMSPI	R/W	0x8Bh	0x8B40h	00h	-	-	-	VGSP TR2[8]	-	-	-	VGMP TR2[8]	0x00h
Description	This command is for VGMP/VGSP Output level control. Please refer to CMD2 Page0 Reg 0x8C40h~0x8E40h.												
Restriction													
Register Availability													
Default													

(E140h) IC ID Code Information

Instruction	WRDDB																													
	R/W	Address		Parameter																										
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
WRDDB	R/W	0xE1h	0xE140h	00h	SID[15:8]						0x01h																			
Description	This command is for Supplier ID Code.																													
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>SID[15:8]</td> <td>MS Byte of Supplier ID</td> <td></td> </tr> </tbody> </table>		Bit	Description									Data	SID[15:8]	MS Byte of Supplier ID															
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Status		Default Value																												
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(E240h) IC ID Code Information

Instruction	R/W	WRDDB																						
		Address		Parameter																				
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0												
WRDDB	R/W	0xE2h	0xE240h	00h	SID[7:0]																			
Description	This command is for Supplier ID Code.																							
	<table border="1"><thead><tr><th>Bit</th><th>Description</th></tr></thead><tbody><tr><td>SID[7:0]</td><td>LS Byte of Supplier ID</td></tr></tbody></table>		Bit	Description	SID[7:0]	LS Byte of Supplier ID	<table border="1"><thead><tr><th>Data</th></tr></thead><tbody><tr><td></td></tr></tbody></table>											Data						
Bit	Description																							
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Status	Availability																							
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Status	Default Value																							
	0xE2h / 0xE240h																							
Power On Sequence	0xD0h																							
S/W Reset	0xD0h																							
H/W Reset	0xD0h																							

(E340h) IC ID Code Information

Instruction	R/W	WRDDB																														
		Address		Parameter																												
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
WRDDB	R/W	0xE3h	0xE340h	00h	MID[15:8]										0x90h																	
Description	This command is for Supplier Elective data such as module number.																															
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>MID[15:8]</td> <td>MS Byte of Supplier Elective Data</td> <td></td> </tr> </tbody> </table>		Bit	Description	Data	MID[15:8]	MS Byte of Supplier Elective Data																									
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Status		Default Value																														
Power On Sequence		0xE3h / 0xE340h																														
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(E440h) IC ID Code Information

Instruction	R/W	WRDDB																							
		Address		Parameter																					
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
WRDDB	R/W	0xE4h	0xE440h	00h	MID[7:0]						0x80h														
Description	This command is for Supplier Elective data such as module number.																								
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MID[7:0]	LS Byte of Supplier Elective Data																								
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H/W Reset	0x80h																								

(E540h) ID1 Code

	WRDID																																																																																			
Instruction	R/W	Address		Parameter																																																																																
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																							
WRDID	R/W	0xE5h	0xE540h	00h	ID1[7:0]						0x00h																																																																									
Description	This command is for Module Manufacture Number																																																																																			
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Status		Default Value																																																																																		
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Power On Sequence		0x00h																																																																																		
S/W Reset		0x00h																																																																																		

(E640h) ID2 Code

Instruction	R/W	WRID																								
		Address		Parameter																						
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
WRID	R/W	0xE6h	0xE640h	00h	ID2[7:0]						0x80h															
Description	This command is for Module/Driver Version Number																									
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>ID2[7:0]</td> <td>Module/Driver Version Number</td> <td></td> </tr> </tbody> </table>		Bit	Description										Data	ID2[7:0]	Module/Driver Version Number										
Bit	Description	Data																								
ID2[7:0]	Module/Driver Version Number																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																									
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Status	Default Value																									
	0xE6h / 0xE640h																									
Power On Sequence	0x80h																									
S/W Reset	0x80h																									
H/W Reset	0x80h																									

(E740h) ID3 Code

	WRID																													
Instruction	R/W	Address		Parameter																										
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
WRID	R/W	0xE7h	0xE740h	00h	ID3[7:0]						0x00h																			
Description	This command is for Module / Driver ID																													
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>ID3[7:0]</td> <td>Module /Driver ID</td> <td></td> </tr> </tbody> </table>		Bit	Description									Data	ID3[7:0]	Module /Driver ID															
Bit	Description	Data																												
ID3[7:0]	Module /Driver ID																													
Restriction																														
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Status		Availability																												
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H/W Reset		0x00h																												

(EE40h~EF40h) MTP Flag Check

Instruction	R/W	RDMPFLG																								
		Address		Parameter																						
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
RDMPFLG1	R	0xEEh	0xEE40h	00h	CMD2P_0_3rd_Done	CMD2P_0_2nd_Done	CMD2P_0_1st_Done	CMD2P_1_1st_Done	CMD2P_1_2nd_Done	CMD2P_2_1st_Done	CMD2P_2_2nd_Done	CMD2P_3_1st_Done	0x00h													
RDMPFLG2	R	0xEFh	0xEF40h	00h	CMD2P_3_2nd_Done	-	-	-	-	-	MTP_BUSY	-	0x00h													
Description	This command is to check MTP status of mapping CMD Pages.																									
	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Data</th></tr> </thead> <tbody> <tr> <td>CMD2P0_1st_Done</td><td>CMD2 Page0 1st MTP status</td><td rowspan="11">0: Not Programmed 1: Programmed</td></tr> <tr> <td>CMD2P0_2nd_Done</td><td>CMD2 Page0 2nd MTP status</td></tr> <tr> <td>CMD2P0_3rd_Done</td><td>CMD2 Page0 3rd MTP status</td></tr> <tr> <td>CMD2P1_1st_Done</td><td>CMD2 Page1 1st MTP status</td></tr> <tr> <td>CMD2P1_2nd_Done</td><td>CMD2 Page1 2nd MTP status</td></tr> <tr> <td>CMD2P2_1st_Done</td><td>CMD2 Page2 1st MTP status</td></tr> <tr> <td>CMD2P2_2nd_Done</td><td>CMD2 Page2 2nd MTP status</td></tr> <tr> <td>CMD2P3_1st_Done</td><td>CMD2 Page3 1st MTP status</td></tr> <tr> <td>CMD2P3_2nd_Done</td><td>CMD2 Page3 2nd MTP status</td></tr> </tbody> </table>		Bit	Description	Data	CMD2P0_1st_Done	CMD2 Page0 1 st MTP status	0: Not Programmed 1: Programmed	CMD2P0_2nd_Done	CMD2 Page0 2nd MTP status	CMD2P0_3rd_Done	CMD2 Page0 3rd MTP status	CMD2P1_1st_Done	CMD2 Page1 1 st MTP status	CMD2P1_2nd_Done	CMD2 Page1 2 nd MTP status	CMD2P2_1st_Done	CMD2 Page2 1 st MTP status	CMD2P2_2nd_Done	CMD2 Page2 2 nd MTP status	CMD2P3_1st_Done	CMD2 Page3 1 st MTP status	CMD2P3_2nd_Done	CMD2 Page3 2 nd MTP status		
Bit	Description	Data																								
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CMD2P0_3rd_Done	CMD2 Page0 3rd MTP status																									
CMD2P1_1st_Done	CMD2 Page1 1 st MTP status																									
CMD2P1_2nd_Done	CMD2 Page1 2 nd MTP status																									
CMD2P2_1st_Done	CMD2 Page2 1 st MTP status																									
CMD2P2_2nd_Done	CMD2 Page2 2 nd MTP status																									
CMD2P3_1st_Done	CMD2 Page3 1 st MTP status																									
CMD2P3_2nd_Done	CMD2 Page3 2 nd MTP status																									
This command is for MTP Program Flow Control.																										
<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Data</th></tr> </thead> <tbody> <tr> <td>MTP_BUSY</td><td>MTP Programming Status</td><td>0: Finish 1: Ongoing</td></tr> </tbody> </table>														Bit	Description	Data	MTP_BUSY	MTP Programming Status	0: Finish 1: Ongoing							
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Status	Default Value																									

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Power On Sequence			
S/W Reset		0xEE40h	0x00h
H/W Reset		0xEF40h	0x00h

CONFIDENTIAL

(F040h) MTP Control

		MTPCTR																													
Instruction	R/W	Address		Parameter																											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
MTPCTR	R/W	0xF0h	0xF040h	00h	OTP_c md2_P 0_PGM _3rdEN	-	OTP_c md2_P 0_PGM _EN	OTP_c md2_P 1_PGM _EN	OTP_c md2_P 2_PGM _EN	OTP_c md2_P 3_PGM _EN	-	-	0x00h																		
Description	This command is to enable MTP program function of corresponding CMD pages.																														
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>OTP_cmd2_P0_PGM_3rdEN</td> <td>Enable CMD2 Page0 3rd program function (only from 0xE140 to 0xE740)</td> <td>0: Disable 1: Enable</td> </tr> <tr> <td>OTP_cmd2_P0_PGM_EN</td> <td>Enable CMD2 Page0 program function</td> <td>0: Disable 1: Enable</td> </tr> <tr> <td>OTP_cmd2_P1_PGM_EN</td> <td>Enable CMD2 Page1 program function</td> <td>0: Disable 1: Enable</td> </tr> <tr> <td>OTP_cmd2_P2_PGM_EN</td> <td>Enable CMD2 Page2 program function</td> <td>0: Disable 1: Enable</td> </tr> <tr> <td>OTP_cmd2_P3_PGM_EN</td> <td>Enable CMD2 Page3 program function</td> <td>0: Disable 1: Enable</td> </tr> </tbody> </table>													Bit	Description	Data	OTP_cmd2_P0_PGM_3rdEN	Enable CMD2 Page0 3 rd program function (only from 0xE140 to 0xE740)	0: Disable 1: Enable	OTP_cmd2_P0_PGM_EN	Enable CMD2 Page0 program function	0: Disable 1: Enable	OTP_cmd2_P1_PGM_EN	Enable CMD2 Page1 program function	0: Disable 1: Enable	OTP_cmd2_P2_PGM_EN	Enable CMD2 Page2 program function	0: Disable 1: Enable	OTP_cmd2_P3_PGM_EN	Enable CMD2 Page3 program function	0: Disable 1: Enable
Bit	Description	Data																													
OTP_cmd2_P0_PGM_3rdEN	Enable CMD2 Page0 3 rd program function (only from 0xE140 to 0xE740)	0: Disable 1: Enable																													
OTP_cmd2_P0_PGM_EN	Enable CMD2 Page0 program function	0: Disable 1: Enable																													
OTP_cmd2_P1_PGM_EN	Enable CMD2 Page1 program function	0: Disable 1: Enable																													
OTP_cmd2_P2_PGM_EN	Enable CMD2 Page2 program function	0: Disable 1: Enable																													
OTP_cmd2_P3_PGM_EN	Enable CMD2 Page3 program function	0: Disable 1: Enable																													
Restriction																															
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Status	Default Value																														
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Power On Sequence	0x00h																														
S/W Reset	0x00h																														
H/W Reset	0x00h																														

(F240h) MTP Control

		MTPW																																			
Instruction	R/W	Address		Parameter																																	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
MTPW	R/W	0xF2h	0xF240h	00h	-	-	-	-	-	-	1	MTP_W	0x02h																								
Description	This command is to control MTP Program function.																																				
	<table border="1"> <thead> <tr> <th>Bit</th><th colspan="3">Description</th><th colspan="3">Data</th></tr> </thead> <tbody> <tr> <td>MTP_W</td><td colspan="3">MTP Program function control</td><td colspan="3" rowspan="3">0: No Programming 1: Execute Programming</td></tr> </tbody> </table>													Bit	Description			Data			MTP_W	MTP Program function control			0: No Programming 1: Execute Programming												
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Power On Sequence		0x02h																																			
S/W Reset		0x02h																																			
H/W Reset		0x02h																																			

(F340h) MTP Control

		MTPW1																																																																																																
Instruction	R/W	Address		Parameter																																																																																														
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																					
MTPW1	W	0xF3h	0xF340h	00h	1	0	1	0	0	1	0	1	0xA5h																																																																																					
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(F440h) MTP Control

		MTPW2																																																																																									
Instruction	R/W	Address		Parameter																																																																																							
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																														
MTPW2	W	0xF4h	0xF440h	00h	0	1	0	1	1	0	1	0	0x5Ah																																																																														
Description	MTP Write Command.																																																																																										
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(F540h) MTP Control

Instruction	R/W	MTPW3																																																																																									
		Address		Parameter																																																																																							
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																														
MTPW3	W	0xF5h	0xF540h	00h	0	0	1	1	1	1	0	0	0x3Ch																																																																														
Description	MTP Write Command.																																																																																										
Restriction																																																																																											
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(FE40h) CMD Mode Switch

		CMD Mode Switch																												
Instruction	R/W	Address		Parameter																										
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
CMD Mode Switch	R/W	0xFEh	0xFE40h	00h	-	-	-	-	CMD_Page[3:0]			0x00h																		
Description	This command is used to switch the Manufacture Command Pages and User Commands sets.																													
	<table border="1"> <thead> <tr> <th>CMD_Page[3:0]</th> <th>Hex Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h (default)</td> <td>User Command Set (UCS = CMD1)</td> </tr> <tr> <td>0001</td> <td>01h</td> <td>Manufacture Command Set Page0 (CMD2 P0)</td> </tr> <tr> <td>0010</td> <td>02h</td> <td>Manufacture Command Set Page1 (CMD2 P1)</td> </tr> <tr> <td>0011</td> <td>03h</td> <td>Manufacture Command Set Page2 (CMD2 P2)</td> </tr> <tr> <td>0100</td> <td>04h</td> <td>Manufacture Command Set Page3 (CMD2 P3)</td> </tr> </tbody> </table>													CMD_Page[3:0]	Hex Value	Description	0000	00h (default)	User Command Set (UCS = CMD1)	0001	01h	Manufacture Command Set Page0 (CMD2 P0)	0010	02h	Manufacture Command Set Page1 (CMD2 P1)	0011	03h	Manufacture Command Set Page2 (CMD2 P2)	0100	04h
CMD_Page[3:0]	Hex Value	Description																												
0000	00h (default)	User Command Set (UCS = CMD1)																												
0001	01h	Manufacture Command Set Page0 (CMD2 P0)																												
0010	02h	Manufacture Command Set Page1 (CMD2 P1)																												
0011	03h	Manufacture Command Set Page2 (CMD2 P2)																												
0100	04h	Manufacture Command Set Page3 (CMD2 P3)																												
Restriction																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
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Power On Sequence	0x00h																													
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(FF40h) RD CMD Status

		RD CMD Status																																																																																														
Instruction	R/W	Address		Parameter																																																																																												
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																			
RD CMD Status	R	0xFFh	0xFF40h	00h	-	-	-	-	Current_CMD_Page			0x01h																																																																																				
Description	This command is used to confirm current CMD Page Settings..																																																																																															
Restriction																																																																																																
Register Availability	<table border="1"> <thead> <tr> <th colspan="5">Status</th><th colspan="8">Availability</th></tr> </thead> <tbody> <tr> <td colspan="5">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="5">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="8">Yes</td></tr> <tr> <td colspan="5">Sleep In</td><td colspan="8" rowspan="7">Yes</td></tr> </tbody> </table>													Status					Availability								Normal Mode On, Idle Mode Off, Sleep Out					Yes								Normal Mode On, Idle Mode On, Sleep Out					Yes								Partial Mode On, Idle Mode Off, Sleep Out					Yes								Partial Mode On, Idle Mode On, Sleep Out					Yes								Sleep In					Yes												
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1.4 MCS: CMD2 Page1 = Gamma Settings

Instruction	R/ W	Address		Parameter									Function	
		MIPI	Others	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaR_1	R/ W	0x00 h	0x0050h	00h	-	-	-	-	-	-	V0R1[9:8]		Gamma	
GmaR_1	R/ W	0x01 h	0x0150h	00h	V0R1[7:0]									Gamma
GmaR_1	R/ W	0x02 h	0x0250h	00h	-	-	-	-	-	-	V1R1[9:8]		Gamma	
GmaR_1	R/ W	0x03 h	0x0350h	00h	V1R1[7:0]									Gamma
GmaR_1	R/ W	0x04 h	0x0450h	00h	-	-	-	-	-	-	V2R1[9:8]		Gamma	
GmaR_1	R/ W	0x05 h	0x0550h	00h	V2R1[7:0]									Gamma
GmaR_1	R/ W	0x06 h	0x0650h	00h	-	-	-	-	-	-	V3R1[9:8]		Gamma	
GmaR_1	R/ W	0x07 h	0x0750h	00h	V3R1[7:0]									Gamma
GmaR_1	R/ W	0x08 h	0x0850h	00h	-	-	-	-	-	-	V4R1[9:8]		Gamma	
GmaR_1	R/ W	0x09 h	0x0950h	00h	V4R1[7:0]									Gamma
GmaR_1	R/ W	0x0A h	0x0A50h	00h	-	-	-	-	-	-	V5R1[9:8]		Gamma	
GmaR_1	R/ W	0x0B h	0x0B50h	00h	V5R1[7:0]									Gamma
GmaR_1	R/ W	0x0C h	0x0C50 h	00h	-	-	-	-	-	-	V6R1[9:8]		Gamma	
GmaR_1	R/ W	0x0D h	0x0D50 h	00h	V6R1[7:0]									Gamma
GmaR_1	R/ W	0x0E h	0x0E50h	00h	-	-	-	-	-	-	V7R1[9:8]		Gamma	
GmaR_1	R/ W	0x0F h	0x0F50h	00h	V7R1[7:0]									Gamma
GmaR_1	R/ W	0x10 h	0x1050h	00h	-	-	-	-	-	-	V8R1[9:8]		Gamma	
GmaR_1	R/ W	0x11 h	0x1150h	00h	V8R1[7:0]									Gamma
GmaR_1	R/ W	0x12 h	0x1250h	00h	-	-	-	-	-	-	V9R1[9:8]		Gamma	
GmaR_1	R/ W	0x13 h	0x1350h	00h	V9R1[7:0]									Gamma
GmaR_1	R/ W	0x14 h	0x1450h	00h	-	-	-	-	-	-	V10R1[9:8]		Gamma	
GmaR_1	R/ W	0x15 h	0x1550h	00h	V10R1[7:0]									Gamma
GmaR_1	R/ W	0x16 h	0x1650h	00h	-	-	-	-	-	-	V11R1[9:8]		Gamma	
GmaR_1	R/ W	0x17 h	0x1750h	00h	V11R1[7:0]									Gamma
GmaR_1	R/ W	0x18 h	0x1850h	00h	-	-	-	-	-	-	V12R1[9:8]		Gamma	

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Instruction	R/ W	Address		Parameter									Function	
		MIPI	Others	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaR_1	R/ W	0x19 h	0x1950h	00h	V12R1[7:0]									Gamma
GmaR_1	R/ W	0x1A h	0x1A50h	00h	-	-	-	-	-	-	-	V13R1[9:8]	Gamma	
GmaR_1	R/ W	0x1B h	0x1B50h	00h	V13R1[7:0]									Gamma
GmaR_1	R/ W	0x1C h	0x1C50 h	00h	-	-	-	-	-	-	-	V14R1[9:8]	Gamma	
GmaR_1	R/ W	0x1D h	0x1D50 h	00h	V14R1[7:0]									Gamma
GmaR_1	R/ W	0x1E h	0x1E50h	00h	-	-	-	-	-	-	-	V15R1[9:8]	Gamma	
GmaR_1	R/ W	0x1F h	0x1F50h	00h	V15R1[7:0]									Gamma
GmaR_1	R/ W	0x20 h	0x2050h	00h	-	-	-	-	-	-	-	V16R1[9:8]	Gamma	
GmaR_1	R/ W	0x21 h	0x2150h	00h	V16R1[7:0]									Gamma
GmaR_1	R/ W	0x22 h	0x2250h	00h	-	-	-	-	-	-	-	V17R1[9:8]	Gamma	
GmaR_1	R/ W	0x23 h	0x2350h	00h	V17R1[7:0]									Gamma
GmaR_1	R/ W	0x24 h	0x2450h	00h	-	-	-	-	-	-	-	V18R1[9:8]	Gamma	
GmaR_1	R/ W	0x25 h	0x2550h	00h	V18R1[7:0]									Gamma
GmaR_1	R/ W	0x26 h	0x2650h	00h	-	-	-	-	-	-	-	V19R1[9:8]	Gamma	
GmaR_1	R/ W	0x27 h	0x2750h	00h	V19R1[7:0]									Gamma
GmaR_1	R/ W	0x28 h	0x2850h	00h	-	-	-	-	-	-	-	V20R1[9:8]	Gamma	
GmaR_1	R/ W	0x29 h	0x2950h	00h	V20R1[7:0]									Gamma
GmaR_1	R/ W	0x2A h	0x2A50h	00h	-	-	-	-	-	-	-	V21R1[9:8]	Gamma	
GmaR_1	R/ W	0x2B h	0x2B50h	00h	V21R1[7:0]									Gamma
GmaR_1	R/ W	0x2D h	0x2D50 h	00h	-	-	-	-	-	-	-	V22R1[9:8]	Gamma	
GmaR_1	R/ W	0x2F h	0x2F50h	00h	V22R1[7:0]									Gamma
GmaR_1	R/ W	0x30 h	0x3050h	00h	-	-	-	-	-	-	-	V23R1[9:8]	Gamma	
GmaR_1	R/ W	0x31 h	0x3150h	00h	V23R1[7:0]									Gamma
GmaR_1	R/ W	0x32 h	0x3250h	00h	-	-	-	-	-	-	-	V24R1[9:8]	Gamma	
GmaR_1	R/ W	0x33 h	0x3350h	00h	V24R1[7:0]									Gamma
GmaG_1	R/	0x34	0x3450h	00h	-	-	-	-	-	-	-	V0G1[9:8]	Gamma	

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Instruction	R/ W	Address		Parameter									Function	
		MIPI	Others	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0		
	W	h												
GmaG_1	R/ W	0x35h	0x3550h	00h	V0G1[7:0]									Gamma
GmaG_1	R/ W	0x36h	0x3650h	00h	-	-	-	-	-	-	V1G1[9:8]		Gamma	
GmaG_1	R/ W	0x37h	0x3750h	00h	V1G1[7:0]									Gamma
GmaG_1	R/ W	0x38h	0x3850h	00h	-	-	-	-	-	-	V2G1[9:8]		Gamma	
GmaG_1	R/ W	0x39h	0x3950h	00h	V2G1[7:0]									Gamma
GmaG_1	R/ W	0x3Ah	0x3A50h	00h	-	-	-	-	-	-	V3G1[9:8]		Gamma	
GmaG_1	R/ W	0x3Bh	0x3B50h	00h	V3G1[7:0]									Gamma
GmaG_1	R/ W	0x3Dh	0x3D50h	00h	-	-	-	-	-	-	V4G1[9:8]		Gamma	
GmaG_1	R/ W	0x3Fh	0x3F50h	00h	V4G1[7:0]									Gamma
GmaG_1	R/ W	0x40h	0x4050h	00h	-	-	-	-	-	-	V5G1[9:8]		Gamma	
GmaG_1	R/ W	0x41h	0x4150h	00h	V5G1[7:0]									Gamma
GmaG_1	R/ W	0x42h	0x4250h	00h	-	-	-	-	-	-	V6G1[9:8]		Gamma	
GmaG_1	R/ W	0x43h	0x4350h	00h	V6G1[7:0]									Gamma
GmaG_1	R/ W	0x44h	0x4450h	00h	-	-	-	-	-	-	V7G1[9:8]		Gamma	
GmaG_1	R/ W	0x45h	0x4550h	00h	V7G1[7:0]									Gamma
GmaG_1	R/ W	0x46h	0x4650h	00h	-	-	-	-	-	-	V8G1[9:8]		Gamma	
GmaG_1	R/ W	0x47h	0x4750h	00h	V8G1[7:0]									Gamma
GmaG_1	R/ W	0x48h	0x4850h	00h	-	-	-	-	-	-	V9G1[9:8]		Gamma	
GmaG_1	R/ W	0x49h	0x4950h	00h	V9G1[7:0]									Gamma
GmaG_1	R/ W	0x4Ah	0x4A50h	00h	-	-	-	-	-	-	V10G1[9:8]		Gamma	
GmaG_1	R/ W	0x4Bh	0x4B50h	00h	V10G1[7:0]									Gamma
GmaG_1	R/ W	0x4Ch	0x4C50h	00h	-	-	-	-	-	-	V11G1[9:8]		Gamma	
GmaG_1	R/ W	0x4Dh	0x4D50h	00h	V11G1[7:0]									Gamma
GmaG_1	R/ W	0x4Eh	0x4E50h	00h	-	-	-	-	-	-	V12G1[9:8]		Gamma	
GmaG_1	R/ W	0x4Fh	0x4F50h	00h	V12G1[7:0]									Gamma

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Instruction	R/ W	Address		Parameter									Function
		MIP1	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	
GmaG_1	R/ W	0x50h	0x5050h	00h	-	-	-	-	-	-	V13G1[9:8]	Gamma	
GmaG_1	R/ W	0x51h	0x5150h	00h	V13G1[7:0]								
GmaG_1	R/ W	0x52h	0x5250h	00h	-	-	-	-	-	-	V14G1[9:8]	Gamma	
GmaG_1	R/ W	0x53h	0x5350h	00h	V14G1[7:0]								
GmaG_1	R/ W	0x54h	0x5450h	00h	-	-	-	-	-	-	V15G1[9:8]	Gamma	
GmaG_1	R/ W	0x55h	0x5550h	00h	V15G1[7:0]								
GmaG_1	R/ W	0x56h	0x5650h	00h	-	-	-	-	-	-	V16G1[9:8]	Gamma	
GmaG_1	R/ W	0x58h	0x5850h	00h	V16G1[7:0]								
GmaG_1	R/ W	0x59h	0x5950h	00h	-	-	-	-	-	-	V17G1[9:8]	Gamma	
GmaG_1	R/ W	0x5Ah	0x5A50h	00h	V17G1[7:0]								
GmaG_1	R/ W	0x5Bh	0x5B50h	00h	-	-	-	-	-	-	V18G1[9:8]	Gamma	
GmaG_1	R/ W	0x5Ch	0x5C50h	00h	V18G1[7:0]								
GmaG_1	R/ W	0x5Dh	0x5D50h	00h	-	-	-	-	-	-	V19G1[9:8]	Gamma	
GmaG_1	R/ W	0x5Eh	0x5E50h	00h	V19G1[7:0]								
GmaG_1	R/ W	0x5Fh	0x5F50h	00h	-	-	-	-	-	-	V20G1[9:8]	Gamma	
GmaG_1	R/ W	0x60h	0x6050h	00h	V20G1[7:0]								
GmaG_1	R/ W	0x61h	0x6150h	00h	-	-	-	-	-	-	V21G1[9:8]	Gamma	
GmaG_1	R/ W	0x62h	0x6250h	00h	V21G1[7:0]								
GmaG_1	R/ W	0x63h	0x6350h	00h	-	-	-	-	-	-	V22G1[9:8]	Gamma	
GmaG_1	R/ W	0x64h	0x6450h	00h	V22G1[7:0]								
GmaG_1	R/ W	0x65h	0x6550h	00h	-	-	-	-	-	-	V23G1[9:8]	Gamma	
GmaG_1	R/ W	0x66h	0x6650h	00h	V23G1[7:0]								
GmaG_1	R/ W	0x67h	0x6750h	00h	-	-	-	-	-	-	V24G1[9:8]	Gamma	
GmaG_1	R/ W	0x68h	0x6850h	00h	V24G1[7:0]								
GmaB_1	R/ W	0x69h	0x6950h	00h	-	-	-	-	-	-	V0B1[9:8]	Gamma	
GmaB_1	R/	0x6Ah	0x6A50h	00h	V0B1[7:0]								

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Instruction	R/ W	Address		Parameter									Function	
		MIPi	Others	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0		
	W	h			-	-	-	-	-	-	-	-		
GmaB_1	R/ W	0x6B h	0x6B50h	00h	-	-	-	-	-	-	V1B1[9:8]	Gamma		
GmaB_1	R/ W	0x6C h	0x6C50 h	00h	V1B1[7:0]									Gamma
GmaB_1	R/ W	0x6D h	0x6D50 h	00h	-	-	-	-	-	-	V2B1[9:8]	Gamma		
GmaB_1	R/ W	0x6E h	0x6E50h	00h	V2B1[7:0]									Gamma
GmaB_1	R/ W	0x6F h	0x6F50h	00h	-	-	-	-	-	-	V3B1[9:8]	Gamma		
GmaB_1	R/ W	0x70 h	0x7050h	00h	V3B1[7:0]									Gamma
GmaB_1	R/ W	0x71 h	0x7150h	00h	-	-	-	-	-	-	V4B1[9:8]	Gamma		
GmaB_1	R/ W	0x72 h	0x7250h	00h	V4B1[7:0]									Gamma
GmaB_1	R/ W	0x73 h	0x7350h	00h	-	-	-	-	-	-	V5B1[9:8]	Gamma		
GmaB_1	R/ W	0x74 h	0x7450h	00h	V5B1[7:0]									Gamma
GmaB_1	R/ W	0x75 h	0x7550h	00h	-	-	-	-	-	-	V6B1[9:8]	Gamma		
GmaB_1	R/ W	0x76 h	0x7650h	00h	V6B1[7:0]									Gamma
GmaB_1	R/ W	0x77 h	0x7750h	00h	-	-	-	-	-	-	V7B1[9:8]	Gamma		
GmaB_1	R/ W	0x78 h	0x7850h	00h	V7B1[7:0]									Gamma
GmaB_1	R/ W	0x79 h	0x7950h	00h	-	-	-	-	-	-	V8B1[9:8]	Gamma		
GmaB_1	R/ W	0x7A h	0x7A50h	00h	V8B1[7:0]									Gamma
GmaB_1	R/ W	0x7B h	0x7B50h	00h	-	-	-	-	-	-	V9B1[9:8]	Gamma		
GmaB_1	R/ W	0x7C h	0x7C50 h	00h	V9B1[7:0]									Gamma
GmaB_1	R/ W	0x7D h	0x7D50 h	00h	-	-	-	-	-	-	V10B1[9:8]	Gamma		
GmaB_1	R/ W	0x7E h	0x7E50h	00h	V10B1[7:0]									Gamma
GmaB_1	R/ W	0x7F h	0x7F50h	00h	-	-	-	-	-	-	V11B1[9:8]	Gamma		
GmaB_1	R/ W	0x80 h	0x8050h	00h	V11B1[7:0]									Gamma
GmaB_1	R/ W	0x81 h	0x8150h	00h	-	-	-	-	-	-	V12B1[9:8]	Gamma		
GmaB_1	R/ W	0x82 h	0x8250h	00h	V12B1[7:0]									Gamma
GmaB_1	R/ W	0x83 h	0x8350h	00h	-	-	-	-	-	-	V13B1[9:8]	Gamma		

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Instruction	R/ W	Address		Parameter									Function	
		MIPI	Others	D15- D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaB_1	R/ W	0x84 h	0x8450h	00h	V13B1[7:0]									Gamma
GmaB_1	R/ W	0x85 h	0x8550h	00h	-	-	-	-	-	-	V14B1[9:8]		Gamma	
GmaB_1	R/ W	0x86 h	0x8650h	00h	V14B1[7:0]									Gamma
GmaB_1	R/ W	0x87 h	0x8750h	00h	-	-	-	-	-	-	V15B1[9:8]		Gamma	
GmaB_1	R/ W	0x88 h	0x8850h	00h	V15B1[7:0]									Gamma
GmaB_1	R/ W	0x89 h	0x8950h	00h	-	-	-	-	-	-	V16B1[9:8]		Gamma	
GmaB_1	R/ W	0x8A h	0x8A50h	00h	V16B1[7:0]									Gamma
GmaB_1	R/ W	0x8B h	0x8B50h	00h	-	-	-	-	-	-	V17B1[9:8]		Gamma	
GmaB_1	R/ W	0x8C h	0x8C50 h	00h	V17B1[7:0]									Gamma
GmaB_1	R/ W	0x8D h	0x8D50 h	00h	-	-	-	-	-	-	V18B1[9:8]		Gamma	
GmaB_1	R/ W	0x8E h	0x8E50h	00h	V18B1[7:0]									Gamma
GmaB_1	R/ W	0x8F h	0x8F50h	00h	-	-	-	-	-	-	V19B1[9:8]		Gamma	
GmaB_1	R/ W	0x90 h	0x9050h	00h	V19B1[7:0]									Gamma
GmaB_1	R/ W	0x91 h	0x9150h	00h	-	-	-	-	-	-	V20B1[9:8]		Gamma	
GmaB_1	R/ W	0x92 h	0x9250h	00h	V20B1[7:0]									Gamma
GmaB_1	R/ W	0x93 h	0x9350h	00h	-	-	-	-	-	-	V21B1[9:8]		Gamma	
GmaB_1	R/ W	0x94 h	0x9450h	00h	V21B1[7:0]									Gamma
GmaB_1	R/ W	0x95 h	0x9550h	00h	-	-	-	-	-	-	V22B1[9:8]		Gamma	
GmaB_1	R/ W	0x96 h	0x9650h	00h	V22B1[7:0]									Gamma
GmaB_1	R/ W	0x97 h	0x9750h	00h	-	-	-	-	-	-	V23B1[9:8]		Gamma	
GmaB_1	R/ W	0x98 h	0x9850h	00h	V23B1[7:0]									Gamma
GmaB_1	R/ W	0x99 h	0x9950h	00h	-	-	-	-	-	-	V24B1[9:8]		Gamma	
GmaB_1	R/ W	0x9A h	0x9A50h	00h	V24B1[7:0]									Gamma
Gma_10p	R/ W	0x9B h	0x9B50h	00h	-	-	-	GMA _10P 1	-	-	-	-	-	Gamma

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(0050h~3350h) Gamma 2.2 Correction Set 1 for Red

Instruction	R/W	GammaR_1											
		Address		Parameter									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaR_1	R/W	0x00h	0x0050h	00h	-	-	-	-	-	-	V0R1[9:8]	0x00h	
		0x01h	0x0150h	00h	V0R1[7:0]								0x00h
		0x02h	0x0250h	00h	-	-	-	-	-	-	V1R1[9:8]	0x00h	
		0x03h	0x0350h	00h	V1R1[7:0]								0x1Ch
		0x04h	0x0450h	00h	-	-	-	-	-	-	V2R1[9:8]	0x00h	
		0x05h	0x0550h	00h	V2R1[7:0]								0x2Ch
		0x06h	0x0650h	00h	-	-	-	-	-	-	V3R1[9:8]	0x00h	
		0x07h	0x0750h	00h	V3R1[7:0]								0x3Ch
		0x08h	0x0850h	00h	-	-	-	-	-	-	V4R1[9:8]	0x00h	
		0x09h	0x0950h	00h	V4R1[7:0]								0x4Ch
		0x0Ah	0x0A50h	00h	-	-	-	-	-	-	V5R1[9:8]	0x00h	
		0x0Bh	0x0B50h	00h	V5R1[7:0]								0x5Ch
		0x0Ch	0x0C50h	00h	-	-	-	-	-	-	V6R1[9:8]	0x00h	
		0x0Dh	0x0D50h	00h	V6R1[7:0]								0x6Ch
		0x0Eh	0x0E50h	00h	-	-	-	-	-	-	V7R1[9:8]	0x00h	
		0x0Fh	0x0F50h	00h	V7R1[7:0]								0x7Ch
		0x10h	0x1050h	00h	-	-	-	-	-	-	V8R1[9:8]	0x00h	
		0x11h	0x1150h	00h	V8R1[7:0]								0x8Ch
		0x12h	0x1250h	00h	-	-	-	-	-	-	V9R1[9:8]	0x00h	
		0x13h	0x1350h	00h	V9R1[7:0]								0x9Ch
		0x14h	0x1450h	00h	-	-	-	-	-	-	V10R1[9:8]	0x00h	
		0x15h	0x1550h	00h	V10R1[7:0]								0xBCh
		0x16h	0x1650h	00h	-	-	-	-	-	-	V11R1[9:8]	0x00h	
		0x17h	0x1750h	00h	V11R1[7:0]								0xDCh

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GammaR_1 R/W	0x18h	0x1850h	00h	-	-	-	-	-	V12R1[9:8]	0x00h
	0x19h	0x1950h	00h	V12R1[7:0]						0xFCh
	0x1Ah	0x1A50h	00h	-	-	-	-	-	V13R1[9:8]	0x01h
	0x1Bh	0x1B50h	00h	V13R1[7:0]						0x3Ch
	0x1Ch	0x1C50h	00h	-	-	-	-	-	V14R1[9:8]	0x01h
	0x1Dh	0x1D50h	00h	V14R1[7:0]						0x7Ch
	0x1Eh	0x1E50h	00h	-	-	-	-	-	V15R1[9:8]	0x01h
	0x1Fh	0x1F50h	00h	V15R1[7:0]						0xBCh
	0x20h	0x2050h	00h	-	-	-	-	-	V16R1[9:8]	0x01h
	0x21h	0x2150h	00h	V16R1[7:0]						0xFCh
	0x22h	0x2250h	00h	-	-	-	-	-	V17R1[9:8]	0x02h
	0x23h	0x2350h	00h	V17R1[7:0]						0x3Ch
	0x24h	0x2450h	00h	-	-	-	-	-	V18R1[9:8]	0x02h
	0x25h	0x2550h	00h	V18R1[7:0]						0x7Ch
	0x26h	0x2650h	00h	-	-	-	-	-	V19R1[9:8]	0x02h
	0x27h	0x2750h	00h	V19R1[7:0]						0xBCh
	0x28h	0x2850h	00h	-	-	-	-	-	V20R1[9:8]	0x02h
	0x29h	0x2950h	00h	V20R1[7:0]						0xFCh
	0x2Ah	0x2A50h	00h	-	-	-	-	-	V21R1[9:8]	0x03h
	0x2Bh	0x2B50h	00h	V21R1[7:0]						0x3Ch
	0x2Dh	0x2D50h	00h	-	-	-	-	-	V22R1[9:8]	0x03h
	0x2Fh	0x2F50h	00h	V22R1[7:0]						0x7Ch
	0x30h	0x3050h	00h	-	-	-	-	-	V23R1[9:8]	0x03h
	0x31h	0x3150h	00h	V23R1[7:0]						0xBCh
	0x32h	0x3250h	00h	-	-	-	-	-	V24R1[9:8]	0x03h
	0x33h	0x3350h	00h	V24R1[7:0]						0xFCh
	This command is used to adjust the gamma 2.2 correction for the red under normal display mode . For GMA_10P1=0 (default),									

Description	Adjust R_0(darkest) via V0R1
	Adjust R_7 via V1R1
	Adjust R_11 via V2R1
	Adjust R_15 via V3R1
	Adjust R_19 via V4R1
	Adjust R_23 via V5R1
	Adjust R_27 via V6R1
	Adjust R_31 via V7R1
	Adjust R_35 via V8R1
	Adjust R_39 via V9R1
	Adjust R_47 via V10R1
	Adjust R_55 via V11R1
	Adjust R_63 via V12R1
	Adjust R_79 via V13R1
	Adjust R_95 via V14R1
	Adjust R_111 via V15R1
	Adjust R_127 via V16R1
	Adjust R_143 via V17R1
	Adjust R_159 via V18R1
	Adjust R_175 via V19R1
	Adjust R_191 via V20R1
	Adjust R_207 via V21R1
	Adjust R_223 via V22R1
	Adjust R_239 via V23R1
	Adjust R_255(brightest) via V24R1
For GMA_10P1=1,	
Adjust R_0(darkest) via V0R1	
Adjust R_7 via V1R1	
Adjust R_11 via V2R1	

Description	Adjust R_15 via V3R1 Adjust R_31 via V7R1 Adjust R_63 via V12R1 Adjust R_95 via V14R1 Adjust R_127 via V16R1 Adjust R_159 via V18R1 Adjust R_191 via V20R1 Adjust R_255(brightest) via V24R1
Restriction	

(3450h~6850h) Gamma 2.2 Correction Set 1 for GREEN

Instruction	R/W	GammaG_1											
		Address		Parameter									
		MIPi	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaG_1	R/W	0x34h	0x3450h	00h	-	-	-	-	-	-	V0G1[9:8]	0x00h	
		0x35h	0x3550h	00h	V0G1[7:0]								0x00h
		0x36h	0x3650h	00h	-	-	-	-	-	-	V1G1[9:8]	0x00h	
		0x37h	0x3750h	00h	V1G1[7:0]								0x1Ch
		0x38h	0x3850h	00h	-	-	-	-	-	-	V2G1[9:8]	0x00h	
		0x39h	0x3950h	00h	V2G1[7:0]								0x2Ch
		0x3Ah	0x3A50h	00h	-	-	-	-	-	-	V3G1[9:8]	0x00h	
		0x3Bh	0x3B50h	00h	V3G1[7:0]								0x3Ch
		0x3Dh	0x3D50h	00h	-	-	-	-	-	-	V4G1[9:8]	0x00h	
		0x3Fh	0x3F50h	00h	V4G1[7:0]								0x4Ch
		0x40h	0x4050h	00h	-	-	-	-	-	-	V5G1[9:8]	0x00h	
		0x41h	0x4150h	00h	V5G1[7:0]								0x5Ch
		0x42h	0x4250h	00h	-	-	-	-	-	-	V6G1[9:8]	0x00h	
		0x43h	0x4350h	00h	V6G1[7:0]								0x6Ch
		0x44h	0x4450h	00h	-	-	-	-	-	-	V7G1[9:8]	0x00h	
		0x45h	0x4550h	00h	V7G1[7:0]								0x7Ch
		0x46h	0x4650h	00h	-	-	-	-	-	-	V8G1[9:8]	0x00h	
		0x47h	0x4750h	00h	V8G1[7:0]								0x8Ch
		0x48h	0x4850h	00h	-	-	-	-	-	-	V9G1[9:8]	0x00h	
		0x49h	0x4950h	00h	V9G1[7:0]								0x9Ch
		0x4Ah	0x4A50h	00h	-	-	-	-	-	-	V10G1[9:8]	0x00h	
		0x4Bh	0x4B50h	00h	V10G1[7:0]								0xBCh
		0x4Ch	0x4C50h	00h	-	-	-	-	-	-	V11G1[9:8]	0x00h	
		0x4Dh	0x4D50h	00h	V11G1[7:0]								0xDCh
		0x4Eh	0x4E50h	00h	-	-	-	-	-	-	V12G1[9:8]	0x00h	
		0x4Fh	0x4F50h	00h	V12G1[7:0]								0xFCh
		0x50h	0x5050h	00h	-	-	-	-	-	-	V13G1[9:8]	0x01h	
		0x51h	0x5150h	00h	V13G1[7:0]								0x3Ch
		0x52h	0x5250h	00h	-	-	-	-	-	-	V14G1[9:8]	0x01h	
		0x53h	0x5350h	00h	V14G1[7:0]								0x7Ch
		0x54h	0x5450h	00h	-	-	-	-	-	-	V15G1[9:8]	0x01h	
		0x55h	0x5550h	00h	V15G1[7:0]								0xBCh
		0x56h	0x5650h	00h	-	-	-	-	-	-	V16G1[9:8]	0x01h	

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GammaG_1 R/W	0x58h	0x5850h	00h	V16G1[7:0]							0xFCh	
	0x59h	0x5950h	00h	-	-	-	-	-	-	V17G1[9:8]	0x02h	
	0x5Ah	0x5A50h	00h	V17G1[7:0]							0x3Ch	
	0x5Bh	0x5B50h	00h	-	-	-	-	-	-	V18G1[9:8]	0x02h	
	0x5Ch	0x5C50h	00h	V18G1[7:0]							0x7Ch	
	0x5Dh	0x5D50h	00h	-	-	-	-	-	-	V19G1[9:8]	0x02h	
	0x5Eh	0x5E50h	00h	V19G1[7:0]							0xBCh	
	0x5Fh	0x5F50h	00h	-	-	-	-	-	-	V20G1[9:8]	0x02h	
	0x60h	0x6050h	00h	V20G1[7:0]							0xFCh	
	0x61h	0x6150h	00h	-	-	-	-	-	-	V21G1[9:8]	0x03h	
	0x62h	0x6250h	00h	V21G1[7:0]							0x3Ch	
	0x63h	0x6350h	00h	-	-	-	-	-	-	V22G1[9:8]	0x03h	
	0x64h	0x6450h	00h	V22G1[7:0]							0x7Ch	
	0x65h	0x6550h	00h	-	-	-	-	-	-	V23G1[9:8]	0x03h	
	0x66h	0x6650h	00h	V23G1[7:0]							0xBCh	
	0x67h	0x6750h	00h	-	-	-	-	-	-	V24G1[9:8]	0x03h	
	0x68h	0x6850h	00h	V24G1[7:0]							0xFCh	
Description	This command is used to adjust the gamma 2.2 correction for the green under normal display mode. For GMA_10P1=0(default), Adjust G_0(darkest) via V0G1 Adjust G_7 via V1G1 Adjust G_11 via V2G1 Adjust G_15 via V3G1 Adjust G_19 via V4G1 Adjust G_23 via V5G1 Adjust G_27 via V6G1 Adjust G_31 via V7G1 Adjust G_35 via V8G1 Adjust G_39 via V9G1 Adjust G_47 via V10G1 Adjust G_55 via V11G1 Adjust G_63 via V12G1 Adjust G_79 via V13G1 Adjust G_95 via V14G1 Adjust G_111 via V15G1 Adjust G_127 via V16G1 Adjust G_143 via V17G1 Adjust G_159 via V18G1 Adjust G_175 via V19G1											

	Adjust G_191 via V20G1 Adjust G_207 via V21G1 Adjust G_223 via V22G1 Adjust G_239 via V23G1 Adjust G_255(brightest) via V24G1
Description	For GMA_10P1=1, Adjust G_0(darkest) via V0G1 Adjust G_7 via V1G1 Adjust G_11 via V2G1 Adjust G_15 via V3G1 Adjust G_31 via V7G1 Adjust G_63 via V12G1 Adjust G_95 via V14G1 Adjust G_127 via V16G1 Adjust G_159 via V18G1 Adjust G_191 via V20G1 Adjust G_255(brightest) via V24G1
Restriction	

(6950h~9A50h) Gamma 2.2 Correction Set 1 for BLUE

Instruction	R/W	GammaB_1											
		Address		Parameter									
		MIP1	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaB_1	R/W	0x69h	0x6950h	00h	-	-	-	-	-	-	-	V0B1[9:8]	0x00h
		0x6Ah	0x6A50h	00h	V0B1[7:0]								0x00h
		0x6Bh	0x6B50h	00h	-	-	-	-	-	-	-	V1B1[9:8]	0x00h
		0x6Ch	0x6C50h	00h	V1B1[7:0]								0x1Ch
		0x6Dh	0x6D50h	00h	-	-	-	-	-	-	-	V2B1[9:8]	0x00h
		0x6Eh	0x6E50h	00h	V2B1[7:0]								0x2Ch
		0x6Fh	0x6F50h	00h	-	-	-	-	-	-	-	V3B1[9:8]	0x00h
		0x70h	0x7050h	00h	V3B1[7:0]								0x3Ch
		0x71h	0x7150h	00h	-	-	-	-	-	-	-	V4B1[9:8]	0x00h
		0x72h	0x7250h	00h	V4B1[7:0]								0x4Ch
		0x73h	0x7350h	00h	-	-	-	-	-	-	-	V5B1[9:8]	0x00h
		0x74h	0x7450h	00h	V5B1[7:0]								0x5Ch
		0x75h	0x7550h	00h	-	-	-	-	-	-	-	V6B1[9:8]	0x00h
		0x76h	0x7650h	00h	V6B1[7:0]								0x6Ch
		0x77h	0x7750h	00h	-	-	-	-	-	-	-	V7B1[9:8]	0x00h
		0x78h	0x7850h	00h	V7B1[7:0]								0x7Ch
		0x79h	0x7950h	00h	-	-	-	-	-	-	-	V8B1[9:8]	0x00h
		0x7Ah	0x7A50h	00h	V8B1[7:0]								0x8Ch
		0x7Bh	0x7B50h	00h	-	-	-	-	-	-	-	V9B1[9:8]	0x00h
		0x7Ch	0x7C50h	00h	V9B1[7:0]								0x9Ch
		0x7Dh	0x7D50h	00h	-	-	-	-	-	-	-	V10B1[9:8]	0x00h
		0x7Eh	0x7E50h	00h	V10B1[7:0]								0xBCh
		0x7Fh	0x7F50h	00h	-	-	-	-	-	-	-	V11B1[9:8]	0x00h
		0x80h	0x8050h	00h	V11B1[7:0]								0xDCh

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GammaB_1	R/W	0x81h	0x8150h	00h	-	-	-	-	-	V12B1[9:8]	0x00h
		0x82h	0x8250h	00h	V12B1[7:0]						0xFCh
		0x83h	0x8350h	00h	-	-	-	-	-	V13B1[9:8]	0x01h
		0x84h	0x8450h	00h	V13B1[7:0]						0x3Ch
		0x85h	0x8550h	00h	-	-	-	-	-	V14B1[9:8]	0x01h
		0x86h	0x8650h	00h	V14B1[7:0]						0x7Ch
		0x87h	0x8750h	00h	-	-	-	-	-	V15B1[9:8]	0x01h
		0x88h	0x8850h	00h	V15B1[7:0]						0xBCh
		0x89h	0x8950h	00h	-	-	-	-	-	V16B1[9:8]	0x01h
		0x8Ah	0x8A50h	00h	V16B1[7:0]						0xFCh
		0x8Bh	0x8B50h	00h	-	-	-	-	-	V17B1[9:8]	0x02h
		0x8Ch	0x8C50h	00h	V17B1[7:0]						0x3Ch
		0x8Dh	0x8D50h	00h	-	-	-	-	-	V18B1[9:8]	0x02h
		0x8Eh	0x8E50h	00h	V18B1[7:0]						0x7Ch
		0x8Fh	0x8F50h	00h	-	-	-	-	-	V19B1[9:8]	0x02h
		0x90h	0x9050h	00h	V19B1[7:0]						0xBCh
		0x91h	0x9150h	00h	-	-	-	-	-	V20B1[9:8]	0x02h
		0x92h	0x9250h	00h	V20B1[7:0]						0xFCh
		0x93h	0x9350h	00h	-	-	-	-	-	V21B1[9:8]	0x03h
		0x94h	0x9450h	00h	V21B1[7:0]						0x3Ch
		0x95h	0x9550h	00h	-	-	-	-	-	V22B1[9:8]	0x03h
		0x96h	0x9650h	00h	V22B1[7:0]						0x7Ch
		0x97h	0x9750h	00h	-	-	-	-	-	V23B1[9:8]	0x03h
		0x98h	0x9850h	00h	V23B1[7:0]						0xBCh
		0x99h	0x9950h	00h	-	-	-	-	-	V24B1[9:8]	0x03h
		0x9Ah	0x9A50h	00h	V24B1[7:0]						0xFCh
		0x9Bh	0x9B50h	00h				GMA10_P1			0x01h
This command is used to adjust the gamma 2.2 correction for the blue under normal display mode.											

	For GMA_10P1=0(default), Adjust B_0(darkest) via V0B1 Adjust B_7 via V1B1 Adjust B_11 via V2B1 Adjust B_15 via V3B1 Adjust B_19 via V4B1 Adjust B_23 via V5B1 Adjust B_27 via V6B1 Description Adjust B_31 via V7B1 Adjust B_35 via V8B1 Adjust B_39 via V9B1 Adjust B_47 via V10B1 Adjust B_55 via V11B1 Adjust B_63 via V12B1 Adjust B_79 via V13B1 Adjust B_95 via V14B1 Adjust B_111 via V15B1 Adjust B_127 via V16B1 Adjust B_143 via V17B1 Adjust B_159 via V18B1 Adjust B_175 via V19B1 Adjust B_191 via V20B1 Adjust B_207 via V21B1 Adjust B_223 via V22B1 Adjust B_239 via V23B1 Adjust B_255(brightest) via V24B1
	For GMA_10P1=1, Adjust B_0(darkest) via V0B1 Adjust B_7 via V1B1

Description	Adjust B_11 via V2B1 Adjust B_15 via V3B1 Adjust B_31 via V7B1 Adjust B_63 via V12B1 Adjust B_95 via V14B1 Adjust B_127 via V16B1 Adjust B_159 via V18B1 Adjust B_191 via V20B1 Adjust B_255(brightest) via V24B1
Restriction	

(FE50h) CMD Mode Switch

0xFE50h		CMD Mode Switch																													
Instruction	R/W	Address		Parameter																											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
CMD Mode Switch	R/W	0xFEh	0xFE50h	00h	-	-	-	-	CMD_Page_Selection				0x00h																		
Description	This command is used to switch the Manufacture Command Pages and User Commands sets. <table border="1"> <thead> <tr> <th>CMD_Page[3:0]</th><th>Hex Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000</td><td>00h (default)</td><td>User Command Set (UCS = CMD1)</td></tr> <tr> <td>0001</td><td>01h</td><td>Manufacture Command Set Page0 (CMD2 P0)</td></tr> <tr> <td>0010</td><td>02h</td><td>Manufacture Command Set Page1 (CMD2 P1)</td></tr> <tr> <td>0011</td><td>03h</td><td>Manufacture Command Set Page2 (CMD2 P2)</td></tr> <tr> <td>0100</td><td>04h</td><td>Manufacture Command Set Page3 (CMD2 P3)</td></tr> </tbody> </table>													CMD_Page[3:0]	Hex Value	Description	0000	00h (default)	User Command Set (UCS = CMD1)	0001	01h	Manufacture Command Set Page0 (CMD2 P0)	0010	02h	Manufacture Command Set Page1 (CMD2 P1)	0011	03h	Manufacture Command Set Page2 (CMD2 P2)	0100	04h	Manufacture Command Set Page3 (CMD2 P3)
CMD_Page[3:0]	Hex Value	Description																													
0000	00h (default)	User Command Set (UCS = CMD1)																													
0001	01h	Manufacture Command Set Page0 (CMD2 P0)																													
0010	02h	Manufacture Command Set Page1 (CMD2 P1)																													
0011	03h	Manufacture Command Set Page2 (CMD2 P2)																													
0100	04h	Manufacture Command Set Page3 (CMD2 P3)																													
Restriction																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
Default																															
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td colspan="2">Power On Sequence</td><td>0xFEh / 0xFE50h</td></tr> <tr> <td colspan="2">S/W Reset</td><td>0x00h</td></tr> <tr> <td colspan="2">H/W Reset</td><td>0x00h</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence		0xFEh / 0xFE50h	S/W Reset		0x00h	H/W Reset		0x00h								
Status	Default Value																														
Power On Sequence		0xFEh / 0xFE50h																													
S/W Reset		0x00h																													
H/W Reset		0x00h																													

(FF50h) RD CMD Status

		RD CMD Status																				
Instruction	R/W	Address		Parameter																		
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0										
RD CMD Status	R	0xFFh	0xFF50h	00h	-	-	-	-	Current_CMD_Page			0x00h										
Description	This command is used to confirm current CMD Page Settings..																					
	CMD_Page[3:0]	Hex Value			Description																	
	0000	00h (default)			User Command Set (UCS = CMD1)																	
	0001	01h			Manufacture Command Set Page0 (CMD2 P0)																	
	0010	02h			Manufacture Command Set Page1 (CMD2 P1)																	
	0011	03h			Manufacture Command Set Page2 (CMD2 P2)																	
	0100	04h			Manufacture Command Set Page3 (CMD2 P3)																	
Restriction																						
Register Availability	Status					Availability																
	Normal Mode On, Idle Mode Off, Sleep Out					Yes																
	Normal Mode On, Idle Mode On, Sleep Out					Yes																
	Partial Mode On, Idle Mode Off, Sleep Out					Yes																
	Partial Mode On, Idle Mode On, Sleep Out					Yes																
	Sleep In					Yes																
Default	Status			Default Value																		
				0xFFh / 0xFF50h																		
	Power On Sequence			0x00h																		
	S/W Reset			0x00h																		
	H/W Reset			0x00h																		

1.5 MCS: CMD2 Page2 = Gamma Settings

Instruction	R/W	Address		Parameter									Function
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	
GmaR_2	R/W	0x00h	0x0060h	00h	-	-	-	-	-	-	-	V0R2[9:8]	Gamma
GmaR_2	R/W	0x01h	0x0160h	00h	V0R2[7:0]								
GmaR_2	R/W	0x02h	0x0260h	00h	-	-	-	-	-	-	-	V1R2[9:8]	Gamma
GmaR_2	R/W	0x03h	0x0360h	00h	V1R2[7:0]								
GmaR_2	R/W	0x04h	0x0460h	00h	-	-	-	-	-	-	-	V2R2[9:8]	Gamma
GmaR_2	R/W	0x05h	0x0560h	00h	V2R2[7:0]								
GmaR_2	R/W	0x06h	0x0660h	00h	-	-	-	-	-	-	-	V3R2[9:8]	Gamma
GmaR_2	R/W	0x07h	0x0760h	00h	V3R2[7:0]								
GmaR_2	R/W	0x08h	0x0860h	00h	-	-	-	-	-	-	-	V4R2[9:8]	Gamma
GmaR_2	R/W	0x09h	0x0960h	00h	V4R2[7:0]								
GmaR_2	R/W	0xA0h	0x0A60h	00h	-	-	-	-	-	-	-	V5R2[9:8]	Gamma
GmaR_2	R/W	0xB0h	0x0B60h	00h	V5R2[7:0]								
GmaR_2	R/W	0xC0h	0x0C60h	00h	-	-	-	-	-	-	-	V6R2[9:8]	Gamma
GmaR_2	R/W	0xD0h	0x0D60h	00h	V6R2[7:0]								
GmaR_2	R/W	0xE0h	0x0E60h	00h	-	-	-	-	-	-	-	V7R2[9:8]	Gamma
GmaR_2	R/W	0xF0h	0x0F60h	00h	V7R2[7:0]								
GmaR_2	R/W	0x10h	0x1060h	00h	-	-	-	-	-	-	-	V8R2[9:8]	Gamma
GmaR_2	R/W	0x11h	0x1160h	00h	V8R2[7:0]								
GmaR_2	R/W	0x12h	0x1260h	00h	-	-	-	-	-	-	-	V9R2[9:8]	Gamma
GmaR_2	R/W	0x13h	0x1360h	00h	V9R2[7:0]								
GmaR_2	R/W	0x14h	0x1460h	00h	-	-	-	-	-	-	-	V10R2[9:8]	Gamma
GmaR_2	R/W	0x15h	0x1560h	00h	V10R2[7:0]								
GmaR_2	R/W	0x16h	0x1660h	00h	-	-	-	-	-	-	-	V11R2[9:8]	Gamma
GmaR_2	R/W	0x17h	0x1760h	00h	V11R2[7:0]								
GmaR_2	R/W	0x18h	0x1860h	00h	-	-	-	-	-	-	-	V12R2[9:8]	Gamma
GmaR_2	R/W	0x19h	0x1960h	00h	V12R2[7:0]								
GmaR_2	R/W	0x1Ah	0x1A60h	00h	-	-	-	-	-	-	-	V13R2[9:8]	Gamma
GmaR_2	R/W	0x1Bh	0x1B60h	00h	V13R2[7:0]								
GmaR_2	R/W	0x1Ch	0x1C60h	00h	-	-	-	-	-	-	-	V14R2[9:8]	Gamma
GmaR_2	R/W	0x1Dh	0x1D60h	00h	V14R2[7:0]								
GmaR_2	R/W	0x1Eh	0x1E60h	00h	-	-	-	-	-	-	-	V15R2[9:8]	Gamma
GmaR_2	R/W	0x1Fh	0x1F60h	00h	V15R2[7:0]								
GmaR_2	R/W	0x20h	0x2060h	00h	-	-	-	-	-	-	-	V16R2[9:8]	Gamma
GmaR_2	R/W	0x21h	0x2160h	00h	V16R2[7:0]								
GmaR_2	R/W	0x22h	0x2260h	00h	-	-	-	-	-	-	-	V17R2[9:8]	Gamma

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Manufacture Command Set (CMD2 Page2 Gamma2)														
Instruction	R/W	Address		Parameter									Function	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaR_2	R/W	0x23h	0x2360h	00h	V17R2[7:0]									Gamma
GmaR_2	R/W	0x24h	0x2460h	00h	-	-	-	-	-	-	-	V18R2[9:8]	Gamma	
GmaR_2	R/W	0x25h	0x2560h	00h	V18R2[7:0]									Gamma
GmaR_2	R/W	0x26h	0x2660h	00h	-	-	-	-	-	-	-	V19R2[9:8]	Gamma	
GmaR_2	R/W	0x27h	0x2760h	00h	V19R2[7:0]									Gamma
GmaR_2	R/W	0x28h	0x2860h	00h	-	-	-	-	-	-	-	V20R2[9:8]	Gamma	
GmaR_2	R/W	0x29h	0x2960h	00h	V20R2[7:0]									Gamma
GmaR_2	R/W	0x2Ah	0x2A60h	00h	-	-	-	-	-	-	-	V21R2[9:8]	Gamma	
GmaR_2	R/W	0x2Bh	0x2B60h	00h	V21R2[7:0]									Gamma
GmaR_2	R/W	0x2Dh	0x2D60h	00h	-	-	-	-	-	-	-	V22R2[9:8]	Gamma	
GmaR_2	R/W	0x2Fh	0x2F60h	00h	V22R2[7:0]									Gamma
GmaR_2	R/W	0x30h	0x3060h	00h	-	-	-	-	-	-	-	V23R2[9:8]	Gamma	
GmaR_2	R/W	0x31h	0x3160h	00h	V23R2[7:0]									Gamma
GmaR_2	R/W	0x32h	0x3260h	00h	-	-	-	-	-	-	-	V24R2[9:8]	Gamma	
GmaR_2	R/W	0x33h	0x3360h	00h	V24R2[7:0]									Gamma
GmaG_2	R/W	0x34h	0x3460h	00h	-	-	-	-	-	-	-	V0G2[9:8]	Gamma	
GmaG_2	R/W	0x35h	0x3560h	00h	V0G2[7:0]									Gamma
GmaG_2	R/W	0x36h	0x3660h	00h	-	-	-	-	-	-	-	V1G2[9:8]	Gamma	
GmaG_2	R/W	0x37h	0x3760h	00h	V1G2[7:0]									Gamma
GmaG_2	R/W	0x38h	0x3860h	00h	-	-	-	-	-	-	-	V2G2[9:8]	Gamma	
GmaG_2	R/W	0x39h	0x3960h	00h	V2G2[7:0]									Gamma
GmaG_2	R/W	0x3Ah	0x3A60h	00h	-	-	-	-	-	-	-	V3G2[9:8]	Gamma	
GmaG_2	R/W	0x3Bh	0x3B60h	00h	V3G2[7:0]									Gamma
GmaG_2	R/W	0x3Dh	0x3D60h	00h	-	-	-	-	-	-	-	V4G2[9:8]	Gamma	
GmaG_2	R/W	0x3Fh	0x3F60h	00h	V4G2[7:0]									Gamma
GmaG_2	R/W	0x40h	0x4060h	00h	-	-	-	-	-	-	-	V5G2[9:8]	Gamma	
GmaG_2	R/W	0x41h	0x4160h	00h	V5G2[7:0]									Gamma
GmaG_2	R/W	0x42h	0x4260h	00h	-	-	-	-	-	-	-	V6G2[9:8]	Gamma	
GmaG_2	R/W	0x43h	0x4360h	00h	V6G2[7:0]									Gamma
GmaG_2	R/W	0x44h	0x4460h	00h	-	-	-	-	-	-	-	V7G2[9:8]	Gamma	
GmaG_2	R/W	0x45h	0x4560h	00h	V7G2[7:0]									Gamma
GmaG_2	R/W	0x46h	0x4660h	00h	-	-	-	-	-	-	-	V8G2[9:8]	Gamma	
GmaG_2	R/W	0x47h	0x4760h	00h	V8G2[7:0]									Gamma
GmaG_2	R/W	0x48h	0x4860h	00h	-	-	-	-	-	-	-	V9G2[9:8]	Gamma	
GmaG_2	R/W	0x49h	0x4960h	00h	V9G2[7:0]									Gamma
GmaG_2	R/W	0x4Ah	0x4A60h	00h	-	-	-	-	-	-	-	V10G2[9:8]	Gamma	
GmaG_2	R/W	0x4Bh	0x4B60h	00h	V10G2[7:0]									Gamma
GmaG_2	R/W	0x4Ch	0x4C60h	00h	-	-	-	-	-	-	-	V11G2[9:8]	Gamma	

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Manufacture Command Set (CMD2 Page2 Gamma2)														
Instruction	R/W	Address		Parameter									Function	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaG_2	R/W	0x4Dh	0x4D60h	00h	V11G2[7:0]									Gamma
GmaG_2	R/W	0x4Eh	0x4E60h	00h	-	-	-	-	-	-	V12G2[9:8]		Gamma	
GmaG_2	R/W	0x4Fh	0x4F60h	00h	V12G2[7:0]									Gamma
GmaG_2	R/W	0x50h	0x5060h	00h	-	-	-	-	-	-	V13G2[9:8]		Gamma	
GmaG_2	R/W	0x51h	0x5160h	00h	V13G2[7:0]									Gamma
GmaG_2	R/W	0x52h	0x5260h	00h	-	-	-	-	-	-	V14G2[9:8]		Gamma	
GmaG_2	R/W	0x53h	0x5360h	00h	V14G2[7:0]									Gamma
GmaG_2	R/W	0x54h	0x5460h	00h	-	-	-	-	-	-	V15G2[9:8]		Gamma	
GmaG_2	R/W	0x55h	0x5560h	00h	V15G2[7:0]									Gamma
GmaG_2	R/W	0x56h	0x5660h	00h	-	-	-	-	-	-	V16G2[9:8]		Gamma	
GmaG_2	R/W	0x58h	0x5860h	00h	V16G2[7:0]									Gamma
GmaG_2	R/W	0x59h	0x5960h	00h	-	-	-	-	-	-	V17G2[9:8]		Gamma	
GmaG_2	R/W	0x5Ah	0x5A60h	00h	V17G2[7:0]									Gamma
GmaG_2	R/W	0x5Bh	0x5B60h	00h	-	-	-	-	-	-	V18G2[9:8]		Gamma	
GmaG_2	R/W	0x5Ch	0x5C60h	00h	V18G2[7:0]									Gamma
GmaG_2	R/W	0x5Dh	0x5D60h	00h	-	-	-	-	-	-	V19G2[9:8]		Gamma	
GmaG_2	R/W	0x5Eh	0x5E60h	00h	V19G2[7:0]									Gamma
GmaG_2	R/W	0x5Fh	0x5F60h	00h	-	-	-	-	-	-	V20G2[9:8]		Gamma	
GmaG_2	R/W	0x60h	0x6060h	00h	V20G2[7:0]									Gamma
GmaG_2	R/W	0x61h	0x6160h	00h	-	-	-	-	-	-	V21G2[9:8]		Gamma	
GmaG_2	R/W	0x62h	0x6260h	00h	V21G2[7:0]									Gamma
GmaG_2	R/W	0x63h	0x6360h	00h	-	-	-	-	-	-	V22G2[9:8]		Gamma	
GmaG_2	R/W	0x64h	0x6460h	00h	V22G2[7:0]									Gamma
GmaG_2	R/W	0x65h	0x6560h	00h	-	-	-	-	-	-	V23G2[9:8]		Gamma	
GmaG_2	R/W	0x66h	0x6660h	00h	V23G2[7:0]									Gamma
GmaG_2	R/W	0x67h	0x6760h	00h	-	-	-	-	-	-	V24G2[9:8]		Gamma	
GmaG_2	R/W	0x68h	0x6860h	00h	V24G2[7:0]									Gamma
GmaB_2	R/W	0x69h	0x6960h	00h	-	-	-	-	-	-	V0B2[9:8]		Gamma	
GmaB_2	R/W	0x6Ah	0x6A60h	00h	V0B2[7:0]									Gamma
GmaB_2	R/W	0x6Bh	0x6B60h	00h	-	-	-	-	-	-	V1B2[9:8]		Gamma	
GmaB_2	R/W	0x6Ch	0x6C60h	00h	V1B2[7:0]									Gamma
GmaB_2	R/W	0x6Dh	0x6D60h	00h	-	-	-	-	-	-	V2B2[9:8]		Gamma	
GmaB_2	R/W	0x6Eh	0x6E60h	00h	V2B2[7:0]									Gamma
GmaB_2	R/W	0x6Fh	0x6F60h	00h	-	-	-	-	-	-	V3B2[9:8]		Gamma	
GmaB_2	R/W	0x70h	0x7060h	00h	V3B2[7:0]									Gamma
GmaB_2	R/W	0x71h	0x7160h	00h	-	-	-	-	-	-	V4B2[9:8]		Gamma	

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Manufacture Command Set (CMD2 Page2 Gamma2)														
Instruction	R/W	Address		Parameter									Function	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaB_2	R/W	0x72h	0x7260h	00h	V4B2[7:0]									Gamma
GmaB_2	R/W	0x73h	0x7360h	00h	-	-	-	-	-	-	-	V5B2[9:8]	Gamma	
GmaB_2	R/W	0x74h	0x7460h	00h	V5B2[7:0]									Gamma
GmaB_2	R/W	0x75h	0x7560h	00h	-	-	-	-	-	-	-	V6B2[9:8]	Gamma	
GmaB_2	R/W	0x76h	0x7660h	00h	V6B2[7:0]									Gamma
GmaB_2	R/W	0x77h	0x7760h	00h	-	-	-	-	-	-	-	V7B2[9:8]	Gamma	
GmaB_2	R/W	0x78h	0x7860h	00h	V7B2[7:0]									Gamma
GmaB_2	R/W	0x79h	0x7960h	00h	-	-	-	-	-	-	-	V8B2[9:8]	Gamma	
GmaB_2	R/W	0x7Ah	0x7A60h	00h	V8B2[7:0]									Gamma
GmaB_2	R/W	0x7Bh	0x7B60h	00h	-	-	-	-	-	-	-	V9B2[9:8]	Gamma	
GmaB_2	R/W	0x7Ch	0x7C60h	00h	V9B2[7:0]									Gamma
GmaB_2	R/W	0x7Dh	0x7D60h	00h	-	-	-	-	-	-	-	V10B2[9:8]	Gamma	
GmaB_2	R/W	0x7Eh	0x7E60h	00h	V10B2[7:0]									Gamma
GmaB_2	R/W	0x7Fh	0x7F60h	00h	-	-	-	-	-	-	-	V11B2[9:8]	Gamma	
GmaB_2	R/W	0x80h	0x8060h	00h	V11B2[7:0]									Gamma
GmaB_2	R/W	0x81h	0x8160h	00h	-	-	-	-	-	-	-	V12B2[9:8]	Gamma	
GmaB_2	R/W	0x82h	0x8260h	00h	V12B2[7:0]									Gamma
GmaB_2	R/W	0x83h	0x8360h	00h	-	-	-	-	-	-	-	V13B2[9:8]	Gamma	
GmaB_2	R/W	0x84h	0x8460h	00h	V13B2[7:0]									Gamma
GmaB_2	R/W	0x85h	0x8560h	00h	-	-	-	-	-	-	-	V14B2[9:8]	Gamma	
GmaB_2	R/W	0x86h	0x8660h	00h	V14B2[7:0]									Gamma
GmaB_2	R/W	0x87h	0x8760h	00h	-	-	-	-	-	-	-	V15B2[9:8]	Gamma	
GmaB_2	R/W	0x88h	0x8860h	00h	V15B2[7:0]									Gamma
GmaB_2	R/W	0x89h	0x8960h	00h	-	-	-	-	-	-	-	V16B2[9:8]	Gamma	
GmaB_2	R/W	0x8Ah	0x8A60h	00h	V16B2[7:0]									Gamma
GmaB_2	R/W	0x8Bh	0x8B60h	00h	-	-	-	-	-	-	-	V17B2[9:8]	Gamma	
GmaB_2	R/W	0x8Ch	0x8C60h	00h	V17B2[7:0]									Gamma
GmaB_2	R/W	0x8Dh	0x8D60h	00h	-	-	-	-	-	-	-	V18B2[9:8]	Gamma	
GmaB_2	R/W	0x8Eh	0x8E60h	00h	V18B2[7:0]									Gamma
GmaB_2	R/W	0x8Fh	0x8F60h	00h	-	-	-	-	-	-	-	V19B2[9:8]	Gamma	
GmaB_2	R/W	0x90h	0x9060h	00h	V19B2[7:0]									Gamma
GmaB_2	R/W	0x91h	0x9160h	00h	-	-	-	-	-	-	-	V20B2[9:8]	Gamma	
GmaB_2	R/W	0x92h	0x9260h	00h	V20B2[7:0]									Gamma
GmaB_2	R/W	0x93h	0x9360h	00h	-	-	-	-	-	-	-	V21B2[9:8]	Gamma	
GmaB_2	R/W	0x94h	0x9460h	00h	V21B2[7:0]									Gamma
GmaB_2	R/W	0x95h	0x9560h	00h	-	-	-	-	-	-	-	V22B2[9:8]	Gamma	
GmaB_2	R/W	0x96h	0x9660h	00h	V22B2[7:0]									Gamma

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Manufacture Command Set (CMD2 Page2 Gamma2)														
Instruction	R/W	Address		Parameter									Function	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0		
GmaB_2	R/W	0x97h	0x9760h	00h	-	-	-	-	-	-	-	V23B2[9:8]	Gamma	
GmaB_2	R/W	0x98h	0x9860h	00h	V23B2[7:0]									Gamma
GmaB_2	R/W	0x99h	0x9960h	00h	-	-	-	-	-	-	-	V24B2[9:8]	Gamma	
GmaB_2	R/W	0x9Ah	0x9A60h	00h	V24B2[7:0]									Gamma
Gma_10p	R/W	0x9B	0x9B60	00h	-	-	-	GMA_10P2	-	-	-	-	Gamma	

(0060h~3360h) Gamma 2.2 Correction Set 2 for Red

Instruction	R/W	GammaR_2											
		Address		Parameter									
		MIP1	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	
GammaR_2	R/W	0x00h	0x0060h	00h	-	-	-	-	-	-	V0R2[9:8]	0x00h	
		0x01h	0x0160h	00h	V0R2[7:0]								
		0x02h	0x0260h	00h	-	-	-	-	-	-	V1R2[9:8]	0x00h	
		0x03h	0x0360h	00h	V1R2[7:0]								
		0x04h	0x0460h	00h	-	-	-	-	-	-	V2R2[9:8]	0x00h	
		0x05h	0x0560h	00h	V2R2[7:0]								
		0x06h	0x0660h	00h	-	-	-	-	-	-	V3R2[9:8]	0x00h	
		0x07h	0x0760h	00h	V3R2[7:0]								
		0x08h	0x0860h	00h	-	-	-	-	-	-	V4R2[9:8]	0x00h	
		0x09h	0x0960h	00h	V4R2[7:0]								
		0x0Ah	0x0A60h	00h	-	-	-	-	-	-	V5R2[9:8]	0x00h	
		0x0Bh	0x0B60h	00h	V5R2[7:0]								
		0x0Ch	0x0C60h	00h	-	-	-	-	-	-	V6R2[9:8]	0x00h	
		0x0Dh	0x0D60h	00h	V6R2[7:0]								
		0x0Eh	0x0E60h	00h	-	-	-	-	-	-	V7R2[9:8]	0x00h	
		0x0Fh	0x0F60h	00h	V7R2[7:0]								
		0x10h	0x1060h	00h	-	-	-	-	-	-	V8R2[9:8]	0x00h	
		0x11h	0x1160h	00h	V8R2[7:0]								
		0x12h	0x1260h	00h	-	-	-	-	-	-	V9R2[9:8]	0x00h	
		0x13h	0x1360h	00h	V9R2[7:0]								
		0x14h	0x1460h	00h	-	-	-	-	-	-	V10R2[9:8]	0x00h	
		0x15h	0x1560h	00h	V10R2[7:0]								
		0x16h	0x1660h	00h	-	-	-	-	-	-	V11R2[9:8]	0x00h	
		0x17h	0x1760h	00h	V11R2[7:0]								
		0x18h	0x1860h	00h	-	-	-	-	-	-	V12R2[9:8]	0x00h	

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GammaR_2	R/W	0x19h	0x1960h	00h	V12R2[7:0]							0xFCh
		0x1Ah	0x1A60h	00h	-	-	-	-	-	-	V13R2[9:8]	0x01h
		0x1Bh	0x1B60h	00h	V13R2[7:0]							0x3Ch
		0x1Ch	0x1C60h	00h	-	-	-	-	-	-	V14R2[9:8]	0x01h
		0x1Dh	0x1D60h	00h	V14R2[7:0]							0x7Ch
		0x1Eh	0x1E60h	00h	-	-	-	-	-	-	V15R2[9:8]	0x01h
		0x1Fh	0x1F60h	00h	V15R2[7:0]							0xBCh
		0x20h	0x2060h	00h	-	-	-	-	-	-	V16R2[9:8]	0x01h
		0x21h	0x2160h	00h	V16R2[7:0]							0xFCh
		0x22h	0x2260h	00h	-	-	-	-	-	-	V17R2[9:8]	0x02h
		0x23h	0x2360h	00h	V17R2[7:0]							0x3Ch
		0x24h	0x2460h	00h	-	-	-	-	-	-	V18R2[9:8]	0x02h
		0x25h	0x2560h	00h	V18R2[7:0]							0x7Ch
		0x26h	0x2660h	00h	-	-	-	-	-	-	V19R2[9:8]	0x02h
		0x27h	0x2760h	00h	V19R2[7:0]							0xBCh
		0x28h	0x2860h	00h	-	-	-	-	-	-	V20R2[9:8]	0x02h
		0x29h	0x2960h	00h	V20R2[7:0]							0xFCh
		0x2Ah	0x2A60h	00h	-	-	-	-	-	-	V21R2[9:8]	0x03h
		0x2Bh	0x2B60h	00h	V21R2[7:0]							0x3Ch
		0x2Dh	0x2D60h	00h	-	-	-	-	-	-	V22R2[9:8]	0x03h
		0x2Fh	0x2F60h	00h	V22R2[7:0]							0x7Ch
		0x30h	0x3060h	00h	-	-	-	-	-	-	V23R2[9:8]	0x03h
		0x31h	0x3160h	00h	V23R2[7:0]							0xBCh
		0x32h	0x3260h	00h	-	-	-	-	-	-	V24R2[9:8]	0x03h
		0x33h	0x3360h	00h	V24R2[7:0]							0xFCh
		This command is used to adjust the gamma 2.2 correction for the red under idle display mode. For GMA_10P2=0(default), Adjust R_0(darkest) via V0R2										

Description	Adjust R_7 via V1R2
	Adjust R_11 via V2R2
	Adjust R_15 via V3R2
	Adjust R_19 via V4R2
	Adjust R_23 via V5R2
	Adjust R_27 via V6R2
	Adjust R_31 via V7R2
	Adjust R_35 via V8R2
	Adjust R_39 via V9R2
	Adjust R_47 via V10R2
	Adjust R_55 via V11R2
	Adjust R_63 via V12R2
	Adjust R_79 via V13R2
	Adjust R_95 via V14R2
	Adjust R_111 via V15R2
	Adjust R_127 via V16R2
	Adjust R_143 via V17R2
	Adjust R_159 via V18R2
	Adjust R_175 via V19R2
	Adjust R_191 via V20R2
	Adjust R_207 via V21R2
	Adjust R_223 via V22R2
	Adjust R_239 via V23R2
	Adjust R_255(brightest) via V24R2
For GMA_10P2=1,	
Adjust R_0(darkest) via V0R2	
Adjust R_7 via V1R2	
Adjust R_11 via V2R2	
Adjust R_15 via V3R2	

	Adjust R_31 via V7R2 Adjust R_63 via V12R2 Adjust R_95 via V14R2 Adjust R_127 via V16R2 Adjust R_159 via V18R2 Adjust R_191 via V20R2 Adjust R_255(brightest) via V24R2
Restriction	

(3460h~6860h) Gamma 2.2 Correction Set 2 for Green

Instruction	R/W	GammaG_2											
		Address		Parameter									
		MIPi	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaG_2	R/W	0x34h	0x3460h	00h	-	-	-	-	-	-	V0G1[9:8]	0x00h	
		0x35h	0x3560h	00h	V0G2[7:0]								0x00h
		0x36h	0x3660h	00h	-	-	-	-	-	-	V1G2[9:8]	0x00h	
		0x37h	0x3760h	00h	V1G2[7:0]								0x1Ch
		0x38h	0x3860h	00h	-	-	-	-	-	-	V2G2[9:8]	0x00h	
		0x39h	0x3960h	00h	V2G2[7:0]								0x2Ch
		0x3Ah	0x3A60h	00h	-	-	-	-	-	-	V3G2[9:8]	0x00h	
		0x3Bh	0x3B60h	00h	V3G2[7:0]								0x3Ch
		0x3Dh	0x3D60h	00h	-	-	-	-	-	-	V4G2[9:8]	0x00h	
		0x3Fh	0x3F60h	00h	V4G2[7:0]								0x4Ch
		0x40h	0x4060h	00h	-	-	-	-	-	-	V5G2[9:8]	0x00h	
		0x41h	0x4160h	00h	V5G2[7:0]								0x5Ch
		0x42h	0x4260h	00h	-	-	-	-	-	-	V6G2[9:8]	0x00h	
		0x43h	0x4360h	00h	V6G2[7:0]								0x6Ch
		0x44h	0x4460h	00h	-	-	-	-	-	-	V7G2[9:8]	0x00h	
		0x45h	0x4560h	00h	V7G2[7:0]								0x7Ch
		0x46h	0x4660h	00h	-	-	-	-	-	-	V8G2[9:8]	0x00h	
		0x47h	0x4760h	00h	V8G2[7:0]								0x8Ch
		0x48h	0x4860h	00h	-	-	-	-	-	-	V9G2[9:8]	0x00h	
		0x49h	0x4960h	00h	V9G2[7:0]								0x9Ch
		0x4Ah	0x4A60h	00h	-	-	-	-	-	-	V10G2[9:8]	0x00h	
		0x4Bh	0x4B60h	00h	V10G2[7:0]								0xBCh
		0x4Ch	0x4C60h	00h	-	-	-	-	-	-	V11G2[9:8]	0x00h	
		0x4Dh	0x4D60h	00h	V11G2[7:0]								0xDCh
		0x4Eh	0x4E60h	00h	-	-	-	-	-	-	V12G2[9:8]	0x00h	

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GammaG_2	R/W	0x4Fh	0x4F60h	00h	V12G2[7:0]							0xFCh
		0x50h	0x5060h	00h	-	-	-	-	-	-	V13G2[9:8]	0x01h
		0x51h	0x5160h	00h	V13G2[7:0]							0x3Ch
		0x52h	0x5260h	00h	-	-	-	-	-	-	V14G2[9:8]	0x01h
		0x53h	0x5360h	00h	V14G2[7:0]							0x7Ch
		0x54h	0x5460h	00h	-	-	-	-	-	-	V15G2[9:8]	0x01h
		0x55h	0x5560h	00h	V15G2[7:0]							0xBCh
		0x56h	0x5660h	00h	-	-	-	-	-	-	V16G2[9:8]	0x01h
		0x58h	0x5860h	00h	V16G2[7:0]							0xFCh
		0x59h	0x5960h	00h	-	-	-	-	-	-	V17G2[9:8]	0x02h
		0x5Ah	0x5A60h	00h	V17G2[7:0]							0x3Ch
		0x5Bh	0x5B60h	00h	-	-	-	-	-	-	V18G2[9:8]	0x02h
		0x5Ch	0x5C60h	00h	V18G2[7:0]							0x7Ch
		0x5Dh	0x5D60h	00h	-	-	-	-	-	-	V19G2[9:8]	0x02h
		0x5Eh	0x5E60h	00h	V19G2[7:0]							0xBCh
		0x5Fh	0x5F60h	00h	-	-	-	-	-	-	V20G2[9:8]	0x02h
		0x60h	0x6060h	00h	V20G2[7:0]							0xFCh
		0x61h	0x6160h	00h	-	-	-	-	-	-	V21G2[9:8]	0x03h
		0x62h	0x6260h	00h	V21G2[7:0]							0x3Ch
		0x63h	0x6360h	00h	-	-	-	-	-	-	V22G2[9:8]	0x03h
		0x64h	0x6460h	00h	V22G2[7:0]							0x7Ch
		0x65h	0x6560h	00h	-	-	-	-	-	-	V23G2[9:8]	0x03h
		0x66h	0x6660h	00h	V23G2[7:0]							0xBCh
		0x67h	0x6760h	00h	-	-	-	-	-	-	V24G2[9:8]	0x03h
		0x68h	0x6860h	00h	V24G2[7:0]							0xFCh
		This command is used to adjust the gamma 2.2 correction for the green under idle display mode. For GMA_10P2=0(default), Adjust G_0(darkest) via V0G2										

Description	Adjust G_7 via V1G2
	Adjust G_11 via V2G2
	Adjust G_15 via V3G2
	Adjust G_19 via V4G2
	Adjust G_23 via V5G2
	Adjust G_27 via V6G2
	Adjust G_31 via V7G2
	Adjust G_35 via V8G2
	Adjust G_39 via V9G2
	Adjust G_47 via V10G2
	Adjust G_55 via V11G2
	Adjust G_63 via V12G2
	Adjust G_79 via V13G2
	Adjust G_95 via V14G2
	Adjust G_111 via V15G2
	Adjust G_127 via V16G2
	Adjust G_143 via V17G2
	Adjust G_159 via V18G2
	Adjust G_175 via V19G2
	Adjust G_191 via V20G2
	Adjust G_207 via V21G2
	Adjust G_223 via V22G2
	Adjust G_239 via V23G2
	Adjust G_255(brightest) via V24G2
For GMA_10P2=1,	
Adjust G_0(darkest) via V0G2	
Adjust G_7 via V1G2	
Adjust G_11 via V2G2	
Adjust G_15 via V3G2	

	Adjust G_31 via V7G2
	Adjust G_63 via V12G2
Description	Adjust G_95 via V14G2
	Adjust G_127 via V16G2
	Adjust G_159 via V18G2
	Adjust G_191 via V20G2
	Adjust G_255(brightest) via V24G2
Restriction	

(6960h~9A60h) Gamma 2.2 Correction Set 2 for Blue

Instruction	R/W	GammaB_2											
		Address		Parameter									
		MIP1	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	
GammaB_2	R/W	0x69h	0x6960h	00h	-	-	-	-	-	-	V0B2[9:8]	0x00h	
		0x6Ah	0x6A60h	00h	V0B2[7:0]								0x00h
		0x6Bh	0x6B60h	00h	-	-	-	-	-	-	V1B2[9:8]	0x00h	
		0x6Ch	0x6C60h	00h	V1B2[7:0]								0x1Ch
		0x6Dh	0x6D60h	00h	-	-	-	-	-	-	V2B2[9:8]	0x00h	
		0x6Eh	0x6E60h	00h	V2B2[7:0]								0x2Ch
		0x6Fh	0x6F60h	00h	-	-	-	-	-	-	V3B2[9:8]	0x00h	
		0x70h	0x7060h	00h	V3B2[7:0]								0x3Ch
		0x71h	0x7160h	00h	-	-	-	-	-	-	V4B2[9:8]	0x00h	
		0x72h	0x7260h	00h	V4B2[7:0]								0x4Ch
		0x73h	0x7360h	00h	-	-	-	-	-	-	V5B2[9:8]	0x00h	
		0x74h	0x7460h	00h	V5B2[7:0]								0x5Ch
		0x75h	0x7560h	00h	-	-	-	-	-	-	V6B2[9:8]	0x00h	
		0x76h	0x7660h	00h	V6B2[7:0]								0x6Ch
		0x77h	0x7760h	00h	-	-	-	-	-	-	V7B2[9:8]	0x00h	
		0x78h	0x7860h	00h	V7B2[7:0]								0x7Ch
		0x79h	0x7960h	00h	-	-	-	-	-	-	V8B2[9:8]	0x00h	
		0x7Ah	0x7A60h	00h	V8B2[7:0]								0x8Ch
		0x7Bh	0x7B60h	00h	-	-	-	-	-	-	V9B2[9:8]	0x00h	
		0x7Ch	0x7C60h	00h	V9B2[7:0]								0x9Ch
		0x7Dh	0x7D60h	00h	-	-	-	-	-	-	V10B2[9:8]	0x00h	
		0x7Eh	0x7E60h	00h	V10B2[7:0]								0xBCh
		0x7Fh	0x7F60h	00h	-	-	-	-	-	-	V11B2[9:8]	0x00h	
		0x80h	0x8060h	00h	V11B2[7:0]								0xDCh
		0x81h	0x8160h	00h	-	-	-	-	-	-	V12B2[9:8]	0x00h	

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GammaB_2	R/W	0x82h	0x8260h	00h	V12B2[7:0]							0xFCh
		0x83h	0x8360h	00h	-	-	-	-	-	-	V13B2[9:8]	0x01h
		0x84h	0x8460h	00h	V13B2[7:0]							0x3Ch
		0x85h	0x8560h	00h	-	-	-	-	-	-	V14B2[9:8]	0x01h
		0x86h	0x8660h	00h	V14B2[7:0]							0x7Ch
		0x87h	0x8760h	00h	-	-	-	-	-	-	V15B2[9:8]	0x01h
		0x88h	0x8860h	00h	V15B2[7:0]							0xBCh
		0x89h	0x8960h	00h	-	-	-	-	-	-	V16B2[9:8]	0x01h
		0x8Ah	0x8A60h	00h	V16B2[7:0]							0xFCh
		0x8Bh	0x8B60h	00h	-	-	-	-	-	-	V17B2[9:8]	0x02h
		0x8Ch	0x8C60h	00h	V17B2[7:0]							0x3Ch
		0x8Dh	0x8D60h	00h	-	-	-	-	-	-	V18B2[9:8]	0x02h
		0x8Eh	0x8E60h	00h	V18B2[7:0]							0x7Ch
		0x8Fh	0x8F60h	00h	-	-	-	-	-	-	V19B2[9:8]	0x02h
		0x90h	0x9060h	00h	V19B2[7:0]							0xBCh
		0x91h	0x9160h	00h	-	-	-	-	-	-	V20B2[9:8]	0x02h
		0x92h	0x9260h	00h	V20B2[7:0]							0xFCh
		0x93h	0x9360h	00h	-	-	-	-	-	-	V21B2[9:8]	0x03h
		0x94h	0x9460h	00h	V21B2[7:0]							0x3Ch
		0x95h	0x9560h	00h	-	-	-	-	-	-	V22B2[9:8]	0x03h
		0x96h	0x9660h	00h	V22B2[7:0]							0x7Ch
		0x97h	0x9760h	00h	-	-	-	-	-	-	V23B2[9:8]	0x03h
		0x98h	0x9860h	00h	V23B2[7:0]							0xBCh
		0x99h	0x9960h	00h	-	-	-	-	-	-	V24B2[9:8]	0x03h
		0x9Ah	0x9A60h	00h	V24B2[7:0]							0xFCh
		This command is used to adjust the gamma 2.2 correction for the blue under idle display mode. For GMA_10P2=0(default), Adjust B_0(darkest) via V0B2										

Description	Adjust B_7 via V1B2
	Adjust B_11 via V2B2
	Adjust B_15 via V3B2
	Adjust B_19 via V4B2
	Adjust B_23 via V5B2
	Adjust B_27 via V6B2
	Adjust B_31 via V7B2
	Adjust B_35 via V8B2
	Adjust B_39 via V9B2
	Adjust B_47 via V10B2
	Adjust B_55 via V11B2
	Adjust B_63 via V12B2
	Adjust B_79 via V13B2
	Adjust B_95 via V14B2
	Adjust B_111 via V15B2
	Adjust B_127 via V16B2
	Adjust B_143 via V17B2
	Adjust B_159 via V18B2
	Adjust B_175 via V19B2
	Adjust B_191 via V20B2
	Adjust B_207 via V21B2
	Adjust B_223 via V22B2
	Adjust B_239 via V23B2
	Adjust B_255(brightest) via V24B2
Description	For GMA_10P2=1,
	Adjust B_0(darkest) via V0B2
	Adjust B_7 via V1B2
	Adjust B_11 via V2B2
	Adjust B_15 via V3B2

	Adjust B_31 via V7B2 Adjust B_63 via V12B2 Adjust B_95 via V14B2 Adjust B_127 via V16B2 Adjust B_159 via V18B2 Adjust B_191 via V20B2 Adjust B_255(brightest) via V24B2
Restriction	

(FE60h) CMD Mode Switch

		CMD Mode Switch																														
Instruction	R/W	Address		Parameter																												
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
CMD Mode Switch	R/W	0xFEh	0x FE60h	00h	-	-	-	-	CMD_Page_Selection				0x00h																			
Description	This command is used to switch the Manufacture Command Pages and User Commands sets. <table border="1"> <thead> <tr> <th>CMD_Page[3:0]</th> <th>Hex Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h (default)</td> <td>User Command Set (UCS = CMD1)</td> </tr> <tr> <td>0001</td> <td>01h</td> <td>Manufacture Command Set Page0 (CMD2 P0)</td> </tr> <tr> <td>0010</td> <td>02h</td> <td>Manufacture Command Set Page1 (CMD2 P1)</td> </tr> <tr> <td>0011</td> <td>03h</td> <td>Manufacture Command Set Page2 (CMD2 P2)</td> </tr> <tr> <td>0100</td> <td>04h</td> <td>Manufacture Command Set Page3 (CMD2 P3)</td> </tr> </tbody> </table>													CMD_Page[3:0]	Hex Value	Description	0000	00h (default)	User Command Set (UCS = CMD1)	0001	01h	Manufacture Command Set Page0 (CMD2 P0)	0010	02h	Manufacture Command Set Page1 (CMD2 P1)	0011	03h	Manufacture Command Set Page2 (CMD2 P2)	0100	04h	Manufacture Command Set Page3 (CMD2 P3)	
CMD_Page[3:0]	Hex Value	Description																														
0000	00h (default)	User Command Set (UCS = CMD1)																														
0001	01h	Manufacture Command Set Page0 (CMD2 P0)																														
0010	02h	Manufacture Command Set Page1 (CMD2 P1)																														
0011	03h	Manufacture Command Set Page2 (CMD2 P2)																														
0100	04h	Manufacture Command Set Page3 (CMD2 P3)																														
Restriction																																
Register Availability	<table border="1"> <thead> <tr> <th colspan="2">Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td colspan="2">Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Partial Mode On, Idle Mode Off, Sleep Out		Yes	Partial Mode On, Idle Mode On, Sleep Out		Yes	Sleep In		Yes	
Status		Availability																														
Normal Mode On, Idle Mode Off, Sleep Out		Yes																														
Normal Mode On, Idle Mode On, Sleep Out		Yes																														
Partial Mode On, Idle Mode Off, Sleep Out		Yes																														
Partial Mode On, Idle Mode On, Sleep Out		Yes																														
Sleep In		Yes																														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <td colspan="3">0xFEh / 0x FE60h</td></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td colspan="3">0x00h</td></tr> <tr> <td>S/W Reset</td><td colspan="3">0x00h</td></tr> <tr> <td>H/W Reset</td><td colspan="3">0x00h</td></tr> </tbody> </table>													Status	Default Value			0xFEh / 0x FE60h			Power On Sequence	0x00h			S/W Reset	0x00h			H/W Reset	0x00h		
Status	Default Value																															
	0xFEh / 0x FE60h																															
Power On Sequence	0x00h																															
S/W Reset	0x00h																															
H/W Reset	0x00h																															

(FF60h) RD CMD Status

		RD CMD Status																										
Instruction	R/W	Address		Parameter																								
		MIFI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
RD CMD Status	R	0xFFh	0xFF60h	00h	-	-	-	-	Current_CMD_Page			0x00h																
Description	This command is used to confirm current CMD Page Settings..																											
	CMD_Page[3:0]	Hex Value			Description																							
	0000	00h (default)			User Command Set (UCS = CMD1)																							
	0001	01h			Manufacture Command Set Page0 (CMD2 P0)																							
	0010	02h			Manufacture Command Set Page1 (CMD2 P1)																							
	0011	03h			Manufacture Command Set Page2 (CMD2 P2)																							
	0100	04h			Manufacture Command Set Page3 (CMD2 P3)																							
Restriction																												
Register Availability	Status						Availability																					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes																					
	Normal Mode On, Idle Mode On, Sleep Out						Yes																					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes																					
	Partial Mode On, Idle Mode On, Sleep Out						Yes																					
	Sleep In						Yes																					
Default	Status				Default Value																							
					0xFFh / 0xFF60h																							
	Power On Sequence				0x01h																							
	S/W Reset				0x01h																							
	H/W Reset				0x01h																							

1.6 MCS: CMD2 Page3 = GOA Timing Control

Manufacture Command Set (CMD2 Page3 GOA Timing)

Instruction	R/W	Address		Parameter										Function						
		MPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0								
GOA_VSR1	R/W	0x00h	0x0070h	00h	VSR1_en	VSR1_pt_en	VSR1_vrst_en	VSR1_wid_Dsel	VSR1_wr_pol	VSR1_bk_pol	VSR1_pcol	-	GOA_VSR1							
GOA_VSR1	R/W	0x01h	0x0170h	00h	-	VSR1_wid_L[10:8]			-	VSR1_prid[10:8]			GOA_VSR1							
GOA_VSR1	R/W	0x02h	0x0270h	00h	VSR1_prid[7:0]															
GOA_VSR1	R/W	0x03h	0x0370h	00h	VSR1_wid_L[7:0]															
GOA_VSR1	R/W	0x04h	0x0470h	00h	VSR1_wid_D[9:8]			VSR1_ofst2[9:8]	VSR1_ofst1[10:8]	VSR1_ofst1[10:8]	VSR1_ofst1[10:8]	-	GOA_VSR1							
GOA_VSR1	R/W	0x05h	0x0570h	00h	VSR1_ofst1[7:0]															
GOA_VSR1	R/W	0x06h	0x0670h	00h	VSR1_ofst2[7:0]															
GOA_VSR1	R/W	0x07h	0x0770h	00h	VSR1_wid_D[7:0]															
GOA_VSR1	R/W	0x08h	0x0870h	00h	-	VSR1_kp_tgl[6:0]														
GOA_VSR2	R/W	0x09h	0x0970h	00h	VSR2_en	VSR2_pt_en	VSR2_vrst_en	VSR2_wid_Dsel	VSR2_wr_pol	VSR2_bk_pol	VSR2_pcol	-	GOA_VSR2							
GOA_VSR2	R/W	0x0Ah	0x0A70h	00h	-	VSR2_wid_L[10:8]			-	VSR2_prid[10:8]			GOA_VSR2							
GOA_VSR2	R/W	0x0Bh	0x0B70h	00h	VSR2_prid[7:0]															
GOA_VSR2	R/W	0x0Ch	0x0C70h	00h	VSR2_wid_L[7:0]															
GOA_VSR2	R/W	0x0Dh	0x0D70h	00h	VSR2_ofst1[adsel]	VSR2_wid_D[9:8]			VSR2_ofst2[9:8]	VSR2_ofst1[10:8]			GOA_VSR2							
GOA_VSR2	R/W	0x0Eh	0x0E70h	00h	VSR2_ofst1[7:0]															
GOA_VSR2	R/W	0x0Fh	0x0F70h	00h	VSR2_ofst2[7:0]															
GOA_VSR2	R/W	0x10h	0x0170h	00h	VSR2_wid_D[7:0]															
GOA_VSR2	R/W	0x11h	0x1170h	00h	-	VSR2_kp_tgl[6:0]														
GOA_VSR3	R/W	0x12h	0x1270h	00h	VSR3_en	VSR3_pt_en	VSR3_vrst_en	VSR3_wid_Dsel	VSR3_wr_pol	VSR3_bk_pol	VSR3_pcol	-	GOA_VSR3							
GOA_VSR3	R/W	0x13h	0x1370h	00h	-	VSR3_wid_L[10:8]			-	VSR3_prid[10:8]			GOA_VSR3							
GOA_VSR3	R/W	0x14h	0x1470h	00h	VSR3_prid[7:0]															
GOA_VSR3	R/W	0x15h	0x1570h	00h	VSR3_wid_L[7:0]															
GOA_VSR3	R/W	0x16h	0x1670h	00h	VSR3_ofst1[adsel]	VSR3_wid_D[9:8]			VSR3_ofst2[9:8]	VSR3_ofst1[10:8]			GOA_VSR3							
GOA_VSR3	R/W	0x17h	0x1770h	00h	VSR3_ofst1[7:0]															
GOA_VSR3	R/W	0x18h	0x1870h	00h	VSR3_ofst2[7:0]															
GOA_VSR3	R/W	0x19h	0x1970h	00h	VSR3_wid_D[7:0]															
GOA_VSR3	R/W	0x1Ah	0x1A70h	00h	-	VSR3_kp_tgl[6:0]														
GOA_VSR4	R/W	0x1Bh	0x1B70h	00h	VSR4_en	VSR4_pt_en	VSR4_vrst_en	VSR4_wid_Dsel	VSR4_wr_pol	VSR4_bk_pol	VSR4_pcol	-	GOA_VSR4							
GOA_VSR4	R/W	0x1Ch	0x1C70h	00h	-	VSR4_wid_L[10:8]			-	VSR4_prid[10:8]			GOA_VSR4							
GOA_VSR4	R/W	0x1Dh	0x1D70h	00h	VSR4_prid[7:0]															
GOA_VSR4	R/W	0x1Eh	0x1E70h	00h	VSR4_wid_L[7:0]															
GOA_VSR4	R/W	0x1Fh	0x1F70h	00h	VSR4_ofst1[adsel]	VSR4_wid_D[9:8]			VSR4_ofst2[9:8]	VSR4_ofst1[10:8]			GOA_VSR4							

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Manufacture Command Set (CMD2 Page3 GOA Timing)																				
Instruction	R/W	Address			Parameter									Function						
		MIP1	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0								
GOA_VSR4	R/W	0x20h	0x2070h	00h	VSR4_ofst1[7:0]									GOA_VSR4						
GOA_VSR4	R/W	0x21h	0x2170h	00h	VSR4_ofst2[7:0]									GOA_VSR4						
GOA_VSR4	R/W	0x22h	0x2270h	00h	VSR4_wid_D[7:0]									GOA_VSR4						
GOA_VSR4	R/W	0x23h	0x2370h	00h	-	VSR4_kp_tgl[6:0]									GOA_VSR4					
GOA_VSR5	R/W	0x24h	0x2470h	00h	VSR5_en	VSR5_pt_en	VSR5_rst_en	VSR5_wid_D_sel	VSR5_wr_pol	VSR5_bk_pol	VSR5_p ol	-	-	GOA_VSR5						
GOA_VSR5	R/W	0x25h	0x2570h	00h	-	VSR5_wid_L[10:8]			-	VSR5_prd[10:8]			GOA_VSR5							
GOA_VSR5	R/W	0x26h	0x2670h	00h	VSR5_prd[7:0]									GOA_VSR5						
GOA_VSR5	R/W	0x27h	0x2770h	00h	VSR5_wid_L[7:0]									GOA_VSR5						
GOA_VSR5	R/W	0x28h	0x2870h	00h	VSR5_of st1_ad_s el	VSR5_wid_D[9:8]			VSR5_ofst2[9:8]	VSR5_ofst1[10:8]			GOA_VSR5							
GOA_VSR5	R/W	0x29h	0x2970h	00h	VSR5_ofst1[7:0]									GOA_VSR5						
GOA_VSR5	R/W	0x2Ah	0x2A70h	00h	VSR5_ofst2[7:0]									GOA_VSR5						
GOA_VSR5	R/W	0x2Bh	0x2B70h	00h	VSR5_wid_D[7:0]									GOA_VSR5						
GOA_VSR5	R/W	0x2Dh	0x2D70h	00h	-	VSR5_kp_tgl[6:0]									GOA_VSR5					
GOA_VSR6	R/W	0x2Fh	0x2F70h	00h	VSR6_en	VSR6_pt_en	VSR6_rst_en	VSR6_wid_D_sel	VSR6_wr_pol	VSR6_bk_pol	VSR6_p ol	-	-	GOA_VSR6						
GOA_VSR6	R/W	0x30h	0x3070h	00h	-	VSR6_wid_L[10:8]			-	VSR6_prd[10:8]			GOA_VSR6							
GOA_VSR6	R/W	0x31h	0x3170h	00h	VSR6_prd[7:0]									GOA_VSR6						
GOA_VSR6	R/W	0x32h	0x3270h	00h	VSR6_wid_L[7:0]									GOA_VSR6						
GOA_VSR6	R/W	0x33h	0x3370h	00h	VSR6_of st1_ad_s el	VSR6_wid_D[9:8]			VSR6_ofst2[9:8]	VSR6_ofst1[10:8]			GOA_VSR6							
GOA_VSR6	R/W	0x34h	0x3470h	00h	VSR6_ofst1[7:0]									GOA_VSR6						
GOA_VSR6	R/W	0x35h	0x3570h	00h	VSR6_ofst2[7:0]									GOA_VSR6						
GOA_VSR6	R/W	0x36h	0x3670h	00h	VSR6_wid_D[7:0]									GOA_VSR6						
GOA_VSR6	R/W	0x37h	0x3770h	00h	-	VSR6_kp_tgl[6:0]									GOA_VSR6					
GOA_VSR7	R/W	0x38h	0x3870h	00h	VSR7_en	VSR7_pt_en	VSR7_rst_en	VSR7_wid_D_sel	VSR7_wr_pol	VSR7_bk_pol	VSR7_p ol	-	-	GOA_VSR7						
GOA_VSR7	R/W	0x39h	0x3970h	00h	-	VSR7_wid_L[10:8]			-	VSR7_prd[10:8]			GOA_VSR7							
GOA_VSR7	R/W	0x3Ah	0x3A70h	00h	VSR7_prd[7:0]									GOA_VSR7						
GOA_VSR7	R/W	0x3Bh	0x3B70h	00h	VSR7_wid_L[7:0]									GOA_VSR7						
GOA_VSR7	R/W	0x3Dh	0x3D70h	00h	VSR7_of st1_ad_s el	VSR7_wid_D[9:8]			VSR7_ofst2[9:8]	VSR7_ofst1[10:8]			GOA_VSR7							
GOA_VSR7	R/W	0x3Fh	0x3F70h	00h	VSR7_ofst1[7:0]									GOA_VSR7						
GOA_VSR7	R/W	0x40h	0x4070h	00h	VSR7_ofst2[7:0]									GOA_VSR7						
GOA_VSR7	R/W	0x41h	0x4170h	00h	VSR7_wid_D[7:0]									GOA_VSR7						
GOA_VSR7	R/W	0x42h	0x4270h	00h	-	VSR7_kp_tgl[6:0]									GOA_VSR7					
GOA_VSR8	R/W	0x43h	0x4370h	00h	VSR8_en	VSR8_pt_en	VSR8_rst_en	VSR8_wid_D_sel	VSR8_wr_pol	VSR8_bk_pol	VSR8_p ol	-	-	GOA_VSR8						
GOA_VSR8	R/W	0x44h	0x4470h	00h	-	VSR8_wid_L[10:8]			-	VSR8_prd[10:8]			GOA_VSR8							
GOA_VSR8	R/W	0x45h	0x4570h	00h	VSR8_prd[7:0]									GOA_VSR8						
GOA_VSR8	R/W	0x46h	0x4670h	00h	VSR8_wid_L[7:0]									GOA_VSR8						

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Manufacture Command Set (CMD2 Page3 GOA Timing)																	
Instruction	R/W	Address			Parameter								Function				
		MPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0					
GOA_VSR8	R/W	0x47h	0x4770h	00h	VSR8_ofst1_ad_sel	VSR8_wid_D[9:8]	VSR8_ofst2[9:8]	VSR8_ofst1[10:8]					GOA_VSR8				
GOA_VSR8	R/W	0x48h	0x4870h	00h	VSR8_ofst1[7:0]								GOA_VSR8				
GOA_VSR8	R/W	0x49h	0x4970h	00h	VSR8_ofst2[7:0]								GOA_VSR8				
GOA_VSR8	R/W	0x4Ah	0x4A70h	00h	VSR8_wid_D[7:0]								GOA_VSR8				
GOA_VSR8	R/W	0x4Bh	0x4B70h	00h	-	VSR8_kp_tgl[6:0]							GOA_VSR8				
GOA_VST	R/W	0x4Ch	0x4C70h	00h	VST_en	-	-	VST_wid_D_sel	VST_pwr_pol	-	VST_polarity	-	GOA_VST				
GOA_VST	R/W	0x4Dh	0x4D70h	00h	-	VST_wid_L[10:8]			-	-	-	-	GOA_VST				
GOA_VST	R/W	0x4Eh	0x4E70h	00h	VST_wid_L[7:0]								GOA_VST				
GOA_VST	R/W	0x4Fh	0x4F70h	00h	VST_ofst1_ad_sel	VST_wid_D[9:8]	VST_ofst2[9:8]	VST_ofst1[10:8]					GOA_VST				
GOA_VST	R/W	0x50h	0x5070h	00h	VST_ofst1[7:0]								GOA_VST				
GOA_VST	R/W	0x51h	0x5170h	00h	VST_ofst2[7:0]								GOA_VST				
GOA_VST	R/W	0x52h	0x5270h	00h	VST_wid_D[7:0]								GOA_VST				
GOA_VEN	R/W	0x53h	0x5370h	00h	VEN_en	VEN_rp_t_en	VEN_vrst_en	VEN_wid_D_sel	VEN_pwr_pol	VEN_bkpol	VEN_polarity	-	GOA_VEN				
GOA_VEN	R/W	0x54h	0x5470h	00h	VEN_ofst1_ad_se	VEN_wid_D[9:8]	VEN_ofst2[9:8]	VEN_ofst1[10:8]					GOA_VEN				
GOA_VEN	R/W	0x55h	0x5570h	00h	VEN_ofst1[7:0]								GOA_VEN				
GOA_VEN	R/W	0x56h	0x5670h	00h	VEN_ofst2[7:0]								GOA_VEN				
GOA_VEN	R/W	0x58h	0x5870h	00h	VEN_wid_D[7:0]								GOA_VEN				
GOA_VEN	R/W	0x59h	0x5970h	00h	-	VEN_kp_tgl[6:0]							GOA_VEN				
GOAOUTSEL1	R/W	0x5Eh	0x5E70h	00h	VSR2_OUT_sel[3:0]				VSR1_OUT_sel[3:0]				GOA Output Selection				
GOAOUTSEL2	R/W	0x5Fh	0x5F70h	00h	VSR4_OUT_sel[3:0]				VSR3_OUT_sel[3:0]				GOA Output Selection				
GOAOUTSEL3	R/W	0x60h	0x6070h	00h	VSR6_OUT_sel[3:0]				VSR5_OUT_sel[3:0]				GOA Output Selection				
GOAOUTSEL4	R/W	0x61h	0x6170h	00h	VSR8_OUT_sel[3:0]				VSR7_OUT_sel[3:0]				GOA Output Selection				
GOAOUTSEL5	R/W	0x62h	0x6270h	00h	VEN_OUT_sel[3:0]				VST_OUT_sel[3:0]				GOA Output Selection				
GOA_VEN	R/W	0x65h	0x6570h	00h	VEN_perid_exp[7:0]								VEN period exp.				
GOA_VEN	R/W	0x66h	0x6670h	00h	VEN_wid_L_exp[7:0]								VEN wid_L exp.				
GOA_VEN	R/W	0x67h	0x6770h	00h	0	VEN_perid_exp[10:8]			0	VEN_wid_L_exp[10:8]			VEN period exp. & VEN wid_L exp				
CMD Mode Switch	R/W	0xFEh	0xFE70h	0	-	-	-	-	CMD_Page[3:0]				CMD Mode Switch				
RD CMD Status	R	0xFFh	0xFF70h	0	-	-	-	-	Current_CMD_Page[3:0]				RD CMD Status				

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(0070h~0870h) GOA_VSR1

Instruction	R/W	GOA_VSR1																	
		Address		Parameter															
MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
GOA_VSR1	R/W	0x00h	0x0070h	00h	VSR1_en	VSR1_rpt_en	VSR1_vrs_t_en	VSR1_wid_D_sel	VSR1_pwr_pol	VSR1_bk_pol	VSR1_pol	-	0x08h						
		0x01h	0x0170h	00h	-	VSR1_wid_L[10:8]			-	VSR1_prid[10:8]			0x00h						
		0x02h	0x0270h	00h	VSR1_prid[7:0]								0x00h						
		0x03h	0x0370h	00h	VSR1_wid_L[7:0]								0x00h						
		0x04h	0x0470h	00h	VSR1_wid_D[9:8]	VSR1_ofst2[9:8]		VSR1_ofst1_a_d_sel	VSR1_ofst1[10:8]			0x00h							
		0x05h	0x0570h	00h	VSR1_ofst1[7:0]								0x00h						
		0x06h	0x0670h	00h	VSR1_ofst2[7:0]								0x00h						
		0x07h	0x0770h	00h	VSR1_wid_D[7:0]								0x00h						
		0x08h	0x0870h	00h	-	VSR1_kp_tgl[6:0]					0x00h								
Description	This command is GOA Timing Control for VSR1.																		
	Bit		Description				Data												
	VSR1_en		VSR1 enable				0: VSR1 disable 1: VSR1 enable												
	VSR1_rpt_en		Enable the repeat function of VSR1				0: disable 1: enable												
	VSR1_vrst_en		Enable the Vsync reset function for VSR1				0: disable 1: enable												
	VSR1_wid_D_sel		The selection of count direction from Hsync for VSR1_wid_D				0: VSR1_wid_D seen as advance 1: VSR1_wid_D seen as delay												
	VSR1_pwr_pol		The Polarity of VSR1 during display off area				0: VSR1 negative polarity 1: VSR1 positive polarity												
	VSR1_bk_pol		The Polarity of VSR1 during blanking area				0: VSR1 negative polarity 1: VSR1 positive polarity												
	VSR1_pol		The Polarity of VSR1 during active area				0: VSR1 negative polarity 1: VSR1 positive polarity												

Bit	Description	Data
VSR1_prid[10:0]	Period that VSR1 repeats (unit: Hsync)	Note: do not exceed vttotal.
Bit	Description	Data
VSR1_wid_L[10:0]	Low pulse width of VSR1 inside a period. (unit: Hsync)	Note: do not exceed VSR1_period.
Bit	Description	Data
VSR1_ofst1_ad_sel	The selection of count direction from Hsync for VSR1_ofst1	0: VSR1_ofst1 seen as advance 1: VSR1_ofst1 seen as delay
VSR1_ofst1[10:0]	Time delay/advance from VSR1 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.
Bit	Description	Data
VSR1_ofst2[9:0]	Time delay from VSR1(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.
Bit	Description	Data
VSR1_wid_D[9:0]	Time delay from VSR1(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.
Bit	Description	Data
VSR1_kp_tgl[6:0]	Keep toggling line number of VSR1_kp_tgl from end of the last display line (unit Hsync)	Note: 1. Total toggle area (unit: Hsync) = back porch +/- VSR1_ofst1 + display line + VSR1_kp_tgl 2. do not exceed vttotal

Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	0070h 0x08h
		0170h 0x00h
		0270h 0x00h
		0370h 0x00h
		0470h 0x00h
		0570h 0x00h
		0670h 0x00h
	S/W Reset	0770h 0x00h
		0870h 0x00h
	H/W Reset	

(0970h~1170h) GOA_VSR2

Instruction	R/W	GOA_VSR2																		
		Address		Parameter																
MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
GOA_VSR2	R/W	0x09h	0x0970h	00h	VSR2_en	VSR2_rpt_en	VSR2_vrs_t_en	VSR2_wid_D_sel	VSR2_pwr_pol	VSR2_bk_pol	VSR2_pol	-	0x08h							
		0x0Ah	0x0A70h	00h	-	VSR2_wid_L[10:8]			-	VSR2_prid[10:8]			0x00h							
		0x0Bh	0x0B70h	00h	VSR2_prid[7:0]								0x00h							
		0x0Ch	0x0C70h	00h	VSR2_wid_L[7:0]								0x00h							
		0x0Dh	0x0D70h	00h	VSR2_o fst1_ad_ sel	VSR2_wid_D[9:8]		VSR2_ofst2[9:8]		VSR2_ofst1[10:8]			0x00h							
		0x0Eh	0x0E70h	00h	VSR2_ofst1[7:0]								0x00h							
		0x0Fh	0x0F70h	00h	VSR2_ofst2[7:0]								0x00h							
		0x10h	0x1070h	00h	VSR2_wid_D[7:0]								0x00h							
		0x11h	0x1170h	00h	-	VSR2_kp_tgl[6:0]								0x00h						
Description	This command is GOA Timing Control for VSR2.																			
	Bit		Description				Data													
	VSR2_en		VSR2 enable				0: VSR2 disable 1: VSR2 enable													
	VSR2_rpt_en		Enable the repeat function of VSR2				0: disable 1: enable													
	VSR2_vrst_en		Enable the Vsync reset function for VSR2				0: disable 1: enable													
	VSR2_wid_D_sel		The selection of count direction from Hsync for VSR2_wid_D				0: VSR2_wid_D seen as advance 1: VSR2_wid_D seen as delay													
	VSR2_pwr_pol		The Polarity of VSR2 during display off area				0: VSR2 negative polarity 1: VSR2 positive polarity													
	VSR2_bk_pol		The Polarity of VSR2 during blanking area				0: VSR2 negative polarity 1: VSR2 positive polarity													
	VSR2_pol		The Polarity of VSR2 during active area				0: VSR2 negative polarity 1: VSR2 positive polarity													

Bit	Description	Data
VSR2_prid[10:0]	Period that VSR2 repeats (unit: Hsync)	Note: do not exceed vttotal.
VSR2_wid_L[10:0]	Low pulse width of VSR2 inside a period. (unit: Hsync)	Note: do not exceed VSR2_period.
VSR2_ofst1_ad_sel	The selection of count direction from Hsync for VSR2_ofst1	0: VSR2_ofst1 seen as advance 1: VSR2_ofst1 seen as delay
VSR2_ofst1[10:0]	Time delay/advance from VSR2 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.
VSR2_ofst2[9:0]	Time delay from VSR2(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.
VSR2_wid_D[9:0]	Time delay from VSR2(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.
VSR2_kp_tgl[6:0]	Keep toggling line number of VSR2_kp_tgl from end of the last display line (unit Hsync)	Note: 3. Total toggle area (unit: Hsync) = back porch +/- VSR2_ofst1 + display line + VSR2_kp_tgl 4. do not exceed vttotal

Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	0970h 0x08h 0A70h 0x00h 0B70h 0x00h 0C70h 0x00h 0D70h 0x00h 0E70h 0x00h 0F70h 0x00h 1070h 0x00h 1170h 0x00h
	S/W Reset	
	H/W Reset	

(1270h~1A70h) GOA_VSR3

Instruction	R/W	GOA_VSR3																	
		Address		Parameter															
MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
GOA_VSR3	R/W	0x12h	0x1270h	00h	VSR3_en	VSR3_rpt_en	VSR3_vrs_t_en	VSR3_wid_D_sel	VSR3_pwr_pol	VSR3_bk_pol	VSR3_pol	-	0x08h						
		0x13h	0x1370h	00h	-	VSR3_wid_L[10:8]			-	VSR3_prid[10:8]			0x00h						
		0x14h	0x1470h	00h	VSR3_prid[7:0]								0x00h						
		0x15h	0x1570h	00h	VSR3_wid_L[7:0]								0x00h						
		0x16h	0x1670h	00h	VSR3_ofst1_ad_sel	VSR3_wid_D[9:8]		VSR3_ofst2[9:8]	VSR3_ofst1[10:8]			0x00h							
		0x17h	0x1770h	00h	VSR3_ofst1[7:0]								0x00h						
		0x18h	0x1870h	00h	VSR3_ofst2[7:0]								0x00h						
		0x19h	0x1970h	00h	VSR3_wid_D[7:0]								0x00h						
		0x1Ah	0x1A70h	00h	-	VSR3_kp_tgl[6:0]								0x00h					
Description	This command is GOA Timing Control for VSR3.																		
	Bit		Description				Data												
	VSR3_en		VSR3 enable				0: VSR3 disable 1: VSR3 enable												
	VSR3_rpt_en		Enable the repeat function of VSR3				0: disable 1: enable												
	VSR3_vrst_en		Enable the Vsync reset function for VSR3				0: disable 1: enable												
	VSR3_wid_D_sel		The selection of count direction from Hsync for VSR3_wid_D				0: VSR3_wid_D seen as advance 1: VSR3_wid_D seen as delay												
	VSR3_pwr_pol		The Polarity of VSR3 during display off area				0: VSR3 negative polarity 1: VSR3 positive polarity												
	VSR3_bk_pol		The Polarity of VSR3 during blanking area				0: VSR3 negative polarity 1: VSR3 positive polarity												
	VSR3_pol		The Polarity of VSR3 during active area				0: VSR3 negative polarity 1: VSR3 positive polarity												

Bit	Description	Data
VSR3_prid[10:0]	Period that VSR3 repeats (unit: Hsync)	Note: do not exceed vttotal.
VSR3_wid_L[10:0]	Low pulse width of VSR3 inside a period. (unit: Hsync)	Note: do not exceed VSR3_period.
VSR3_ofst1_ad_sel	The selection of count direction from Hsync for VSR3_ofst1	0: VSR3_ofst1 seen as advance 1: VSR3_ofst1 seen as delay
VSR3_ofst1[10:0]	Time delay/advance from VSR3 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.
VSR3_ofst2[9:0]	Time delay from VSR3(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.
VSR3_wid_D[9:0]	Time delay from VSR3(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.
VSR3_kp_tgl[6:0]	Keep toggling line number of VSR3_kp_tgl from end of the last display line (unit Hsync)	Note: 5. Total toggle area (unit: Hsync) = back porch +/- VSR3_ofst1 + display line + VSR3_kp_tgl 6. do not exceed vttotal
<p>The timing diagram illustrates the relationship between the Hync signal (horizontal sync), vcent_rst (vertical center reset), Source (video source), and VSRn (Vertical Scan Rate Controller). The diagram shows the sequence of lines: BP (Back Porch), Dummy, 1st/2nd line, 3rd/4th line, 5th/6th line, and 7th/8th line. Key parameters are indicated: VSRn_wid_L (width of the low pulse in the period), VSRn_ofst1 (time delay from VSR3 to the last back porch line), VSRn_ofst2 (time delay from VSR3 start to hsync), VSRn_Wid_D (time delay from VSR3 start to hsync), and VSRn_prid (period of VSR3 repeats). The VSRn_pol parameter is also mentioned, indicating high active (1) or low active (0).</p>		

Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	1270h 0x08h 1370h 0x00h 1470h 0x00h 1570h 0x00h 1670h 0x00h 1770h 0x00h 1870h 0x00h 1970h 0x00h 1A70h 0x00h
	S/W Reset	
	H/W Reset	

(1B70h~2370h) GOA_VSR4

Instruction	R/W	GOA_VSR4																			
		Address		Parameter																	
		MPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
GOA_VSR4	R/W	0x1Bh	0x1B70h	00h	VSR4_en	VSR4_rpt_en	VSR4_vrs_t_en	VSR4_wid_D_sel	VSR4_pwr_pol	VSR4_bk_pol	VSR4_pol	-	0x08h								
		0x1Ch	0x1C70h	00h	-	VSR4_wid_L[10:8]			-	VSR4_prid[10:8]			0x00h								
		0x1Dh	0x1D70h	00h	VSR4_prid[7:0]																
		0x1Eh	0x1E70h	00h	VSR4_wid_L[7:0]																
		0x1Fh	0x1F70h	00h	VSR4_ofst1_a_d_sel	VSR4_wid_D[9:8]		VSR4_ofst2[9:8]		VSR4_ofst1[10:8]			0x00h								
		0x20h	0x2070h	00h	VSR4_ofst1[7:0]																
		0x21h	0x2170h	00h	VSR4_ofst2[7:0]																
		0x22h	0x2270h	00h	VSR4_wid_D[7:0]																
		0x23h	0x2370h	00h	-	VSR4_kp_tgl[6:0]															
Description	This command is GOA Timing Control for VSR4.																				
	Bit		Description					Data													
	VSR4_en		VSR4 enable					0: VSR4 disable 1: VSR4 enable													
	VSR4_rpt_en		Enable the repeat function of VSR4					0: disable 1: enable													
	VSR4_vrst_en		Enable the Vsync reset function for VSR4					0: disable 1: enable													
	VSR4_wid_D_sel		The selection of count direction from Hsync for VSR4_wid_D					0: VSR4_wid_D seen as advance 1: VSR4_wid_D seen as delay													
	VSR4_pwr_pol		The Polarity of VSR4 during display off area					0: VSR4 negative polarity 1: VSR4 positive polarity													
	VSR4_bk_pol		The Polarity of VSR4 during blanking area					0: VSR4 negative polarity 1: VSR4 positive polarity													
	VSR4_pol		The Polarity of VSR4 during active area					0: VSR4 negative polarity 1: VSR4 positive polarity													

Bit	Description	Data
VSR4_prid[10:0]	Period that VSR4 repeats (unit: Hsync)	Note: do not exceed vttotal.

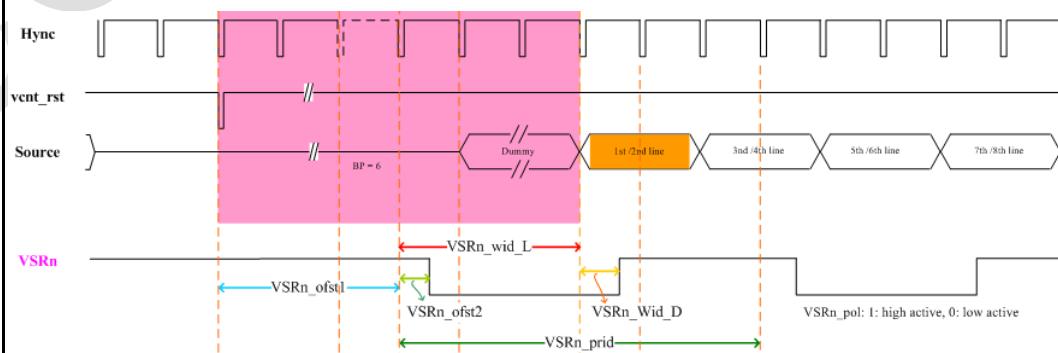
Bit	Description	Data
VSR4_wid_L[10:0]	Low pulse width of VSR4 inside a period. (unit: Hsync)	Note: do not exceed VSR4_period.

Bit	Description	Data
VSR4_ofst1_ad_sel	The selection of count direction from Hsync for VSR4_ofst1	0: VSR4_ofst1 seen as advance 1: VSR4_ofst1 seen as delay
VSR4_ofst1[10:0]	Time delay/advance from VSR4 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.

Bit	Description	Data
VSR4_ofst2[9:0]	Time delay from VSR4(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.

Bit	Description	Data
VSR4_wid_D[9:0]	Time delay from VSR4(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.

Bit	Description	Data
VSR4_kp_tgl[6:0]	Keep toggling line number of VSR4_kp_tgl from end of the last display line (unit Hsync)	Note: 7. Total toggle area (unit: Hsync) = back porch +/- VSR4_ofst1 + display line + VSR4_kp_tgl 8. do not exceed vttotal



Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	1B70h 0x08h 1C70h 0x00h 1D70h 0x00h 1E70h 0x00h 1F70h 0x00h 2070h 0x00h 2170h 0x00h 2270h 0x00h 2370h 0x00h
	S/W Reset	
	H/W Reset	

(2470h~2D70h) GOA_VSR5

Instruction	R/W	GOA_VSR5																																		
		Address		Parameter																																
MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
GOA_VSR5	R/W	0x24h	0x2470h	00h	VSR5_en	VSR5_rpt_en	VSR5_vrs_t_en	VSR5_wid_D_sel	VSR5_pwr_pol	VSR5_bk_pol	VSR5_pol	-	0x08h																							
		0x25h	0x2570h	00h	-	VSR5_wid_L[10:8]			-	VSR5_prid[10:8]			0x00h																							
		0x26h	0x2670h	00h	VSR5_prid[7:0]								0x00h																							
		0x27h	0x2770h	00h	VSR5_wid_L[7:0]								0x00h																							
		0x28h	0x2870h	00h	VSR5_ofst1_a_d_sel	VSR5_wid_D[9:8]		VSR5_ofst2[9:8]	VSR5_ofst1[10:8]			0x00h																								
		0x29h	0x2970h	00h	VSR5_ofst1[7:0]								0x00h																							
		0x2Ah	0x2A70h	00h	VSR5_ofst2[7:0]								0x00h																							
		0x2Bh	0x2B70h	00h	VSR5_wid_D[7:0]								0x00h																							
		0x2Dh	0x2D70h	00h	-	VSR5_kp_tgl[6:0]					0x00h																									
Description	This command is GOA Timing Control for VSR5.																																			
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>VSR5_en</td> <td>VSR5 enable</td> <td>0: VSR5 disable 1: VSR5 enable</td> </tr> <tr> <td>VSR5_rpt_en</td> <td>Enable the repeat function of VSR5</td> <td>0: disable 1: enable</td> </tr> <tr> <td>VSR5_vrst_en</td> <td>Enable the Vsync reset function for VSR5</td> <td>0: disable 1: enable</td> </tr> <tr> <td>VSR5_wid_D_sel</td> <td>The selection of count direction from Hsync for VSR5_wid_D</td> <td>0: VSR5_wid_D seen as advance 1: VSR5_wid_D seen as delay</td> </tr> <tr> <td>VSR5_pwr_pol</td> <td>The Polarity of VSR5 during display off area</td> <td>0: VSR5 negative polarity 1: VSR5 positive polarity</td> </tr> <tr> <td>VSR5_bk_pol</td> <td>The Polarity of VSR5 during blanking area</td> <td>0: VSR5 negative polarity 1: VSR5 positive polarity</td> </tr> <tr> <td>VSR5_pol</td> <td>The Polarity of VSR5 during active area</td> <td>0: VSR5 negative polarity 1: VSR5 positive polarity</td> </tr> </tbody> </table>													Bit	Description	Data	VSR5_en	VSR5 enable	0: VSR5 disable 1: VSR5 enable	VSR5_rpt_en	Enable the repeat function of VSR5	0: disable 1: enable	VSR5_vrst_en	Enable the Vsync reset function for VSR5	0: disable 1: enable	VSR5_wid_D_sel	The selection of count direction from Hsync for VSR5_wid_D	0: VSR5_wid_D seen as advance 1: VSR5_wid_D seen as delay	VSR5_pwr_pol	The Polarity of VSR5 during display off area	0: VSR5 negative polarity 1: VSR5 positive polarity	VSR5_bk_pol	The Polarity of VSR5 during blanking area	0: VSR5 negative polarity 1: VSR5 positive polarity	VSR5_pol	The Polarity of VSR5 during active area
Bit	Description	Data																																		
VSR5_en	VSR5 enable	0: VSR5 disable 1: VSR5 enable																																		
VSR5_rpt_en	Enable the repeat function of VSR5	0: disable 1: enable																																		
VSR5_vrst_en	Enable the Vsync reset function for VSR5	0: disable 1: enable																																		
VSR5_wid_D_sel	The selection of count direction from Hsync for VSR5_wid_D	0: VSR5_wid_D seen as advance 1: VSR5_wid_D seen as delay																																		
VSR5_pwr_pol	The Polarity of VSR5 during display off area	0: VSR5 negative polarity 1: VSR5 positive polarity																																		
VSR5_bk_pol	The Polarity of VSR5 during blanking area	0: VSR5 negative polarity 1: VSR5 positive polarity																																		
VSR5_pol	The Polarity of VSR5 during active area	0: VSR5 negative polarity 1: VSR5 positive polarity																																		

Bit	Description	Data
VSR5_prid[10:0]	Period that VSR5 repeats (unit: Hsync)	Note: do not exceed vttotal.

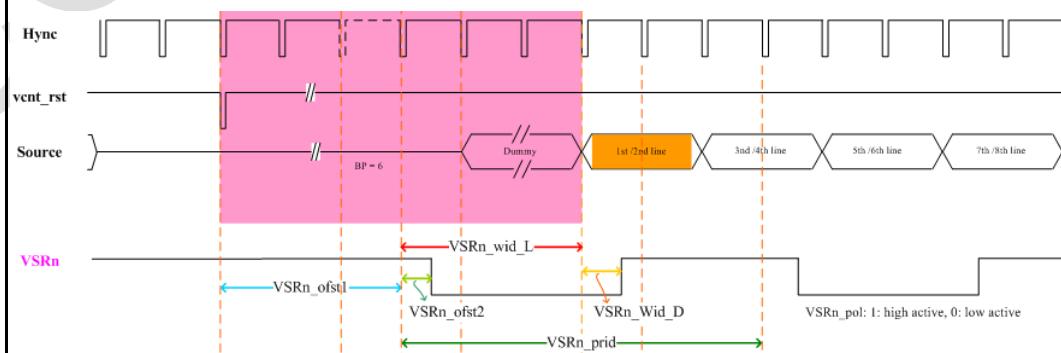
Bit	Description	Data
VSR5_wid_L[10:0]	Low pulse width of VSR5 inside a period. (unit: Hsync)	Note: do not exceed VSR5_period.

Bit	Description	Data
VSR5_ofst1_ad_sel	The selection of count direction from Hsync for VSR5_ofst1	0: VSR5_ofst1 seen as advance 1: VSR5_ofst1 seen as delay
VSR5_ofst1[10:0]	Time delay/advance from VSR5 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.

Bit	Description	Data
VSR5_ofst2[9:0]	Time delay from VSR5(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.

Bit	Description	Data
VSR5_wid_D[9:0]	Time delay from VSR5(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.

Bit	Description	Data
VSR5_kp_tgl[6:0]	Keep toggling line number of VSR5_kp_tgl from end of the last display line (unit Hsync)	Note: 9. Total toggle area (unit: Hsync) = back porch +/- VSR5_ofst1 + display line + VSR5_kp_tgl 10. do not exceed vttotal



Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	2470h 0x08h 2570h 0x00h 2670h 0x00h 2770h 0x00h 2870h 0x00h 2970h 0x00h 2A70h 0x00h 2B70h 0x00h 2D70h 0x00h
	S/W Reset	
	H/W Reset	

(2F70h~3770h) GOA_VSR6

Instruction	R/W	GOA_VSR6																	
		Address		Parameter															
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
GOA_VSR6	R/W	0x2Fh	0x2F70h	00h	VSR6_en	VSR6_rpt_en	VSR6_vrs_t_en	VSR6_wid_D_sel	VSR6_pwr_pol	VSR6_bk_pol	VSR6_pol	-	0x08h						
		0x30h	0x3070h	00h	-	VSR6_wid_L[10:8]			-	VSR6_prid[10:8]			0x00h						
		0x31h	0x3170h	00h	VSR6_prid[7:0]								0x00h						
		0x32h	0x3270h	00h	VSR6_wid_L[7:0]								0x00h						
		0x33h	0x3370h	00h	VSR6_ofst1_a_d_sel	VSR6_wid_D[9:8]		VSR6_ofst2[9:8]	VSR6_ofst1[10:8]			0x00h							
		0x34h	0x3470h	00h	VSR6_ofst1[7:0]								0x00h						
		0x35h	0x3570h	00h	VSR6_ofst2[7:0]								0x00h						
		0x36h	0x3670h	00h	VSR6_wid_D[7:0]								0x00h						
		0x37h	0x3770h	00h	-	VSR6_kp_tgl[6:0]						0x00h							
Description	This command is GOA Timing Control for VSR6.																		
	Bit	Description				Data													
	VSR6_en	VSR6 enable				0: VSR6 disable 1: VSR6 enable													
	VSR6_rpt_en	Enable the repeat function of VSR6				0: disable 1: enable													
	VSR6_vrst_en	Enable the Vsync reset function for VSR6				0: disable 1: enable													
	VSR6_wid_D_sel	The selection of count direction from Hsync for VSR6_wid_D				0: VSR6_wid_D seen as advance 1: VSR6_wid_D seen as delay													
	VSR6_pwr_pol	The Polarity of VSR6 during display off area				0: VSR6 negative polarity 1: VSR6 positive polarity													
	VSR6_bk_pol	The Polarity of VSR6 during blanking area				0: VSR6 negative polarity 1: VSR6 positive polarity													
	VSR6_pol	The Polarity of VSR6 during active area				0: VSR6 negative polarity 1: VSR6 positive polarity													

Bit	Description	Data
VSR6_prid[10:0]	Period that VSR6 repeats (unit: Hsync)	Note: do not exceed vttotal.

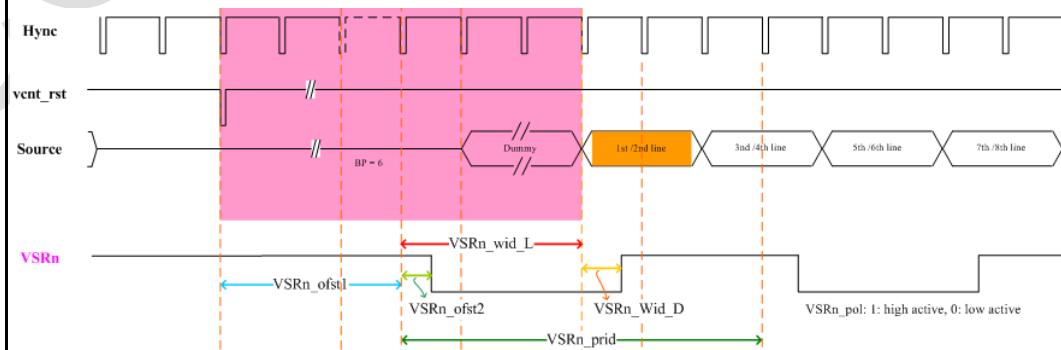
Bit	Description	Data
VSR6_wid_L[10:0]	Low pulse width of VSR6 inside a period. (unit: Hsync)	Note: do not exceed VSR6_period.

Bit	Description	Data
VSR6_ofst1_ad_sel	The selection of count direction from Hsync for VSR6_ofst1	0: VSR6_ofst1 seen as advance 1: VSR6_ofst1 seen as delay
VSR6_ofst1[10:0]	Time delay/advance from VSR6 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.

Bit	Description	Data
VSR6_ofst2[9:0]	Time delay from VSR6(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.

Bit	Description	Data
VSR6_wid_D[9:0]	Time delay from VSR6(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.

Bit	Description	Data
VSR6_kp_tgl[6:0]	Keep toggling line number of VSR6_kp_tgl from end of the last display line (unit Hsync)	Note: 11. Total toggle area (unit: Hsync) = back porch +/- VSR6_ofst1 + display line + VSR6_kp_tgl 12. do not exceed vttotal

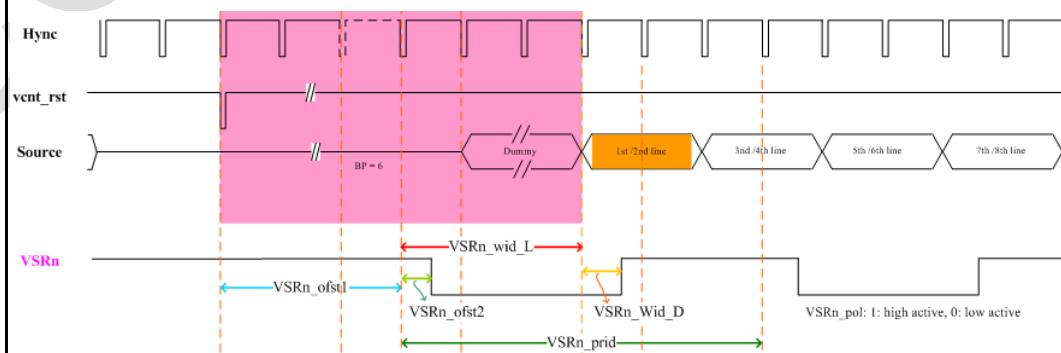


Restriction																			
Register Availability	Status	Availability																	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
	Normal Mode On, Idle Mode On, Sleep Out	Yes																	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																	
	Partial Mode On, Idle Mode On, Sleep Out	Yes																	
	Sleep In	Yes																	
Default	Status	Default Value																	
	Power On Sequence	<table border="1"><tr><td>2F70h</td><td>0x08h</td></tr><tr><td>3070h</td><td>0x00h</td></tr><tr><td>3170h</td><td>0x00h</td></tr><tr><td>3270h</td><td>0x00h</td></tr><tr><td>3370h</td><td>0x00h</td></tr><tr><td>3470h</td><td>0x00h</td></tr><tr><td>3570h</td><td>0x00h</td></tr><tr><td>3670h</td><td>0x00h</td></tr><tr><td>3770h</td><td>0x00h</td></tr></table>	2F70h	0x08h	3070h	0x00h	3170h	0x00h	3270h	0x00h	3370h	0x00h	3470h	0x00h	3570h	0x00h	3670h	0x00h	3770h
2F70h	0x08h																		
3070h	0x00h																		
3170h	0x00h																		
3270h	0x00h																		
3370h	0x00h																		
3470h	0x00h																		
3570h	0x00h																		
3670h	0x00h																		
3770h	0x00h																		
S/W Reset																			
H/W Reset																			

(3870h~4270h) GOA_VSR7

Instruction	R/W	GOA_VSR7																	
		Address		Parameter															
MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
GOA_VSR7	R/W	0x38h	0x3870h	00h	VSR7_en	VSR7_rpt_en	VSR7_vrs_t_en	VSR7_wid_D_sel	VSR7_pwr_pol	VSR7_bk_pol	VSR7_pol	-	0x08h						
		0x39h	0x3970h	00h	-	VSR7_wid_L[10:8]			-	VSR7_prid[10:8]			0x00h						
		0x3Ah	0x3A70h	00h	VSR7_prid[7:0]								0x00h						
		0x3Bh	0x3B70h	00h	VSR7_wid_L[7:0]								0x00h						
		0x3Dh	0x3D70h	00h	VSR7_ofst1_a_d_sel	VSR7_wid_D[9:8]		VSR7_ofst2[9:8]	VSR7_ofst1[10:8]			0x00h							
		0x3Fh	0x3F70h	00h	VSR7_ofst1[7:0]								0x00h						
		0x40h	0x4070h	00h	VSR7_ofst2[7:0]								0x00h						
		0x41h	0x4170h	00h	VSR7_wid_D[7:0]								0x00h						
		0x42h	0x4270h	00h	-	VSR7_kp_tgl[6:0]				VSR7_kp_tgl[6:0]				0x00h					
Description	This command is GOA Timing Control for VSR7.																		
	Bit	Description				Data													
	VSR7_en	VSR7 enable				0: VSR7 disable 1: VSR7 enable													
	VSR7_rpt_en	Enable the repeat function of VSR7				0: disable 1: enable													
	VSR7_vrst_en	Enable the Vsync reset function for VSR7				0: disable 1: enable													
	VSR7_wid_D_sel	The selection of count direction from Hsync for VSR7_wid_D				0: VSR7_wid_D seen as advance 1: VSR7_wid_D seen as delay													
	VSR7_pwr_pol	The Polarity of VSR7 during display off area				0: VSR7 negative polarity 1: VSR7 positive polarity													
	VSR7_bk_pol	The Polarity of VSR7 during blanking area				0: VSR7 negative polarity 1: VSR7 positive polarity													
	VSR7_pol	The Polarity of VSR7 during active area				0: VSR7 negative polarity 1: VSR7 positive polarity													

Bit	Description	Data
VSR7_prid[10:0]	Period that VSR7 repeats (unit: Hsync)	Note: do not exceed vttotal.
VSR7_wid_L[10:0]	Low pulse width of VSR7 inside a period. (unit: Hsync)	Note: do not exceed VSR7_period.
VSR7_ofst1_ad_sel	The selection of count direction from Hsync for VSR7_ofst1	0: VSR7_ofst1 seen as advance 1: VSR7_ofst1 seen as delay
VSR7_ofst1[10:0]	Time delay/advance from VSR7 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.
VSR7_ofst2[9:0]	Time delay from VSR7(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.
VSR7_wid_D[9:0]	Time delay from VSR7(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.
VSR7_kp_tgl[6:0]	Keep toggling line number of VSR7_kp_tgl from end of the last display line (unit Hsync)	Note: 13. Total toggle area (unit: Hsync) = back porch +/- VSR7_ofst1 + display line + VSR7_kp_tgl 14. do not exceed vttotal



Restriction																			
Register Availability	Status	Availability																	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
	Normal Mode On, Idle Mode On, Sleep Out	Yes																	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																	
	Partial Mode On, Idle Mode On, Sleep Out	Yes																	
	Sleep In	Yes																	
Default	Status	Default Value																	
	Power On Sequence	<table border="1"><tr><td>3870h</td><td>0x08h</td></tr><tr><td>3970h</td><td>0x00h</td></tr><tr><td>3A70h</td><td>0x00h</td></tr><tr><td>3B70h</td><td>0x00h</td></tr><tr><td>3D70h</td><td>0x00h</td></tr><tr><td>3F70h</td><td>0x00h</td></tr><tr><td>4070h</td><td>0x00h</td></tr><tr><td>4170h</td><td>0x00h</td></tr><tr><td>4270h</td><td>0x00h</td></tr></table>	3870h	0x08h	3970h	0x00h	3A70h	0x00h	3B70h	0x00h	3D70h	0x00h	3F70h	0x00h	4070h	0x00h	4170h	0x00h	4270h
3870h	0x08h																		
3970h	0x00h																		
3A70h	0x00h																		
3B70h	0x00h																		
3D70h	0x00h																		
3F70h	0x00h																		
4070h	0x00h																		
4170h	0x00h																		
4270h	0x00h																		
S/W Reset																			
H/W Reset																			

(4370h~4B70h) GOA_VSR8

Instruction	R/W	GOA_VSR8																		
		Address		Parameter																
MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
GOA_VSR8	R/W	0x43h	0x4370h	00h	VSR8_en	VSR8_rpt_en	VSR8_vrs_t_en	VSR8_wid_D_sel	VSR8_pwr_pol	VSR8_bk_pol	VSR8_pol	-	0x08h							
		0x44h	0x4470h	00h	-	VSR8_wid_L[10:8]			-	VSR8_prid[10:8]			0x00h							
		0x45h	0x4570h	00h	VSR8_prid[7:0]								0x00h							
		0x46h	0x4670h	00h	VSR8_wid_L[7:0]								0x00h							
		0x47h	0x4770h	00h	VSR8_ofst1_a_d_sel	VSR8_wid_D[9:8]		VSR8_ofst2[9:8]		VSR8_ofst1[10:8]			0x00h							
		0x48h	0x4870h	00h	VSR8_ofst1[7:0]								0x00h							
		0x49h	0x4970h	00h	VSR8_ofst2[7:0]								0x00h							
		0x4Ah	0x4A70h	00h	VSR8_wid_D[7:0]								0x00h							
		0x4Bh	0x4B70h	00h	-	VSR8_kp_tgl[6:0]								0x00h						
Description	This command is GOA Timing Control for VSR8.																			
	Bit		Description				Data													
	VSR8_en		VSR8 enable				0: VSR8 disable 1: VSR8 enable													
	VSR8_rpt_en		Enable the repeat function of VSR8				0: disable 1: enable													
	VSR8_vrst_en		Enable the Vsync reset function for VSR8				0: disable 1: enable													
	VSR8_wid_D_sel		The selection of count direction from Hsync for VSR8_wid_D				0: VSR8_wid_D seen as advance 1: VSR8_wid_D seen as delay													
	VSR8_pwr_pol		The Polarity of VSR8 during display off area				0: VSR8 negative polarity 1: VSR8 positive polarity													
	VSR8_bk_pol		The Polarity of VSR8 during blanking area				0: VSR8 negative polarity 1: VSR8 positive polarity													
	VSR8_pol		The Polarity of VSR8 during active area				0: VSR8 negative polarity 1: VSR8 positive polarity													

Bit	Description	Data
VSR8_prid[10:0]	Period that VSR8 repeats (unit: Hsync)	Note: do not exceed vttotal.
VSR8_wid_L[10:0]	Low pulse width of VSR8 inside a period. (unit: Hsync)	Note: do not exceed VSR8_period.
VSR8_ofst1_ad_sel	The selection of count direction from Hsync for VSR8_ofst1	0: VSR8_ofst1 seen as advance 1: VSR8_ofst1 seen as delay
VSR8_ofst1[10:0]	Time delay/advance from VSR8 to last back porch line each frame(unit: Hsync)	Note: do not exceed vttotal.
VSR8_ofst2[9:0]	Time delay from VSR8(falling or rising) start to hsync. (unit: dclk)	Note: do not exceed httotal.
VSR8_wid_D[9:0]	Time delay from VSR8(rising or falling) start to hsync. ((unit: dclk))	Note: do not exceed httotal.
VSR8_kp_tgl[6:0]	Keep toggling line number of VSR8_kp_tgl from end of the last display line (unit Hsync)	Note: 15. Total toggle area (unit: Hsync) = back porch +/- VSR8_ofst1 + display line + VSR8_kp_tgl 16. do not exceed vttotal

Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	4370h 0x08h 4470h 0x00h 4570h 0x00h 4670h 0x00h 4770h 0x00h 4870h 0x00h 4970h 0x00h 4A70h 0x00h 4B70h 0x00h
	S/W Reset	
	H/W Reset	

(4C70h~5270h) GOA_VST

Instruction	R/W	GOA_VST																										
		Address		Parameter																								
		MPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
GOA_VST	R/W	0x4Ch	0x4C70h	00h	VST_en	-	-	VST_wid_D_sel	VST_pwr_pol	-	VST_polarity	-	0x08h															
		0x4Dh	0x4D70h	00h	-	VST_wid_L[10:8]			-	-	-	-	0x00h															
		0x4Eh	0x4E70h	00h	VST_wid_L[7:0]								0x00h															
		0x4Fh	0x4F70h	00h	VST_ofst1_ad_sel	VST_wid_D[9:8]		VST_ofst2[9:8]		VST_ofst1[10:8]			0x00h															
		0x50h	0x5070h	00h	VST_ofst1[7:0]								0x00h															
		0x51h	0x5170h	00h	VST_ofst2[7:0]								0x00h															
		0x52h	0x5270h	00h	VST_wid_D[7:0]								0x00h															
Description	This command is GOA Timing Control for VST.																											
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VST_en	VST enable	0: VST disable 1: VST enable																										
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VST_ofst1_ad_se I	The selection of count direction from Hsync for VST_ofst1	0: VST_ofst1 seen as advance 1: VST_ofst1 seen as delay																											
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H/W Reset																													

(5370h~5970h) GOA_VEN

Instruction	R/W	GOA_VEN																																			
		Address		Parameter																																	
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
GOA_VEN	R/W	0x53h	0x5370h	00h	VEN_en	VEN_rp_en	VEN_vrst_en	VEN_wid_D_sel	VEN_pwr_pol	VEN_bk_pol	VEN_pol	-	0x08h																								
		0x54h	0x5470h	00h	VEN_ofst1_ad_sel	VEN_wid_D[9:8]		VEN_ofst2[9:8]		VEN_ofst1[10:8]			0x00h																								
		0x55h	0x5570h	00h	VEN_ofst1[7:0]								0x00h																								
		0x56h	0x5670h	00h	VEN_ofst2[7:0]								0x00h																								
		0x58h	0x5870h	00h	VEN_wid_D[7:0]								0x00h																								
		0x59h	0x5970h	00h	-	VEN_kp_tgl[6:0]								0x00h																							
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	Power On Sequence	
	S/W Reset	
	H/W Reset	

5370h	0x08h
5470h	0x00h
5570h	0x00h
5670h	0x00h
5870h	0x00h
5970h	0x00h

CONFIDENTIAL

(5E70h~6270h) GOA Output Selection

Instruction	R/ W	GOAOUTSEL																																																																																					
		Address		Parameter																																																																																			
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																										
GOAOUTSEL 1	R/ W	0x5Eh	0x5E70h	00h	VSR2_OUT_sel[3:0]			VSR1_OUT_sel[3:0]			0x00h																																																																												
GOAOUTSEL 2	R/ W	0x5Fh	0x5F70h	00h	VSR4_OUT_sel[3:0]			VSR3_OUT_sel[3:0]			0x00h																																																																												
GOAOUTSEL 3	R/ W	0x60h	0x6070h	00h	VSR6_OUT_sel[3:0]			VSR5_OUT_sel[3:0]			0x00h																																																																												
GOAOUTSEL 4	R/ W	0x61h	0x6170h	00h	VSR8_OUT_sel[3:0]			VSR7_OUT_sel[3:0]			0x00h																																																																												
GOAOUTSEL 5	R/ W	0x62h	0x6270h	00h	VEN_OUT_sel[3:0]			VST_OUT_sel[3:0]			0x00h																																																																												
Description	This command is used to set GOA output mapping.																																																																																						
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Bit	Data																																																																																						
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Power On Sequence
S/W Reset
H/W Reset

0x5E70h	0x00h
0x5F70h	0x00h
0x6070h	0x00h
0x6170h	0x00h
0x6270h	0x00h

CONFIDENTIAL

(6570h~6770h) GOA_VEN

		GOA_VEN																											
Instruction	R/ W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
BC_Perid& Wid_LUT20 ~22	R/ W	0x65h	0x6570h	00h	VEN_perid_exp[7:0]										0x00h														
		0x66h	0x6670h	00h	VEN_wid_L_exp[7:0]										0x00h														
		0x67h	0x6770h	00h	-	VEN_perid_exp[10:8]			-	VEN_wid_L_exp[10:8]				0x00h															
Description		This command is used to set VEN period and low duration.																											
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(FE70h) CMD Mode Switch

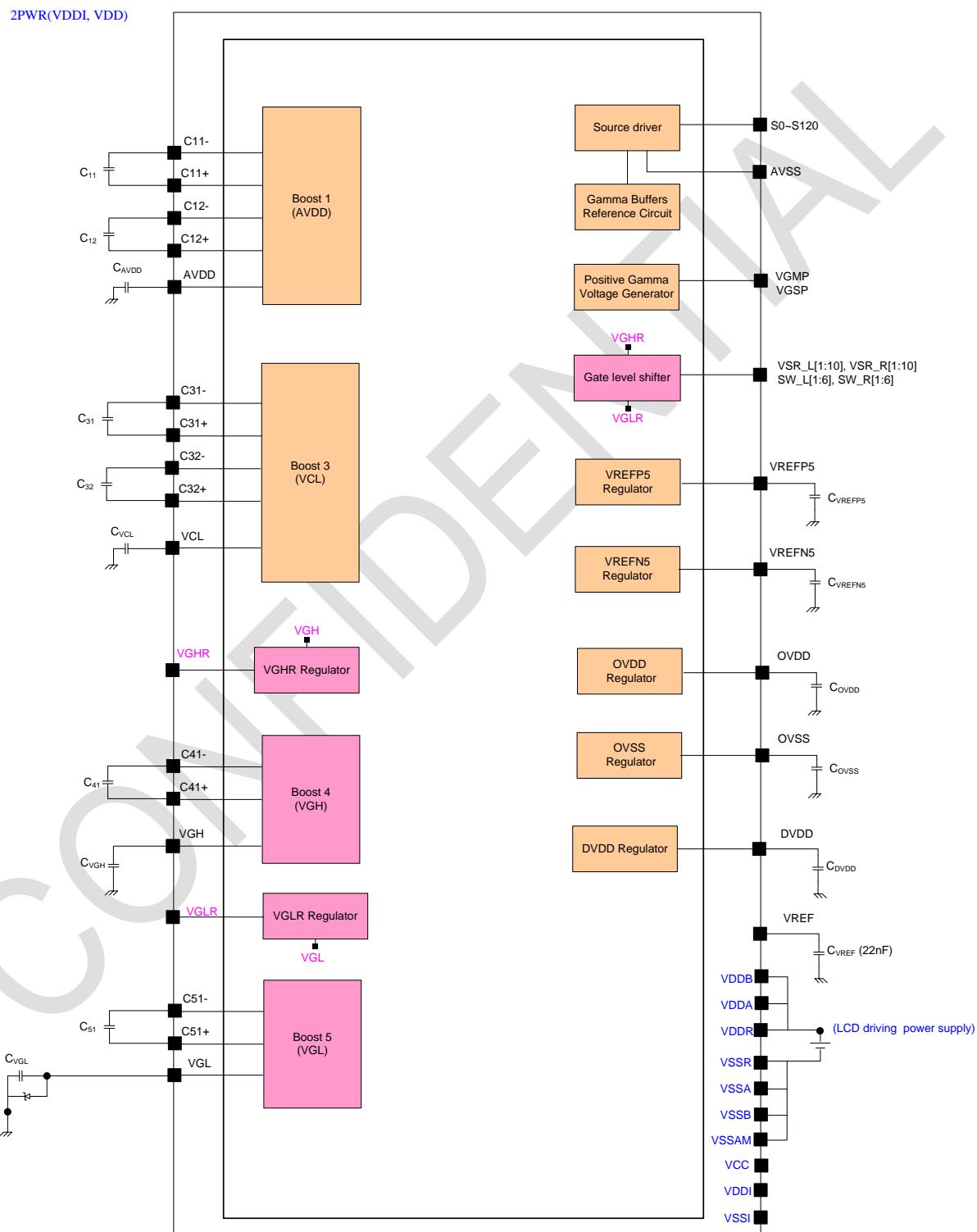
	CMD Mode Switch																														
Instruction	R/W	Address		Parameter																											
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
CMD Mode Switch	R/W	0xFEh	0xFE70h	00h	-	-	-	-	CMD_Page_Selection	0x00h																					
Description	<p>This command is used to switch the Manufacture Command Pages and User Commands sets.</p> <table border="1"> <thead> <tr> <th>CMD_Page[3:0]</th> <th>Hex Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h (default)</td> <td>User Command Set (UCS = CMD1)</td> </tr> <tr> <td>0001</td> <td>01h</td> <td>Manufacture Command Set Page0 (CMD2 P0)</td> </tr> <tr> <td>0010</td> <td>02h</td> <td>Manufacture Command Set Page1 (CMD2 P1)</td> </tr> <tr> <td>0011</td> <td>03h</td> <td>Manufacture Command Set Page2 (CMD2 P2)</td> </tr> <tr> <td>0100</td> <td>04h</td> <td>Manufacture Command Set Page3 (CMD2 P3)</td> </tr> </tbody> </table>													CMD_Page[3:0]	Hex Value	Description	0000	00h (default)	User Command Set (UCS = CMD1)	0001	01h	Manufacture Command Set Page0 (CMD2 P0)	0010	02h	Manufacture Command Set Page1 (CMD2 P1)	0011	03h	Manufacture Command Set Page2 (CMD2 P2)	0100	04h	Manufacture Command Set Page3 (CMD2 P3)
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(FF70h) RD CMD Status

	RD CMD Status																												
Instruction	R/W	Address		Parameter																									
		MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
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2. Power Generation

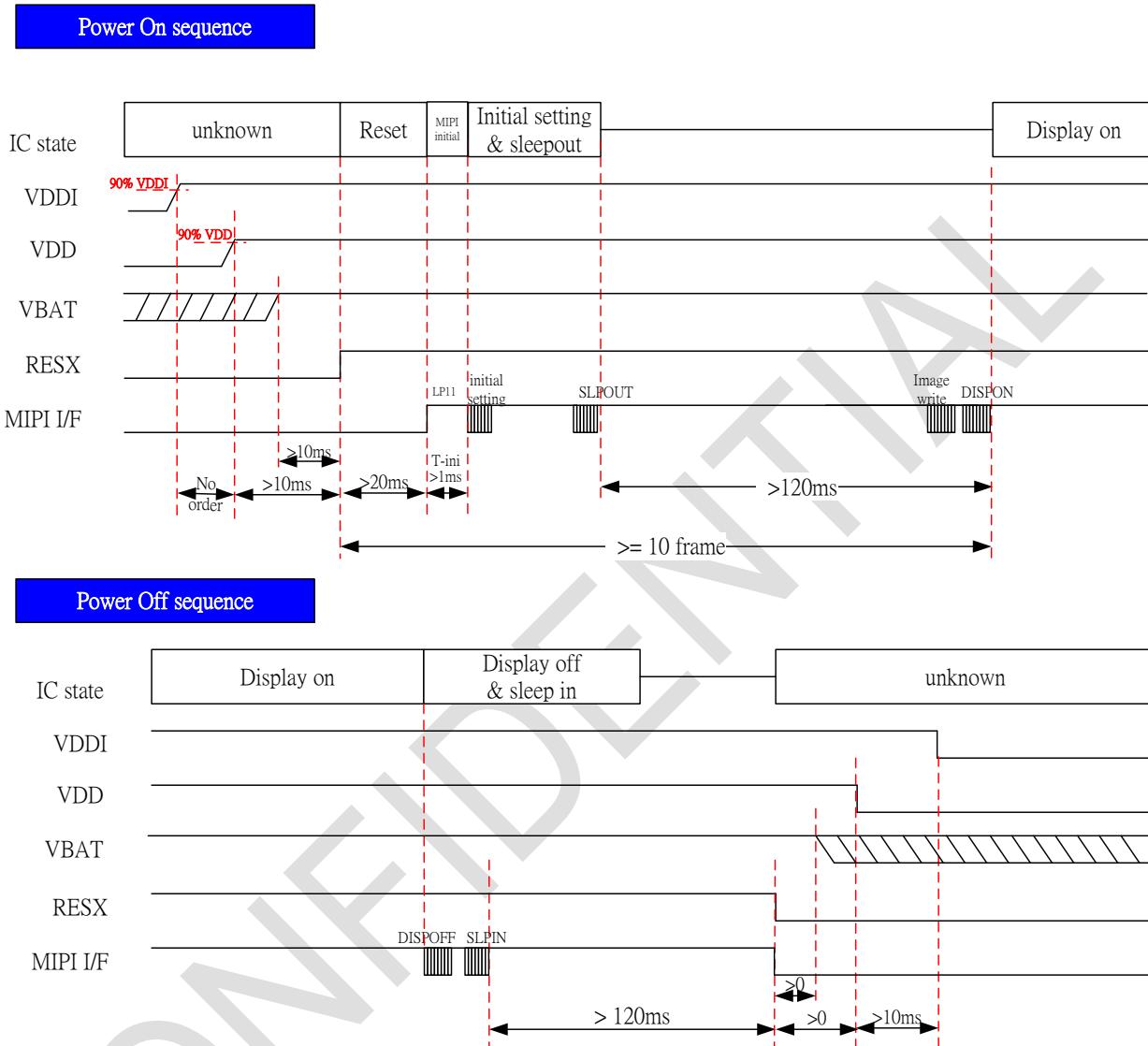
2.1 DC/DC Converter Circuit



2.2 External Components

No.	Signal name	Values	Max ability
1	VDDA, VDDR, VDBB	Cap , 2.2uF	6.3V
2	VREF	Cap , 22nF	6.3V
3	DVDD	Cap , 1.0uF	6.3V
4	VREFN5	Cap , 1.0uF	10V
5	VREFP5	Cap , 1.0uF	10V
6	OVDD(BVP3D)	Cap , 2.2uF	10V
7	OVSS(BVN3D)	Cap , 2.2uF	10V
8	C11P/C11N	Cap , 1.0uF	6.3V
9	C12P/C12N	Cap , 1.0uF	6.3V
10	AVDD	Cap , 2.2uF	10V
11	C31P/C31N	Cap , 1.0uF	6.3V
12	C32P/C32N	Cap , 1.0uF	6.3V
13	VCL	Cap , 2.2uF	10V
14	C41P/C41N	Cap , 1.0uF	16V
15	VGH	Cap , 2.2uF	25V
16	C51P/C51N	Cap , 1.0uF	16V
17	VGL	Cap , 2.2uF	25V
18	VGL (VGL-GND)	Schottky Diode	

2.3 Power on/off sequence and timing



2.4 Power Level Modes

Normal display mode on = NORON

Partial mode on = PTLON

Idle mode off = IDMOFF

Idle mode on = IDMON

Sleep out = SLPOUT

Sleep in = SLPIN

Deep standby mode = DSTBON

Definition example:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.

6. Deep Standby Mode.

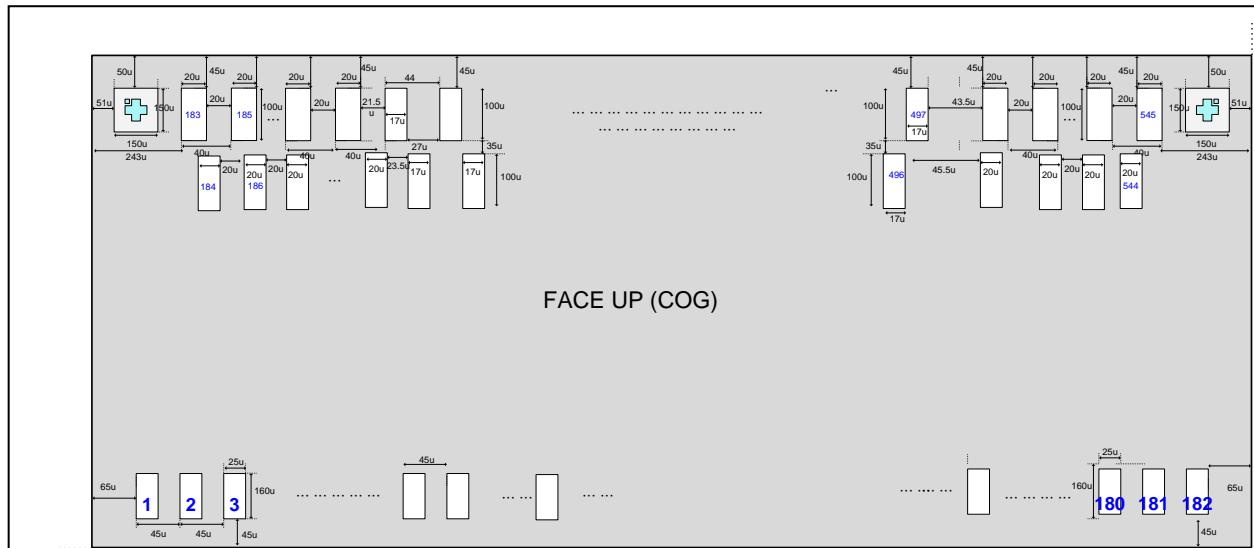
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.

7. Power Off Mode

In this mode, VDDI and VDDA/VDDR/VDBB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

3. Pad Diagram and Coordination



- Chip thickness: 200/300 um