
RWTH AACHEN UNIVERSITY


SW Debugging for Multi-tile Systems: The EURETILE Methodology and Tools

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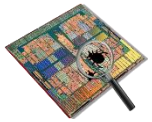


MAD Workshop, HiPEAC Fall CSW
9.10.14, Athens, Greece

HiPEAC COMPILATION ARCHITECTURE

ICE

Institute for Communication Technologies and Embedded Systems

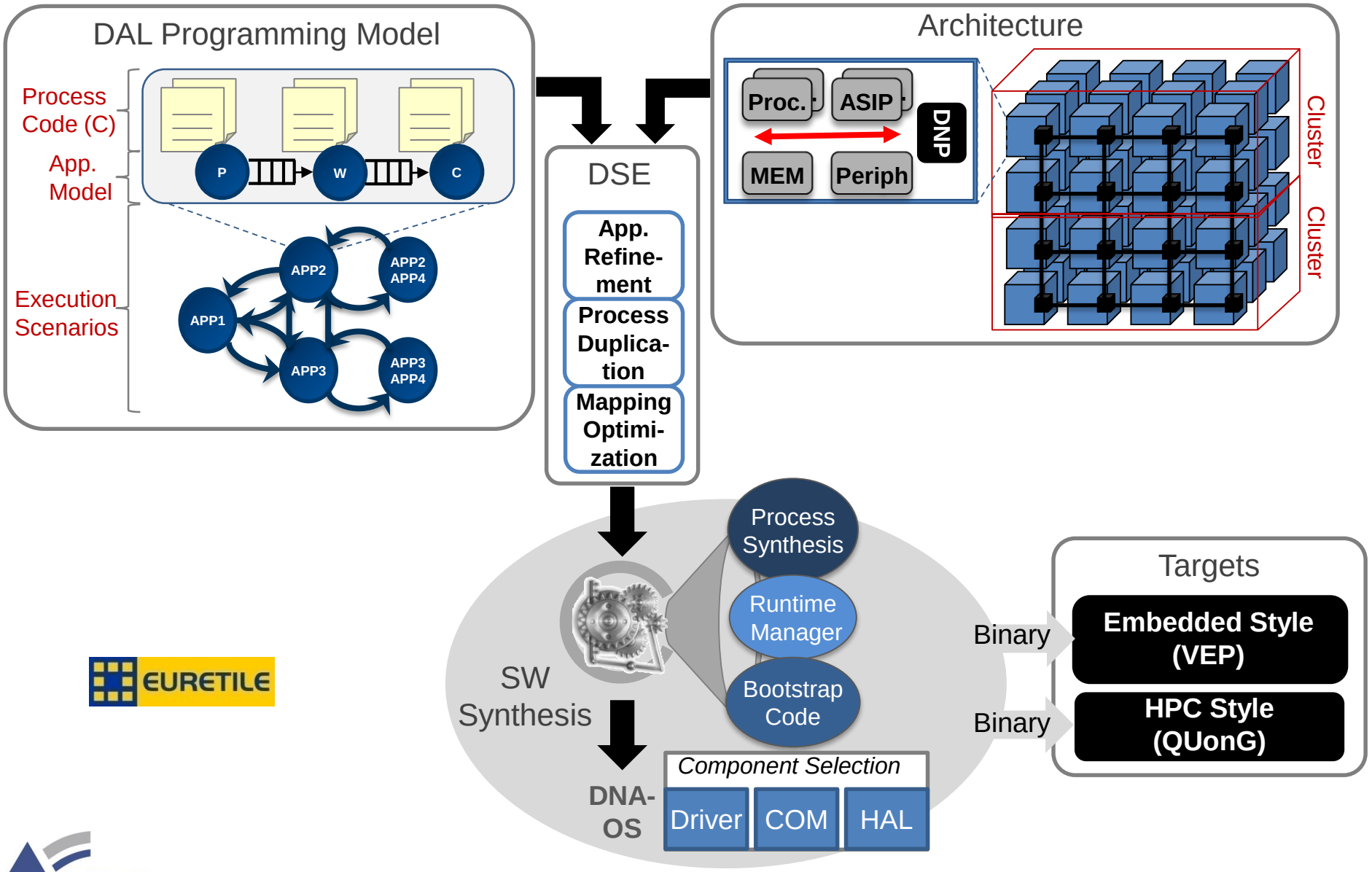
EURETILE Overview

- EURETILE: EUropean REference TIled architecture Experiment (www.euretile.eu)
  - FET Concurrent Tera-Device Computing (FP7)
  - 6M EUR
- Duration: 2010 – 2014
- Partners:

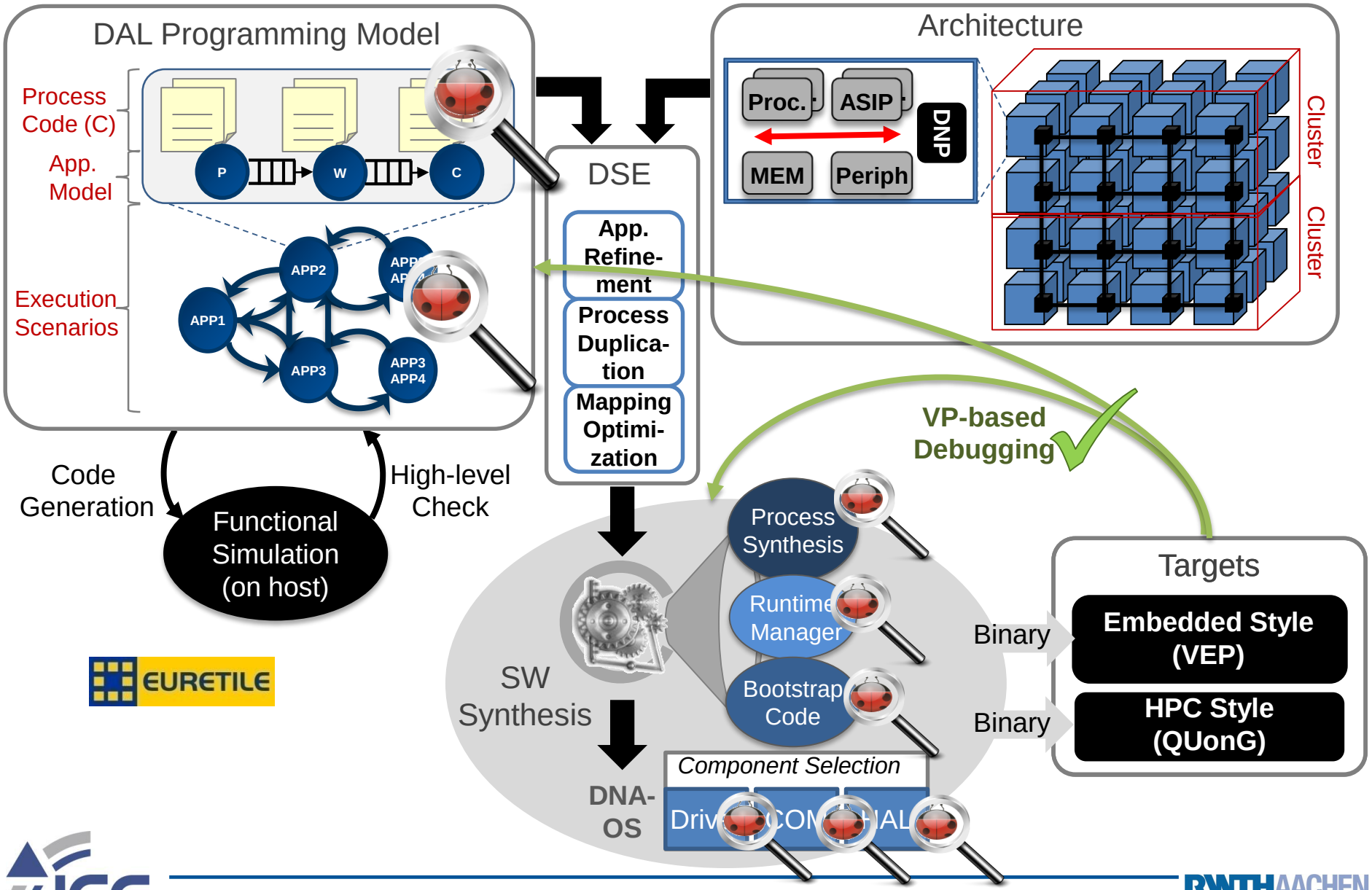
INFN ETH Zürich Université Joseph Fourier GRENOBLE TARGET THE ASIP COMPANY RWTH AACHEN UNIVERSITY

- **Goal:**
  - Brain-inspired and fault-tolerant foundational innovations on massively parallel tiled architectures
  - Corresponding programming paradigm

EURETILE Overview



EURETILE, How to Debug?



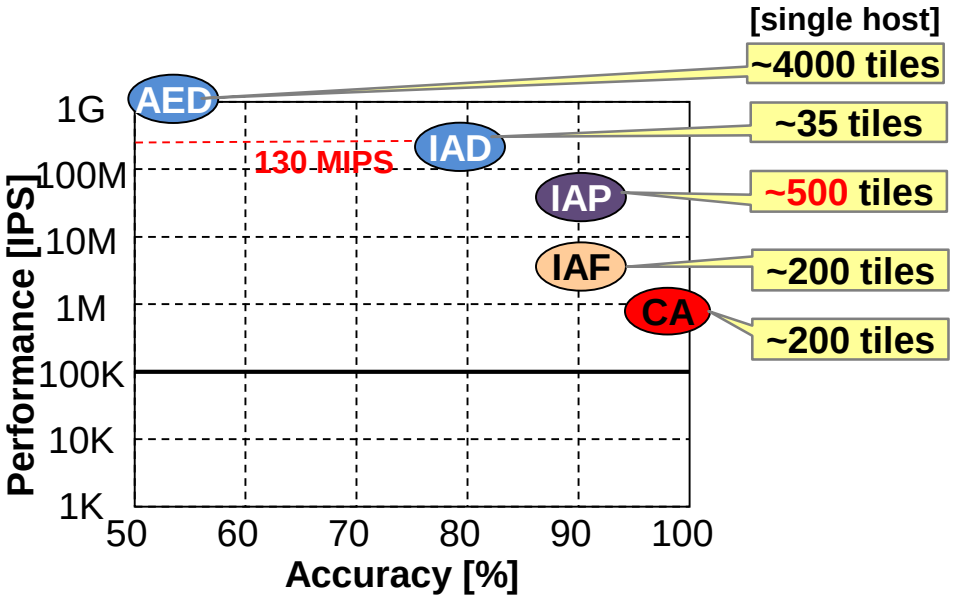
Agenda

- Introduction
- The Virtual EURETILE Platform
- Tools for Whole-system Debugging
- Concurrency Event Monitors and Concurrency Analysis
- Conclusions

VEP: Virtual Platform for SW Development and Debugging

- **Advantages**
  - Early availability
  - Run unmodified target SW binary
  - Optimal for debugging concurrency issues
  - Non-intrusive inspection and reproducibility

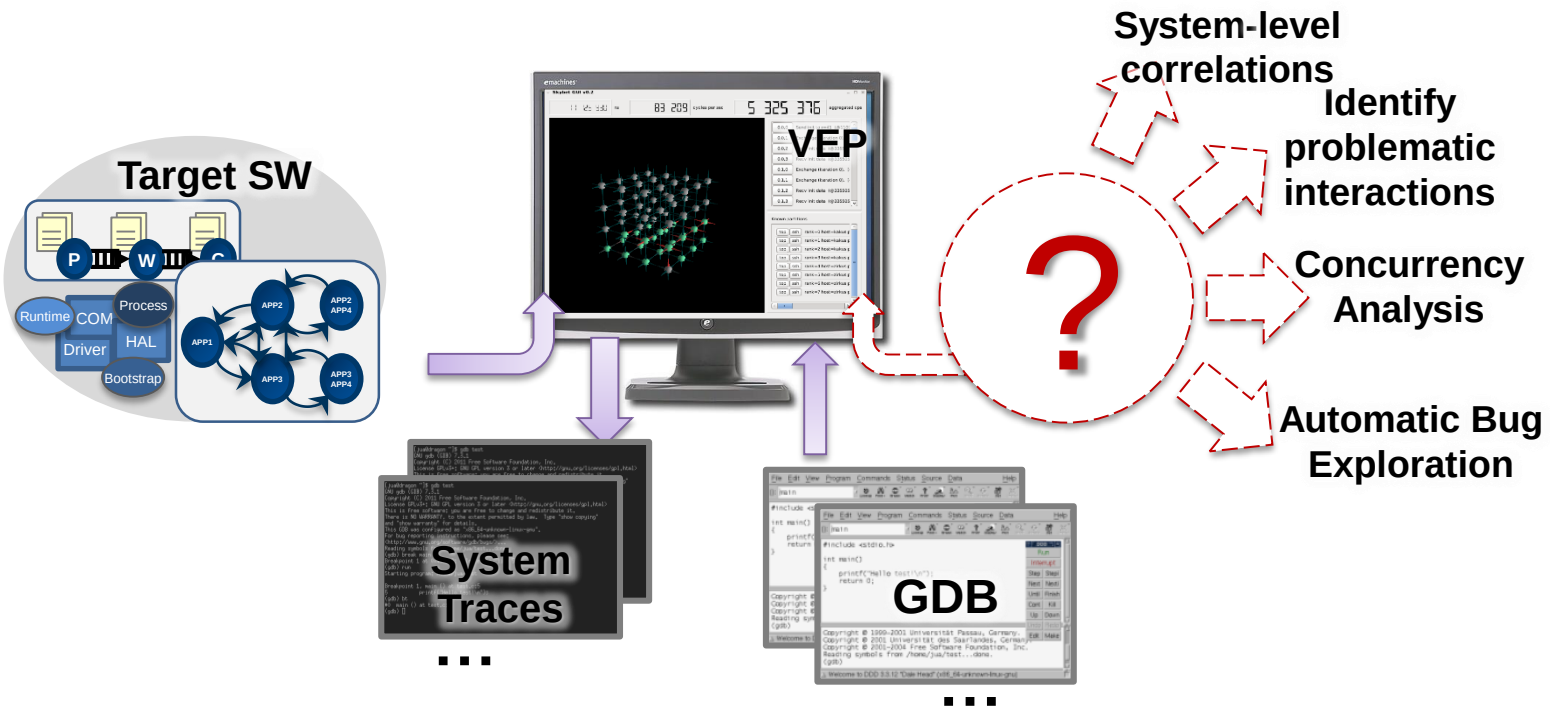
- **VEP Supporting Technologies**
  - Multiple levels of abstraction
  - 2 parallel SystemC kernels
    - parSC (2.2x in quad-core)
    - SCope (4x in quad-core)
  - Distributed SystemC (diSC)
    - Runs on multiple hosts
  - Fault Injection



CA : cycle accurate
IAF : instruction accurate JIT-CC, full
IAP : instruction accurate JIT-CC, plain (no debug)
IAD : instruction accurate, DBT
AED : abstract execution device (host-compiled)

- **Traditional debug augmentations**
  - System loggers: single- or multi-file, tile and component filtering, packets over the network, SW, buses, memories, peripherals…
  - GDB coupling

… but many GDB windows, huge traces…



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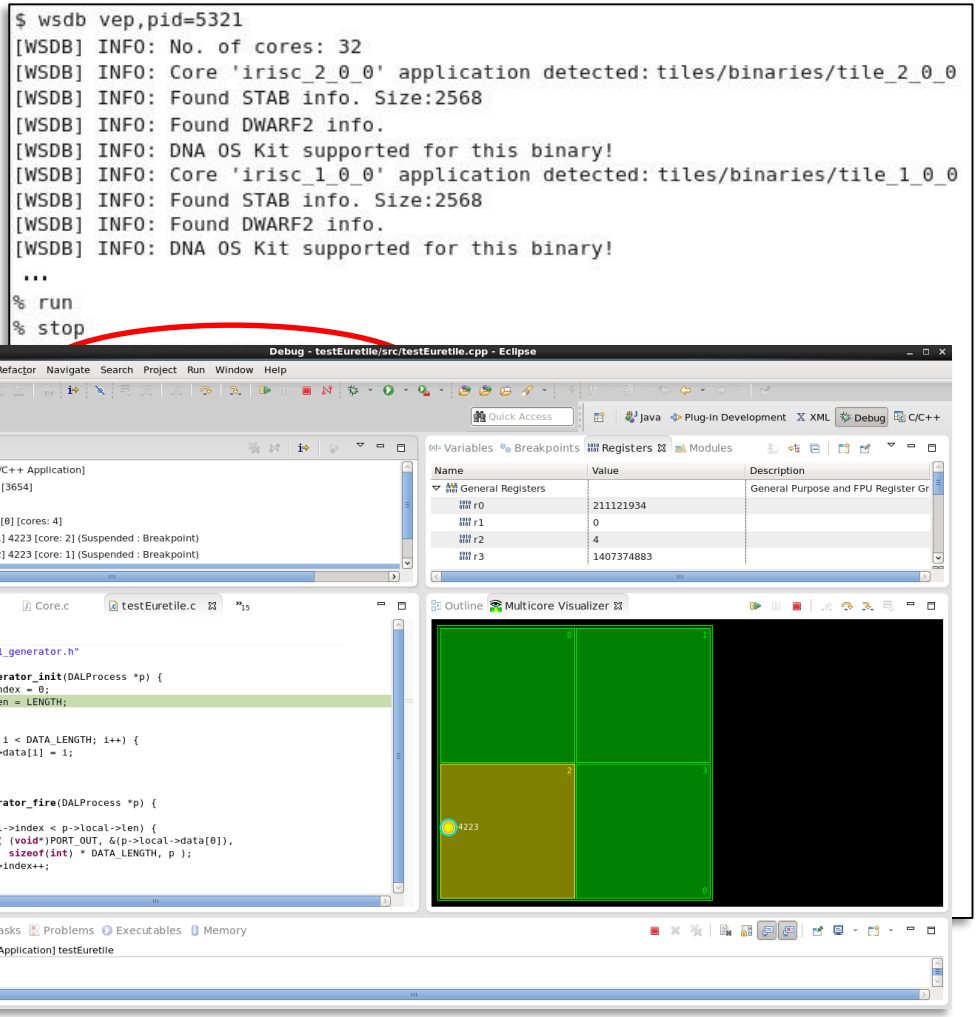
WSDB: Whole-system Debugger

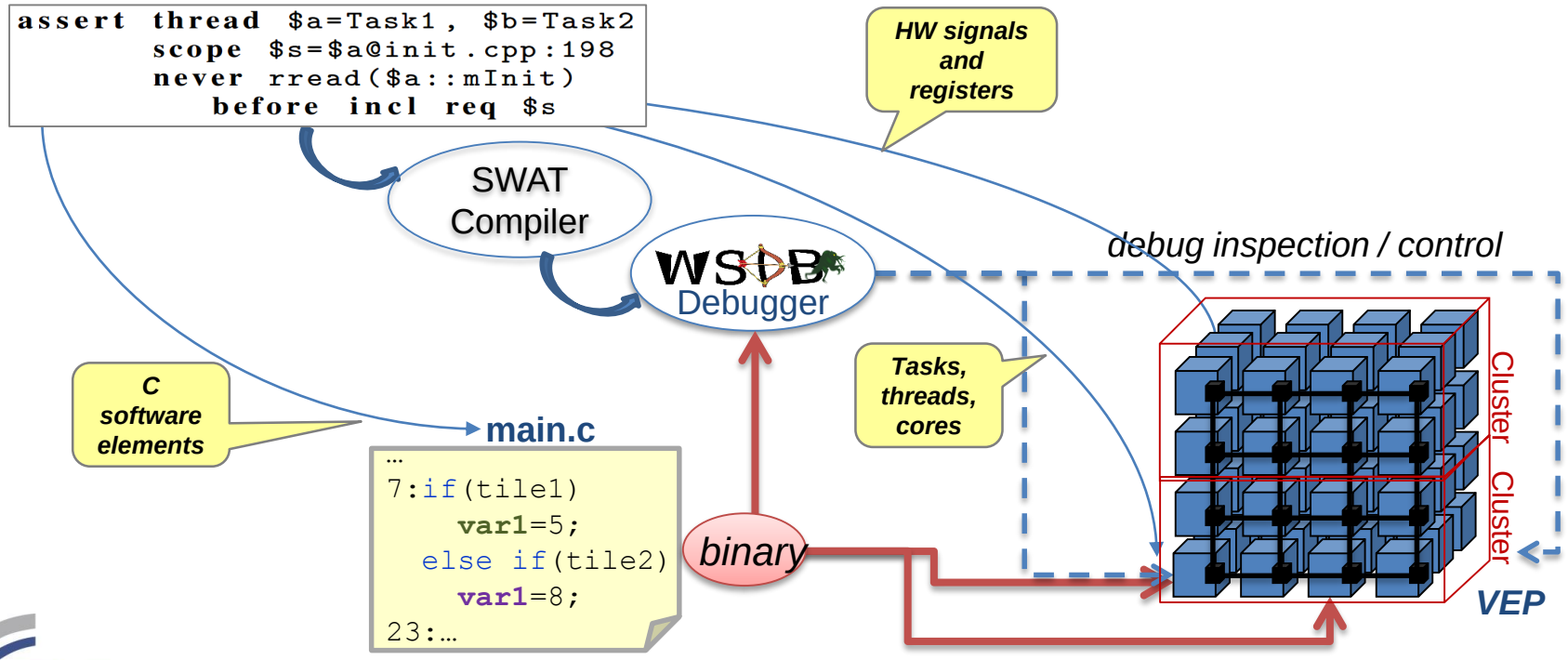
- Source Debugger Back-end
  - Single interface for:
    - Inspection/control of multiple cores
    - Different targets, core ABIs, unwinders and OS-trackers
  - Component-based architecture for portability and extensibility
  - C++ and SWIG tcl APIs
  - Command-line interface
  - Network protocol (with Eclipse CDT/DSF plug-in)
  - Can be linked into the VP



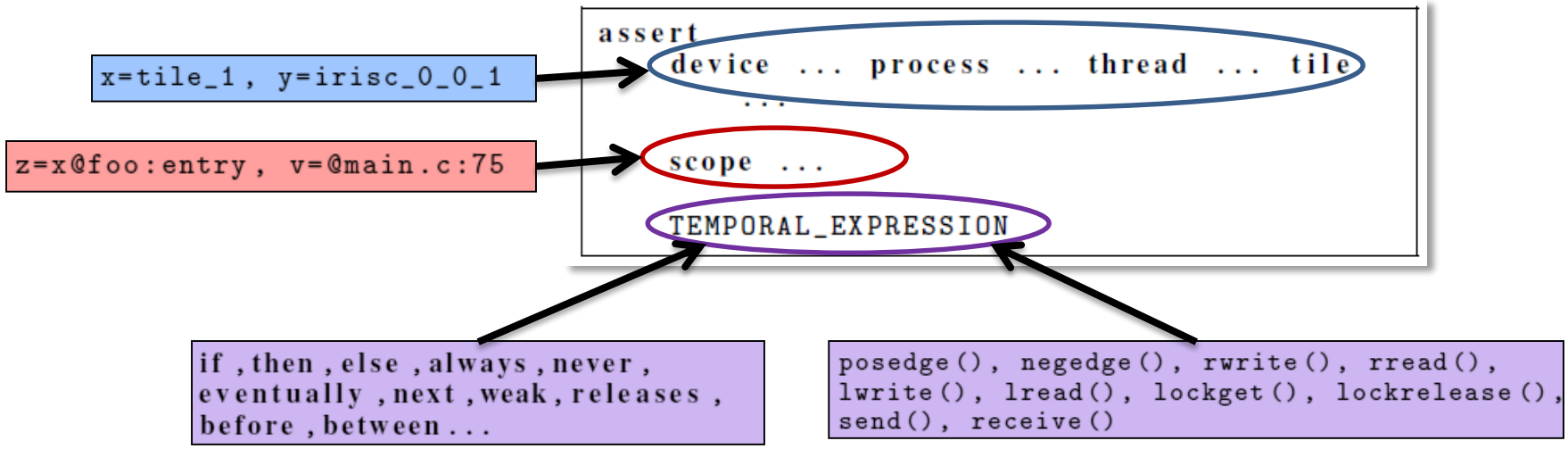
SWAT: Language for System-Wide Assertions

- Multi-tile program analysis, concurrency and HW/SW bugs
- Easy way to capture user knowledge, covering:
  - → SW contexts (*thread*, *process*), variables
  - → HW *devices*, signals, registers
  - → Concurrency-related *events* (e.g., OS events)
  - → Linear Temporal Logic (LTL)

… in a single non-intrusive assertion!



The SWAT Language



- Examples

```
assert thread $a=Task1, $b=Task2
       scope $s=$a@init.cpp:198
       never rread($a::mInit)
          before incl req $s
```

```
assert iterator tile it
 scope r = it@irq_mask_and_backup.c:6
       s = it@irq_mask_restore:entry
 always if lwrite( r::irq_stat ) then next s
```

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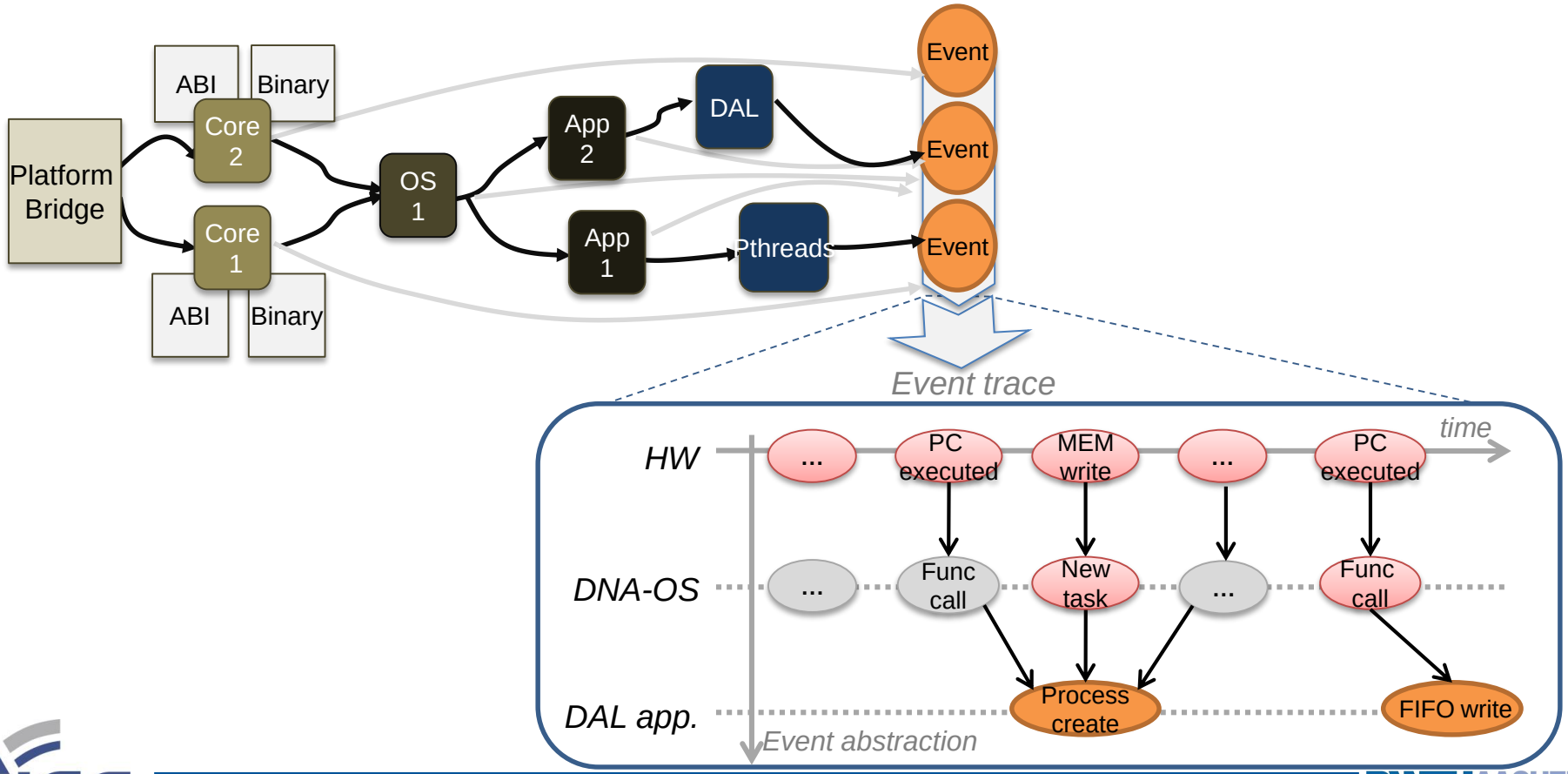
Concurrency Event Monitors

- High-level events for analysis but fully trackable to origins
- Approach
  - Grouping of low level events into programmer-relevant events
  - Propagation of semantic information to higher-level trace

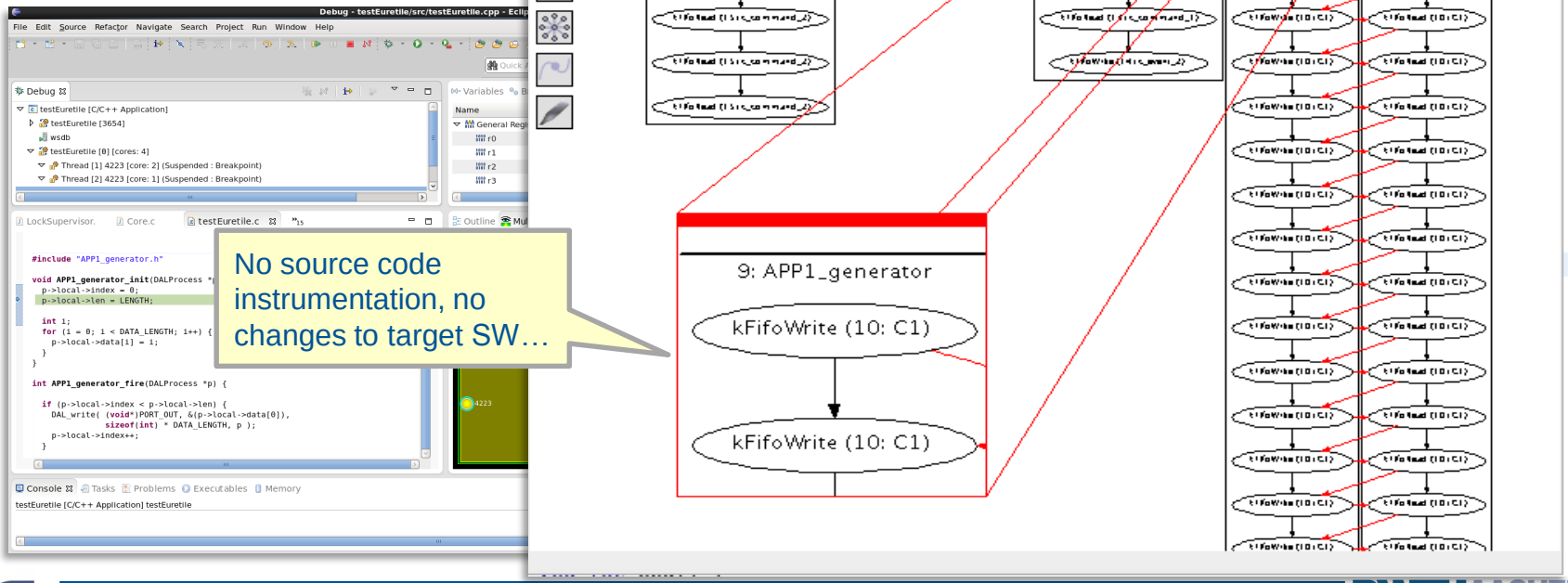


Concurrency Analysis: Ordering Constraints Detection

- High-level trace reveals the order of dependent events
- Analyzes: happens-before, shared resource (visit/modify), dependency, domination, false-dependency
- Bug Exploration: ordering constraint swap

- Drawback:
  - VP slowdown
  - ~2x-30x for the VEP

Example:
* 2016 High-level events
* 2,3x slowdown



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Conclusions

- **Debuggers for multi-tile systems:**
  - Facilitate intuitive ways to deal with problems at system-level
  - Present information to developer at the right abstraction
  - Consider different concurrent interleavings

- **EURETILE's debugging infrastructure:**
  - Virtual Platform in the loop
  - Debugger able to control/inspect all the tiles and correlate inter-tile data
  - Framework for non-intrusive system-wide assertions
  - Programmer-level (DAL) monitoring framework with concurrency analysis

Thanks!
&
Questions?

References

- L. G. Murillo, R. Buecs, R., D. Hincapie, R. Leupers, and G. Ascheid, SWAT: Assertion-based Debugging of Concurrency Issues at System Level, in ASP-DAC'15, Chiba/Tokyo, Japan, Jan. 2015, (accepted for publication)
- L. G. Murillo, R. Buecs, D. Hincapie, R. Leupers and G. Ascheid, Assertion-based Debugging of Concurrency Issues in Many-core Systems across HW/SW Boundaries, in DAC'14 WIP, June 2014, San Francisco, USA.
- L. Schor, I. Bacivarov, L. G. Murillo, et.al., "EURETILE Design Flow: Dynamic and Fault Tolerant Mapping of Multiple Applications onto Many-Tile Systems", in ISPA'14, , Aug. 2014, Milan, Italy.
- L. G. Murillo, S. Wawroschek, J. Castrillon, R. Leupers and G. Ascheid: "Automatic Detection of Concurrency Bugs through Event Ordering Constraints", in DATE'14, Mar. 2014, Dresden, Germany
- J. H. Weinstock, C. Schumacher, R. Leupers, et.al.,"Time-Decoupled Parallel SystemC Simulation" in DATE'14, , Mar. 2014, Dresden, Germany
- C. Schumacher, J. H. Weinstock, R. Leupers, et.al. legaSCi: Legacy SystemC Model Integration into Parallel Simulators. ACM Transactions on Embedded Computing Systems. 2013
- L. Schor, H. Yang, I. Bacivarov and L. Thiele. Expandable Process Networks to Efficiently Specify and Explore Task, Data, and Pipeline Parallelism. In CASES'13, Montreal, Canada, Oct. 2013
- Roberto Ammendola, et.al. "Design and implementation of a modular, low latency, fault-aware, FPGA-based Network Interface" in ReConFig 2013
- Paolucci, P.S., Bacivarov, I., Goossens, G., Leupers, R., Rousseau, F., Schumacher, C., Thiele, L., Vicini, P., "EURETILE 2010-2012 summary: first three years of activity of the European Reference Tiled Experiment.", (2013)
- C. Schumacher, J. H. Weinstock, R. Leupers and G. Ascheid. Cause and effect of nondeterministic behavior in sequential and parallel SystemC simulators. In HLDVT'12, Nov 2012, Huntington Beach (California-USA)
- L. Schor, I. Bacivarov, D. Rai, H. Yang, S.-H. Kang, and L. Thiele. Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems. In CASES'12, Tampere, Finland, p. 71-80, Oct. 2012.
- A. Chagoya-Garzon, F. Rousseau, F. Pétrot. Multi-Device Driver Synthesis Flow for Heterogeneous Hierarchical Systems. Euromicro Conference on Digital System Design, Sept 2012, Izmir, Turkey.
- L. G. Murillo, J. Harnath, R. Leupers and G. Ascheid. Scalable and Retargetable Debugger Architecture for Heterogeneous MPSoCs. System, Software, SoC and Silicon Debug Conference (S4D '12), Sep 2012, Vienna Austria
- L. G. Murillo, W. Zhou, J. Eusse, R. Leupers, G. Ascheid. Debugging Concurrent MPSoC Software with Bug Pattern Descriptions. System, Software, SoC and Silicon Debug Conference (S4D '11), Oct 2011, Munich (Germany)
- C. Schumacher, R. Leupers, D. Petras and A. Hoffmann. parSC: Synchronous Parallel SystemC Simulation on Multi-Core Host Architectures. In CODES/ISSS '10, October, 2010, Scottsdale, Arizona, USA
- X. Guerin and F. Petrot, A System Framework for the Design of Embedded Software Targeting Heterogeneous Multi-core SoCs,º in ASAP 2009