Lab 09 : Single Cycle Processor and Control Unit

Name:

Sign the following statement:

On my honor, as an Aggie, I have neither given nor received unauthorized aid on this academic work

1   Objective

The objective of this lab is to implement the main control unit and integrate it with the data path, to build a complete, single-cycle processor microarchitecture.

2   Pre-requisite

For this lab you are expected to be familiar with the MIPS single-cycle processor from the textbook microarchitecture.

3   Introduction

In this lab, you will complete the control unit for the single-cycle MIPS processor and assemble all of the datapath components constructed in previous labs using Verilog. You will also execute some test programs on your single-cycle processor. By the end of this lab, you should thoroughly understand the internal operation of the MIPS single-cycle processor.

4 Processor

This version of MIPS implements the single-cycle processor given in Figure 1 and supports the following instructions: `add`, `sub`, `and`, `or`, `slt`, `lw`, `sw`, `beq`, and `j` as well as many of their immediate equivalents. The instruction formats are the same as the real MIPS instruction set.

Our model of the single-cycle MIPS processor divides the machine into two major units: the control and the data path. You have already built many of the datapath components such as the ALU, the data memory, the sign extender, etc.
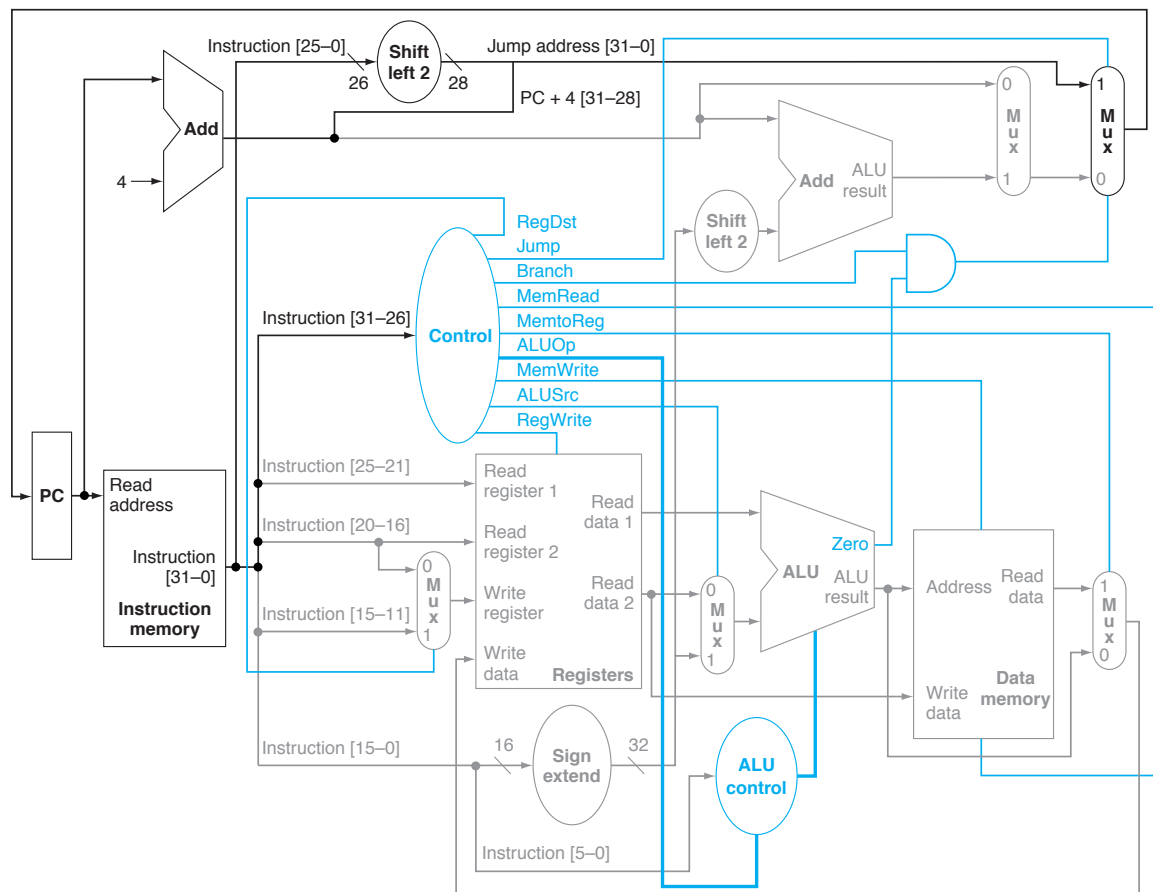

Fig. 1: MIPS schematic

You have also built the ALU control module that is needed for this version of the MIPS processor. You are provided with the instruction memory (read only), which is pre-initialized with test programs. Your task is to complete the Main Control unit, connect all

modules together, and simulate the code.

5 Control Unit

Complete the control unit Verilog code found in `SingleCycleControl.v` for the data path shown in Figure 1 that supports R-type, load/store word, immediate, branch and jump instructions. All opcodes that you must implement are defined above the module definition. Your control unit should be implemented based on the truth table that you filled during the prelab.
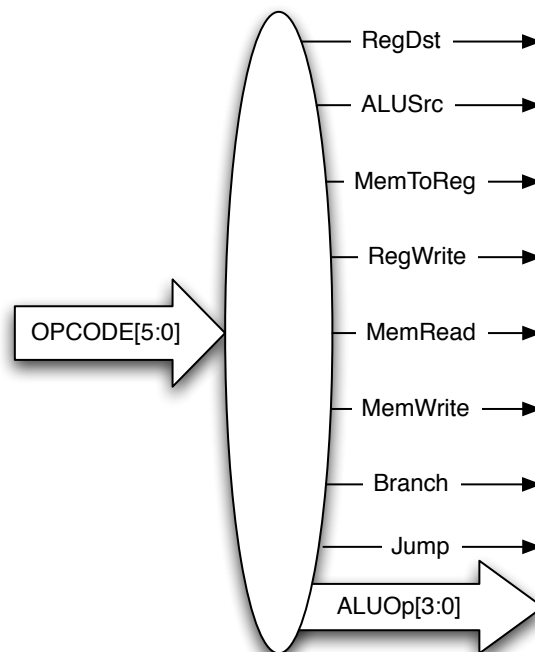

Fig. 2: Main Control Unit

6 The Datapath

The provided `SingleCycleProc.v` module partially implements the single cycle processor. You will need complete this code and ensure that all connections are properly made. The comments in the code will provide hints as to what is missing.

7   Diagnostic and Testing

Your code should simulate properly with the test programs provided. Each program tests different parts of your processor. Ensure proper operation of each test and make any necessary corrections to your code. Once all tests have successfully completed, demo your progress to the TA.

8   Questions

1. In `SingleCycleProcTest.v`, the clock Period is defined by the macro `HalfClockPeriod`. Try changing this value. What is the smallest value for which the processor does not fail tests?

2. Considering the delays in your datapath and control unit, what is the maximum clock speed for your design? List the components which are part of the critical path and which instructions utilize the critical path.

3. In what ways is this design inefficient? How would you improve it?

4. Briefly describe what each of the test programs do and what instructions they might be testing.

9   Deliverables

Please turn-in the following:

- All of your verilog modules.

- Results of the testbench.

- Filled out PDF form.