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library IEEE;
use IEEE.STD LOGIC 1164.ALL;
entity decoder_5_32 is
     Port ( S : in STD_LOGIC_VECTOR (4 downto 0);
           A : out STD LOGIC VECTOR (31 downto 0));
end decoder_5_32;
architecture Behavioral of decoder 5 32 is
A(0) \le \text{not } S(4) and not S(3) and not S(2) and not S(1) and not S(0) after 1 ns;
A(1) \leftarrow \text{not } S(4) \text{ and not } S(3) \text{ and not } S(2) \text{ and not } S(1) \text{ and } S(0) \text{ after } 1 \text{ ns};
A(2) \le \text{not } S(4) and not S(3) and not S(2) and S(1) and not S(0) after 1 ns;
A(3) \le not S(4) and not S(3) and not S(2) and S(1) and S(0) after 1 ns;
A(4) \leftarrow \text{not } S(4) \text{ and not } S(3) \text{ and } S(2) \text{ and not } S(1) \text{ and not } S(0) \text{ after } 1 \text{ ns};
A(5) \le \text{not } S(4) \text{ and not } S(3) \text{ and } S(2) \text{ and not } S(1) \text{ and } S(0) \text{ after } 1 \text{ ns};
A(6) \le not S(4) and not S(3) and S(2) and S(1) and not S(0) after 1 ns;
A(7) \le \text{not } S(4) \text{ and not } S(3) \text{ and } S(2) \text{ and } S(1) \text{ and } S(0) \text{ after } 1 \text{ ns};
A(8) \le not S(4) and S(3) and not S(2) and not S(1) and not S(0) after 1 ns;
A(9) \leftarrow \text{not } S(4) \text{ and } S(3) \text{ and not } S(2) \text{ and not } S(1) \text{ and } S(0) \text{ after } 1 \text{ ns};
A(10) \le not S(4) and S(3) and not S(2) and S(1) and not S(0) after 1 ns;
A(11) \le \text{not } S(4) \text{ and } S(3) \text{ and not } S(2) \text{ and } S(1) \text{ and } S(0) \text{ after } 1 \text{ ns};
A(12) \leftarrow \text{not } S(4) \text{ and } S(3) \text{ and } S(2) \text{ and not } S(1) \text{ and not } S(0) \text{ after } 1 \text{ ns};
A(13) \leftarrow \text{not } S(4) \text{ and } S(3) \text{ and } S(2) \text{ and not } S(1) \text{ and } S(0) \text{ after } 1 \text{ ns};
A(14) \leftarrow S(4) and S(3) and S(2) and S(1) and not S(0) after 1 ns;
A(15) \le not S(4) and S(3) and S(2) and S(1) and S(0) after 1 ns;
A(16) \leftarrow S(4) and not S(3) and not S(2) and not S(1) and not S(0) after 1 ns;
A(17) \le S(4) and not S(3) and not S(2) and not S(1) and S(0) after 1 ns;
A(18) \le S(4) and not S(3) and not S(2) and S(1) and not S(0) after 1 ns;
A(19) \le S(4) and not S(3) and not S(2) and S(1) and S(0) after 1 ns;
A(20) \leftarrow S(4) and not S(3) and S(2) and not S(1) and not S(0) after 1 ns;
A(21) \le S(4) and not S(3) and S(2) and not S(1) and S(0) after 1 ns;
A(22) \le S(4) and not S(3) and S(2) and S(1) and not S(0) after 1 ns;
A(23) \le S(4) and not S(3) and S(2) and S(1) and S(0) after 1 ns;
A(24) \leftarrow S(4) and S(3) and not S(2) and not S(1) and not S(0) after 1 ns;
A(25) \leftarrow S(4) and S(3) and not S(2) and not S(1) and S(0) after 1 ns;
A(26) \le S(4) and S(3) and not S(2) and S(1) and not S(0) after 1 ns;
A(27) \le S(4) and S(3) and not S(2) and S(1) and S(0) after 1 ns;
A(28) \le S(4) and S(3) and S(2) and not S(1) and not S(0) after 1 ns;
A(29) \le S(4) and S(3) and S(2) and not S(1) and S(0) after 1 ns;
A(30) \le S(4) and S(3) and S(2) and S(1) and not S(0) after 1 ns;
A(31) \le S(4) and S(3) and S(2) and S(1) and S(0) after 1 ns;
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end Behavioral: