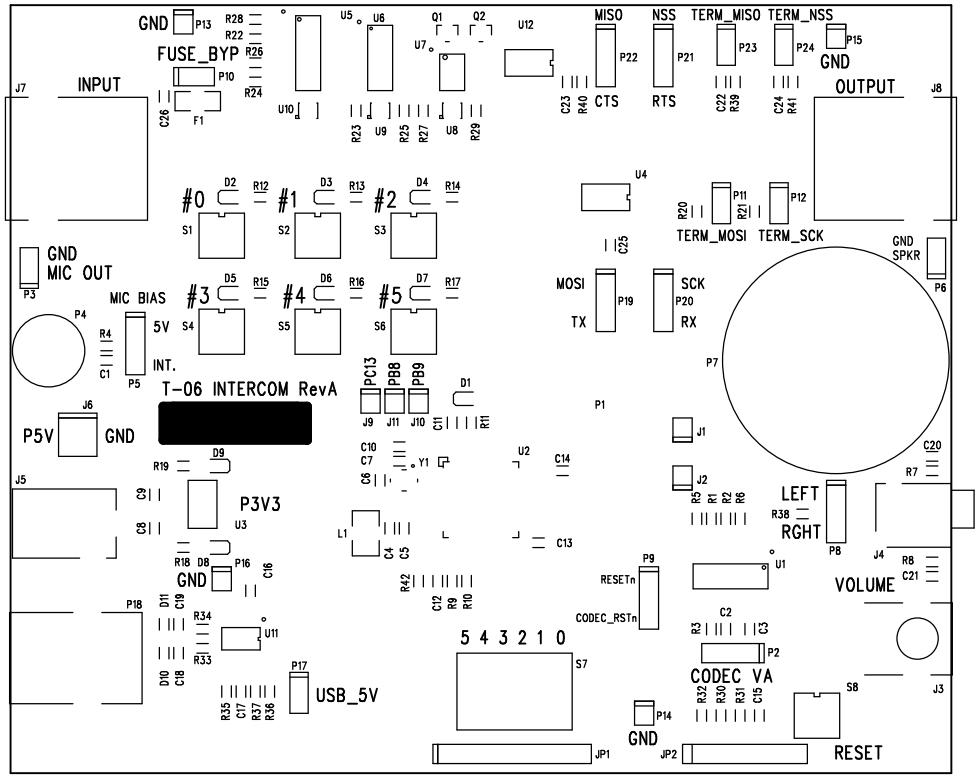

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PRIMARY SIDE SILK SCREEN

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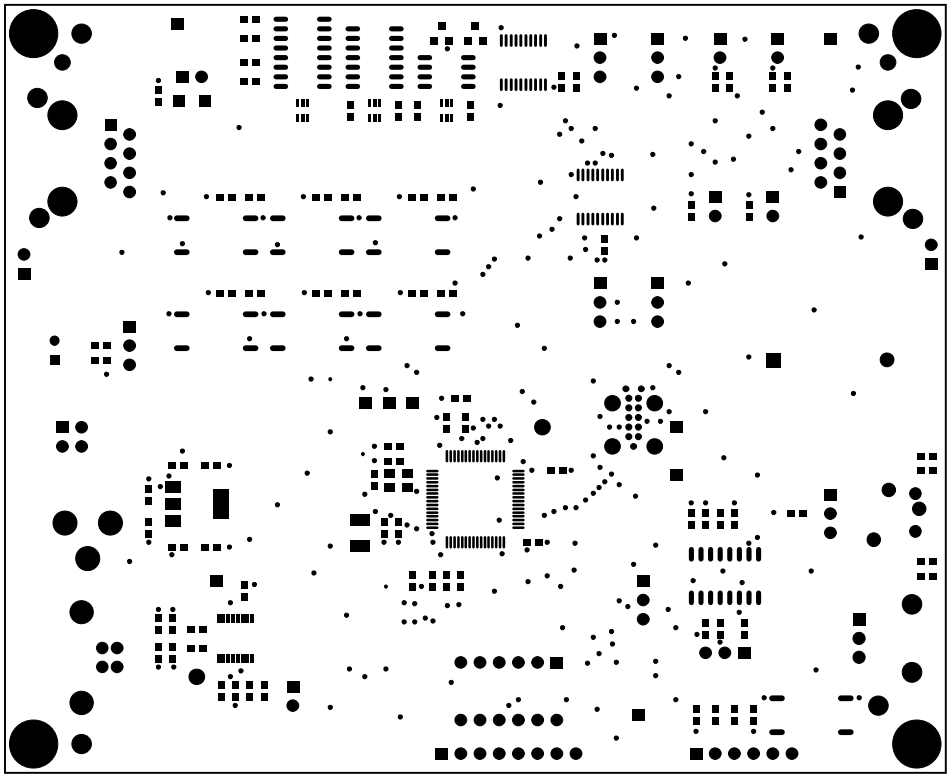

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PRIMARY SIDE SOLDER MASK

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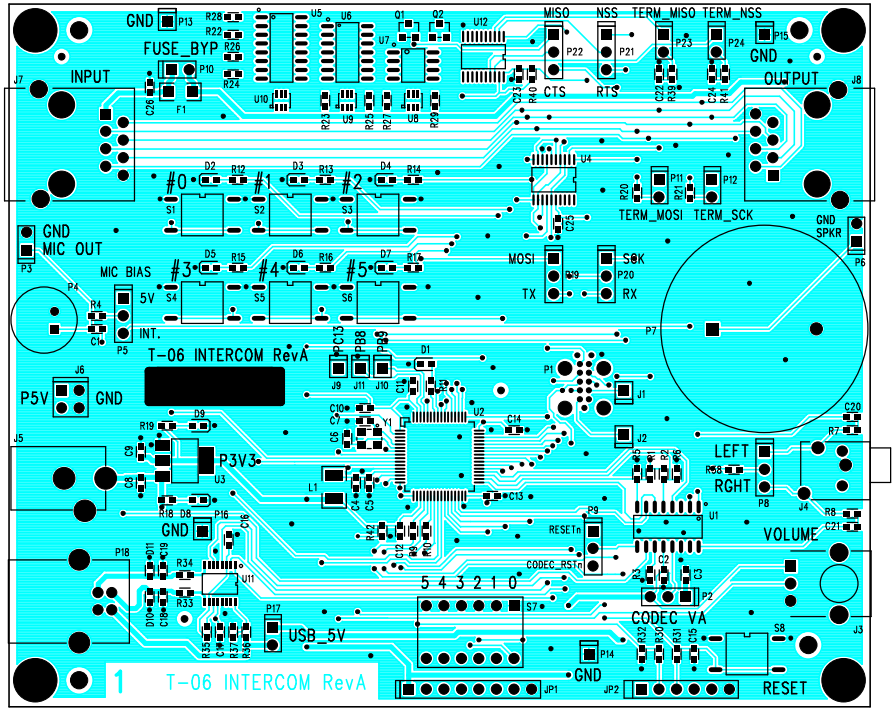

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PRIMARY SIDE SILK SCREEN

PRIMARY SIDE (LAYER 1)

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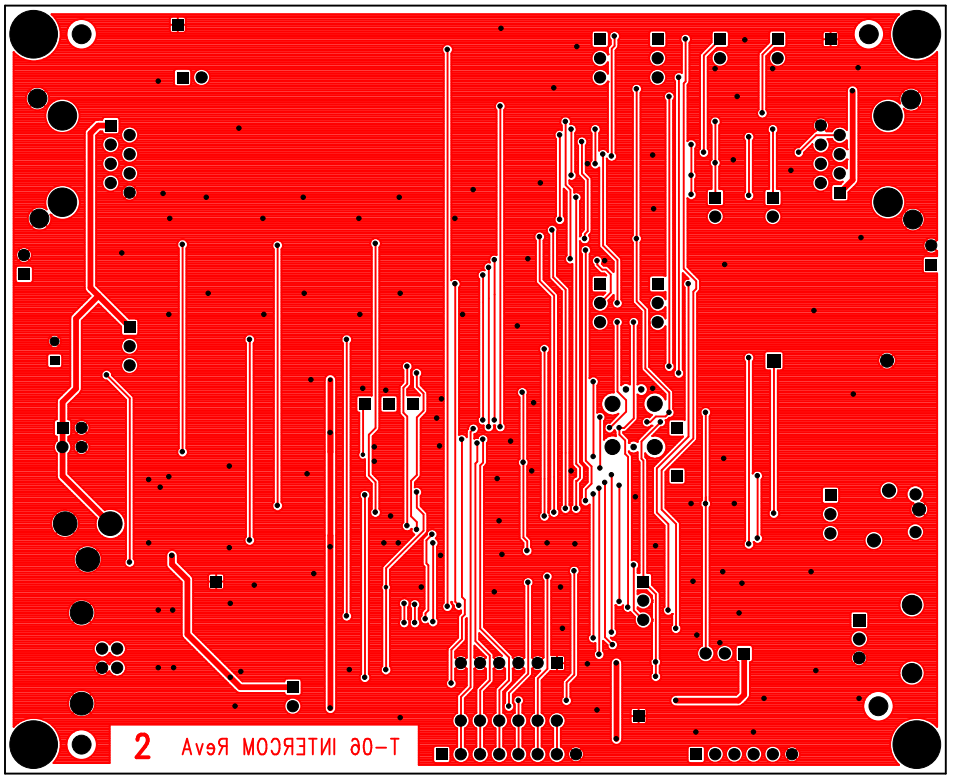

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SECONDARY SIDE (LAYER 2)

SECONDARY SIDE SILK SCREEN

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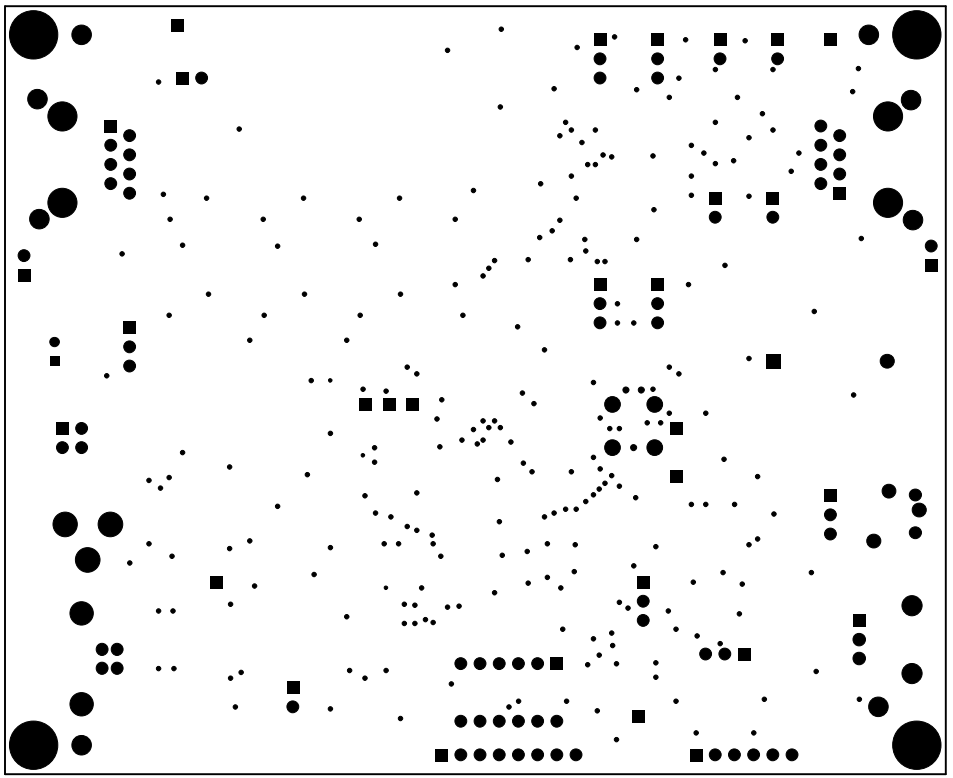

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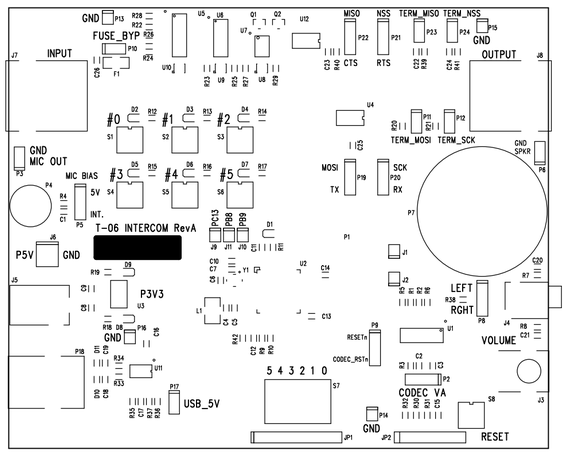
SECONDARY SIDE SOLDER MASK

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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INTERCOM RevA
PRIMARY SIDE SILK SCREEN

PRIMARY SIDE

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DRAWN: Tyler Seitz	DATED: 11/16/2016	
CHECKED:	DATED:	
QUALITY CONTROL:	DATED:	
RELEASED:	DATED:	

COMPANY: T-06 @ Portland State University
1930 SW 4th Ave #500
PORTLAND, OR 97201
PHONE: (503) 547-4784

TITLE: ASSY, INTERCOM

CODE:	SIZE:	DRAWING NO:	REV:
	C		A

SCALE:

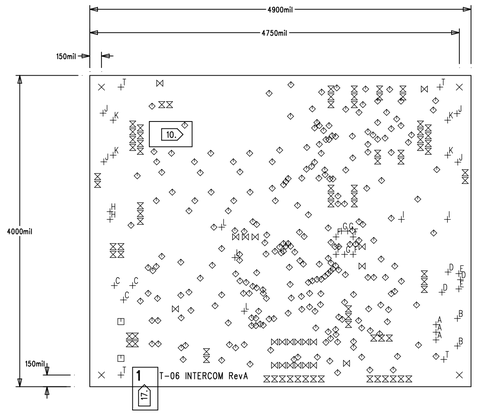
SHEET: 1 OF 2

REVISIONS				
LTR	DESCRIPTION	DATE	DR	APPROVED

PCB FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

1. PRIMARY SIDE SHOWN.
2. TWO LAYER PCB
3. FABRICATE PER IPC-6012, CLASS 2, CURRENT REV.
   PCB SHALL BE RoHS COMPLIANT.
4. DETERMINE ACCEPTABILITY PER IPC-A-600, CURRENT REV.
   25% BREAKOUT PERMITTED ON VIAS IF INTERFACE
   BETWEEN CONDUCTOR AND TERMINAL AREA OF PAD IS 100%.

   BOARDS TO BE 100% ELECTRICALLY TESTED FOR CONTINUITY
   (OPENS AND SHORTS).
   CERTIFICATION OF THIS TEST REQUIRED
   WITH EACH SHIPMENT FOR EACH DATE CODE SUPPLIED. CERTIFICATION TO
   INCLUDE THE MOVING PIXEL P.O. #, P/N, AND QUANTITY OF EACH DATE CODE.
5. MATERIAL PER MIL-P-13949, CURRENT REV. USE 0.062" +/-10%
   THICK 170Tg FR408. BOARD TO BE
   MEASURED OUTER METAL-TO-METAL THICKNESS.
6. PLATE TO 1.0 OZ COPPER NOMINAL ON SURFACE LAYERS, 1.0 OZ
   COPPER NOMINAL IN HOLES AND INTERIOR LAYERS IF PRESENT.
   MINIMUM COPPER THICKNESS ANYWHERE ON BOARD IS 0.0006".
7. TOOLING HOLES OF DIAMETER UP TO 0.126" ARE NON-PLATED AND MAY
   OR MAY NOT BE PRESENT IN DESIGN AS PER SUPPLIED ARTWORK.
   IF PRESENT IN DESIGN THEY SHALL BE MARKED "T". ALL OTHER HOLES
   SHALL BE PLATED OR NON-PLATED ACCORDING TO HOLE CHART.
8. HOLE SIZES GIVEN ARE FINISHED DIMENSIONS.
9. SOLDERMASK BOTH SIDES OVER BARE COPPER PER IPC-SM-840,
   CLASS 2, CURRENT REV, AND MANUFACTURERS SPECIFICATIONS.
   NO BARE COPPER ALLOWED. NO SOLDER MASK
   PERMISSIBLE ON COMPONENT PADS AS PER SUPPLIED ARTWORK.
   SURFACE FINISH: ENIG
10. DATE CODE, UL RECOGNIZED VENDOR MARK, AND UL94V-0 MARK REQUIRED.
    DATE CODE SHALL USE FOUR NUMERALS, GIVING WORK WEEK
    AND YEAR, EG., 2814 STANDS FOR THE 28TH WEEK OF 2014.
    THESE MARKS SHALL BE MADE IN COPPER AND SHALL BE LOCATED
    ON THE SECONDARY SIDE OF THE PCB.
11. SCREEN COMPONENT ID WITH NON-CONDUCTING WHITE INK.
    COMPONENT ID REGISTRATION TO BE WITHIN +/- 0.005" OF ITS
    RESPECTIVE COMPONENT LAYER.
    NO SILKSCREEN INK PERMISSIBLE ON COMPONENT PADS
    OR IN PADS AS PER SUPPLIED ARTWORK.
12. ETCH TOLERANCE +0.001" - 0.002". TOTAL TRACE REDUCTION
    CANNOT EXCEED 20%.
13. FRONT-TO-BACK REGISTRATION TO BE WITHIN +/-0.005".
14. BOARD WARP TO BE NO GREATER THAN 2.0%.
15. LAYER CONFIGURATION DIAGRAM:
    PRIMARY SIDE COMPONENT I.D.
    PRIMARY SIDE SOLDER MASK
    CIRCUIT LAYER #1 (PRIMARY SIDE)
    CIRCUIT LAYER #2 (SECONDARY SIDE)
    SECONDARY SIDE SOLDER MASK
    SECONDARY SIDE COMPONENT I.D.
16. THIEVING PERMITTED. MAINTAIN 0.050" MINIMUM CLEARANCE TO COPPER FEATURES
    IN SUPPLIED GERBER FILES.
17. THIEVING NOT PERMITTED OVER LAYER ID.
18. SOLDERMASK TO BE GREEN IN COLOR.



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INTERCOM RevA

PRIMARY SIDE (LAYER 1)

SIZE	QTY	SYM	PLATED	TOL
0.126	4		NO	+/-0.003
0.156	4		YES	+/-0.003
0.09	2		YES	+/-0.003
0.012	244		YES	+0.000/-0.003
0.035	78		YES	+/-0.003
0.04	21		YES	+/-0.003
0.04331	3	A	YES	+/-0.003
0.08268	2	B	YES	+/-0.003
0.062	3	C	YES	+/-0.003
0.05	3	D	YES	+/-0.003
0.063	2	E	YES	+/-0.003
0.093	4		NO	+/-0.003
0.04	3	G	NO	+/-0.003
0.02756	2	H	YES	+/-0.003
0.04921	2		YES	+/-0.003
0.067	4		YES	+/-0.003
0.128	4	K	YES	+/-0.003
0.01	3		YES	+/-0.003

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SOLDER OR PLATING
PLUG ACCEPTABLE IN
HOLES UP TO 0.021"

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCES ARE:
.X +/- 0.03 ANGLES: +/- 1 DEG.
.XX +/- 0.02 HOLES: SEE TABLE
.XXX +/- 0.010

ORIG.	DATE	
DRAWN Tyler Seitz	11/16/2016	
ENGR.		
MFG.		
QA		

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TITLE: PCB, INTERCOM

SIZE		DRAWING NO.	REV
D	SHT 1 OF 1		A

T06-PCB Layout- Interco - Wed Nov 16 23:39:46 2016