

A

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# BRAKING IO

## POD 5

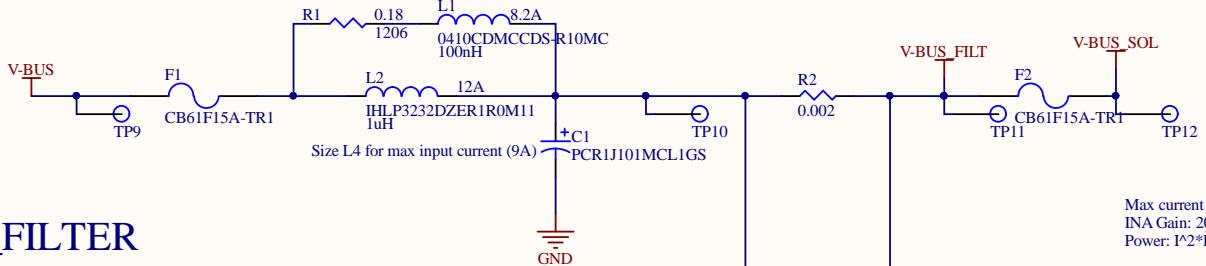
REV 1

Title <b>Braking IO PCB</b>		Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706	
Engineer:	Revision:		
Date: 10/29/2019	Time: 7:05:47 PM	Sheet of	
File: <a href="#">braking_io.SchDoc</a>			

A

A

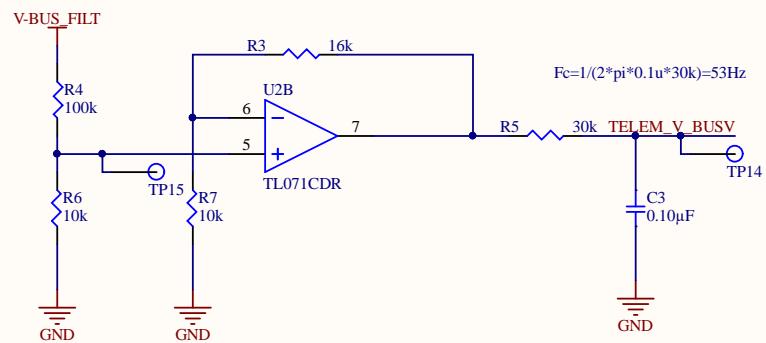
should change upstream fuse to be higher current rating than downstream.



## BUS\_FILTER

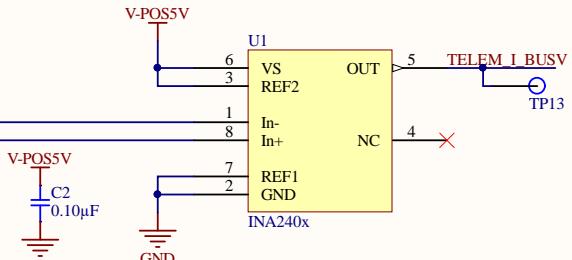
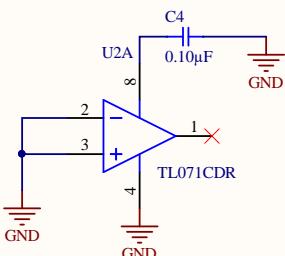
Filter design reference: <http://www.ti.com/lit/an/snva538/snva538.pdf>  
<http://ecee.colorado.edu/~rwe/papers/APEC99.pdf>

Max current draw:  $9A \rightarrow 9A \cdot 0.01\Omega = 0.09V$   
 INA Gain:  $200V/V \rightarrow 4.0V$  at Max current  
 Power:  $I^2 \cdot R = 4A \cdot 0.01 = 0.04W$



GAIN: 1.6V/V  
 MIN BUS VOLTAGE: 20V → 1.82V  
 MAX BUS VOLTAGE: 28V → 2.54V

## VOLTAGE TELEMETRY



## CURRENT TELEM

Max current draw:  $9A \rightarrow 9A \cdot 0.002\Omega = 0.018V$   
 INA Gain:  $200V/V \rightarrow 3.6V$  at Max current  
 Power:  $I^2 \cdot R = 4A \cdot 0.01 = 0.04W$

Title <b>Bus Filter</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 10/29/2019	Time: 7:05:47 PM	1500 Engineering Drive
File: bus_filter.SchDoc		Madison, WI 53706

**BADGER**  
**LOOP**

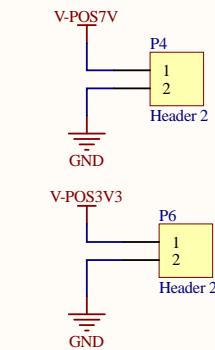
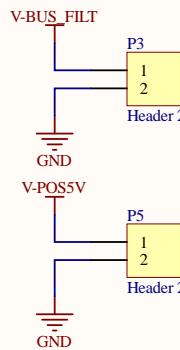
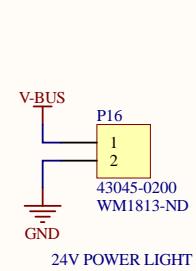
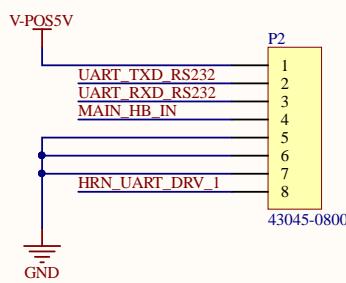
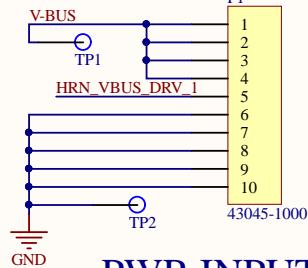
1

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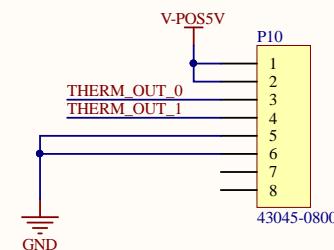
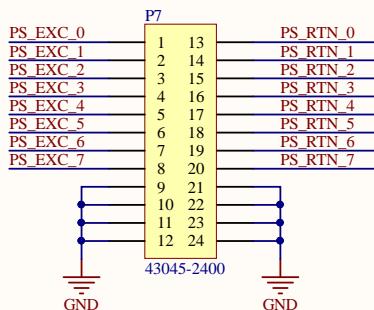
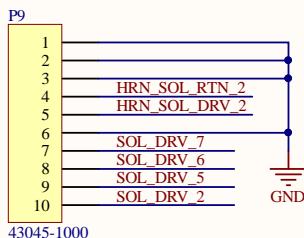
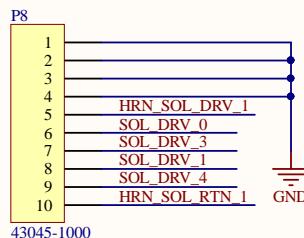
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4

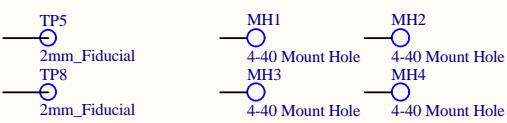
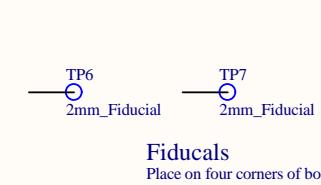
A



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Mount Holes  
Avoid routing under screw head

### Title Connectors

Engineer:	Revision:
Date: 10/29/2019	Time: 7:05:47 PM
File: connectors.SchDoc	Sheet of

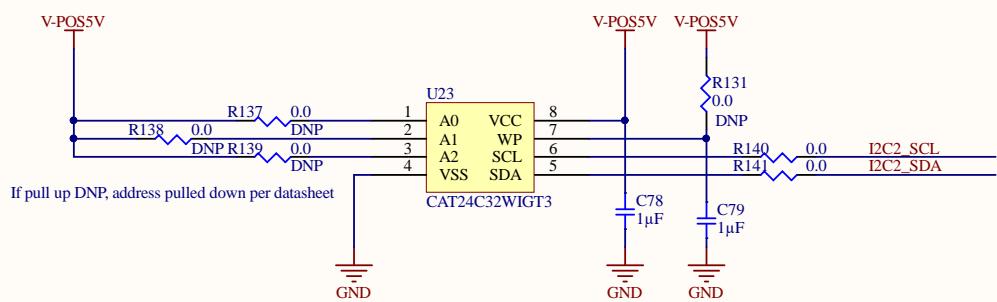
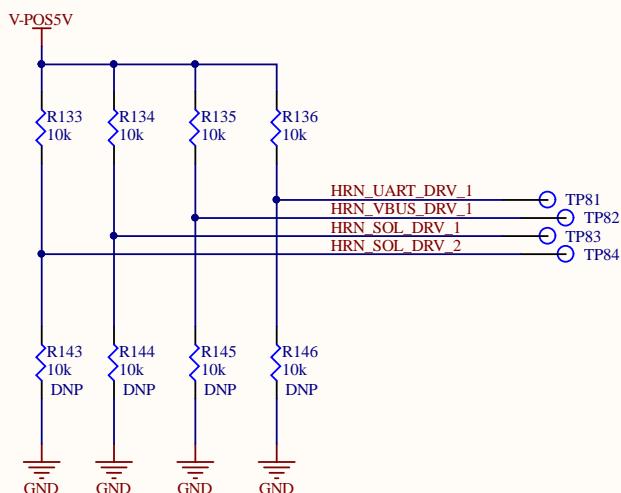
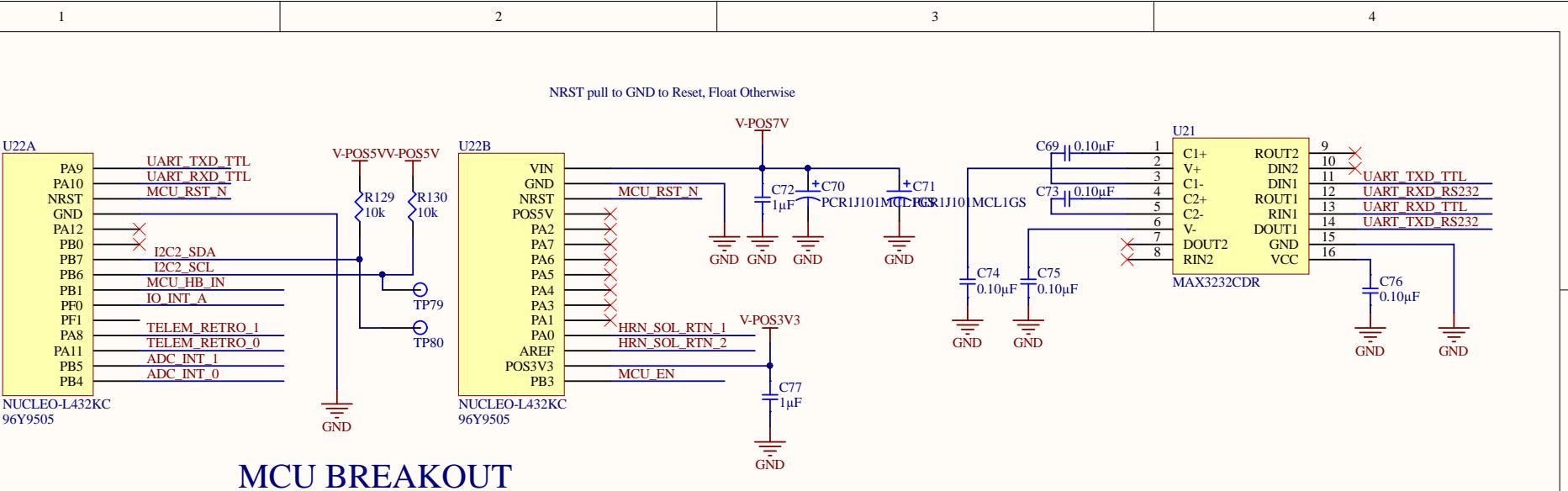
**BADGER**  
**LOOP**

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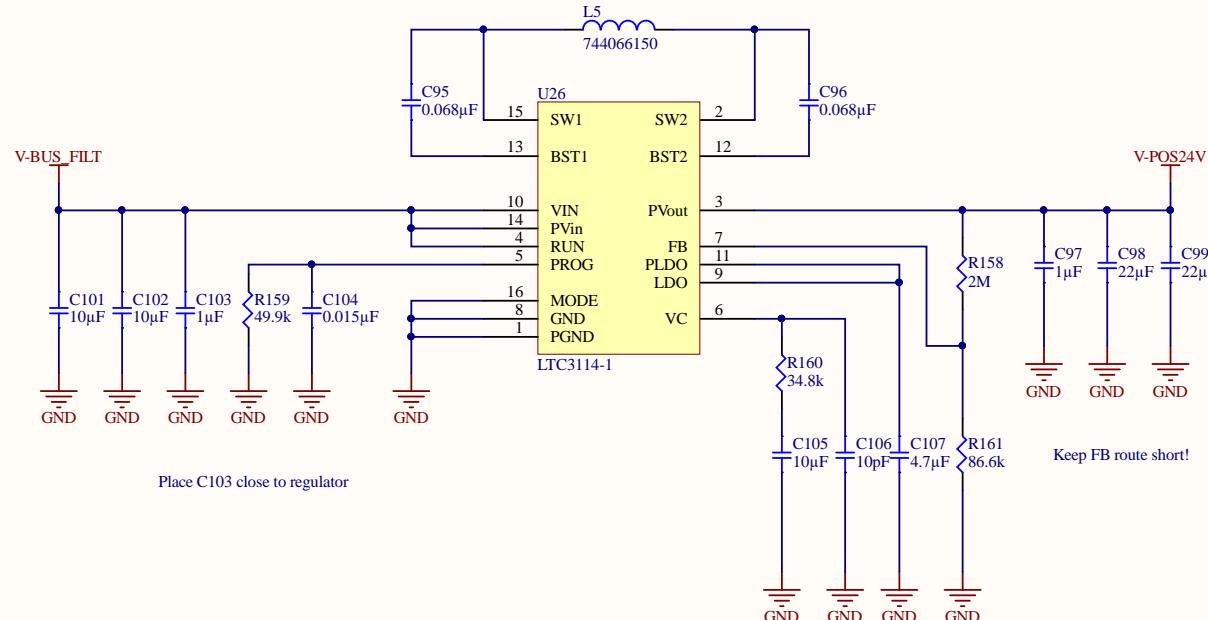


Title <b>Microcontroller</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 10/29/2019	Time: 7:05:47 PM	1500 Engineering Drive
File: mcu.SchDoc		Madison, WI 53706

**BADGER  
LOOP**

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Title **Power 24V**

Badgerloop Electrical  
133 Engineering Research Building  
1500 Engineering Drive  
Madison, Wi 53706



Engineer:	Revision:
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Date: 10/29/2019	Time: 7:05:47 PM
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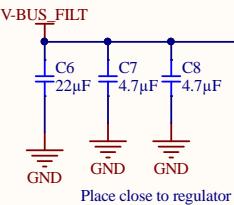
Sheet	of
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File: power_24V.SchDoc
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**A**

Notes:  
Follow layout reference design  
Place bypass caps close to regulator  
Keep hot loops as short as possible  
Possible to replace ceramic bulk cap with a tantalum.

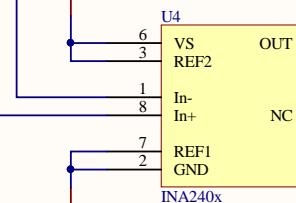
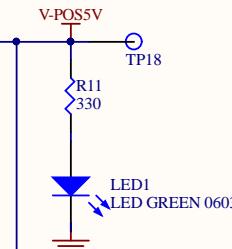
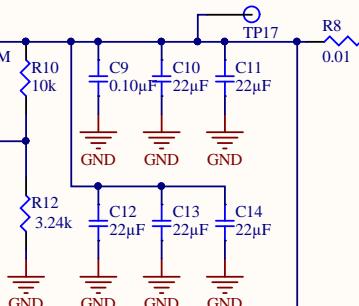
Replace with Tantalum?  
Place close to regulator  
[See https://github.com/badgerloop-software/hardware/tree/master/braking\\_io/design](https://github.com/badgerloop-software/hardware/tree/master/braking_io/design)



## 5V SUPPLY

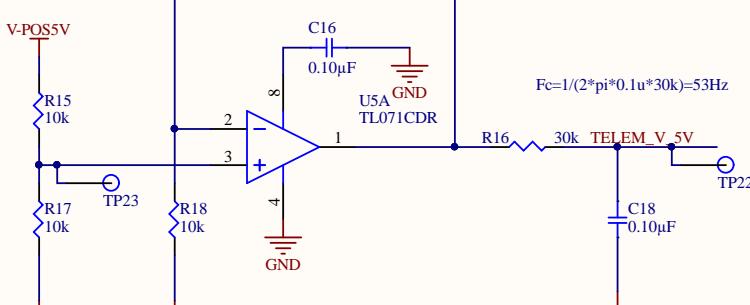
VIN MIN: 8V VIN MAX: 35V  
IOUT MAX: Up to 2A  
 $V_{OUT} = (R_1 * 1.221) * (R_2 + 1.221)$   
 $V_{OUT} = (10K * 1.221) / (3.24K) + 1.221 = 4.989V$  nominal

Keep SNS route short and fat!



## CURRENT TELEMETRY

Max current draw: 2A -> 2A \* 0.01Ohm = 0.02V  
INA Gain: 200V/V -> 4.0V at Max current  
Power:  $I^2 * R = 4A * 0.01 = 0.04W$



## VOLTAGE TELEMETRY

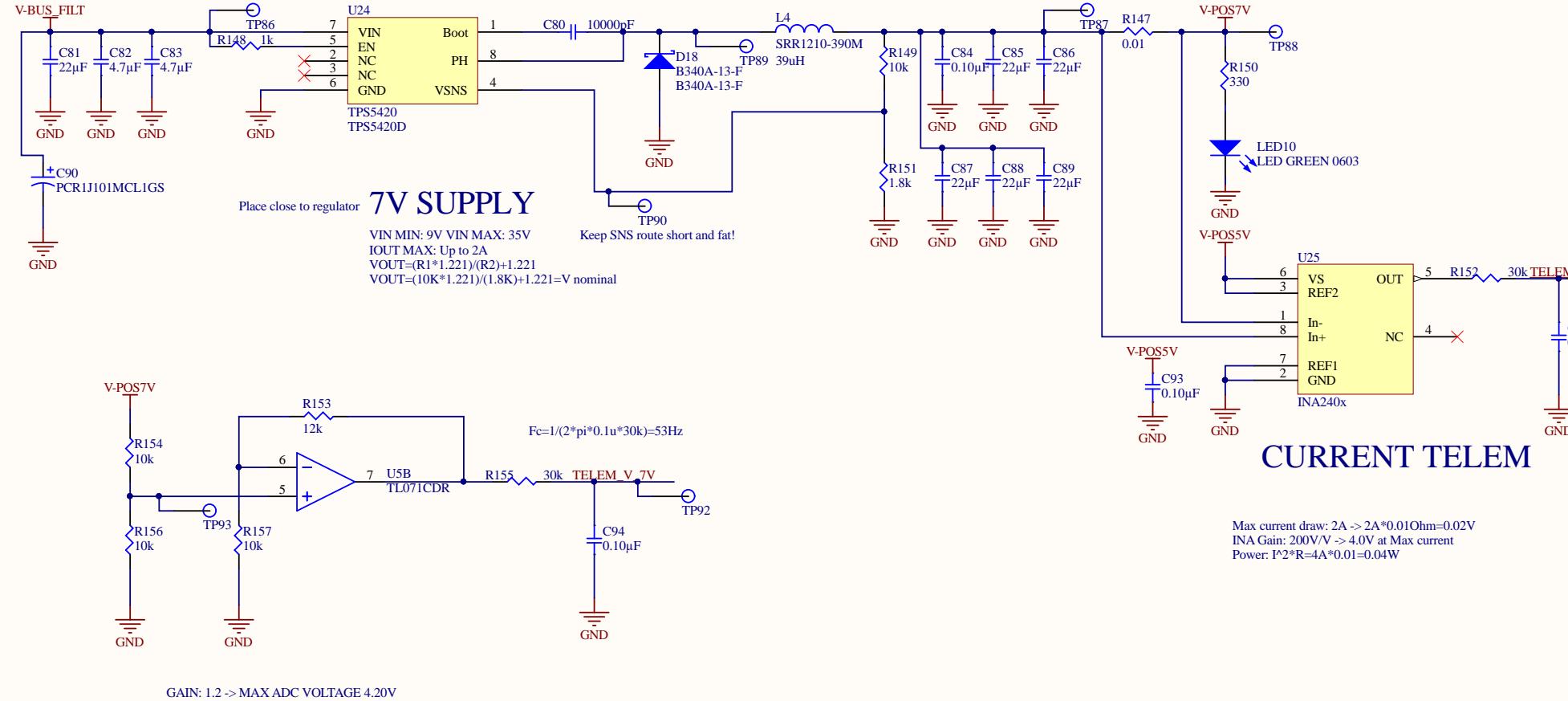
Title	Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706	
Engineer:	Revision:	
Date: 10/29/2019	Time: 7:05:47 PM	Sheet of
File: power_5V.SchDoc		

**BADGER  
LOOP**

A

Notes:  
Follow layout reference design  
Place bypass caps close to regulator  
Keep hot loops as short as possible  
Possible to replace ceramic bulk cap with a tantalum.

Replace with Tantalum?  
Place close to regulator  
See [https://github.com/badgerloop-software/hardware/tree/master/braking\\_io/design](https://github.com/badgerloop-software/hardware/tree/master/braking_io/design)

Title **7V SUPPLY**

Engineer:

Revision:

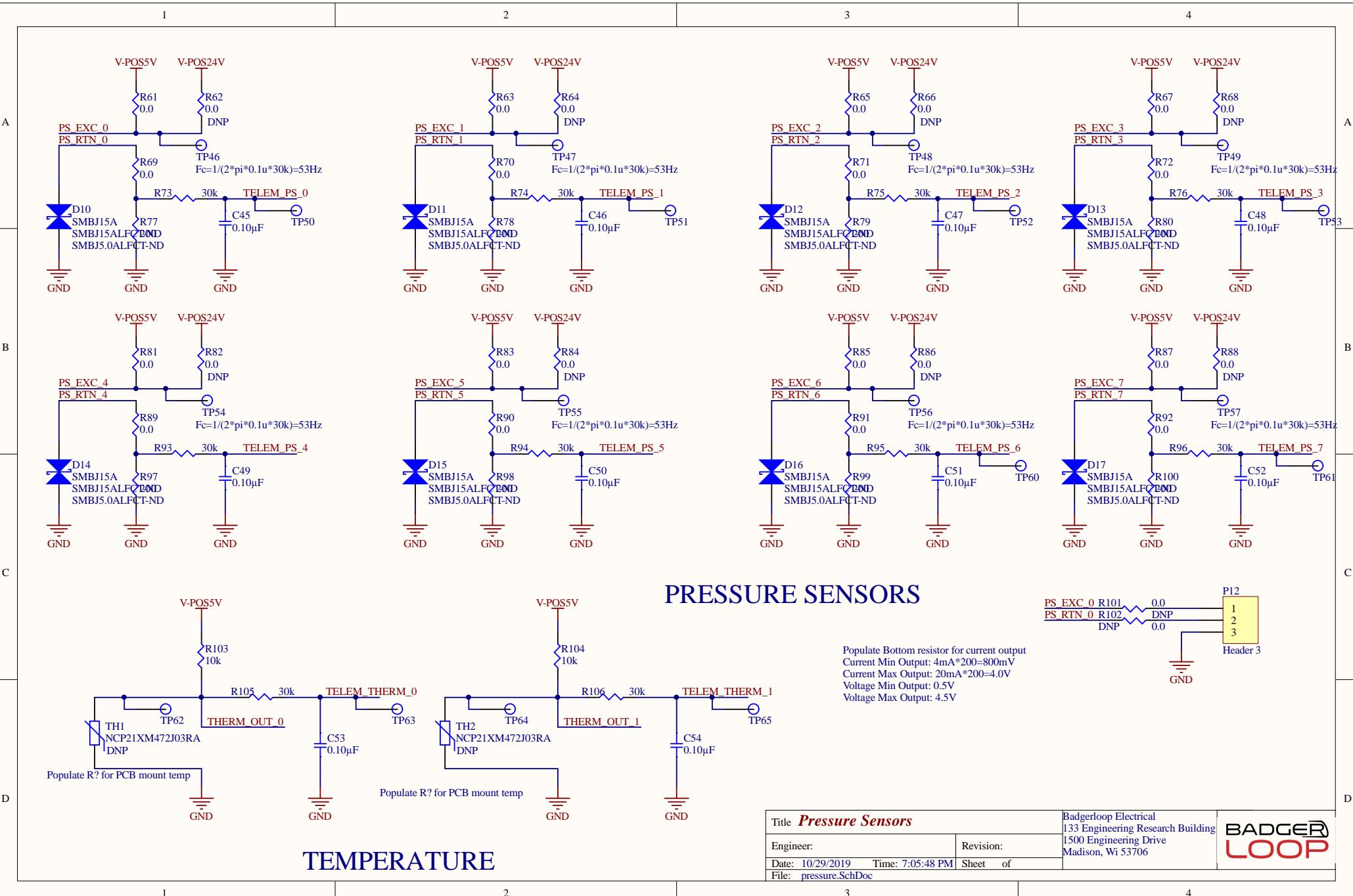
Date: 10/29/2019 Time: 7:05:48 PM

Sheet of

File: [power\\_7V.SchDoc](#)

Badgerloop Electrical  
133 Engineering Research Building  
1500 Engineering Drive  
Madison, WI 53706

**BADGER**  
**LOOP**



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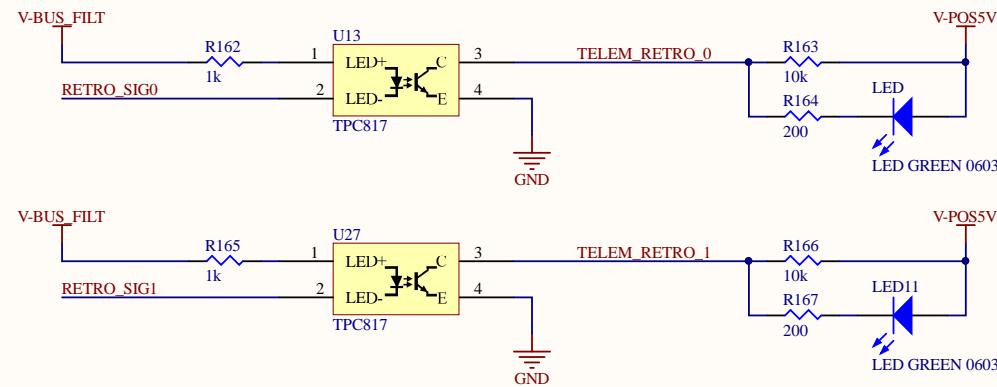
B

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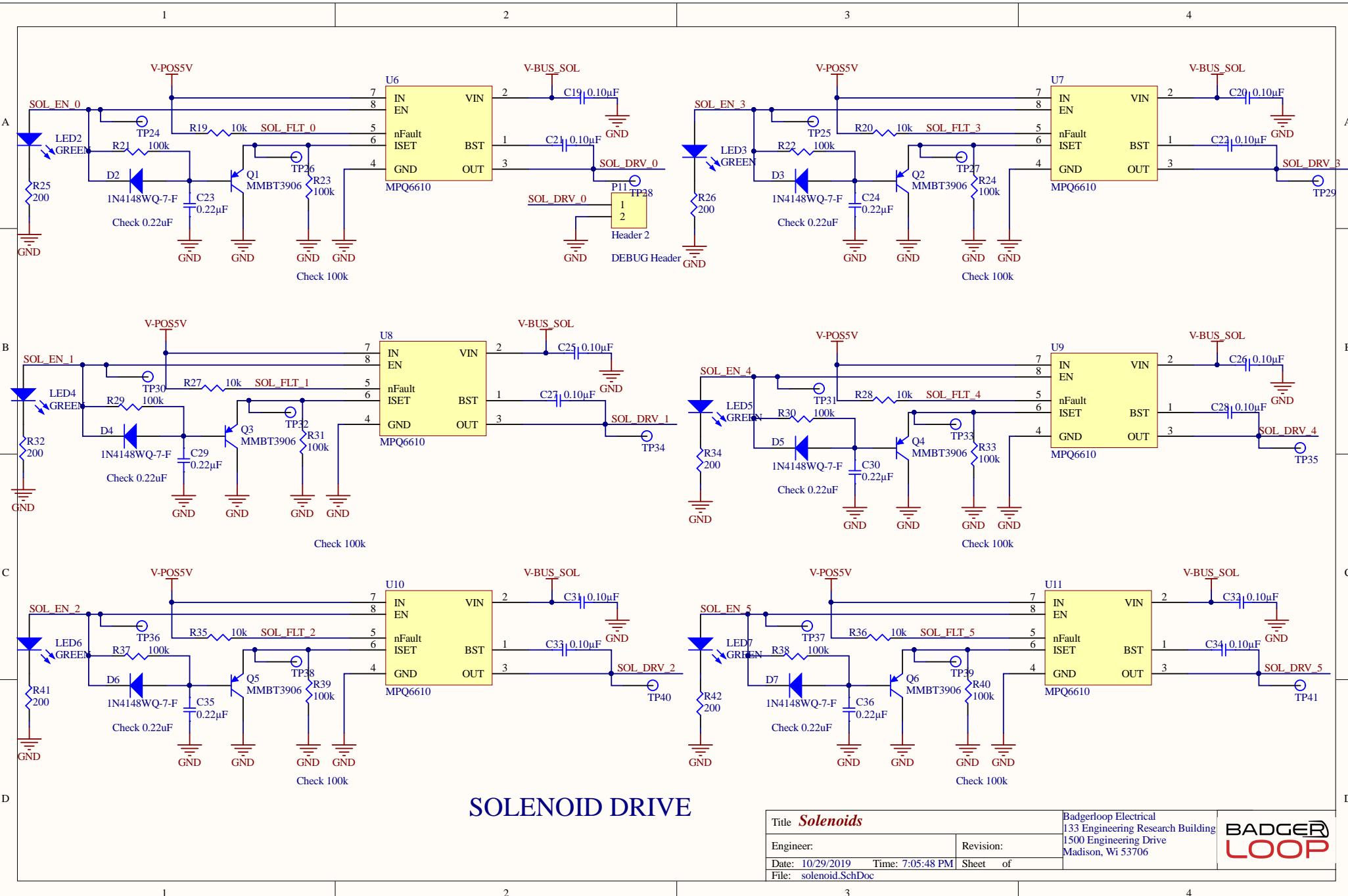
C

D

D



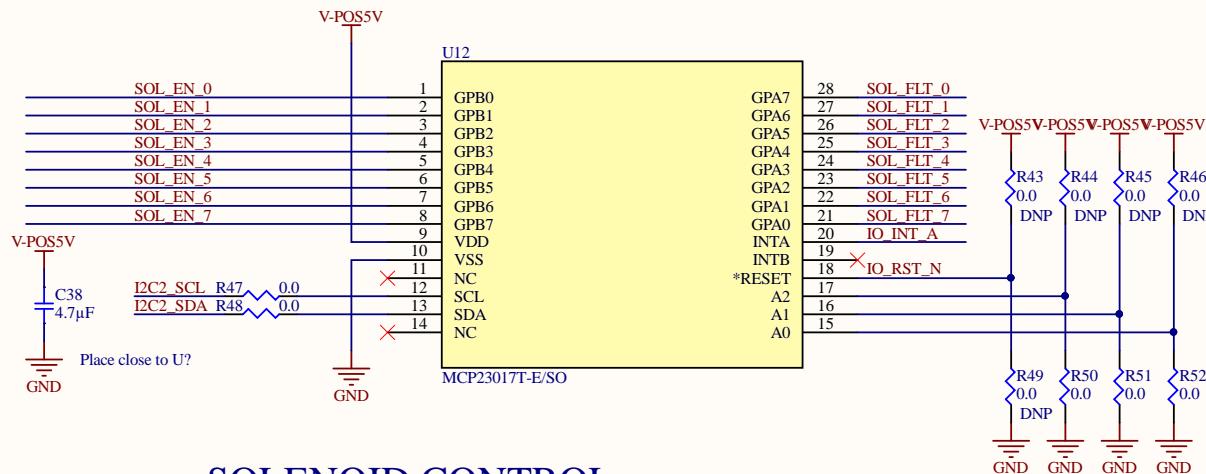
Title <i>Retro</i>		Badgerloop Electrical
Engineer:		133 Engineering Research Building
Date: 10/29/2019	Time: 7:05:48 PM	1500 Engineering Drive Madison, Wi 53706
File: retro.SchDoc		Sheet of



Title <b>Solenoids</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 10/29/2019	Time: 7:05:48 PM	1500 Engineering Drive
File: solenoid.SchDoc		Madison, WI 53706

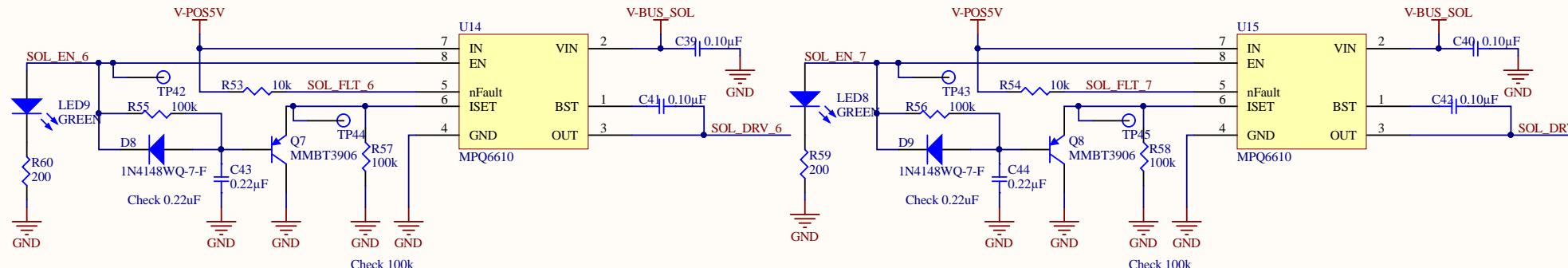
**BADGER  
LOOP**

A



## SOLENOID CONTROL

C



## SOLENOID DRIVE

Title <b>Solenoid Control</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 10/29/2019	Time: 7:05:48 PM	1500 Engineering Drive Madison, WI 53706
File: solenoid_drv.SchDoc		<b>BADGER</b> <b>LOOP</b>

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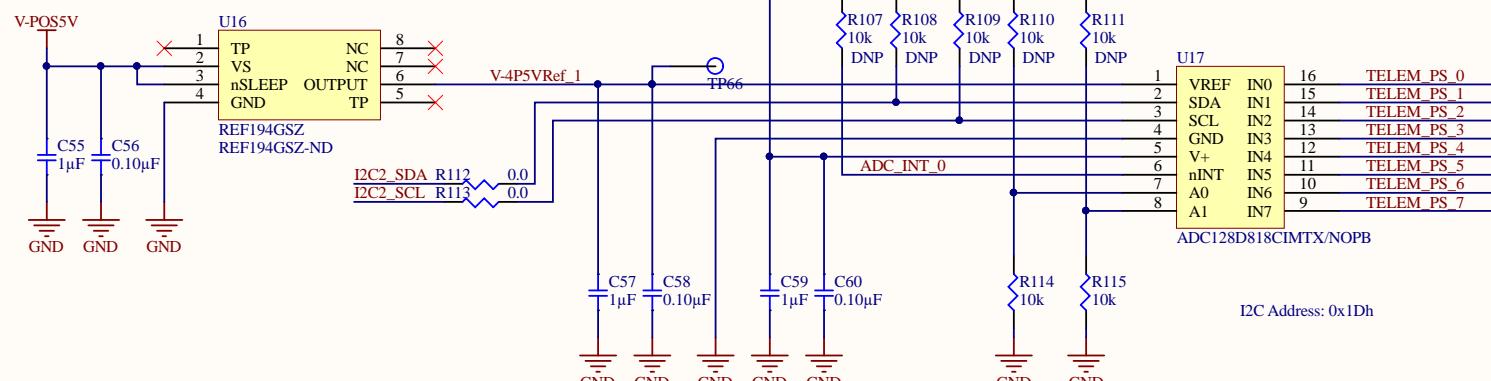
D

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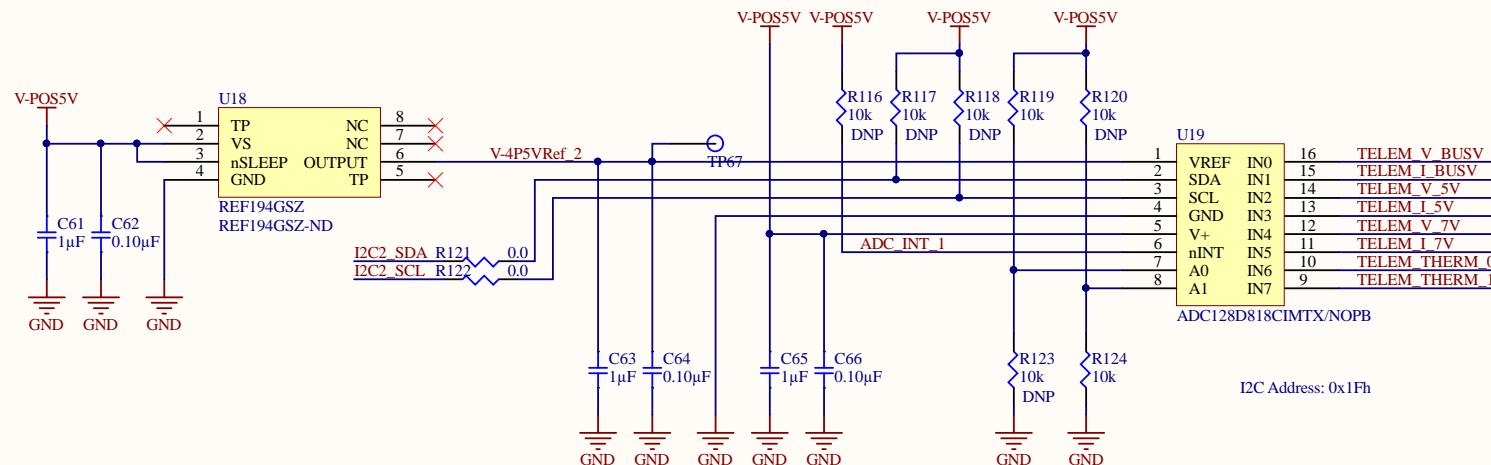
B

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## PRESSURE



## RAIL AND TEMPERATURE

Title <b>ADC</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 10/29/2019	Time: 7:05:48 PM	1500 Engineering Drive
File: telemetry_adc.SchDoc		Madison, WI 53706

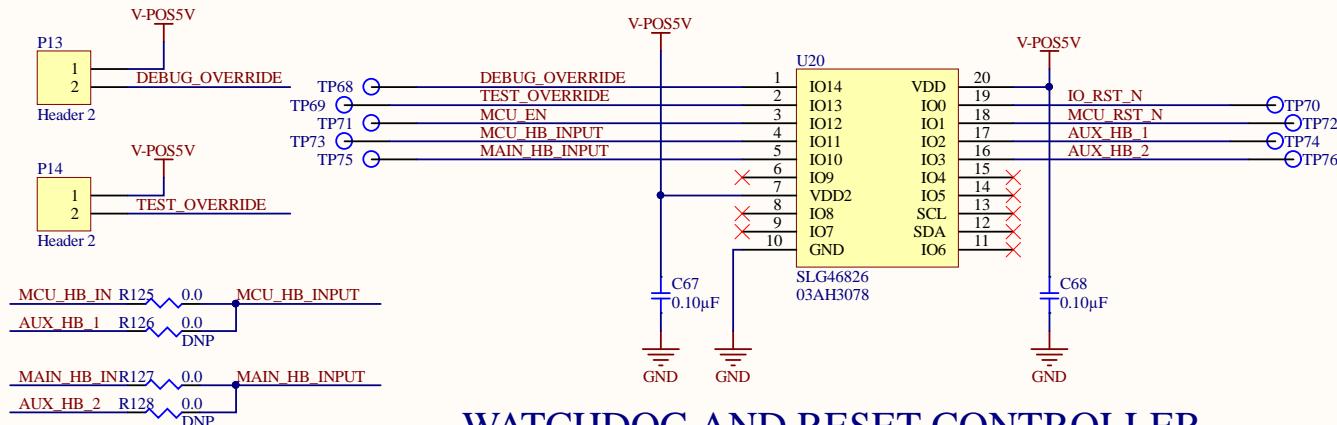
**BADGER**  
**LOOP**

1

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## WATCHDOG AND RESET CONTROLLER

## DEBUG

IO pin selection is arbitrary. Can be adjusted internally for better layout  
Currently- Inputs on Left, outputs on right

Modes of operation:  
Debug: EN signal is always on when SLG has power  
Populate Jumper 1  
Test: 10Hz signal internal signal is recirculated to mimic heartbeat  
Populate Jumper 2  
Operation: U2 expects 10Hz heartbeat. If no heartbeat for 1s after 20s Power on reset MCP\_RST\_N will fall and MCU\_RST\_N will pulse for 200ms

Silego Image here:  
[https://github.com/badgerloop-software/hardware/blob/master/silego/watchdog\\_gp6](https://github.com/badgerloop-software/hardware/blob/master/silego/watchdog_gp6)

## Silego Image PDF Outputs:

Title <b>Watchdog</b>	Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706	<b>BADGER</b> <b>LOOP</b>
Engineer:	Revision:	
Date: 10/29/2019	Time: 7:05:49 PM	Sheet of
File: watchdog.SchDoc		

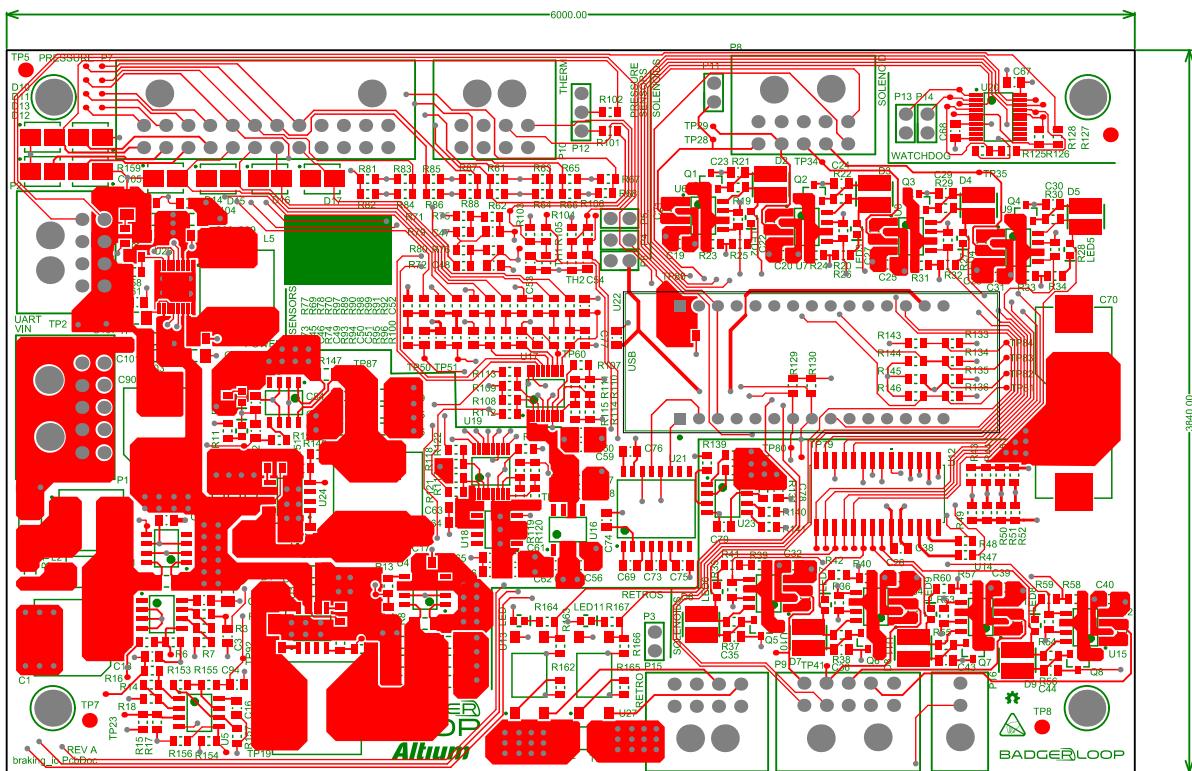
A

A

Layer	Name	Material	Thickness	Constant	Board Layer	Stack
	Top Overlay					
	Top Solder	Solder Resist	0.40mil	3.5		
1	Top Layer	Copper	1.40mil			
	Dielectric 2	FR-4	18.70mil	4.9		
2	GND	Copper	1.40mil			
	Dielectric 1	FR-4	18.70mil	4.9		
3	PWR	Copper	1.40mil			
	Dielectric 3	FR-4	18.70mil	4.9		
4	Bottom Layer	Copper	1.40mil			
	Bottom Solder	Solder Resist	0.40mil	3.5		
	Bottom Overlay					
Total board thickness:			62.50mil			

B

B



C

C

Top Layer

**BADGER  
LOOP**

Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

RCastle, BTob  
JEslinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
10/29/2019

FILE NAME:  
braking\_in\_PchDoc

7, TITLE: braking io.PcbDoc

PART NO.:

REV:  
A

SCA  
1:1

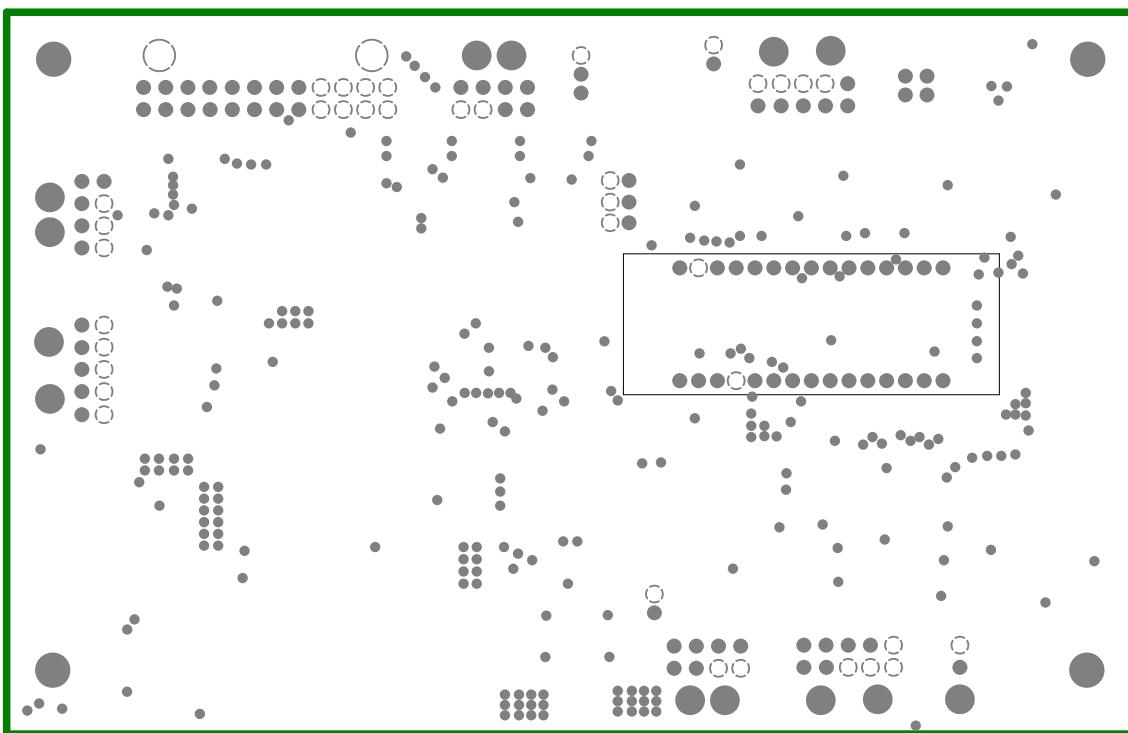
A

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	1.40mil		
	Dielectric 2	FR-4	18.70mil	4.9	
2	GND	Copper	1.40mil		
	Dielectric 1	FR-4	18.70mil	4.9	
3	PWR	Copper	1.40mil		
	Dielectric 3	FR-4	18.70mil	4.9	
4	Bottom Layer	Copper	1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness:

62.50mil

B



GND

D

**BADGER  
LOOP**

Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
10/29/2019

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO.:  
Braking Input Output Controller

REV:  
A

DWG NO:

SCALE:  
1:1

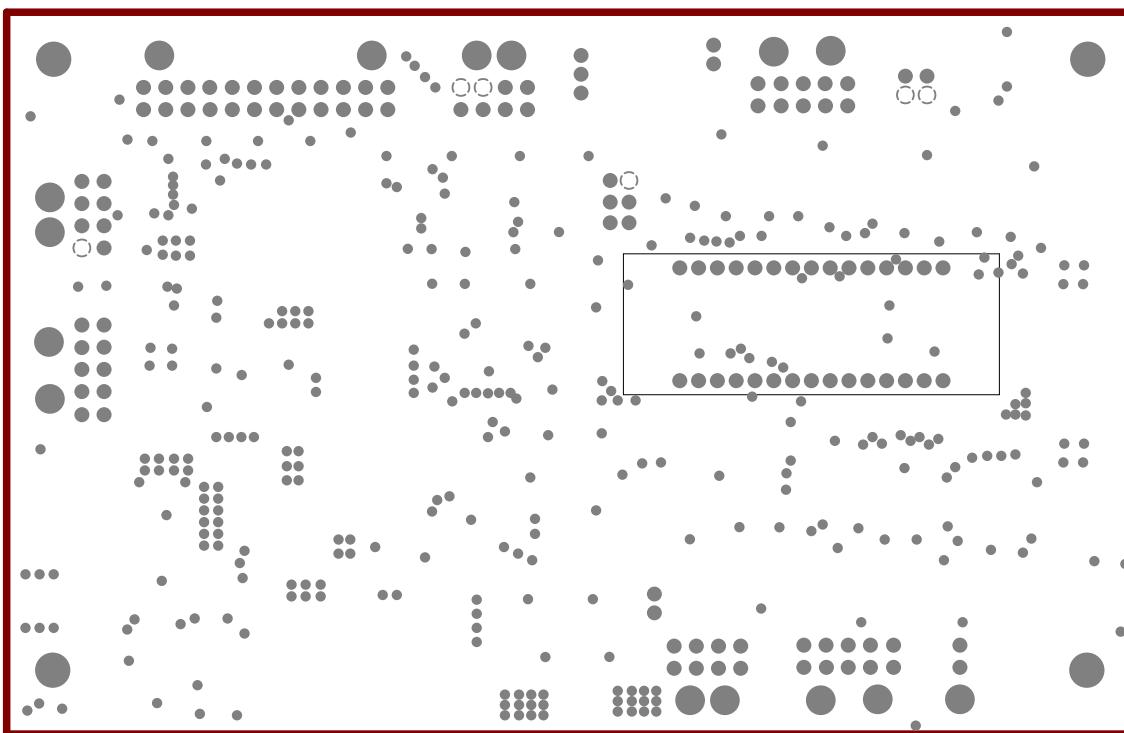
A

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	1.40mil		
	Dielectric 2	FR-4	18.70mil	4.9	
2	GND	Copper	1.40mil		
	Dielectric 1	FR-4	18.70mil	4.9	
3	PWR	Copper	1.40mil		
	Dielectric 3	FR-4	18.70mil	4.9	
4	Bottom Layer	Copper	1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness:

62.50mil

B



PWR

D

**BADGER  
LOOP**

Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
10/29/2019

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO.:  
Braking Input Output Controller

REV:  
A

SCALE:  
1:1

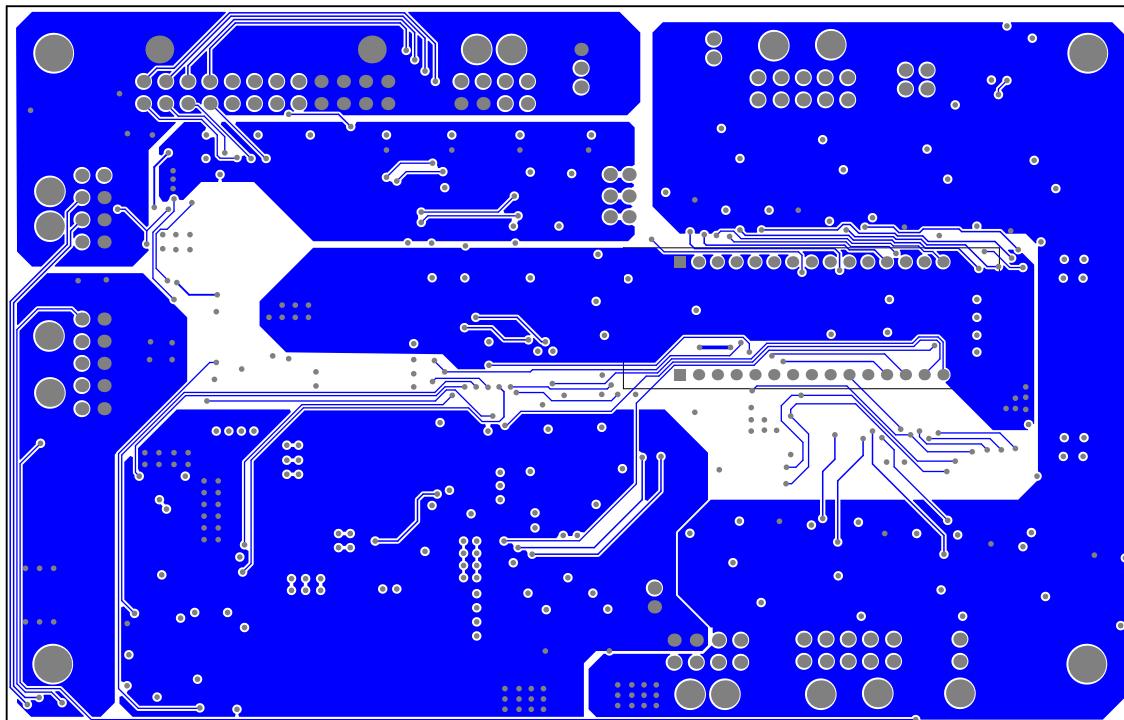
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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	1.40mil		
	Dielectric 2	FR-4	18.70mil	4.9	
2	GND	Copper	1.40mil		
	Dielectric 1	FR-4	18.70mil	4.9	
3	PWR	Copper	1.40mil		
	Dielectric 3	FR-4	18.70mil	4.9	
4	Bottom Layer	Copper	1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness:

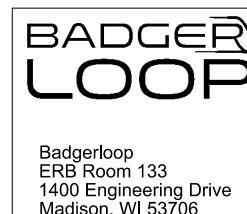
62.50mil

B



Bottom Layer

D



ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
10/29/2019

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO.:  
Braking Input Output Controller

REV:  
A

DWG NO:

SCALE:  
1:1

A

B

C

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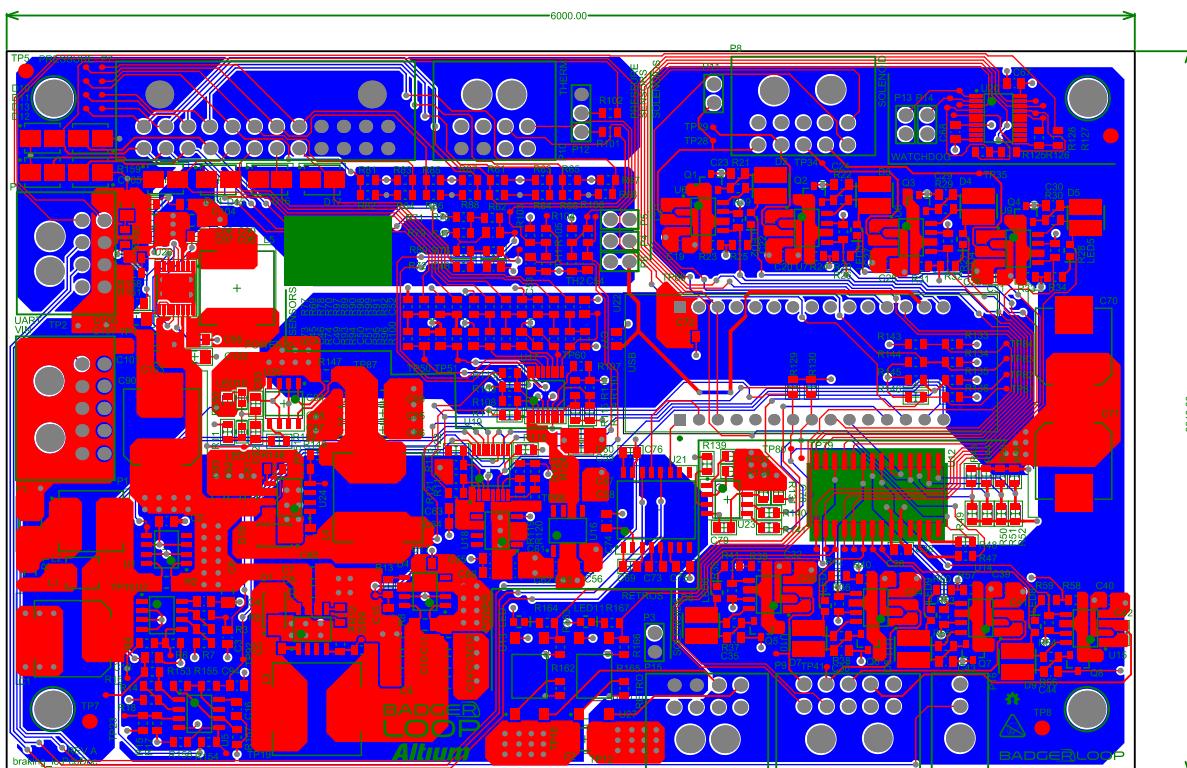
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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	1.40mil		
	Dielectric 2	FR-4	18.70mil	4.9	
2	GND	Copper	1.40mil		
	Dielectric 1	FR-4	18.70mil	4.9	
3	PWR	Copper	1.40mil		
	Dielectric 3	FR-4	18.70mil	4.9	
4	Bottom Layer	Copper	1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness:

62.50mil

B



C

D

A

B

C

D

**BADGER  
LOOP**

Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
10/29/2019

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO.:  
Braking Input Output Controller

REV:  
A

DWG NO:

SCALE:  
1:1