Mahendar R

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◇DOB: Oct 20, 2002 ◇ Gender: Male

SUMMARY

VLSI Verification Engineer with experience in SystemVerilog, UVM, and verification of APB, AHB, AXI, SPI, and I2C protocols. Skilled in building UVM components, constrained-random tests, assertions, scoreboards, and coverage-driven verification. Hands-on with RTL debugging, functional coverage closure, waveform analysis, and tools such as VCS, QuestaSim, and ModelSim.

INTERNSHIP

Embedded Hardware Engineer - Technofly solutions Oct '22 — Oct '22, Bengaluru, India

Assisted in the design and development of embedded systems for various applications, gaining hands-on experience with microcontrollers, firmware programming, and hardware integration.

VLSI Design Intern – Rooman Technologies Oct '24 — Mar'25, Bengaluru, India

Designed and verified a 4-bit priority encoder using Verilog/SystemVerilog and UVM. Built key UVM components, performed simulation and debugging on EDA Playground, and validated all test scenarios with 100% pass results.

Professional VLSI Training – ChipEdge Technologies Jun'25 – Nov'25, Bengaluru, India

Completed hands-on training in SystemVerilog, UVM, and functional verification, developing testbenches for APB, AHB, AXI, SPI, and I2C protocols. Built reusable UVM components and gained experience in coverage, assertions, debugging, and simulation using VCS, QuestaSim, and ModelSim.

EDUCATION

Bachelors in BE, SAMBHRAM INSTITUTE OF TECHNOLOGY (GPA: 8.27/ 82.7%) Bengaluru, India

PUC in Department of Pre-University, SRI JAGADGURU RENUKACHARYA COLLEGE OF SCIENCE ARTS AND COMMERCE (GPA: 85.5) Bengaluru, India

Highschool in SSLC, SHUSHRUTI VIDYA SAMASTE (GPA: 88.32) Bengaluru, India

AWARDS

STUDENT PRESIDENT OF IETE CHAPTER Feb '24

Served as the president of the IETE chapter.

SECRETARY OF SAIT VEERAHOYSALA (LEO CLUB) Sep '24

Served as secretary of LIONS LEO CLUB

DGCA APPROVED REMOTE PILOT Jul '24

Achieved DGCA approval as a remote pilot.

BEST OUTGOING STUDENT OF THE BATCH May' 25

Honoured for exceptional leadership, performance, and overall excellence.

VLSI PROJECTS

AXI 3 Protocol Verification using UVM

- Built a complete AXI UVM environment including driver, monitor, agent, sequencer, scoreboard, predictor, and functional coverage.
- Developed directed and constrained-random tests for fixed, increment, wrap, error, and reset scenarios, verifying all read/write channels and handshake behavior.
- Achieved 100% functional coverage and validated protocol correctness through detailed waveform analysis.

APB Protocol Verification using SystemVerilog & UVM

- Built both a SystemVerilog testbench and a complete UVM environment including driver, monitor, agent, predictor, scoreboard, and functional coverage.
- Developed multiple tests for read, write, reset, zero-wait, SLVERR, and random scenarios using sequences and constrained-random stimulus.
- Achieved 100% functional correctness with complete coverage closure and verified all waveforms across test scenarios.

AHB Bus System Verification using SystemVerilog

- Built a structured SystemVerilog verification environment including driver, monitor, generator, scoreboard, and functional coverage.
- Developed nine directed testcases covering read, write, burst, and increment operations, validating protocol handshakes and signal behavior.
- Achieved 100% functional coverage, confirming complete correctness of address, data, and control signal interactions through waveform analysis.

I2C EEPROM Controller — RTL Design & Verification

- Built the RTL design of an I2C Master/Slave EEPROM controller using FSM-based logic for start/stop conditions, addressing, and data transfer.
- Developed a SystemVerilog testbench to verify ACK/NACK behavior, byte-wise read/write operations, and timing constraints.
- Achieved correct protocol functionality validated through simulation waveforms and memory updates.

SPI Master/Slave Interface — RTL Design & Testing

- Built SPI Master and Slave RTL modules implementing shift-register-based serial communication with CPOL/CPHA modes..
- Developed a SystemVerilog testbench to test MOSI/MISO data transfers, chip-select operation, and clock-driven signal transitions.
- Achieved accurate serial data exchange and verified proper protocol timing through waveform analysis.

EMBEDDED PROJECT

Soldier Health And Position Monitoring System Using Arduino And Iot

- Developed a wearable health and location tracking system for soldier safety.
- Selected for KSCST Government Exhibition and published as a research paper.

SKILLS

Languages: Verilog, SystemVerilog, C, Python
VLSI & Verification: UVM, Functional Verification, Assertions (SVA), Constrained-Random Testing, Coverage, Scoreboard Development and Coverage Analysis
Protocols: APB, AHB, AXI, SPI, I2C
Tools: QuestaSim, ModelSim, Synopsys VCS, Vivado, EDA playground
Operating Systems: Linux