Instruction Set Reference Table

Assembler	Machine code	Function	Description
add R_{d}, R_{s}, R_{t}	0000 dddd ssss 0000 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} + R_{\mathrm{t}}$	Add
addi R_{d}, R_{s}, immed	0001 dddd ssss 0000 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} + \int(immed)$	Add Immediate
addu R_{d}, R_{s}, R_{t}	0000 dddd ssss 0001 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} + R_{\mathrm{t}}$	Add Unsigned
addui R_{d}, R_{s}, immed	0001 dddd ssss 0001 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} + immed$	Add Unsigned Immediate
sub R_{d}, R_{s}, R_{t}	0000 dddd ssss 0010 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} - R_{\mathrm{t}}$	Subtract
subi R_{d}, R_{s}, immed	0001 dddd ssss 0010 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} - \int(immed)$	Subtract Immediate
subu R_{d}, R_{s}, R_{t}	0000 dddd ssss 0011 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} - R_{\mathrm{t}}$	Subtract Unsigned
subui R_{d}, R_{s}, immed	0001 dddd ssss 0011 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} - immed$	Subtract Unsigned Immediate
mult R_{d}, R_{s}, R_{t}	0000 dddd ssss 0100 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \times R_{\mathrm{t}}$	Multiply
multi R_{d}, R_{s}, immed	0001 dddd ssss 0100 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \times \int(immed)$	Multiply Immediate
multu R_{d}, R_{s}, R_{t}	0000 dddd ssss 0101 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \times R_{\mathrm{t}}$	Multiply Unsigned
multui R_{d}, R_{s}, immed	0001 dddd ssss 0101 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \times immed$	Multiply Unsigned Immediate
div R_{d}, R_{s}, R_{t}	0000 dddd ssss 0110 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \div R_{\mathrm{t}}$	Divide
divi R_{d}, R_{s}, immed	0001 dddd ssss 0110 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \div \int(immed)$	Divide Immediate
divu R_{d}, R_{s}, R_{t}	0000 dddd ssss 0111 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \div R_{\mathrm{t}}$	Divide Unsigned
divui R_{d}, R_{s}, immed	0001 dddd ssss 0111 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \div immed$	Divide Unsigned Immediate
rem R_{d}, R_{s}, R_{t}	0000 dddd ssss 1000 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ \%\ R_{\mathrm{t}}$	Remainder
remi R_{d}, R_{s}, immed	0001 dddd ssss 1000 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ \%\ \int(immed)$	Remainder Immediate
remu R_{d}, R_{s}, R_{t}	0000 dddd ssss 1001 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ \%\ R_{\mathrm{t}}$	Remainder Unsigned
remui R_{d}, R_{s}, immed	0001 dddd ssss 1001 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ \%\ immed$	Remainder Unsigned Immediate
lhi R_{d}, immed	0011 dddd ssss 1110 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow immed \ll 16$	Load High Immediate
la R_{d}, address	1100 dddd 0000 aaaa aaaa aaaa aaaa aaaa	$R_{\mathrm{d}} \leftarrow address$	Load Address

Table 1: Arithmetic Instructions

and R_{d}, R_{s}, R_{t}	0000 dddd ssss 1011 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ AND\ R_{\mathrm{t}}$	Bitwise AND
andi R_{d}, R_{s}, immed	0001 dddd ssss 1011 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ AND\ immed$	Bitwise AND Immediate
or R_{d}, R_{s}, R_{t}	0000 dddd ssss 1101 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ OR\ R_{\mathrm{t}}$	Bitwise OR
ori R_{d}, R_{s}, immed	0001 dddd ssss 1101 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ OR\ immed$	Bitwise OR Immediate
xor R_{d}, R_{s}, R_{t}	0000 dddd ssss 1111 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ XOR\ R_{\mathrm{t}}$	Bitwise XOR
xori R_{d}, R_{s}, immed	0001 dddd ssss 1111 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}}\ XOR\ immed$	Bitwise XOR Immediate
sll R_{d}, R_{s}, R_{t}	0000 dddd ssss 1010 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \ll R_{\mathrm{t}}$	Shift Left Logical
slli R_{d}, R_{s}, immed	0001 dddd ssss 1010 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \ll immed$	Shift Left Logical Immediate
srl R_{d}, R_{s}, R_{t}	0000 dddd ssss 1100 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \gg R_{\mathrm{t}}$	Shift Right Logical
srli R_{d}, R_{s}, immed	0001 dddd ssss 1100 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow R_{\mathrm{s}} \gg immed$	Shift Right Logical Immediate
sra R_{d}, R_{s}, R_{t}	0000 dddd ssss 1110 0000 0000 0000 tttt	$R_{\mathrm{d}} \leftarrow \int(R_{\mathrm{s}} \gg R_{\mathrm{t}})$	Shift Right Arithmetic
srai R_{d}, R_{s}, immed	0001 dddd ssss 1110 iiii iiii iiii iiii	$R_{\mathrm{d}} \leftarrow \int(R_{\mathrm{s}} \gg immed)$	Shift Right Arithmetic Immediate

Table 2: Bitwise Instructions

slt R_d, R_s, R_t	0010 dddd ssss 0000 0000 0000 0000 tttt	$R_d \leftarrow R_s < R_t$	Set on Less than
slti R_d, R_s, immed	0011 dddd ssss 0000 iiii iiii iiii iiii	$R_d \leftarrow R_s < \int(immed)$	Set on Less than Immediate
sltu R_d, R_s, R_t	0010 dddd ssss 0001 0000 0000 0000 tttt	$R_d \leftarrow R_s < R_t$	Set on Less than Unsigned
sltui R_d, R_s, immed	0011 dddd ssss 0001 iiii iiii iiii iiii	$R_d \leftarrow R_s < immed$	Set on Less than Unsigned Immediate
sgt R_d, R_s, R_t	0010 dddd ssss 0010 0000 0000 0000 tttt	$R_d \leftarrow R_s > R_t$	Set on Greater than
sgti R_d, R_s, immed	0011 dddd ssss 0010 iiii iiii iiii iiii	$R_d \leftarrow R_s > \int(immed)$	Set on Greater than Immediate
sgtu R_d, R_s, R_t	0010 dddd ssss 0011 0000 0000 0000 tttt	$R_d \leftarrow R_s > R_t$	Set on Greater than Unsigned
sgtui R_d, R_s, immed	0011 dddd ssss 0011 iiii iiii iiii iiii	$R_d \leftarrow R_s > immed$	Set on Greater than Unsigned Immediate
sle R_d, R_s, R_t	0010 dddd ssss 0100 0000 0000 0000 tttt	$R_d \leftarrow R_s \leq R_t$	Set on Less than or Equal
slei R_d, R_s, immed	0011 dddd ssss 0100 iiii iiii iiii iiii	$R_d \leftarrow R_s \leq \int(immed)$	Set on Less or Equal Immediate
sleu R_d, R_s, R_t	0010 dddd ssss 0101 0000 0000 0000 tttt	$R_d \leftarrow R_s \leq R_t$	Set on Less or Equal Unsigned
sleui R_d, R_s, immed	0011 dddd ssss 0101 iiii iiii iiii iiii	$R_d \leftarrow R_s \leq immed$	Set on Less or Equal Unsigned Imm
sge R_d, R_s, R_t	0010 dddd ssss 0110 0000 0000 0000 tttt	$R_d \leftarrow R_s \geq R_t$	Set on Greater than or Equal
sgei R_d, R_s, immed	0011 dddd ssss 0110 iiii iiii iiii iiii	$R_d \leftarrow R_s \geq \int(immed)$	Set on Greater or Equal Immediate
sgeu R_d, R_s, R_t	0010 dddd ssss 0111 0000 0000 0000 tttt	$R_d \leftarrow R_s \geq R_t$	Set on Greater or Equal Unsigned
sgeui R_d, R_s, immed	0011 dddd ssss 0111 iiii iiii iiii iiii	$R_d \leftarrow R_s \geq immed$	Set on Greater or Equal Unsigned Imm
seq R_d, R_s, R_t	0010 dddd ssss 1000 0000 0000 0000 tttt	$R_d \leftarrow R_s = R_t$	Set on Equal
seqi R_d, R_s, immed	0011 dddd ssss 1000 iiii iiii iiii iiii	$R_d \leftarrow R_s = \int(immed)$	Set on Equal Immediate
sequ R_d, R_s, R_t	0010 dddd ssss 1001 0000 0000 0000 tttt	$R_d \leftarrow R_s = R_t$	Set on Equal Unsigned
sequi R_d, R_s, immed	0011 dddd ssss 1001 iiii iiii iiii iiii	$R_d \leftarrow R_s = immed$	Set on Equal Unsigned Immediate
sne R_d, R_s, R_t	0010 dddd ssss 1010 0000 0000 0000 tttt	$R_d \leftarrow R_s \neq R_t$	Set on Not Equal
snei R_d, R_s, immed	0011 dddd ssss 1010 iiii iiii iiii iiii	$R_d \leftarrow R_s \neq \int(immed)$	Set on Not Equal Immediate
sneu R_d, R_s, R_t	0010 dddd ssss 1011 0000 0000 0000 tttt	$R_d \leftarrow R_s \neq R_t$	Set on Not Equal Unsigned
sneui R_d, R_s, immed	0011 dddd ssss 1011 iiii iiii iiii iiii	$R_d \leftarrow R_s \neq immed$	Set on Not Equal Unsigned Immediate

Table 3: Test Instructions

Branch Instructions			
j address	0100 0000 0000 aaaa aaaa aaaa aaaa aaaa	$PC \leftarrow Address$	Jump
jr R_s	0101 0000 ssss 0000 0000 0000 0000 0000	$PC \leftarrow R_s$	Jump to Register
jal address	0110 0000 0000 aaaa aaaa aaaa aaaa aaaa	\$ra $\leftarrow PC,\ PC \leftarrow Address$	Jump and Link
jalr R_s	0111 0000 ssss 0000 0000 0000 0000 0000	\$ra $\leftarrow PC,\ PC \leftarrow R_s$	Jump and Link Register
beqz R_s, offset	1010 0000 ssss oooo oooo oooo oooo oooo	$if(R_s = 0)\ PC \leftarrow PC + offset$	Branch on equal to 0
bnez R_s, offset	1011 0000 ssss oooo oooo oooo oooo oooo	$if(R_s \neq 0)\ PC \leftarrow PC + offset$	Branch on not equal to 0
Memory Instructions			
lw R_d, offset(R_s)	1000 dddd ssss oooo oooo oooo oooo oooo	$R_d \leftarrow MEM[R_s + offset]$	Load word
sw R_d, offset(R_s)	1001 dddd ssss oooo oooo oooo oooo oooo	$MEM[R_s + offset] \leftarrow R_d$	Store word
Special Instructions			
movgs R_d, R_s	0011 0000 0000 1100 0000 0000 0000 0000	$R_d \leftarrow R_s$	Move General to Special Register
movsg R_d, R_s	0011 0000 0000 1101 0000 0000 0000 0000	$R_d \leftarrow R_s$	Move Special to General Register
break	0010 0000 0000 1100 0000 0000 0000 0000		Generate Break Point Exception
syscall	0010 0000 0000 1101 0000 0000 0000 0000		Generate Syscall Exception
rfe	0010 0000 0000 1110 0000 0000 0000 0000	$PC \leftarrow$ \$ear	Return from Exception

Table 4: Other Instructions