

如何解决设计难点 (第三部分)

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AHEAD OF WHAT'S POSSIBLE™

ADI智库
一站式电子技术宝库

中级第七讲：电源 关键参数的测试与 优化



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电源设计中要考虑的几个问题

- 效率
- V_{out}纹波
- 动态响应
- 体积

电源设计中要考虑的几个问题—效率

- ▶ 效率 – 控制芯片
- ▶ 同步控制
- ▶ Burst Mode (轻载效率最高)
- ▶ Pulse Skipping (轻载效率较高)
- ▶ Forced Current continuous Mode (FCM) (轻载效率最低)

设计中要考虑的几个问题—效率

- ▶ 效率 – MOSFET
- ▶ 导通损耗: $R_{ds(on)}$ (R_{dson} vs Temp)
- ▶ 开关损耗: Rising/Falling time, F_{sw} ,
- ▶ 驱动损耗: Q_g , 电荷低
- ▶ 二极管反向恢复: I_{rr} (reverse recovery current)
- ▶ 体二极管导通损耗: dead time

设计中要考虑的几个问题—效率

- ▶ 效率 – 二极管、电感、电容
- ▶ 二极管：顺向导通损耗、开关损耗（含反向恢复过程）
- ▶ 电感：铜损，磁损
- ▶ 电容：ESR

设计中要考虑的几个问题—Vout纹波

- ▶ Vout纹波 – LC filter, Fsw, Controller (Burst/PS/DCM/CCM)
- ▶ 源：电感电流纹波
- ▶ 相关因素：开关频率，电感大小，电容大小及ESR
- ▶ 抑制方法：高Fsw，大电感，大电容（低ESR），增加输出滤波电路（LC）。

设计中要考虑的几个问题-动态，体积，温度范围

- 动态响应 – ΔV 越小越好，Response time越快越好，但必须以稳定为前提。
- 体积 – 开关频率高，体积小
- 温度范围 –
 - 控制芯片 (- 40 ~ 125 degC)
 - 电感 (- 40 ~ 125 degC)
 - 电容 (- 40 ~ 105/125 degC) vs 寿命
 - PCB: related to material.

BUCK电路计算实例

电气规格：

输入：6.5V-16V

输出：1.8V/20A

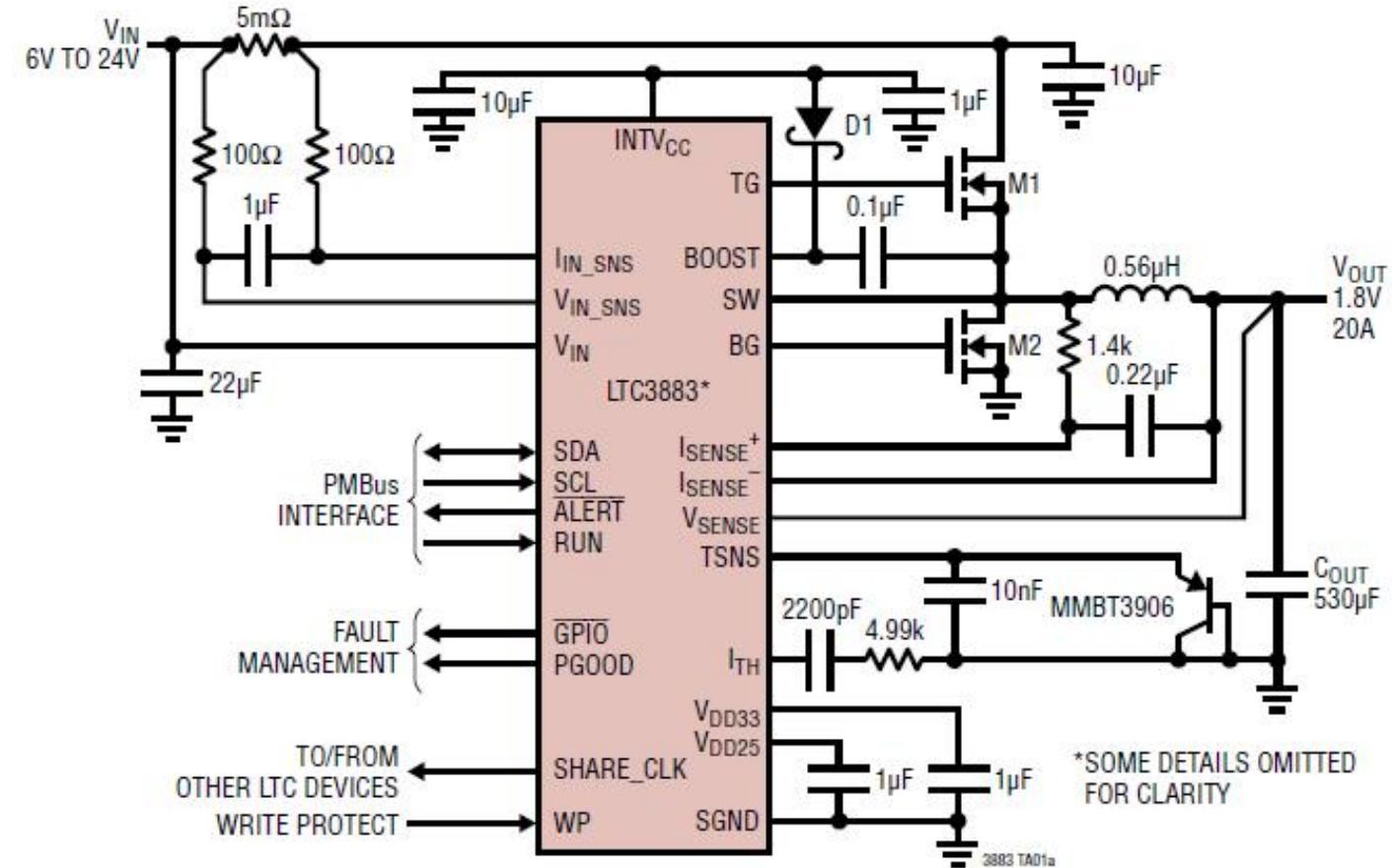
效率：90% (12Vin@满载)

纹波：30mVpk-pk

动态：3%*Vo (10A–20A)

需要PMBus接口监控

方案：LTC3883



BUCK电路计算实例

1.开关频率选择

- 根据效率，体积选择开关频率
- 最小on-time考慮 45ns
- Controller发热考慮 16V输入选择500Khz

BUCK电路计算实例

2.电感选择

一般原则: $\Delta I_L = 0.2I_O$ to $0.4I_O$ 去计算电感
 $\Delta I_L = 0.4 * 20 = 8A$

$$\Delta I_L = \frac{1.8 * (1 - V_{OUT}/V_{IN})}{L \cdot f_S};$$

$$L = \frac{1.8 * (1 - 1.8/16)}{8.500k} = 0.399\mu H;$$

$$I_{L(MAX)} = 20 + 0.5\Delta I_L = 24A$$

Part number ¹ <i>Click to get parts</i>	Inductance ² ±20% (μ H)	DCR (mOhms) ³		SRF typ ⁴ (MHz)	Isat (A) ⁵	Irms (A) ⁶		Height max (in. / mm)
		typ	max			20°C rise	40°C rise	
XAL1580-401ME_	0.40	0.50	0.70	53.0	111	47.0	60.0	0.323 / 8.2
XAL1580-741ME_	0.74	0.72	0.86	35.1	86.0	43.2	59.7	0.323 / 8.2
XAL1580-102ME_	1.00	0.93	1.12	30.0	73.5	40.6	57.5	0.323 / 8.2
XAL1580-132ME_	1.30	1.15	1.38	26.2	65.0	34.6	46.7	0.315 / 8.0
XAL1580-182ME_	1.80	1.61	1.93	21.3	57.0	33.2	43.8	0.315 / 8.0
XAL1580-202ME_	2.00	1.91	2.29	20.1	51.0	29.5	39.9	0.315 / 8.0
XAL1580-302ME_	3.00	2.62	3.10	16.0	43.0	25.6	34.4	0.315 / 8.0
XAL1580-452ME_	4.50	3.82	4.58	12.5	34.2	20.4	27.0	0.315 / 8.0
XAL1580-532ME_	5.30	4.35	5.22	11.8	33.0	19.5	26.5	0.315 / 8.0
XAL1580-612ME_	6.10	5.66	6.79	11.7	31.0	16.9	22.6	0.315 / 8.0

最大纹波电流出现在最高输入

电感量计算要按照最高输入电压计算

要求小于电感饱和电流

BUCK电路计算实例

电感损耗包括铜损（直流和交流）+铁损

直流铜损很容易计算，交流铜损和铁损很难计算，和频率、材料相关，借助于厂家online

Inductor parameters Change Frequency 500 kHz Ipeak 24.00 A IDC 20.00 A Ripple pk-pk 40%

Show all parts Actual size Free sample Part number XAL1580-401 L actual at 24.00 A μH nominal μH Isat A Irms A DCR max at 25°C mOhms Total losses mW Part temp. °C Temp. rating °C Length mm Width mm Height mm

Change sorting Change ambient temperature 25 °C

Output Rail # 1 Design Specs Vin min : 6.5 V Vin nom : 12 V Vin max : 24 V Sw. Freq : 500 kHz Vout : 1.8 V Iout : 20 A Ta : 55 °C

Inductor Inductor : XAL1580-401 L : 0.4 uH DCR : 0.5 mΩ θwa : 19 °C/W Select

Inductor Loss Tw : 55 °C DCR @ Tw : 0.5 mΩ DCR Loss : 0.2 W Core Loss : W Total Loss : 0.2 W

Current Waveform Current (A) Time (μs)

Inductance vs Ipeak Current Inductance (μH) Current (A)

Inductor losses and temperature rise at 500 kHz, 20 Arms, 8 A ΔIL XAL1580-401

Total losses	473 mW
Core + AC winding loss	273 mW
DCR typ. loss	200 mW
Temperature rise at 25°C ambient	11 °C

Waveform and AC loss calculations assume 50% duty cycle in continuous conduction mode.

To analyze inductor behaviour in a specific converter topology, use the [DC-DC Inductor Finder](#) tool.

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3.MOSFET 选择

- 开关管和同步整流管都是N沟道
- 开关管和整流管通常选型不一样
- Q_g 影响开关损耗
- R_{dson} 影响导通损耗
- Q_g 影响控制器发热
- 成本

BUCK电路计算实例

开关管

选择BSC050N03LS作为开关管

关键参数：

V_{DS}: 30V

R_{DSON}: 6mohm@5V驱动

Q_G: 17nC @5V驱动

P_{LOSS}=P_{CON}+P_{SW}+P_{GATE}

导通损耗P_{CON}:

$$P_{CON} = R_{DS(on)} \times I_{QSW(RMS)}^2 = R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12} \right)$$

$$P_{CON} = I_o^2 * D * R_{DSON} = 20^2 * \left(\frac{1.8}{12}\right) * 6m = 0.36W$$

BSC050N03LS G

Product Summary

V _{DS}	30	V
R _{DS(on),max}	5	mΩ
I _D	80	A

BUCK电路计算实例

$$P_{SW} = V_{IN} \times I_{OUT} \times F_S \times \frac{(Q_{gs2} + Q_{gd})}{I_g}$$

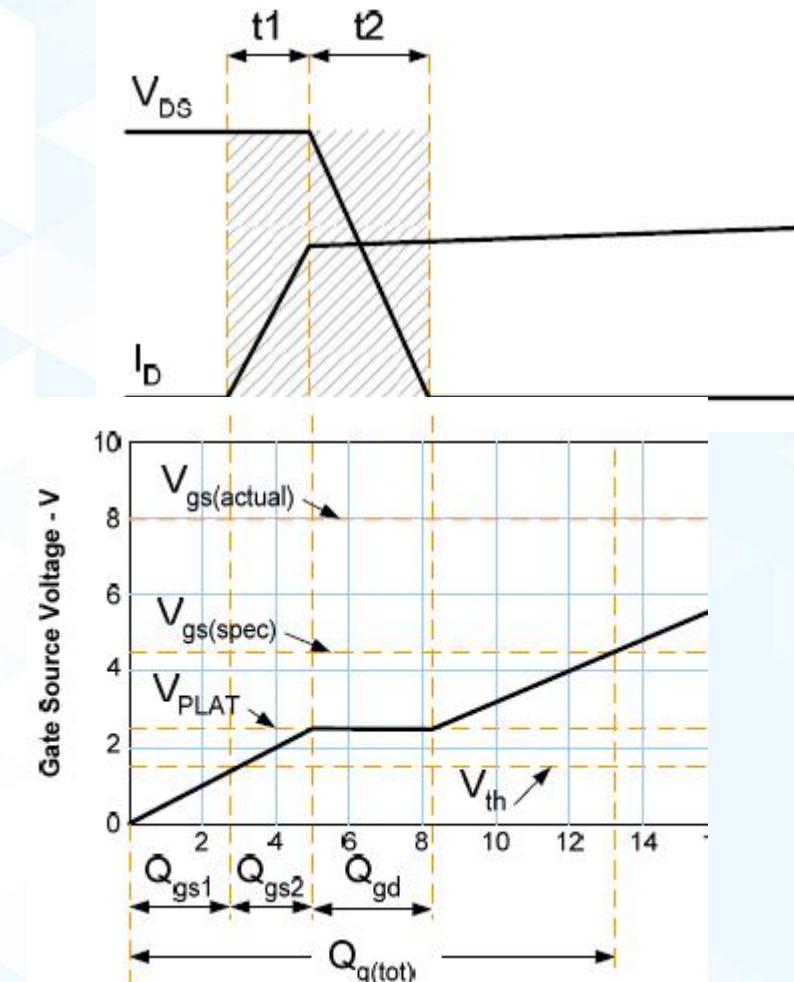
$$P_{swon}=0.5*12*(20-4)*500k*(6n/0.5)=0.576W$$

$$P_{swoff}=0.5*12*(20+4) *500k* (6n/1) =0.432W$$

$$P_{gate}=V_G*Q_g*f_s=5*13n*500k=0.0325W$$

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	6.3	8.4	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.2	4.3	
Gate to drain charge	Q_{gd}		-	2.9	4.8	
Switching charge	Q_{sw}		-	6.0	8.9	
Gate charge total	Q_g		-	13	17	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	V



BUCK电路计算实例

同步整流管

选择BSC011N03LS作为开关管

关键参数：

V_{DS}: 30V

R_{DSON}: 1.2mohm@5V驱动

Q_G: 34nC @5V驱动

P_{loss}=P_{con}+P_{diode}+P_{gate}

导通损耗P_{con}:

$$I_o^2 * (1 - D) * R_{DSON} = 20^2 * \left(1 - \frac{1.8}{12}\right) * 1.2m = 0.408W$$



OptiMOS™ Power-MOSFET

Features

- Optimized for high performance SMPS
- Integrated monolithic Schottky-like diode
- Very low on-resistance R_{DSON} @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance

BSC011N03LSI

Product Summary

V _{DS}	30	V
R _{DSON,max}	1.1	mΩ
I _D	100	A
Q _{OSS}	45	nC
Q _{G(0V..10V)}	68	nC

BUCK电路计算实例

$$P_{gate} = V_G * Q_g * f_s = 5 * 34n * 500k = 0.085W$$

$$P_{diode} = V_F * I_o * (T_{dead1} + T_{dead2}) * F_s = 0.56 * 20 * 40n * 500k = 0.224W$$

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	10.1	13.4	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.8	-	
Gate to drain charge	Q_{gd}		-	10.6	14	
Switching charge	Q_{sw}		-	13.9	-	
Gate charge total	Q_g		-	34	45	
Gate plateau voltage	$V_{plateau}$		-	2.4	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	96	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=12\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.56	0.7	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=12\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$	-	5	-	nC

BUCK电路计算实例

如果开关管采样同步整流的MOS,损耗显著变大! ! !

$$P_{con} = I_o^2 * D * R_{dson} = 20^2 * \left(\frac{1.8}{12}\right) * 1.2m = 0.072W$$

$$P_{swon} = 0.5 * 12 * (20 - 4) * 500k * (13.9n / 0.5) = 1.334W$$

$$P_{swoff} = 0.5 * 12 * (20 + 4) * 500k * (13.9n / 1) = 1.0W$$

$$P_{gate} = V_G * Q_g * f_s = 5 * 34n * 500k = 0.085W$$

	BSC050N03LS	BSC011N03LS
开关管导通损耗	0.36W	0.072W
开关管开通损耗	0.576W	1.334W
开关管关断损耗	0.432W	1.0W
开关管驱动损耗	0.0325W	0.085W
开关管总损耗	1.4W	2.5W

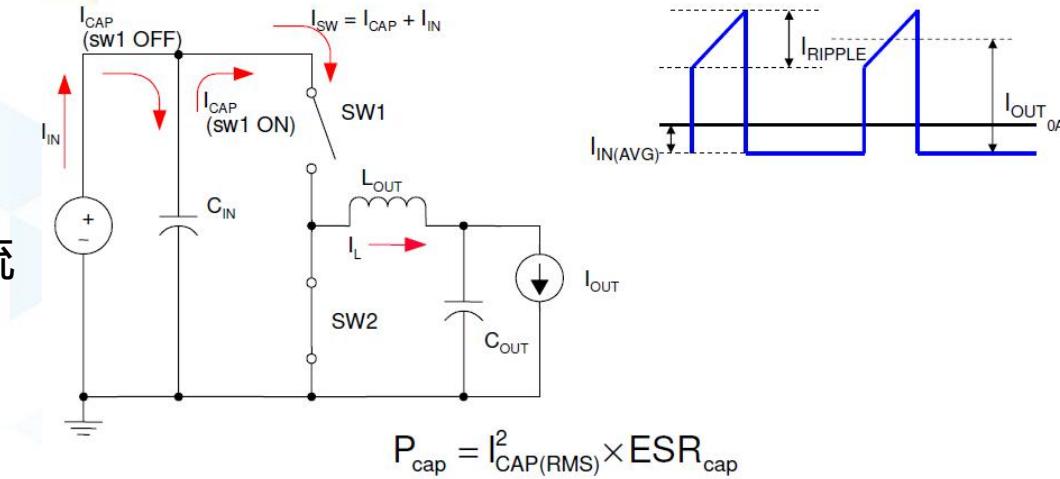
4.电容选择考虑

- 损耗
- 纹波电流的能力
- 温度范围
- 纹波电压-ESR, Capacitance, ESL
- Transient纹波
- 寿命
- 成本、尺寸

BUCK电路计算实例

输入电容选择

- 输入电容选择经常被忽视
- 电解和陶瓷的组合最佳
- 对于BUCK电路，输入电容的纹波电流大于输出电容的纹波电流
- 当D=0.5时，纹波电流最大，为一半的输出电流



BUCK电路计算实例

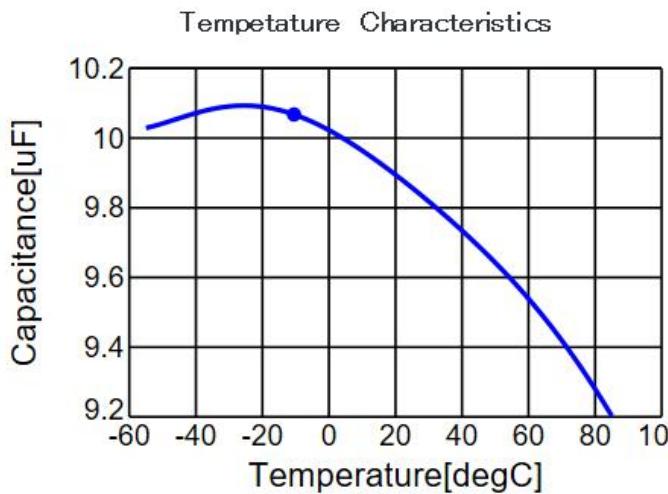
输入电容选择

$$I_{C_{IN}(RMS)} = I_{OUT(MAX)} * \sqrt{D(1 - D)} = 20 * \sqrt{0.15(1 - 0.15)} = 7.14A$$

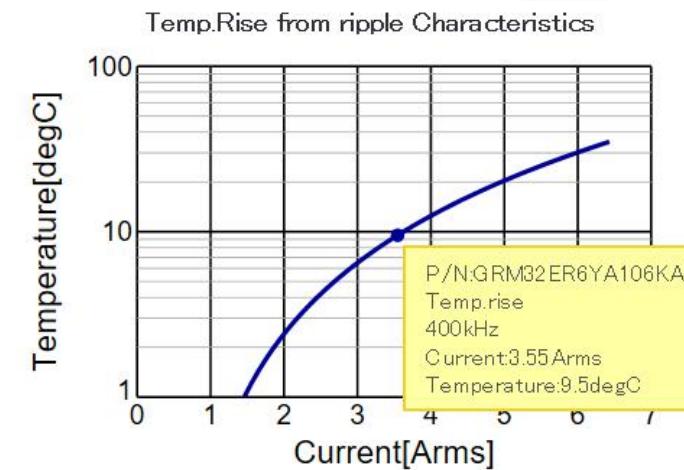
选择2个GRM32ER6YA106KA12并联+35SVPF120M OS-CON电容

关键参数：X5R,35V,10uF, 11mohm ESR

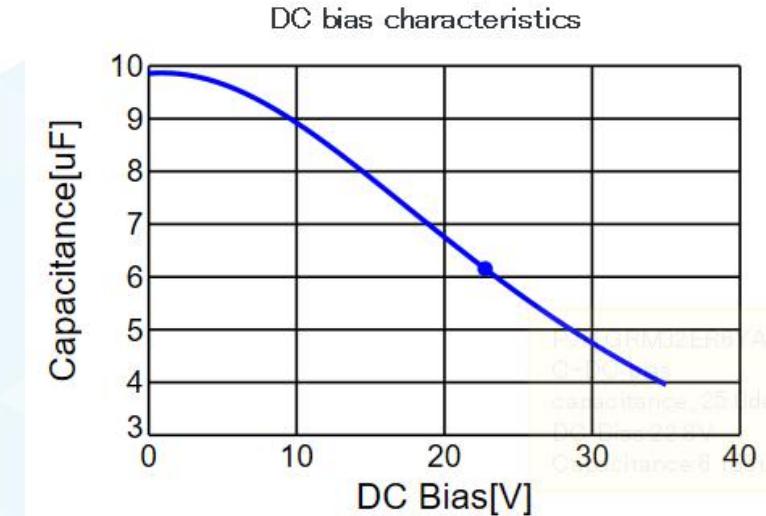
$$P_{loss} = 7.14^2 * 5.5m = 0.28W$$



GRM32ER6YA106KA12, capacitance,
DC0.0V, AC1.0Vrms



GRM32ER6YA106KA12 (80kHz 400kHz
 800kHz)



GRM32ER6YA106KA12, capacitance,
25.0degC, AC1.0Vrms

BUCK电路计算实例

输出电容选择

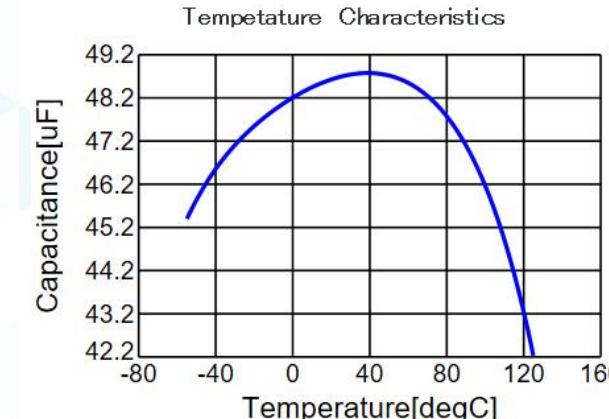
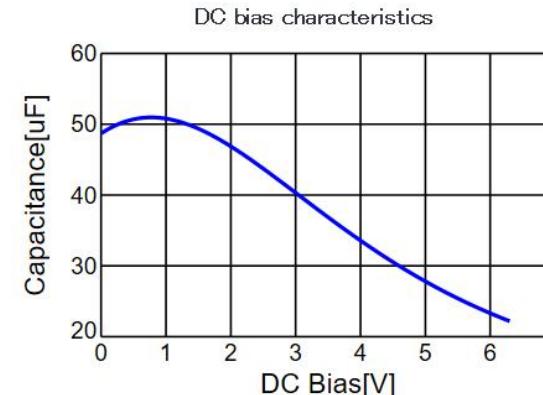
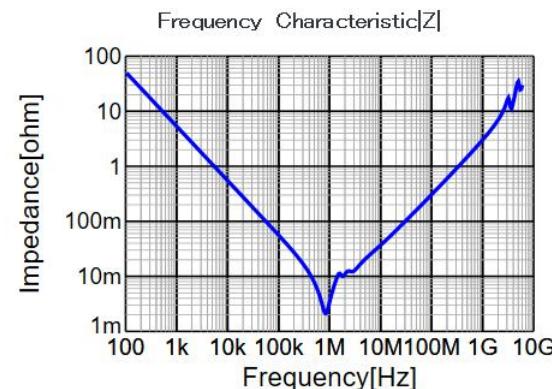
- $V_{RIPPLE} = \Delta I_L \cdot \left(ESR_{C_{OUT}} + \frac{1}{8f_S C_{OUT}} \right)$ 输出纹波，容性分量+阻性分量

选择Murata GCM32ER70J476ME19

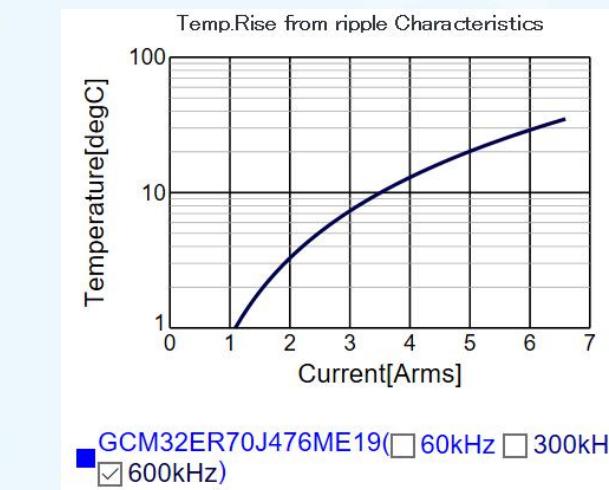
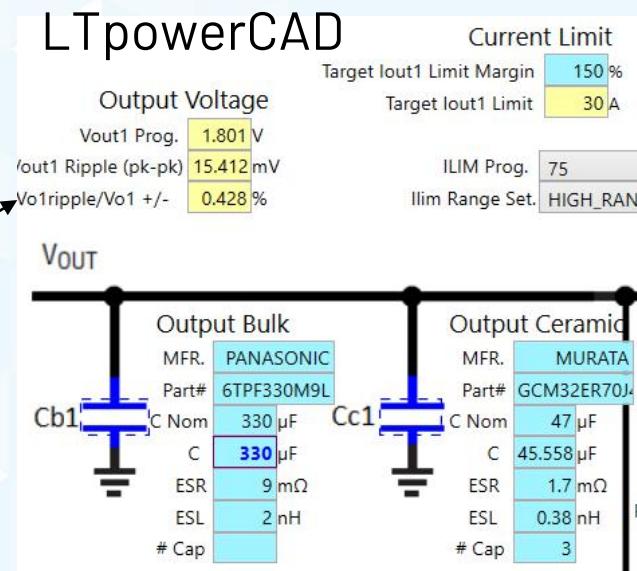
参数：20% X7R 1210 47uF 6.3V 1.7MOHM

$$V_{RIPPLE} = 8 \cdot \left(1.7m + \frac{1}{8*500k*47uF*0.8} \right) = 67mV \quad 1\text{个电容}$$

$$V_{RIPPLE} = 8 \cdot \left(1.7/3m + \frac{1}{8*500k*3*47uF*0.8} \right) = 23mV \quad 3\text{个电容}$$

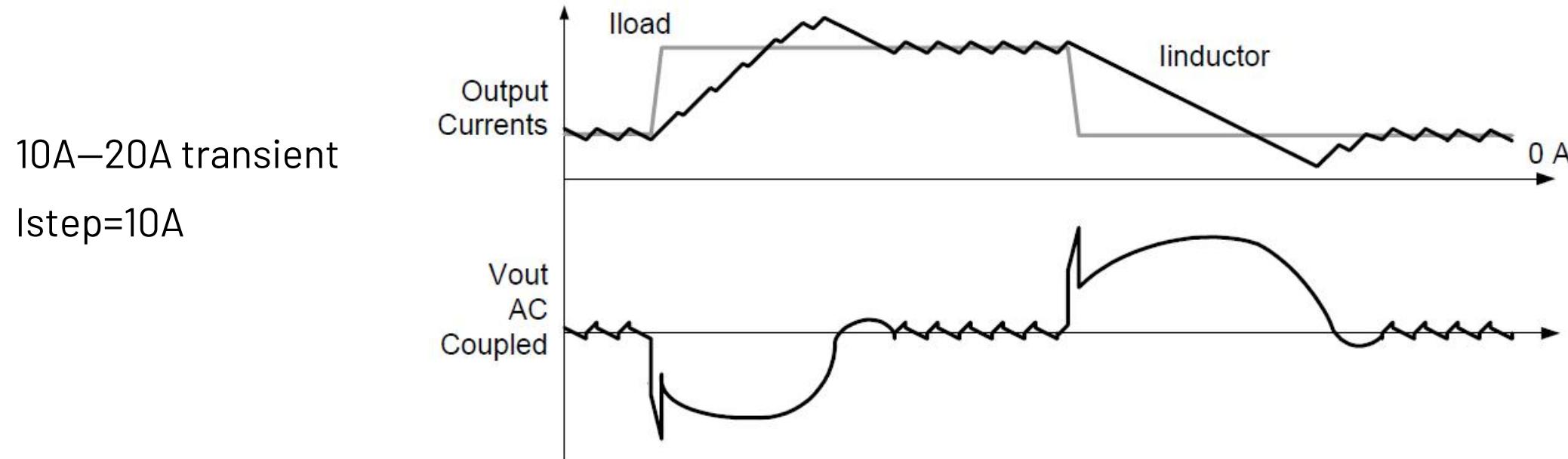


GCM32ER70J476ME19, capacitance, DC0.0V, AC0.5Vrms



输出电容选择

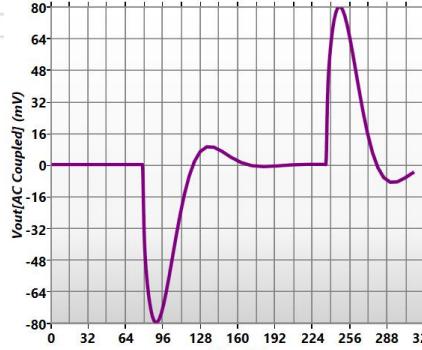
- 对于高压输出的情况，往往需要陶瓷和电解的组合
- Transient的要求往往比纹波要求高很多，往往也需要电解去hold
- 关键看环路要花多长时间去响应并让电感电流追上新的负载电流



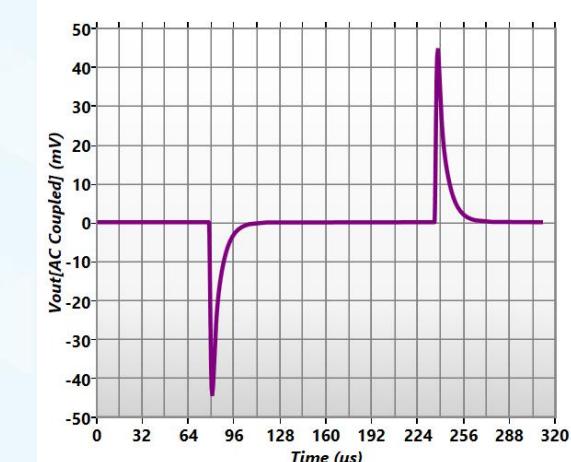
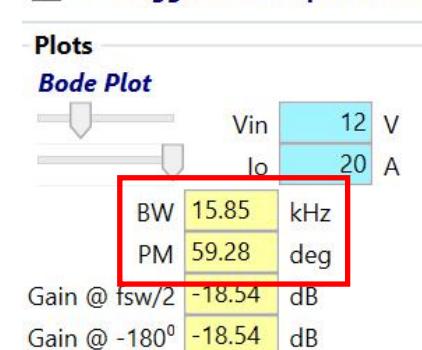
BUCK电路计算实例

输出电容选择

$I^*t=U_{under}^*C_o$ 关键时t很难计算，和环路相关，借助LTpowerCAD去选择。



3*47uF MLCC+2*330uF



Controller损耗 Rsense损耗

- 控制器主要是LDO损耗
开关管: 17nC 同步管: 34nC Fs: 500K
 $Qg * F_s = 25.5 \text{mA}$
LDO损耗: $(12 - 5) * 25.5 \text{mA} = 0.18 \text{W}$
- Rsense损耗
考虑1.5倍的额定电流为过流点, 取2毫欧
 $P_{loss} = 20^2 * 2 \text{m} = 0.8 \text{W}$
- RinSense损耗
取5毫欧

$$P_{loss} = \left(\frac{P_{in}}{V_{in}}\right)^2 * 5 \text{m} = \left(\frac{1.8 * \frac{20}{0.9}}{12}\right)^2 * 5 \text{m} = 0.05 \text{W}$$

BUCK电路计算实例

损耗总结

理论计算	Total 3.9W loss	
开关管导通损耗	0.36W	9.23%
开关管开通损耗	0.576W	14.77%
开关管关断损耗	0.432W	11.07%
开关管驱动损耗	0.0325W	0.83%
同步管导通损耗	0.408W	10.46%
同步管驱动损耗	0.085W	2.18%
体二极管损耗	0.224W	5.74%
IC LDO损耗	0.18W	4.62%
电感DCR损耗	0.2W	5.13%
电感磁损	0.273W	7.0%
Rsense损耗	0.8W	20.51%
RinSense损耗	0.05W	1.3%
输入电容损耗	0.28W	7.18%

0.3W

数据来自厂家网站

基本match

LTpowerCAD计算值

- Control Fet Conduction (0.355W,9.27%)
- Control Fet Turn On (0.566W,14.78%)
- Control Fet Turn Off (0.302W,7.89%)
- Control Fet Driving (0.036W,0.94%)
- Sync Fet Conduction (0.403W,10.52%)
- Sync Fet Driving (0.093W,2.43%)
- Sync Fet Body Diode (0.245W,6.4%)
- IC LDO (0.18W,4.7%)
- Inductor DCR (0.202W,5.27%)
- Inductor Core (0.273W,7.13%)
- Rsense (0.81W,21.15%)
- RinSense (0.055W,1.44%)
- Cin Losses (0.31W,8.09%)

中级第八讲：电源 PCB布局、布线、 调试要点及注意事 项



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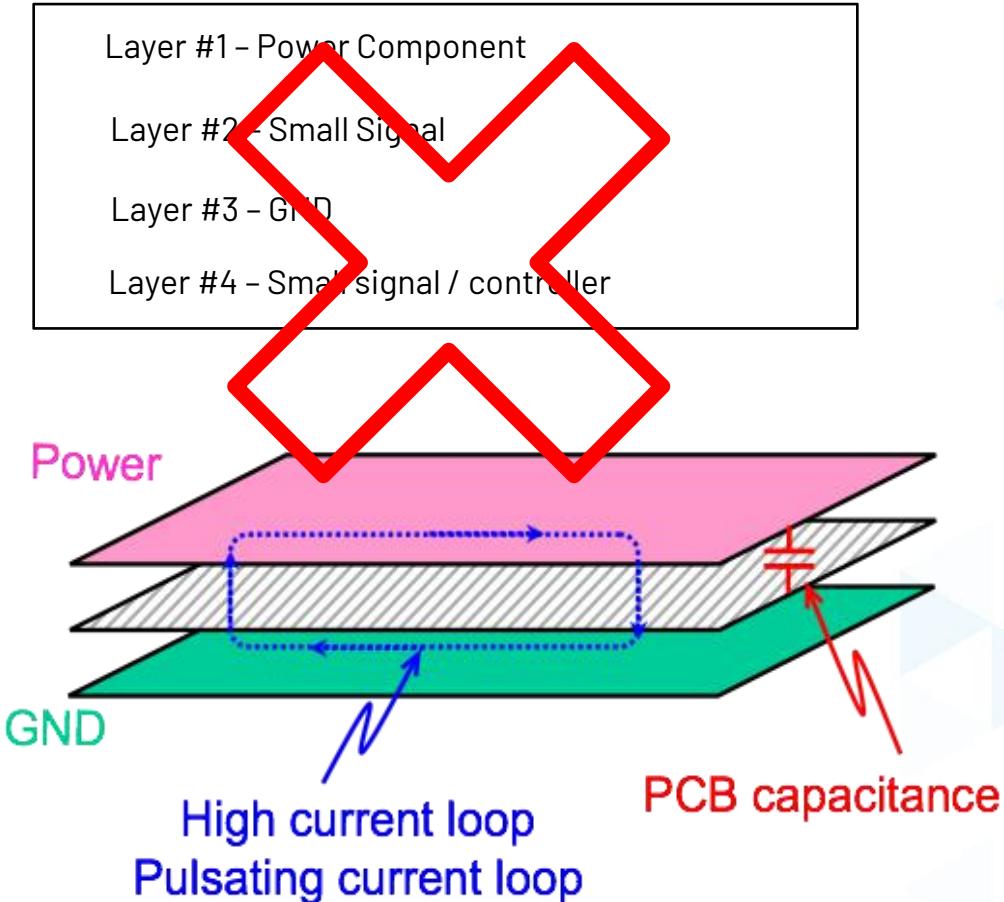
- 功率部分
- 信号部分
- MOSFET 驱动部分
- 实例

几个建议及忠告

- 电源工程师必须与PCB Layout工程师紧密合作以应对极具挑战的电源设计
- 在系统设计布局规划上，电源电路应该尽可能靠近负载电路
- 散热回路应该尽可能靠近电源电路以减少热阻
- 选择正确的板层数量和铜厚
- 在有散热对流的板上，注意大尺寸的被动器件（电感，大电容）布局，不要阻碍芯片和MOSFET的空气对流

板层堆叠问题

哪一种板层堆叠设计最优?

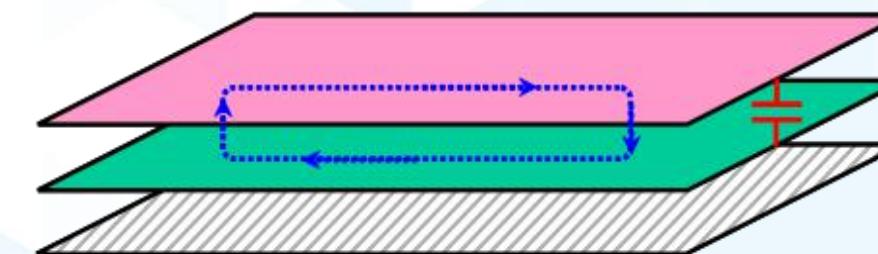


Layer #1 - Power Component

Layer #2 - GND

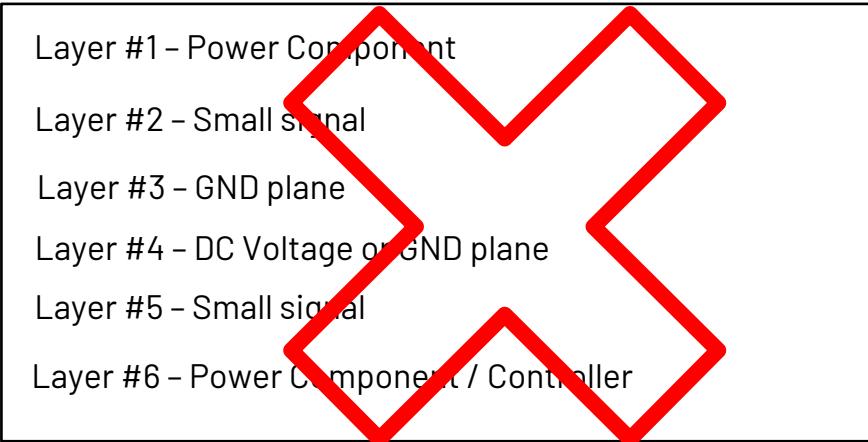
Layer #3 - Small Signal

Layer #4 - Small signal / controller



放置一个地平面紧邻电源层以获得最小的环路阻抗，
然后再考虑其它小信号层

哪一种板层堆叠设计最优?



阻抗基准：

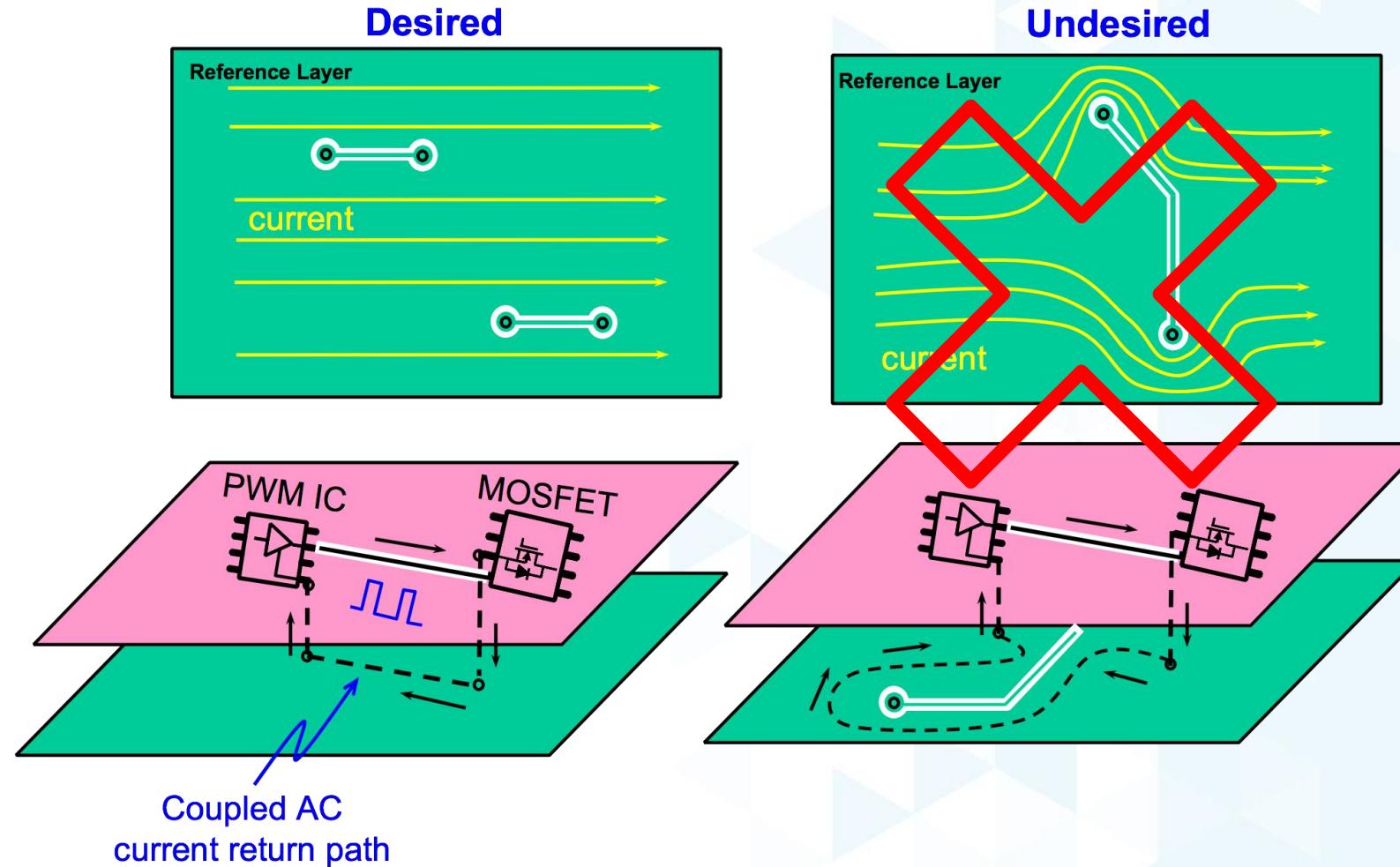
通常选择直流电源或地平面作为交流参考平面。

一个基本的准则：

一般情况下，不应分割多层PCB设计的参考平面。

电路板布局及走线

如果小信号走线不得不在参考层走线：
请选择对阻抗影响最小的走线而非横跨走线以降低电源参考层的阻抗



铜厚和宽度计算

Copper resistivity (Ohm/cm): $S(T) = 1.724 \cdot 10^{-6} \cdot [1 + 0.0039 \cdot (T - 20)]$
铜电阻率

T - Copper temperature in °C

Resistance of copper
铜电阻

$$R(T) = \frac{S(T)[\Omega / cm] \cdot Length[cm]}{Width[cm] \cdot Thickness[cm]}$$

$$= \frac{S(T)[\Omega / cm] \cdot \frac{1000mils}{2.54cm} \cdot Length[mils]}{Width[mils] \cdot Thickness[mils]}$$

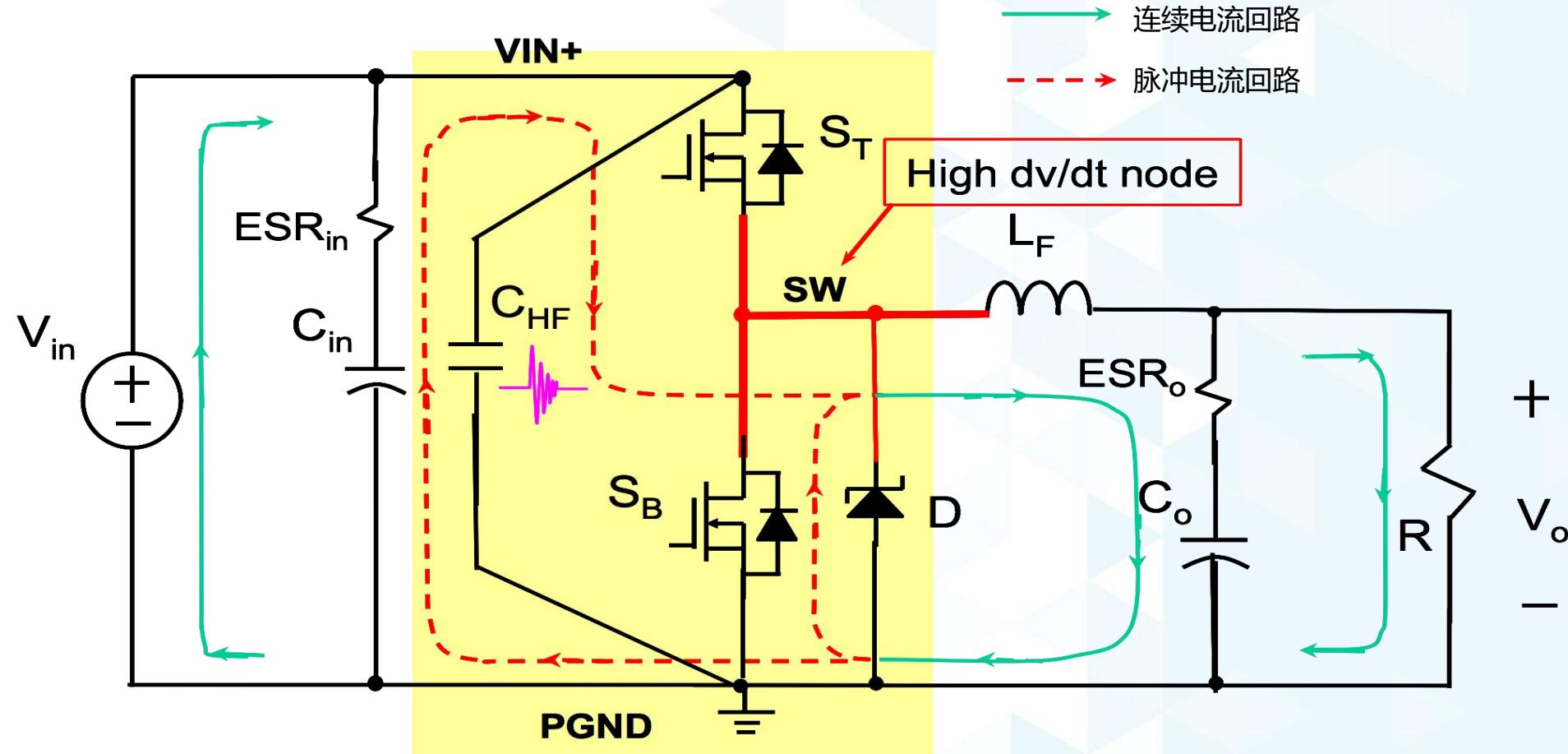
0.5 Oz 铜厚 = 0.7 mil = 17.78 μM
1.0 Oz 铜厚 = 1.4 mil = 35.56 μM
2.0 Oz 铜厚 = 2.8 mil = 71.12 μM
4.0 Oz 铜厚 = 5.6 mil = 142.24 μM

范例: 10z 铜厚(1.4 mil 厚度), 50mils线宽 (1.27mm线宽) , 2000mils线长 (50.8mm 线长), at 70 °C with 2A current:

$$R_{copper} = 23 m\Omega, V_{copper} = 46 mV, P_{loss} = 0.92 W$$

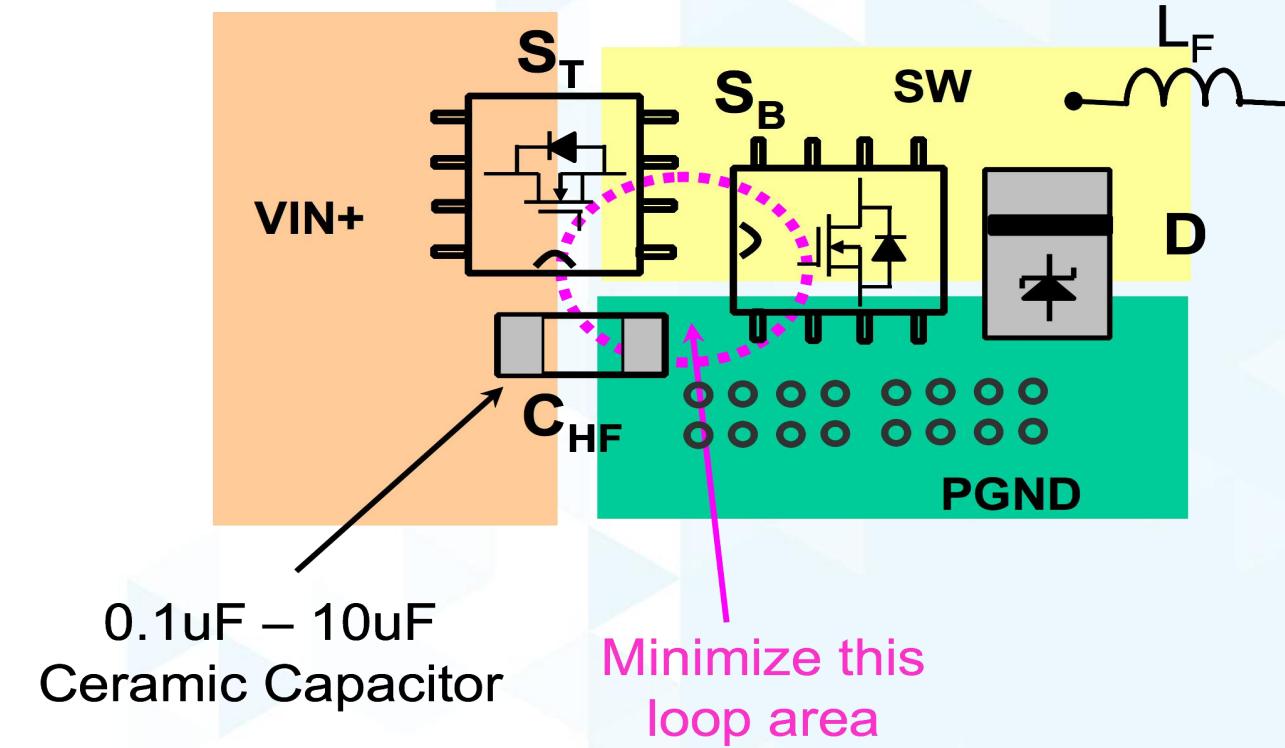
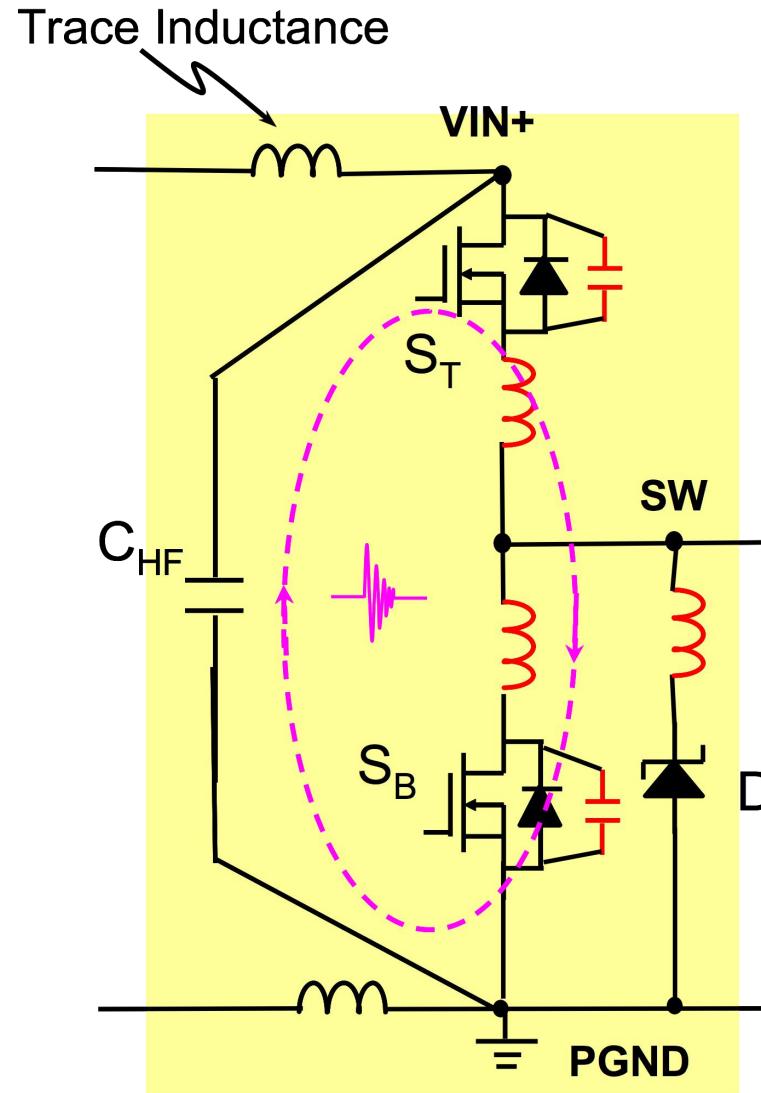
对于所有功率系统设计，推荐使用20z甚至更厚的铜厚

BUCK电路布局及走线



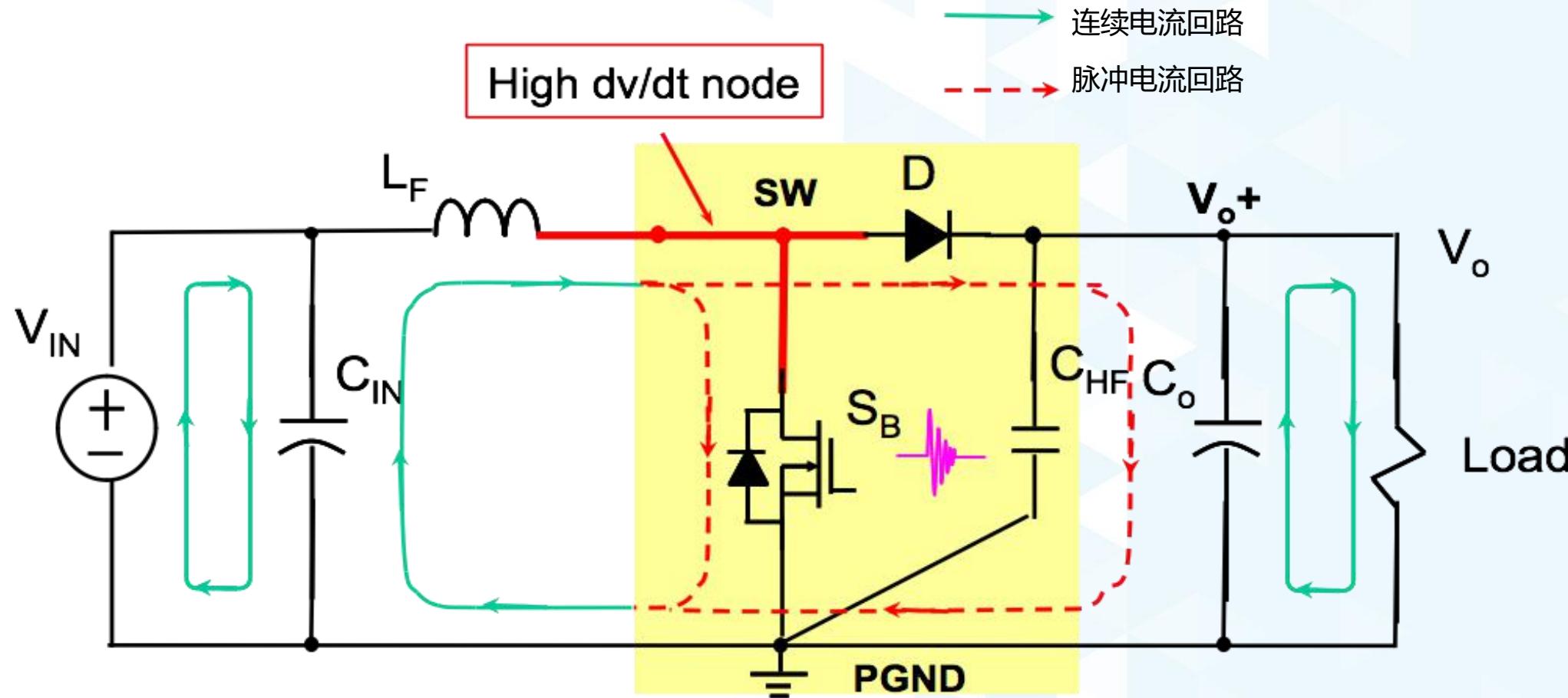
- 找到连续电流和断续电流的回路
- 特别注意使得流过脉冲电流的回路面积最小， dV/dt 的开关点与其他线路隔开

BUCK电路布局及走线



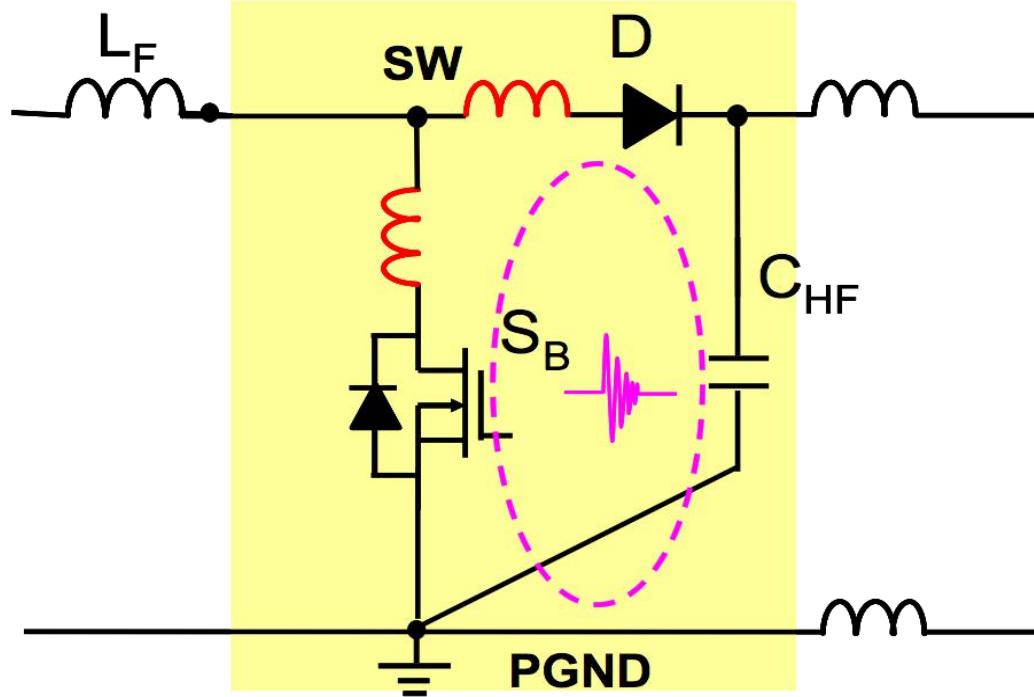
- 高频滤波电容与MOSFET尽可能靠近放置
- 尽可能使高频滤波电容、MOSFET的上管、下管在同一层面
- 放置多个过孔降低功率回路的阻抗

BOOST电路布局及走线

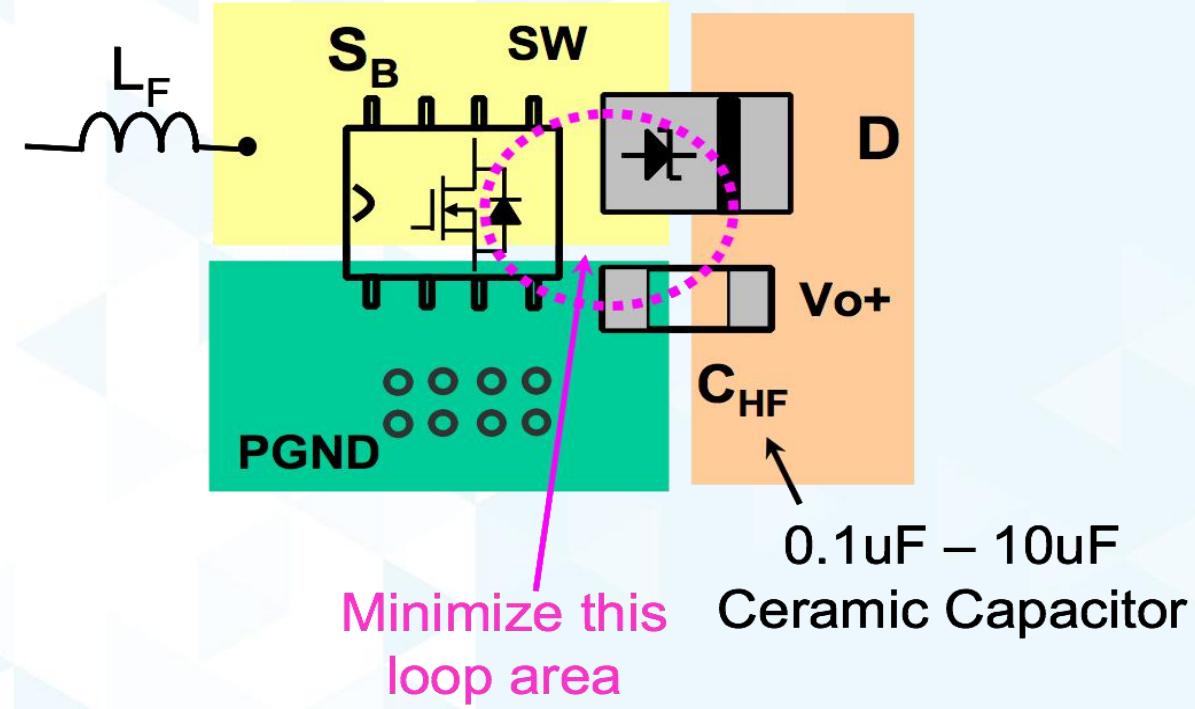


- 输出侧的脉冲电流回路所围的区域应尽可能小

BOOST电路布局及走线



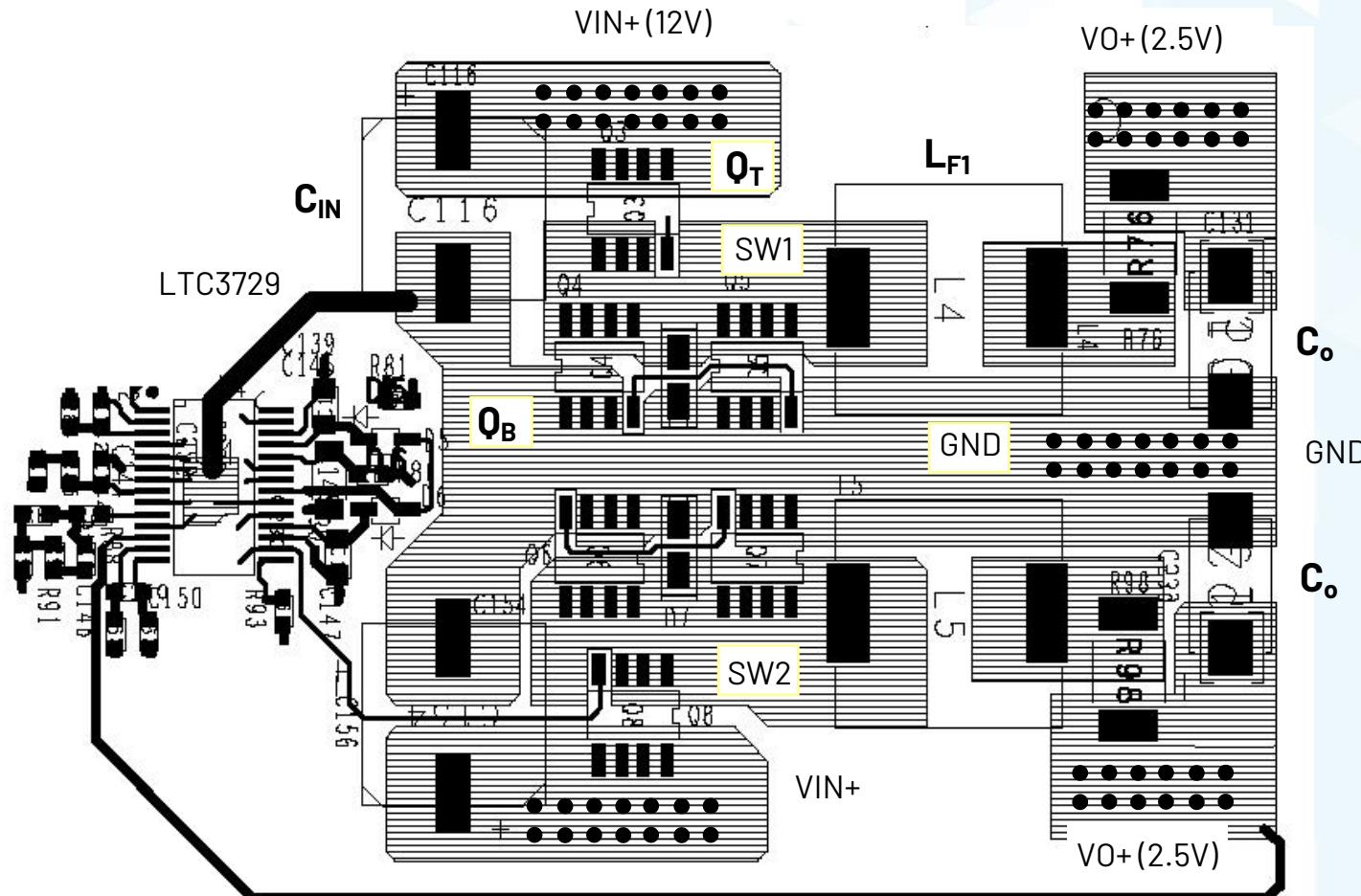
(a)



(b)

- 输出侧的脉冲电流回路所围的区域应尽可能小

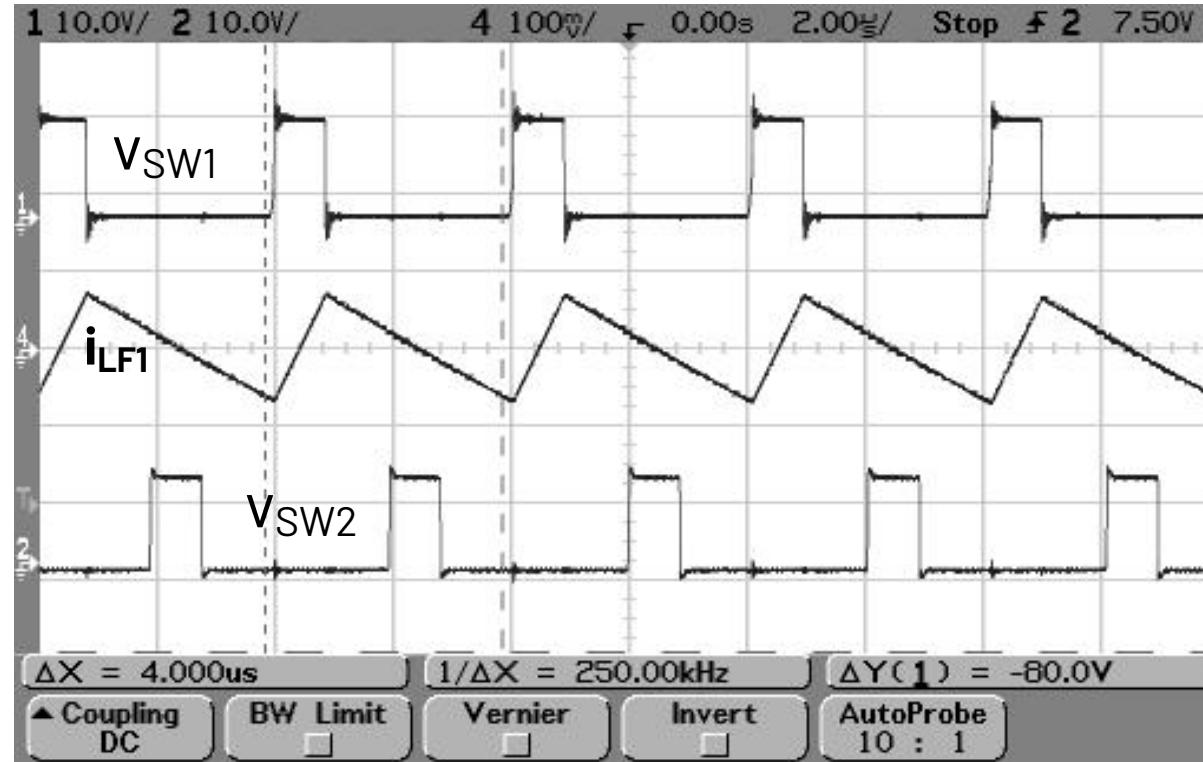
高频噪声问题



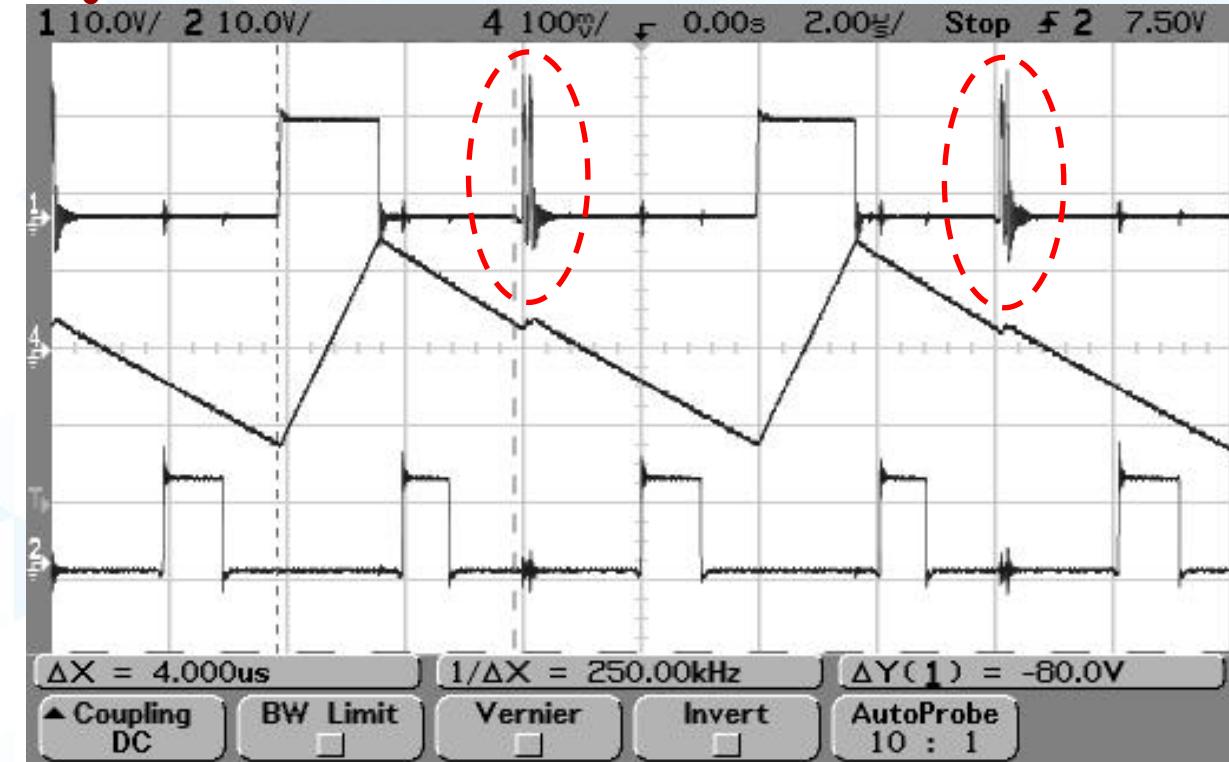
高频噪声问题

高频噪声问题@重载

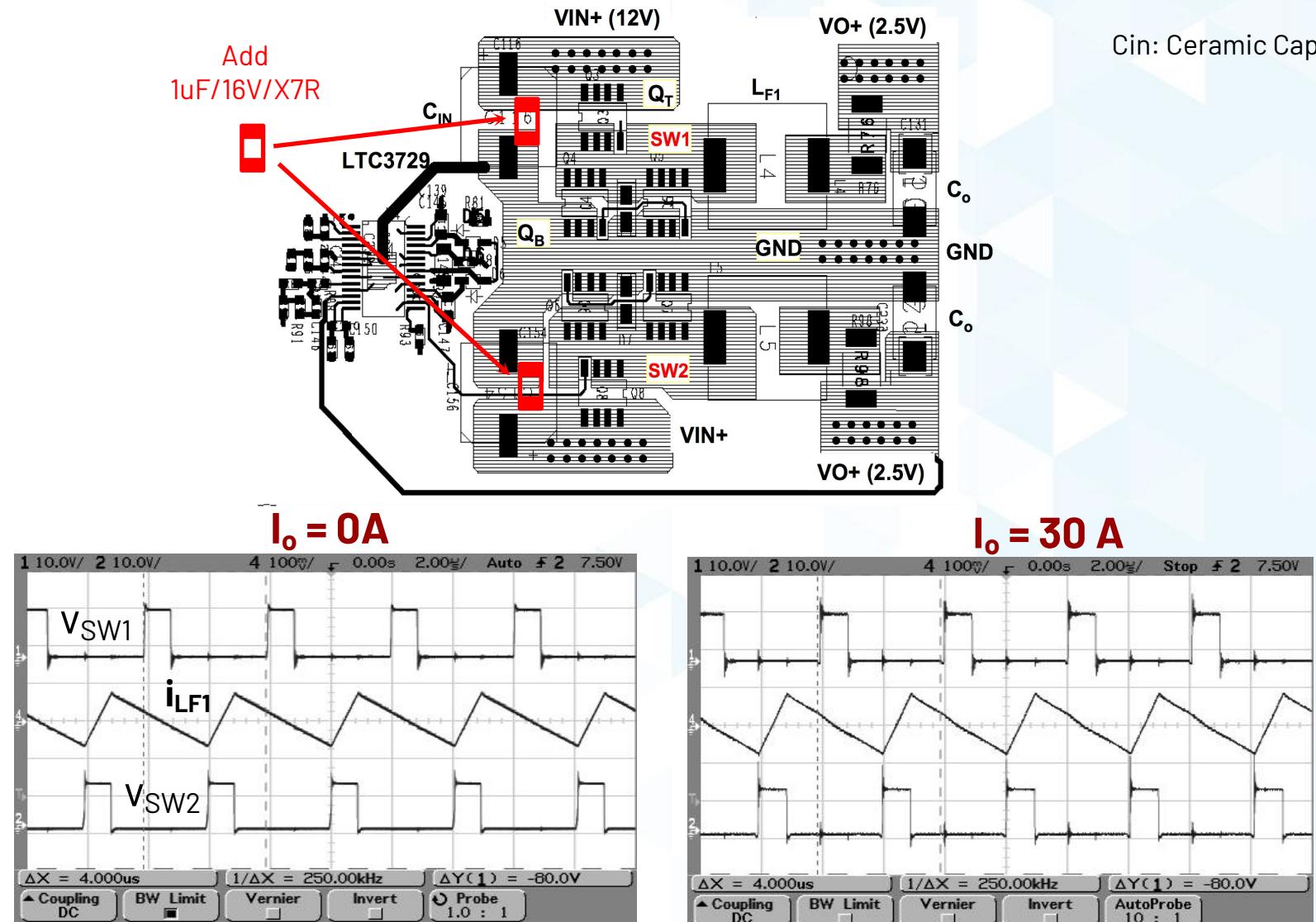
$I_o = 0A$



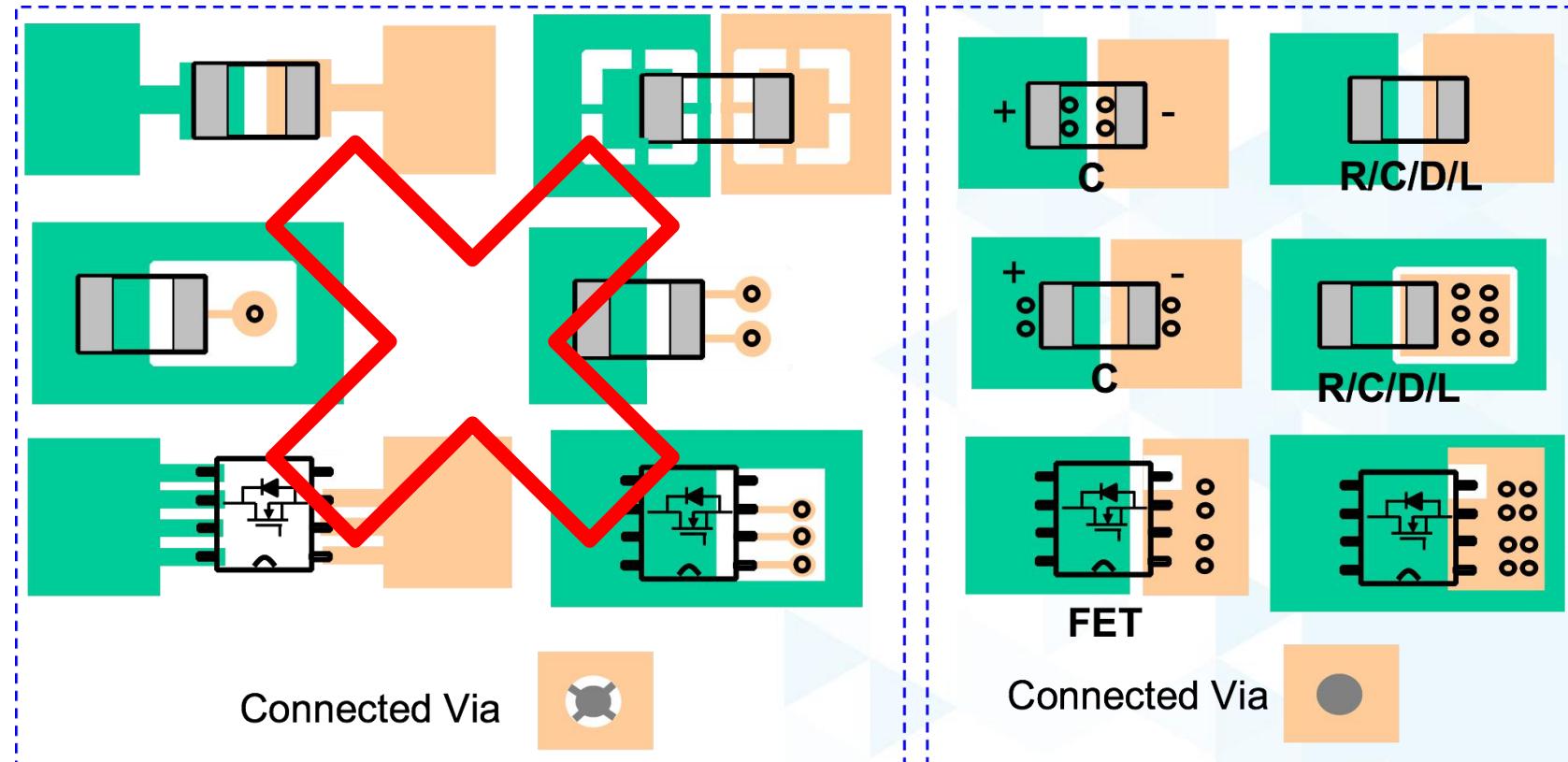
$I_o >= 13.3 A$



高频噪声问题

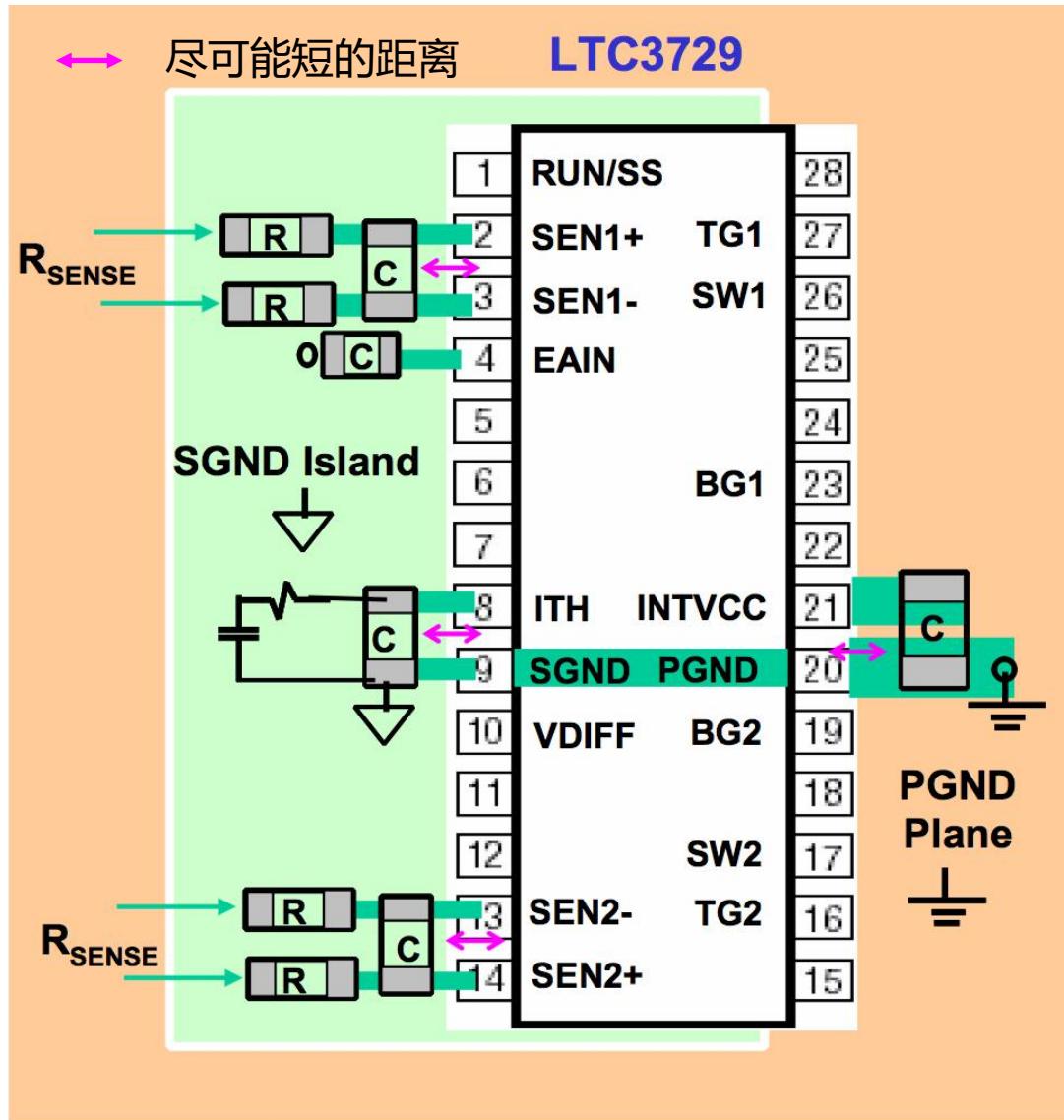


电路板布局及走线



- 功率器件铺铜尽可能宽、短
- 层间连接用多个过孔降低阻抗
- 功率元件焊盘与铜箔的连接禁止用很细的走线或者十字连接
- 尽可能降低走线的阻抗

去耦电容与分割地平面



- 以下信号对地参考使用信号地**SGND**:

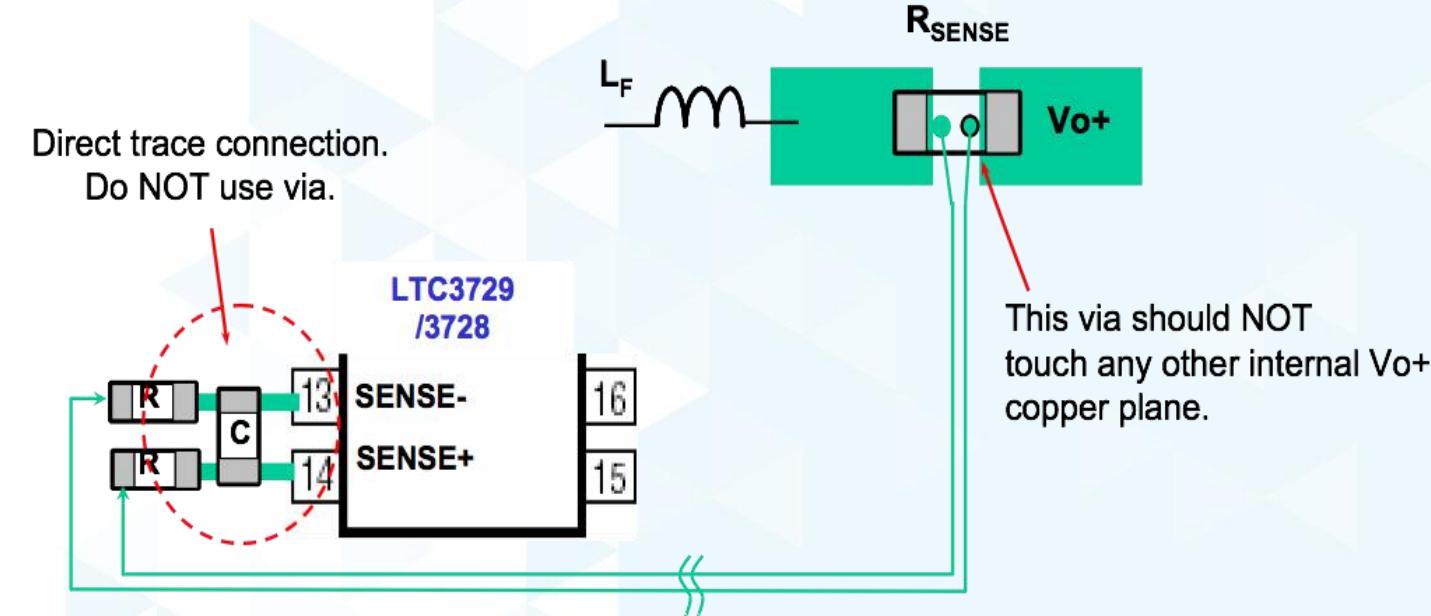
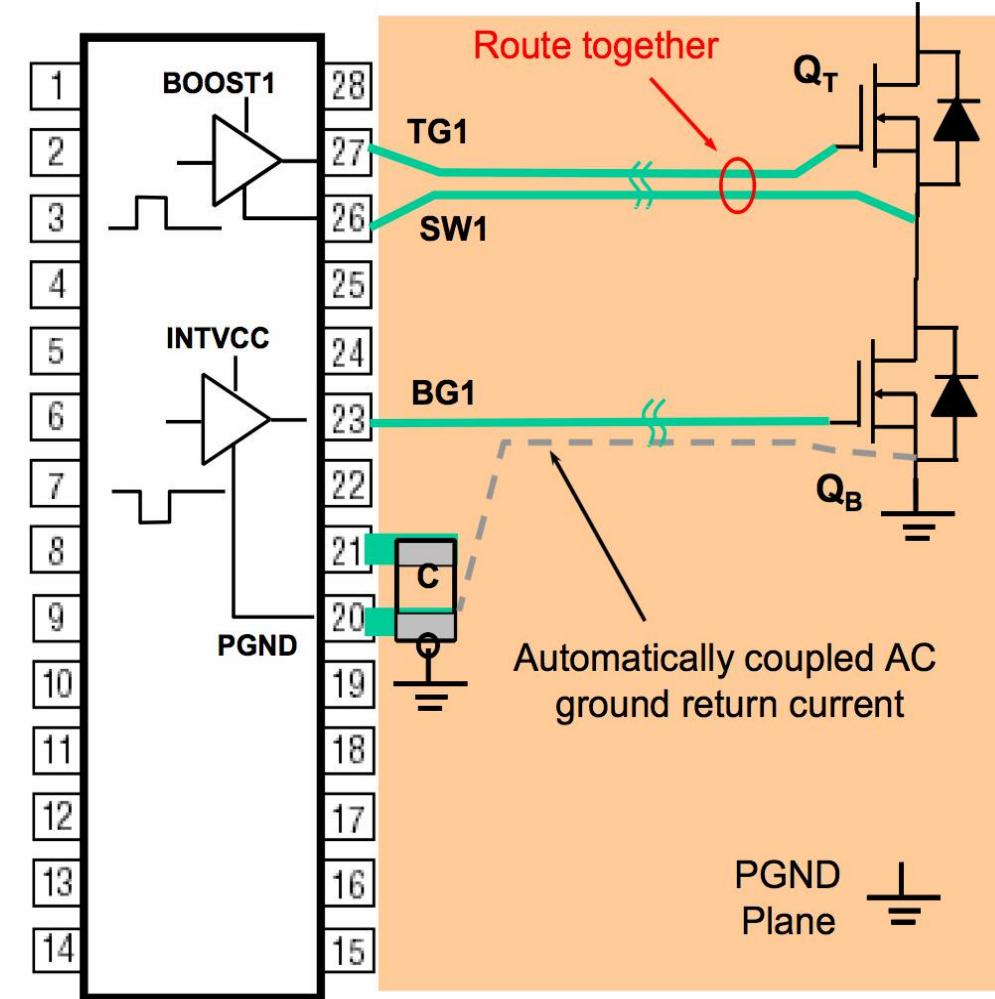
- EAIN, RUN/SS, ITH, UVADJ, PHAMD,
- PLLIN, PLLFTR, FCB, CLKOUT

- 以下信号对地参考使用功率地**PGND**:

- BOOST, +5V, PGND, INTVCC

信号地**SGND**和功率地**PGND**, 可以在芯片下方单点连接在一起

走线注意事项



凯尔文连接

- 远离噪声高的走线或铺铜区域
- 或者用地平面来屏蔽外部干扰

• 最敏感的走线

电流采样(Sense+/-), 误差放大器输入引脚(Vfb), 误差放大器输出引脚(ITH or VComp), SGND

- Sense+ / - 尽量成对走线, 或走差分线
- 走线空间尽量小, 滤波电容靠近芯片引脚, 滤波电阻靠近滤波电容。
- 其他敏感信号远离噪声大的走线

特别注意Vfb的连接和走线

• 比较敏感的走线

**远端输出电压侦测运放的输入 / 输出 (Vos+/-, Diffout),
同步脉冲输入端 (PLLFR), 同步脉冲输出端 (CLKOUT)**

- 同步脉冲输出端 (CLKOUT) 是一个敏感信号, 同时也是噪声较高的信号, 与其他的小信号走线分开。

• 噪声最大的走线

SW, TG, BOOST, BG

- 与其他的敏感走线分开
- 在相邻的两层上避免SW铺铜与敏感走线重叠
- SW和TG走线尽量近的走线或差分线, 以降低回路的阻抗

**输入路径，输出路径，大电容布局，
层数规划、分层规划、铜箔厚度。**

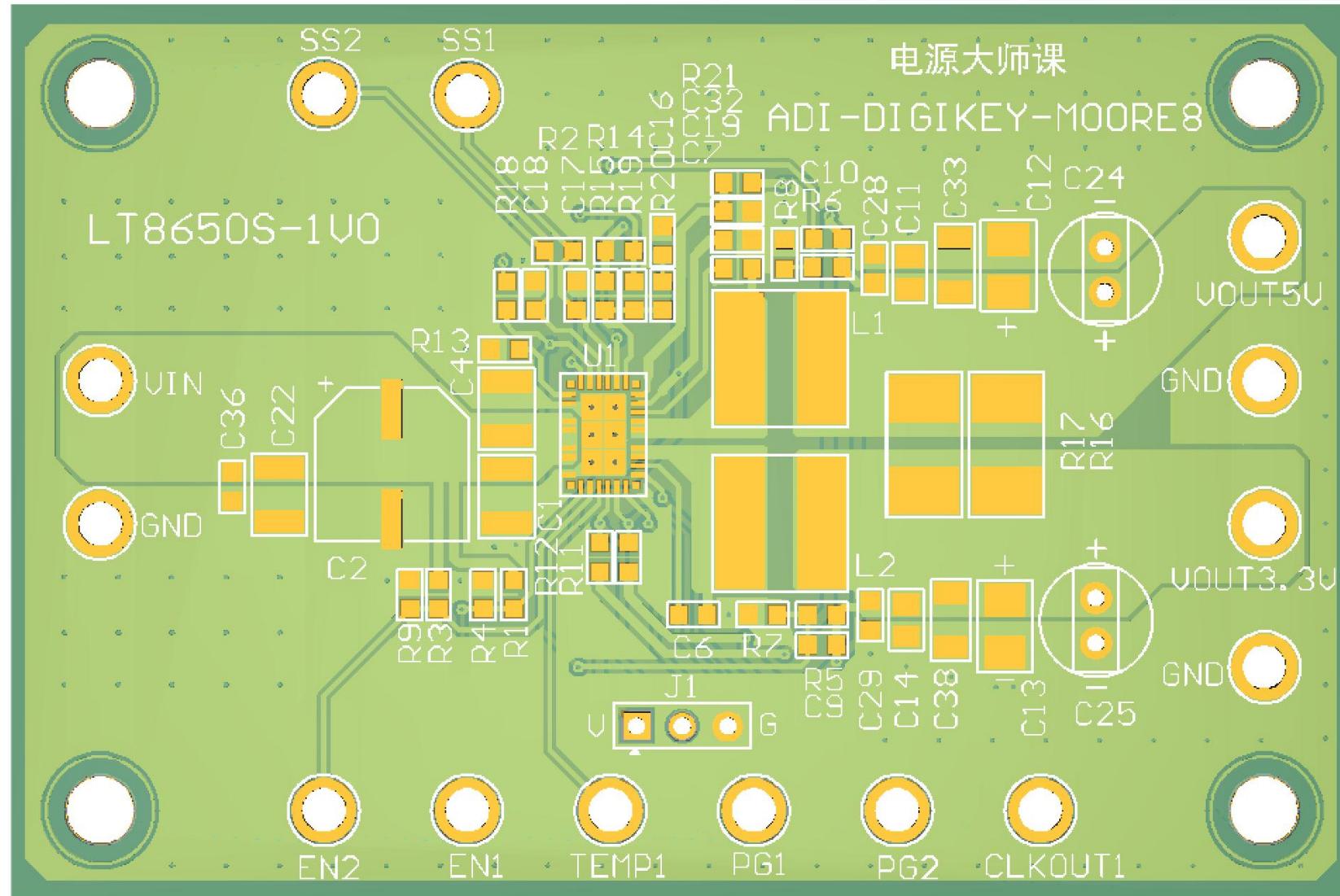
• 功率部分

- 功率器件摆放
- 铺铜规划
- 找出有电流断续的回路
- 去耦电容距离MOSFET近
- 大电流走线短、宽，过孔多

• 控制器部分

- 去耦电容距离芯片近
- SGND、PGND分开
- 电流采样电路
- 敏感走线、噪声高的走线分开
- 驱动信号走线
- 选择合适的线宽

布局走线分析范例



中级实战题目：低 静态电流，低噪声 bUCK电路设计实践

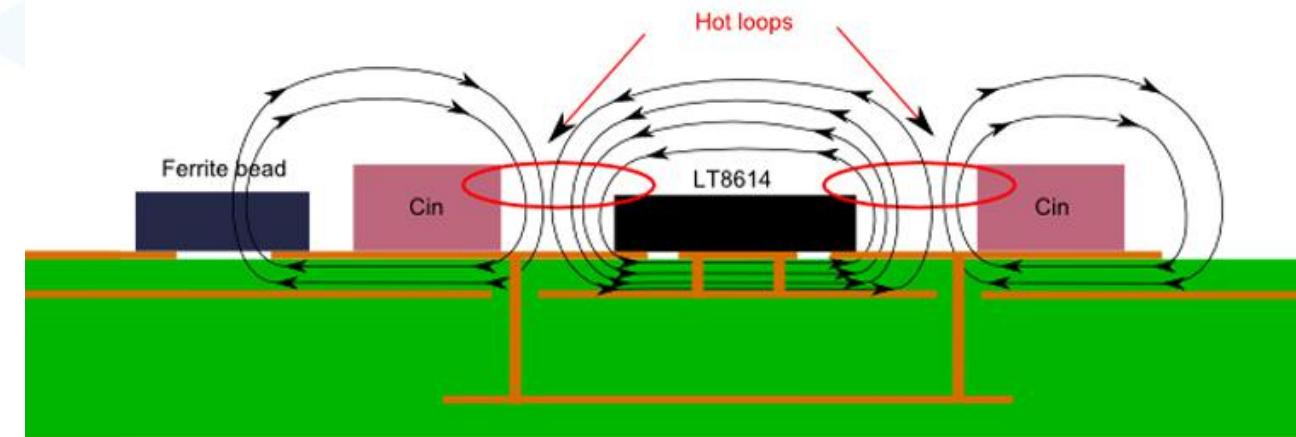
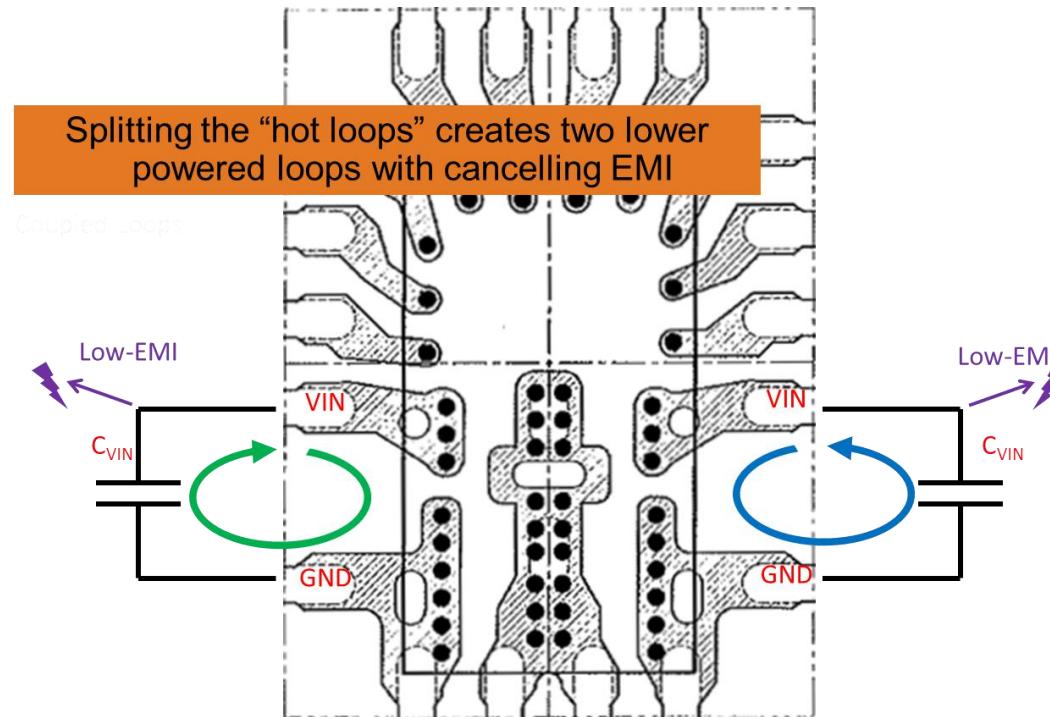


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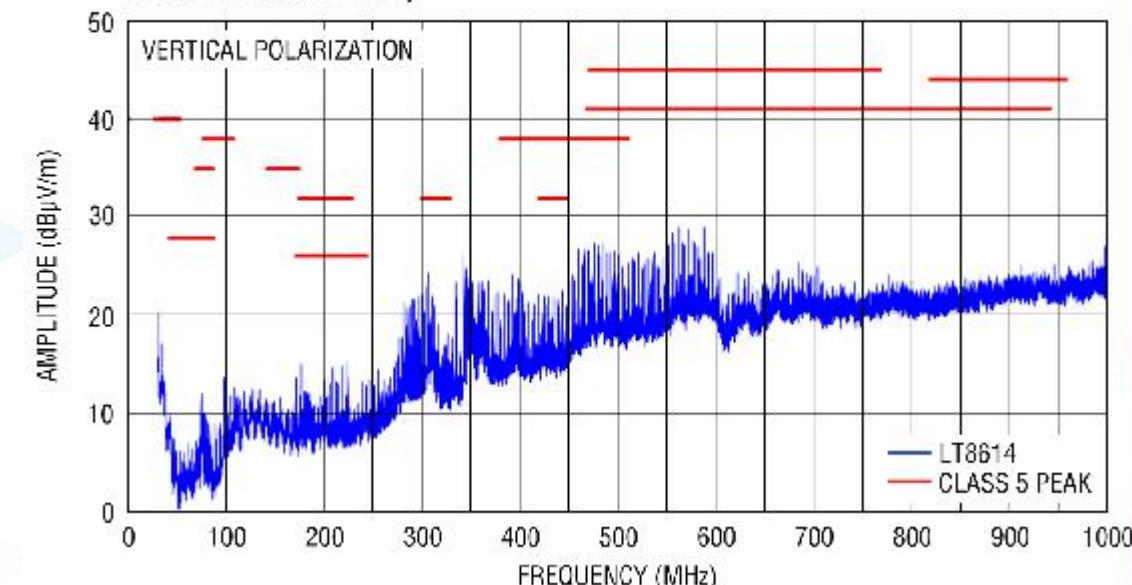
设计一个BUCK降压DC/DC电源

- ▶ 如何实现一个小于10mV纹波 (50%阻性负载)
- ▶ 如何实现一个小于5uA待机电流
- ▶ 如何设计一个转换效率在93%以上

创新技术 - 低 EMI 开关电源



Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



- ◆ The two high current loops cancel each others magnetic field, almost like enclosing the circuit in a metal box

Silent Switcher Platform – Innovations To Deal with Hot Loop

- ▶ Buck regulator platform
 - 20dB EMI improvement – No compromise in efficiency and size!
- ▶ Offers customers:
 - High frequency
 - High efficiency
 - High current
 - Low EMI noise
 - Solder joint reliability
- ▶ Technologies
 - Circuits
 - Process/devices
 - Package
 - In-package passive

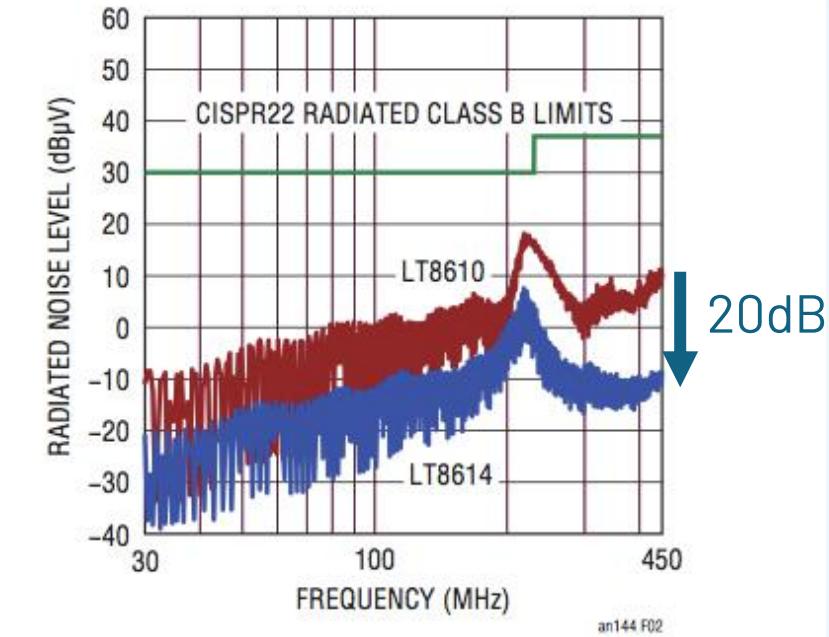
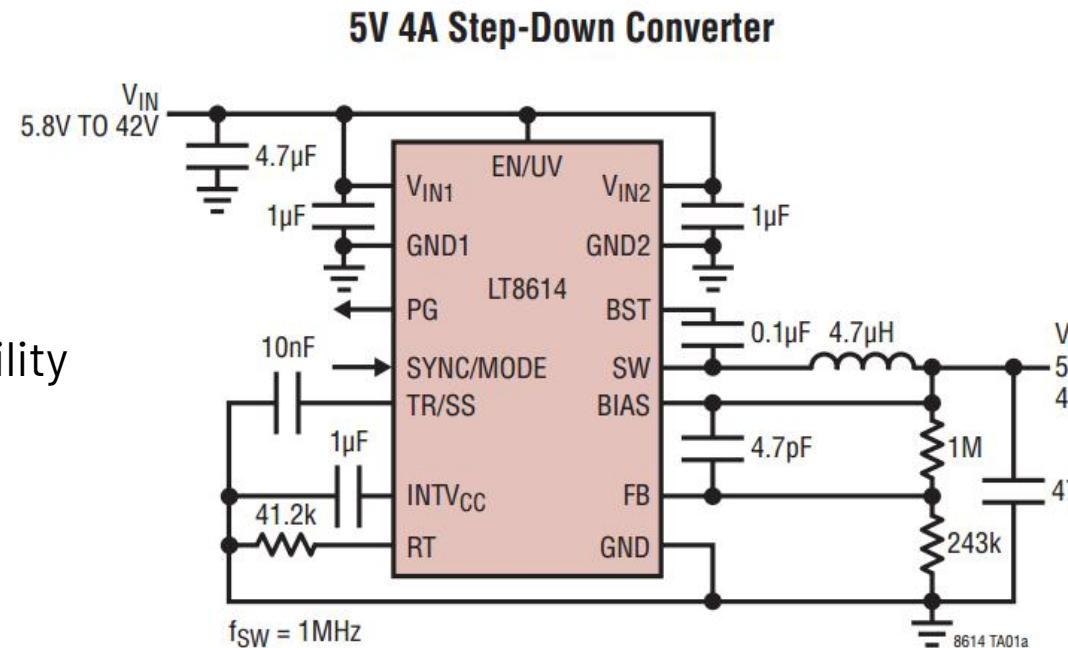
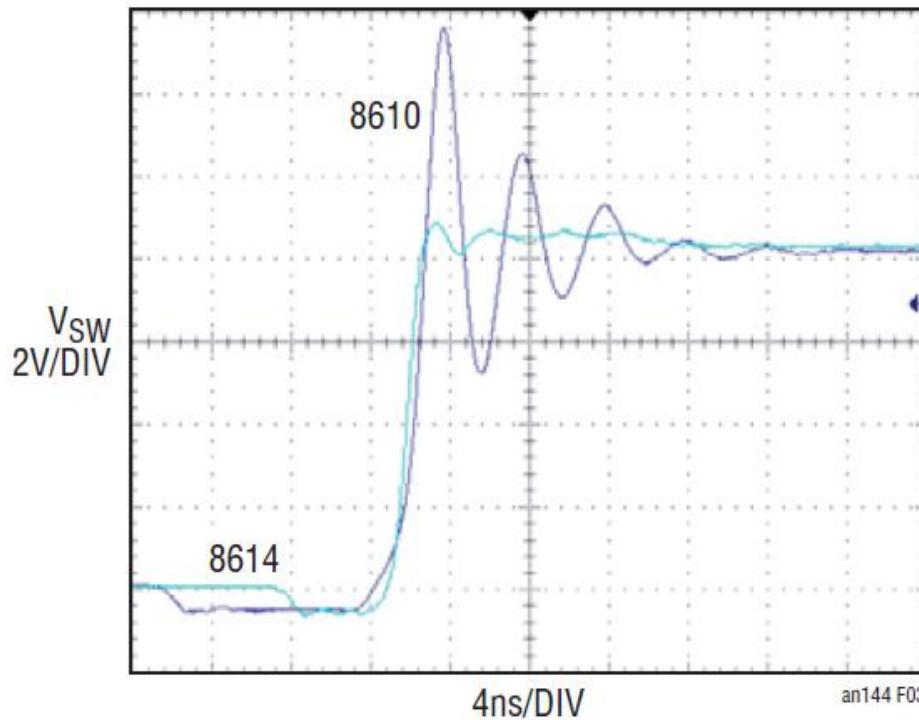


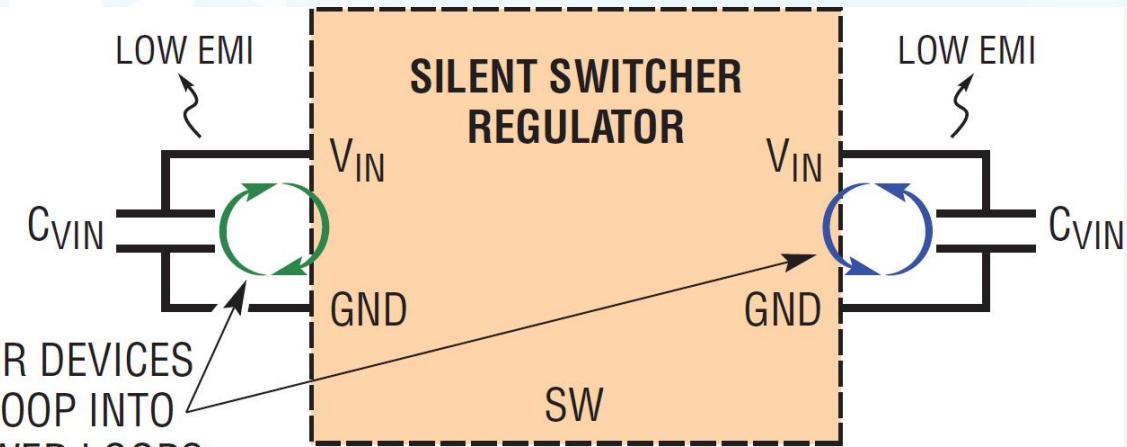
Figure 2. LT8610 and LT8614 700kHz 14V to 3.3V 2A Radiated EMI in GTEM Corrected for OATS

Silent Switcher Eliminates Switch Ringing

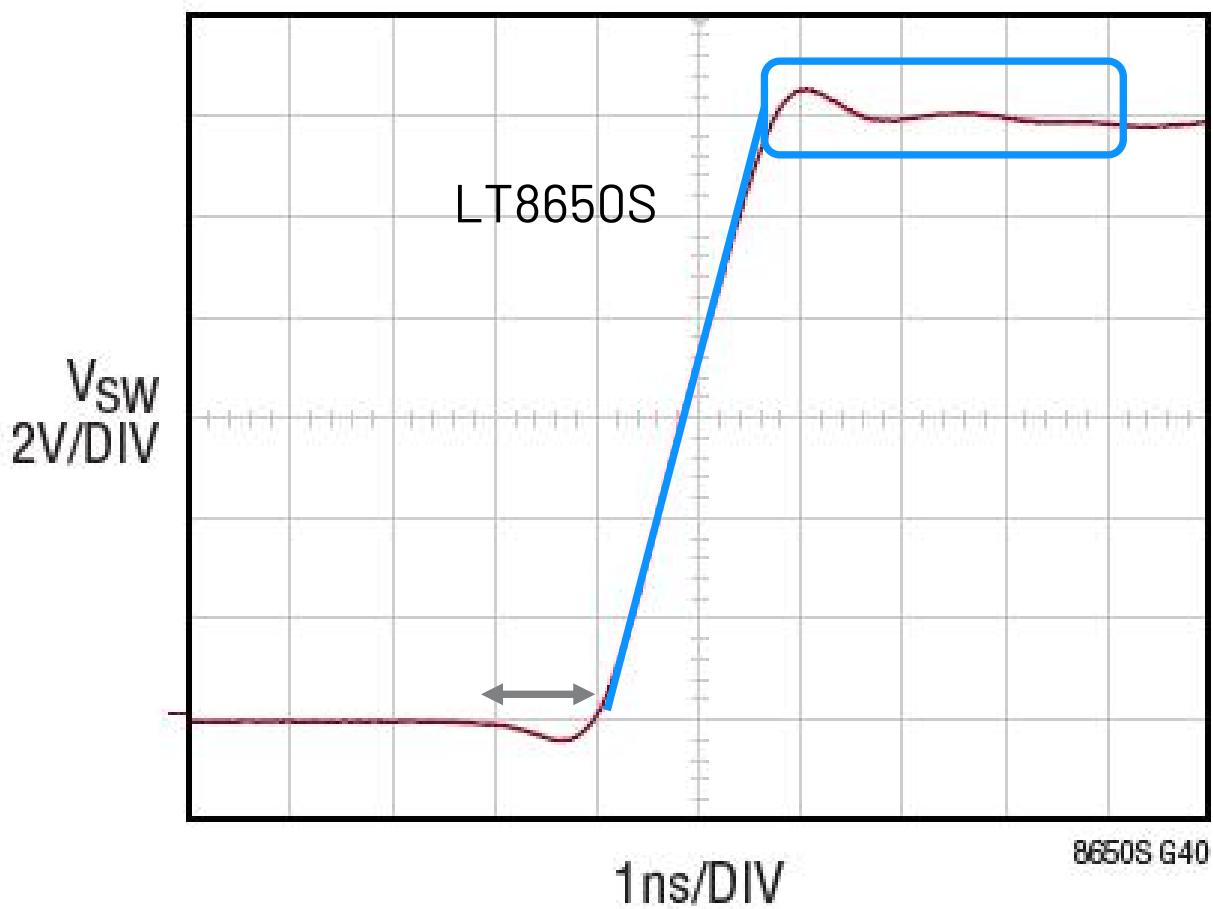
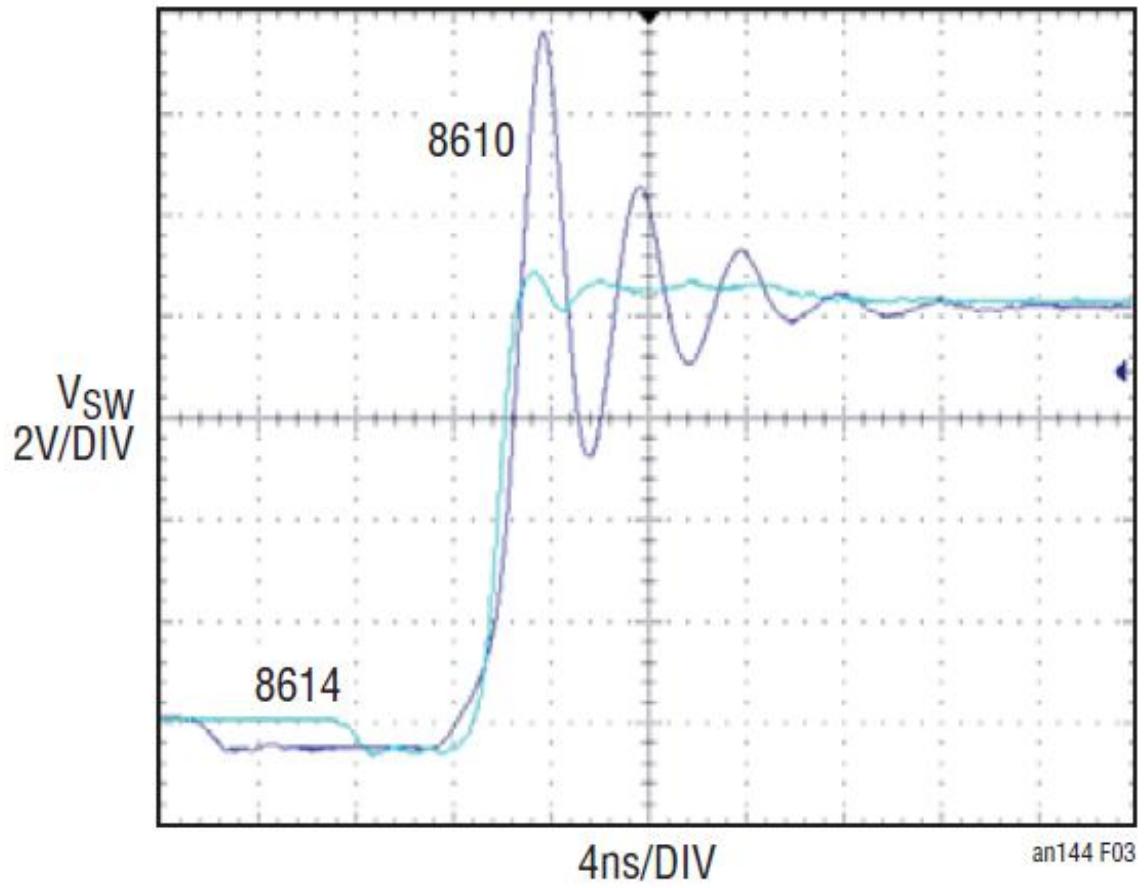


t_e

SILENT SWITCHER DEVICES
SPLIT THE HOT LOOP INTO
TWO LOWER POWER LOOPS
WITH MUTUALLY CANCELLING
MAGNETIC FIELDS



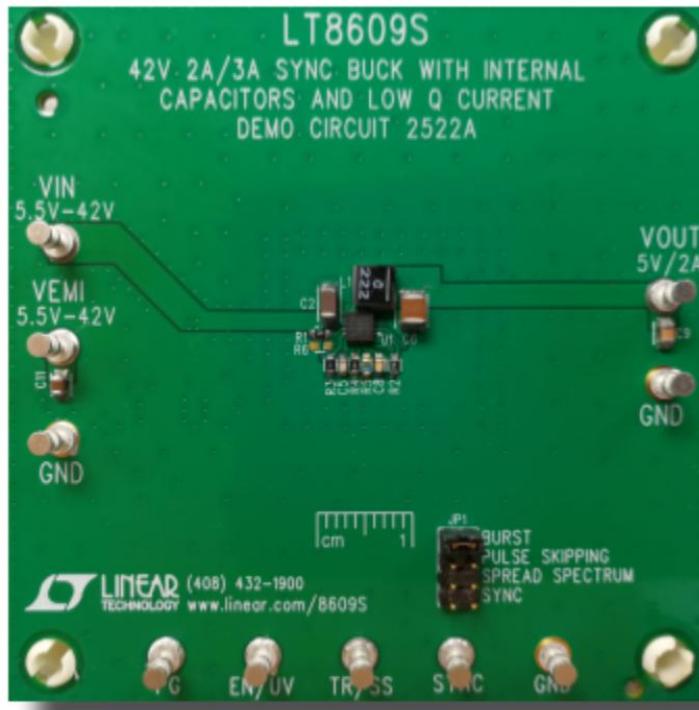
Pushing Performance Further



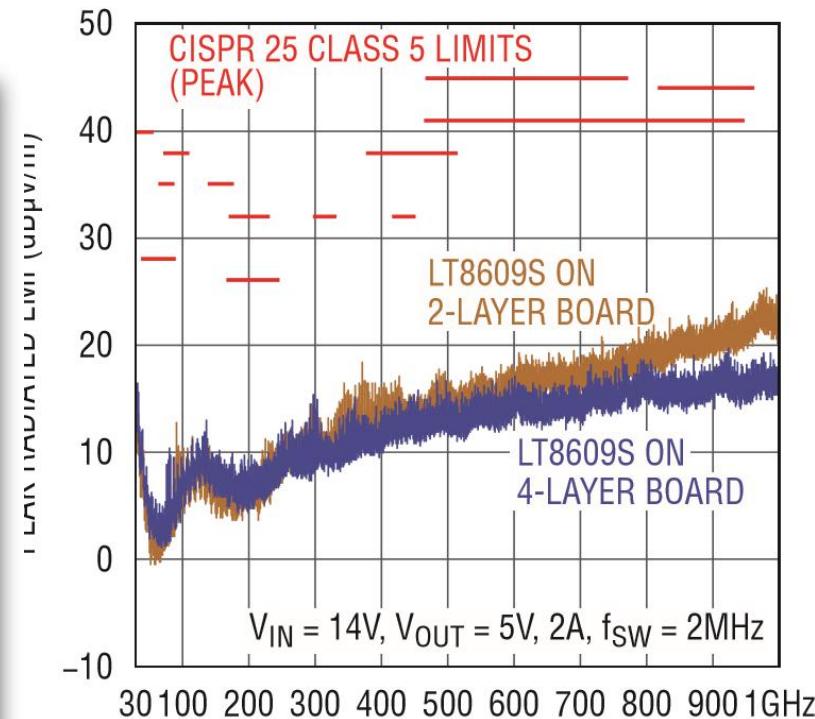
二层板也能实现低 EMI 设计

Spacing Between Layer 1 and GND Layer 2 is not as Critical

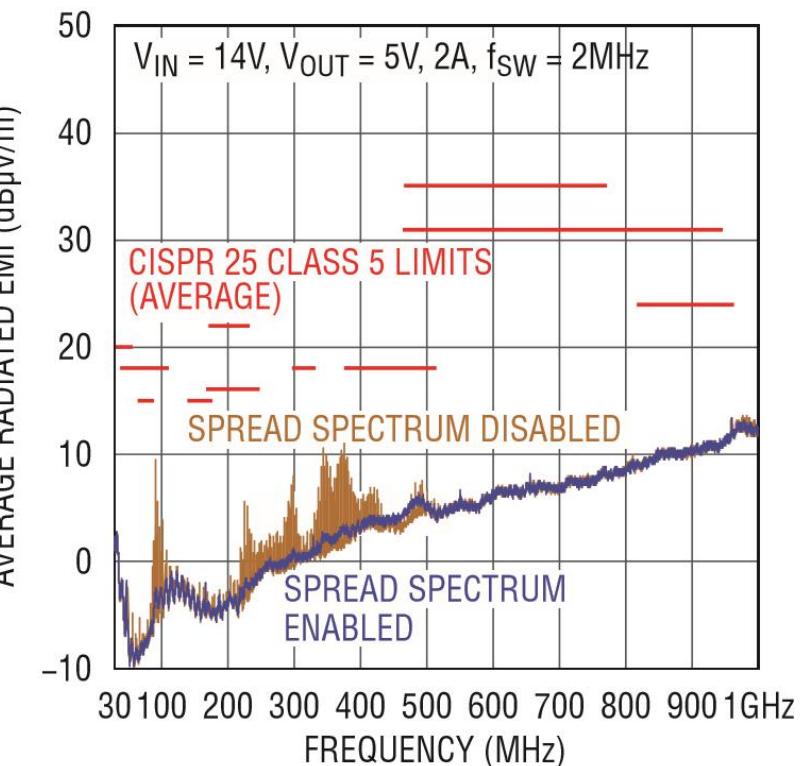
LT8609S 2-Layer
Demonstration Circuit



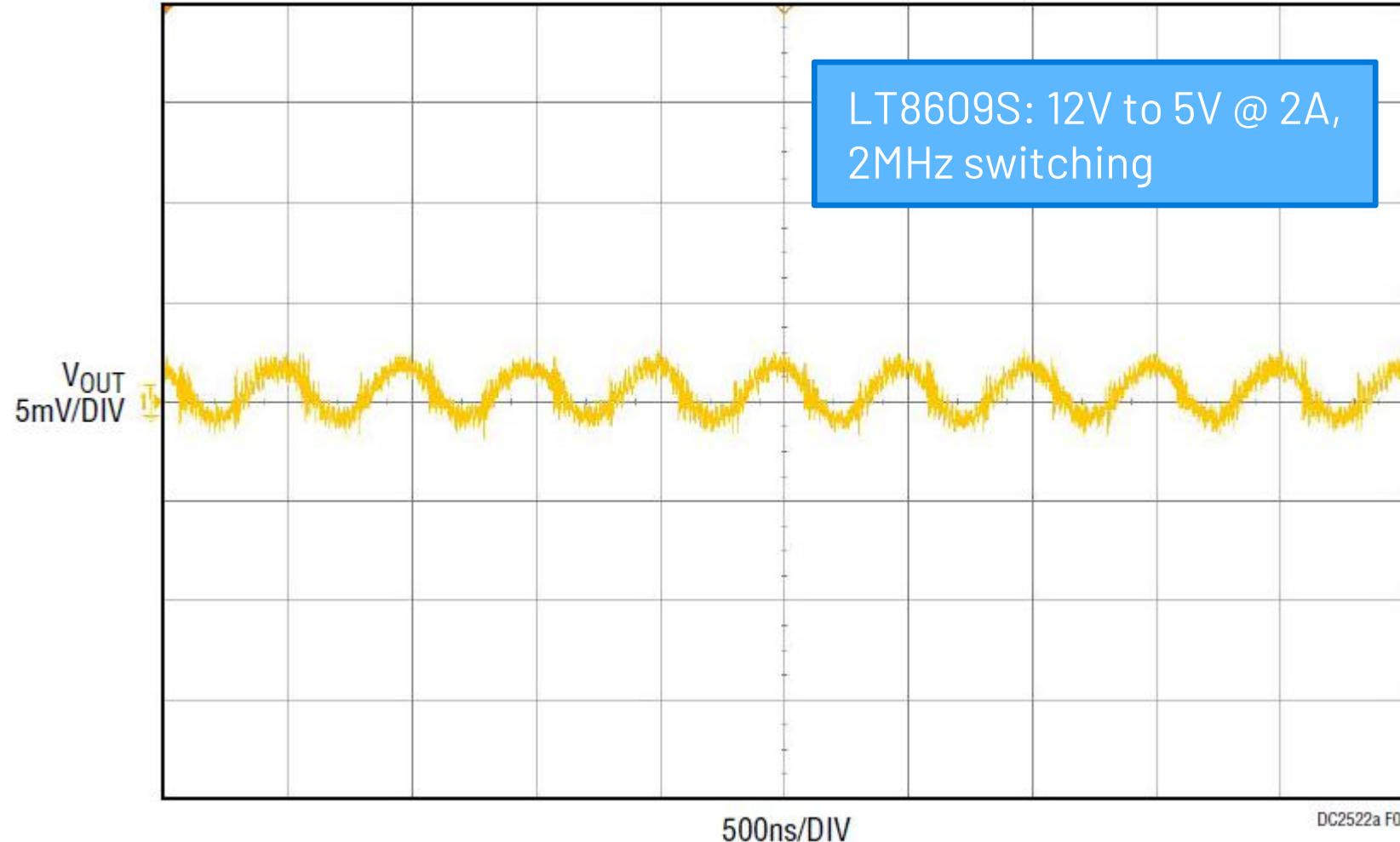
EMI is low on both 2-layer LT8609S and 4-layer LT8609S solutions.



2-layer Average EMI passes CISPR 25 Class 5 with room to spare.

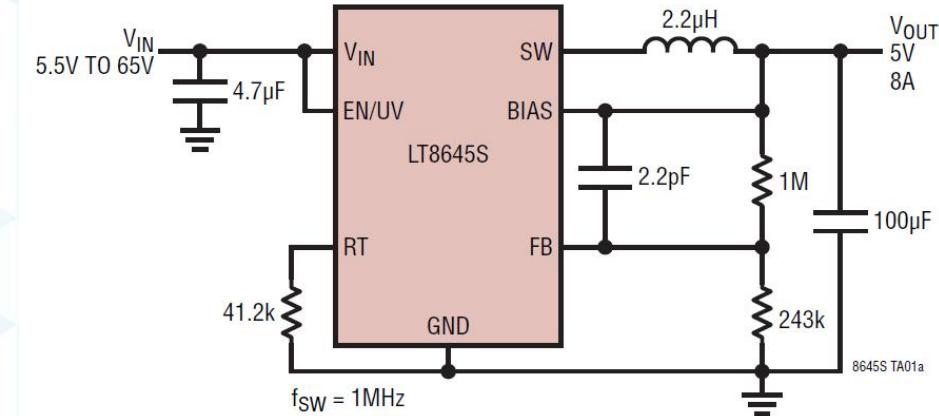


Silent Switcher 2 提供极低的电源纹波

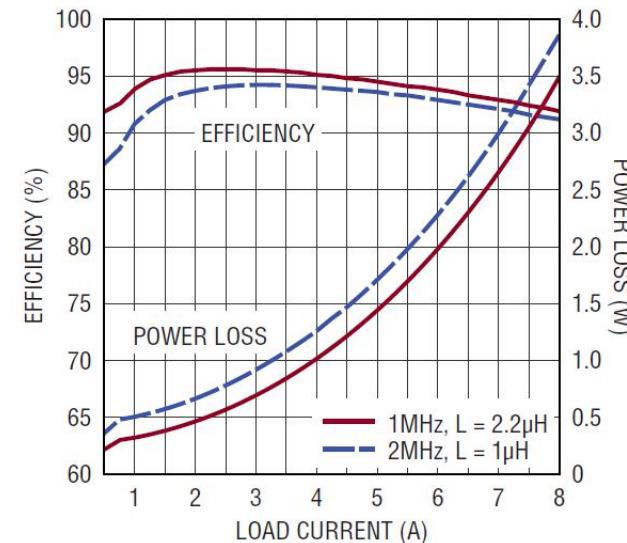


LT8645S/46S 65V, 8A Synchronous Buck Silent Switcher 2, $2.5\mu\text{A } I_{\text{Q}}$

- ▶ Silent Switcher®2 architecture
 - Internal bypass capacitors reduce radiated EMI
 - Optional spread spectrum modulation
 - Ultralow EMI on any PCB, eliminate PCB layout sensitivity
- ▶ Wide input range: 3.4V to **65V**
- ▶ High efficiency at high frequency:
 - Up to 95% at 1MHz, $12V_{\text{IN}}$ to $5V_{\text{OUT}}$
 - Up to 94% at 2MHz, $12V_{\text{IN}}$ to $5V_{\text{OUT}}$
- ▶ Ultralow quiescent current Burst Mode® operation
 - $2.5\mu\text{A } I_{\text{Q}}$ regulating $12V_{\text{IN}}$ to $3.3V_{\text{OUT}}$ (LT8645S)
 - Output ripple $<10\text{mV}_{\text{P-P}}$
- ▶ Fast minimum switch-on time: 40ns
- ▶ External compensation (LT8646S): Fast response and current sharing
- ▶ Adjustable and synchronizable: 200kHz to 2.2MHz
- ▶ Small 4mm x 6mm 32-pin LQFN packager



12V_{IN} to 5V_{OUT} Efficiency



Silent Switcher Family

DEVICE	# OF OUTPUTS	V _{IN} RANGE	OUTPUT CURRENT	PEAK EFFICEINCY AT 2MHz, 12V TO 5V	I ₀	FEATURES	PACKAGES
LT8650S	2	3V – 42V	4A + 4A on both channels or 6A on either channel	94.60%	6.2µA	Silent Switcher 2	6mm x 4mm x 0.95mm LQFN
LT8645S	1	3.4V – 65V	8A	94%	2.5µA	Silent Switcher 2	6mm x 4mm x 0.95mm LQFN
LT8643S	1	3.4V – 42V	6A continuous 7A peak	95%	120µA	Silent Switcher 2, external compensation	4mm x 4mm x 0.94mm LQFN
LT8640S	1	3.4V – 42V	6A continuous 7A peak	95%	2.5µA	Silent Switcher 2	4mm x 4mm x 0.94mm LQFN
LT8609S	1	3V – 42V	2A continuous 3A peak	93%	2.5µA	Silent Switcher 2	3mm x 3mm x 0.94mm LQFN
LT8640 LT8640-1	1	3.4V – 42V	5A continuous 7A peak	95%	2.5µA	Silent Switcher, LT8640 pulse skipping, LT8640-1 forced continuous	3mm x 4mm QFN-18
LT8641	1	3V – 65V	3.5A continuous 5A peak	94%	2.5µA	Silent Switcher	3mm x 4mm QFN-18
LT8614	1	3.4V – 42V	4A	94%	2.5µA	Silent Switcher. Low ripple Burst Mode operation	3mm x 4mm QFN-18

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