

Crosstalk Analysis in Passively Addressed Soft Resistive Heating Arrays

Dhirodaatto Sarkar^{ID}, Jue Wang^{ID}, Member, IEEE, and Alex Chortos^{ID}, Member, IEEE

Abstract—Finding applications in fields such as manipulation platforms and gas sensors, various strategies have been developed to enhance scale and resolution of resistive heating arrays, including integration of diodes/transistors. However, emerging applications in soft robotics and wearable devices prioritize systems that can be fabricated over large areas using low-cost materials, and benefit from simplified control. Utilizing common row/column electrodes to address heating elements, matrix addressing reduces the complexity of control inputs. Passive matrices require no semiconductor components, further minimizing device complexity. Despite these advantages, thermal and electrical crosstalk hinder passive matrix addressing. In this study, we present a novel systematic analysis of the crosstalk in passive matrix resistive heating arrays, addressing both electrical and thermal couplings. We employ theoretical and computational approaches to investigate the effects of materials and array geometry on crosstalk. Through COMSOL multiphysics simulations, we quantify crosstalk as a function of the conductivity of the constituent materials and array geometry. The computational approach allows us to decouple the effects of electrical and thermal crosstalk. Additionally, Pattern Search is used to optimize array designs, minimizing crosstalk and voltage input and revealing trade-offs at various array scales (illustrated in a 16×16 array). Furthermore, we study the significant impact of thermal patterns and control methods on crosstalk by implementing progressive scan. This work provides insights and optimization strategies for the design of resistive heating arrays used as actuators or sensors in soft robotics and wearable devices, highlighting its practical significance in the advancement of these emerging applications.

Index Terms—Resistive heating arrays, passive matrix addressing, electrical-thermal coupling, crosstalk.

I. INTRODUCTION

RESISTIVE heating systems find applications in fields ranging from additive manufacturing (Microheater Array Powder Sintering [MAPS] [1]) to building affordable testing kits for COVID testing (Loop-Mediated Isothermal Amplification [LAMP] [2]) as well as building micromanipulation platforms [3], [4], microlens arrays [5], flexible tactile displays [6], chemical gas sensors [7], generating 2D strain fields [8], solid propellant micro-thruster arrays for micro-nano satellites [9]

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as well as fingerprint sensing systems [10]. In thermal arrays, it is ideal to be able to control the temperature of each pixel independently. However, due to the diffusive nature of thermal energy, crosstalk occurs whenever the elements' ranges of effect overlap, resulting in effective thermal coupling. Previous work on thermal arrays has used various strategies to reduce thermal crosstalk. Strategies such as embedded microfluidics [11] and multistage insulation methods [12] have been used to reduce thermal crosstalk in multichannel slotted arrays and microarray sensors respectively. However, in many emerging fields, such as wearable devices and soft robotics, additional metrics need to be considered such as mechanical flexibility or stretchability and compatibility with large area fabrication methods and low-cost materials, e.g. screen printing of composite conductors. This work will explore thermal crosstalk in polymer-based thermal arrays.

Thermal crosstalk results from the diffusion of thermal energy. However, in electrically-addressed heaters, the coupling between pixels can also be affected by electrical crosstalk. Electrical crosstalk is determined by the choice of electrical addressing method, which refers to the approach used to electrically deliver power to each pixel in an array. Direct addressing consists of connecting two wires to each pixel. The pixels can be electrically and physically separate, minimizing thermal crosstalk and eliminating electrical crosstalk. However, this approach can be cumbersome because it requires at least M^2 electrical connections to control an array of $M \times M$ pixels. Matrix addressing involves using orthogonal arrays of electrodes to selectively address pixels, reducing the number of required connections to $2M$. Active matrix addressing uses a transistor in each pixel to eliminate electrical crosstalk, but the conductive traces connecting pixels still allow thermal conduction between pixels, increasing thermal crosstalk compared to direct addressing. However, including a transistor in each pixel requires complex fabrication processes. For systems that need to be large-area (e.g. soft robots) or low cost (e.g. wearable heaters), or miniaturized (e.g. resistive memory), including transistors can be prohibitive. Passive matrix addressing uses orthogonal arrays of electrodes to address pixels without transistors, and has been used in RRAM Crossbar Arrays [13], programmable shape morphing surfaces [14], liquid crystal displays [15], electrochromic displays [16] as well as sensor arrays [17].

However, such a design works by effectively electrically coupling elements in rows and columns. The thermal energy generated by these parasitic current paths contribute to the thermal crosstalk that already exists due to the common electrode

TABLE I
DEFAULT DEVICE CONSTRUCTION AND ESTIMATED ENVIRONMENTAL PARAMETERS

Parameter Origin	Parameter	Parameter Description	Sample Value [Unit]
Structural	M	Number of Pixels	6
Structural	w_e	Pixel Dimension / Electrode Width	3.5 [mm]
Structural	f_w	Width Factor	1
Structural	f_s	Spacing Factor	1
Structural	t_e	Electrode Thickness	0.2 [mm]
Structural	t_r	High Resistive Heating Layer Thickness	0.16 [mm]
Thermal	h	Convective Heat Flux Coefficient	10 [W/m^2K]
Thermal	k	Electrode Thermal Conductivity	70 [W/mK]
Electrical	σ_e	Electrode Electrical Conductivity	$4.0322 \times 10^4 [S/m]$
Electrical	σ_r	Heating Layer Electrical Conductivity	$0.1929 [S/m]$
Electrical	η	Conductivity Ratio $\rightarrow \log_{10} \left(\frac{\sigma_e}{\sigma_r} \right)$	5.32

lines since unwanted pixels are also activated when trying to activate certain patterns. Thus, one must not only consider the thermal interactions but also electrical couplings. In fact, thermal analysis of similar structures can be seen in the study of Electrical Re-RAM devices, where each element thermally interacts with its neighbors through common electrode lines which results in device degradation [18], with thermal crosstalk analysis done in [19], where the authors discussed the analysis by considering a coupling matrix where the temperature propagation of a heated pixel to non-heated pixel is found on a pixel-by-pixel basis and used to construct a matrix relating changes in temperature of all pixels to temperature of the pixels.

Now, to build heater arrays with a passively addressed element heating structure, reducing the voltage input required as well as the thermal crosstalk between pixels ends up being a set of conflicting requirements. In order to reduce thermal crosstalk, one might consider increasing the resistance of the heating layer, which allows for more complex connective electrode geometry (and this higher thermal and electrical resistance for the electrode connective volumes) while maintaining device functionality. However, the higher the resistance for the heating layer, the higher the voltage input required to maintain the same power input to the element.

This means that the electrical properties of the array would also have to be taken into account in addition to the thermal properties to design the device structure, since structural changes to reduce thermal crosstalk might affect the electrical subsystem forcing large voltage drops across the electrodes, thus prohibiting the addressing of heating elements in the array. This effect is studied in this paper to understand the conditions under which the device is feasible and has the lowest thermal crosstalk.

II. DEVICE CONSTRUCTION AND CONCEPT

The device works on the principle of Joule Heating, where a current(I) flowing through an element of resistance(R) generates heat(Q) given by $Q = I^2R$. This heat source can then be used to interfere with the environment in many ways, an example of which is the controlled deformation of an actuating layer made of phase-change material to make a tactile display as in [6]. To generate heat in each pixel, we use a crossbar passive matrix of electrodes. Investigation is needed to understand the effects of material properties and geometry on the effectiveness of addressing.

In order to investigate the crosstalk and validity of the device, one needs to parameterize the device design.

The structural, thermal, and electrical parameters that can be used to inform device design, along with default values used, which are addressed in the study can be found in Table I and can be visualized in Figs. 1 and 2.

The major parameters of interest are the spacing factor f_s which gives the ratio between the spacing length and the pixel dimensions, the width factor f_w which gives the ratio between the width of the electrode between pixels and the pixel dimensions, and the conductivity ratio η which gives the ratio of the electrical conductivities of the materials used in the electrodes to the high resistive heating layer. It is noted that the parameters f_s, f_w are incorporated to directly influence the thermal crosstalk by changing the thermal resistance of the connective electrode volume through which heat propagates between pixels. Ideally, minimal heat should be generated within the electrodes. A layer with higher resistivity is included between the electrodes to locally generate heat. Thus, the ratio of conductivities between the electrodes and resistive layer (η) is a key material parameter to tune in the array design.

Now, in order to characterize the performance of a design, a set of parameters is necessary to describe the performance of the device, as well as give an idea of the effect of each considered subsystem. We define these parameters as the total thermal crosstalk (C_{tot}) which is the temperature crosstalk observed in some passively addressed thermal array and has a purely thermal component as well as a coupled electrical-thermal component, pure thermal crosstalk (C_{th}) which is the temperature crosstalk observed in a the same array which is directly addressed (removing the electrical-thermal component of crosstalk), and electrical crosstalk (C_{elec}) which is the electrical current crosstalk in the same passively addressed array. The total thermal crosstalk may be used to describe the observed temperature discrepancy in non-addressed pixels of the array in the presence of passive addressing, given by :

$$C_{tot} = \frac{\text{Max}(T_{p_{i,j}^l}) - T_0}{T_p - T_0}, \quad (1)$$

where $T_{p_{i,j}^l}$ is the temperatures of the set of pixels sharing a row or column with the addressed pixel, T_p is the temperature of the addressed pixel, T_0 is the initial temperature of the array (room temperature).

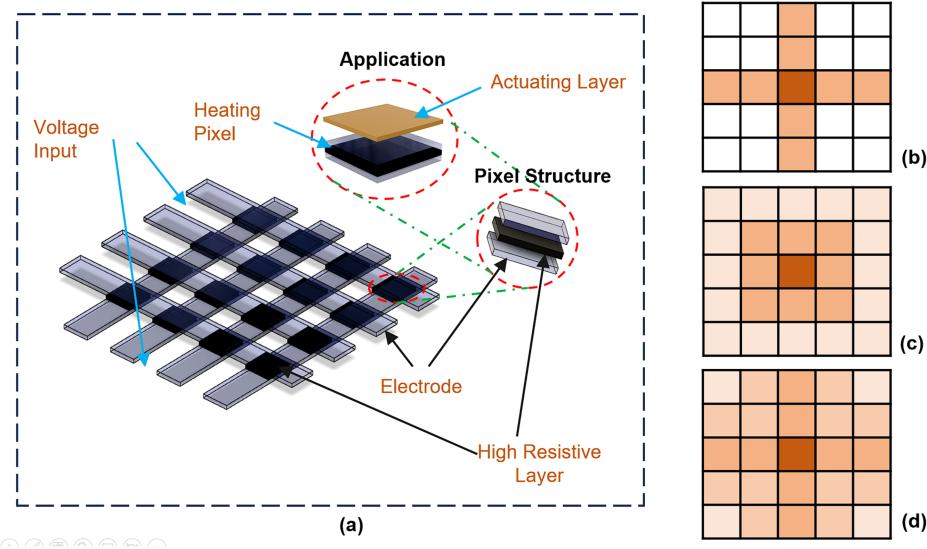


Fig. 1. (a) Schematic of passive matrix device structure; (b) Pure Electrical Crosstalk due to Passive Addressing; (c) Pure Thermal Crosstalk due to connective electrode volume without considering passive addressing; (d) Expected Thermal Distribution due to interacting Thermal and Electrical Crosstalk.

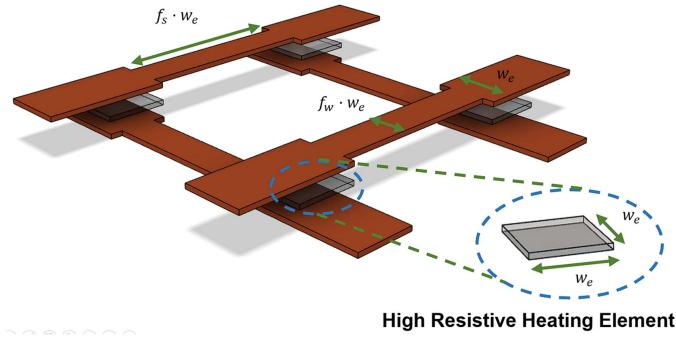


Fig. 2. Visualization of Structural Parameters in Table I.

The pure thermal crosstalk may be used to describe the observed temperature discrepancy in non-addressed pixels of the array if the pixel array was directly addressed, thus neglecting the electrical coupling due to passive addressing, given by the same functional form as (1), evaluated with the alternate version of the device.

The electrical crosstalk may be used to describe the leakage currents in non-addressed pixels of the passively addressed heating array, formed as a result of the electrical coupling, and can be given by :

$$C_{elec} = \frac{\text{Max}(I_{p_{i,j}})}{I_p} \quad (2)$$

, where $I_{p_{i,j}}$ are the currents through the set of pixels sharing a row or column with the addressed pixel, I_p is the current through the addressed pixel.

Furthermore, it might be possible to use C_{tot} to separate the candidate designs into feasible/infeasible or valid/invalid groups based on if $C_{tot} < 1$. C_{tot} being greater than 1 implies that, for the target pixel being addressed to reach T_{req} , there must exist at least another pixel in the same row/column of the addressed

pixel which has a higher temperature, which would clearly mean that the device is not functioning as intended.

III. REDUCED ORDER MODELLING OF PASSIVELY ADDRESSED ELECTRICAL SUBSYSTEM

In order to understand the effect that passive matrix addressing of pixels has on the underlying electrical subsystem, we consider a reduced order model as shown in Fig. 3. Taking the center of the pixel top and bottom as the numbered nodes (V_{11}, V'_{11}, \dots) as the nodal voltages to be solved for assuming one is given the input voltage vectors x, y . Furthermore, the representative resistances R_L, R_C, R_1 (where R_L is the resistance of the heating element, R_C is the resistance of the connective electrode volume between pixels and R_1 is the resistance of the electrode volume between point of application of the voltage input and the first pixel) can be re-written using device parameters, with ρ_e, ρ_r representing resistivities of the electrode and heating layer materials: $R_1 = \frac{l_0 \rho_e}{t_e w_e}$, $R_L = \frac{10^7 t_r \rho_e}{w_e^2}$, $R_C = \frac{L \rho_e}{t_e w_e}$, where $L = (f_s + 1)w_e$ and l_0 represents the offset length from the edge of the electrode where voltage is applied and the center of the closest pixel on the same row/column. Then, using Kirchoff's Laws, one can derive equations of the form shown below for some pixel i, j :

$$\begin{cases} \frac{V_{i,j} - V'_{i,j}}{R_L} + \sum_{i_n, j_n}^{N_r} \frac{V_{i,j} - V_{i_n, j_n}}{R_C} + \sum_{x_n}^{BC_x} \frac{V_{i,j} - x_n}{R_1} = 0 \\ \frac{V'_{i,j} - V_{i,j}}{R_L} + \sum_{i_n, j_n}^{N_c} \frac{V'_{i,j} - V'_{i_n, j_n}}{R_C} + \sum_{y_n}^{BC_y} \frac{V'_{i,j} - y_n}{R_1} = 0 \end{cases}, \quad (3)$$

where BC_x, x_n refer to possible row voltage inputs at some boundary pixel ($i = 0$), BC_y, y_n refer to possible voltage column voltage inputs at some boundary pixel ($j = 0$), N_r, N_c refers to any set of pixels i_n, j_n that may be row neighbors or column neighbors respectively.

Thus, we are able to set up $2M$ equations for $2M$ unknown nodal voltages which can be found by solving the associated

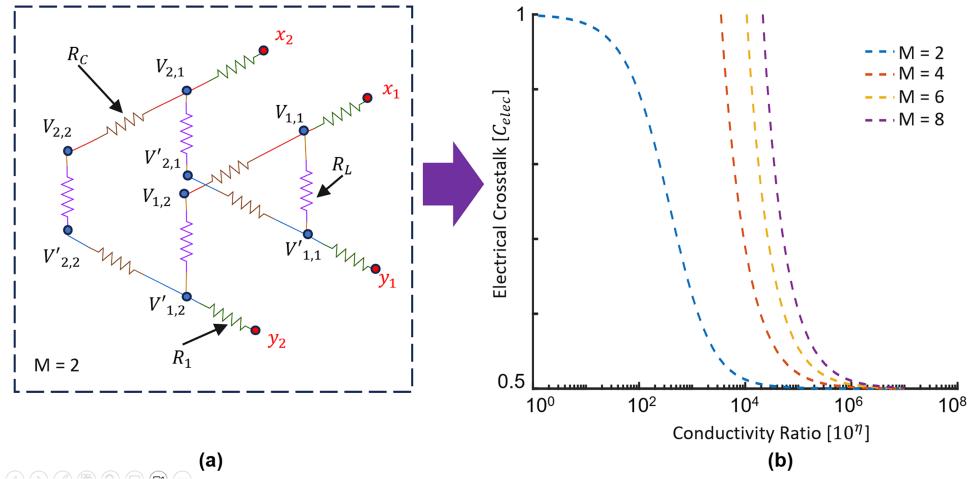


Fig. 3. (a) Schematic of Electrical Model considered for a sample \$2 \times 2\$ pixel array; (b) Effect of Conductivity Ratio and Array Size on Electrical Crosstalk.

linear system of equations, given voltage vectors \$x, y\$. It is then found that the conductivity ratio \$\eta\$ plays an important role on the electrical crosstalk observed in the system.

Now, one can try to analyze the associated electrical crosstalk (2) to understand the effect of passive addressing on the choice of conductivity ratio (\$\eta\$), which in turn affects the choice of materials and geometry of the electrode and high resistive layer. The electrical crosstalk for this system can be rewritten using the found nodal voltages as:

$$C_{elec} = \frac{\text{Max}(V_{i_n,j_n} - V'_{i_n,j_n})}{(V_{i_p,j_p} - V'_{i_p,j_p})} \quad (4)$$

Noting that the electrical crosstalk is influenced by the conductivity ratio as well as the array size, the relevant parameters are varied and the data is plotted in Fig. 3(b). It can then be noted that beyond a critical conductivity ratio, the electrical crosstalk reaches an asymptote at a value of 0.5. Furthermore, increasing the array size increases the requirements on this critical conductivity ratio. Thus, we can expect that a geometrically similar design when scaled up to a larger array size will suffer significant performance degradation due to the electrical coupling crosstalk due to the passive addressing scheme. This confirms the need to account for the electrical crosstalk in addition to the thermal crosstalk, when designing such a device.

IV. QUASI-STATIC MODELLING AND CROSSTALK EVALUATION USING COMSOL

While the reduced order model is valuable to conceptually understand the effect of parameter choices, finite element modeling can provide predictions for large array sizes and any combination of materials parameters while also taking into account crosstalk due to the combined effect of the electrical and thermal subsystems. We use COMSOL to solve the corresponding Electric-Thermal Coupled Finite Element Problem for the full device.

First, the geometry of the device is built according to the device construction shown in Figs. 1 and 2 and the input parameters as given in Table I. Then, considering the interest in

the steady-state temperature distribution in the device, one can use a “Stationary Solver” in COMSOL with the default settings. The physics modules needed to describe the device function are the “Electric Currents” Module and “Heat Transfer in Solids”. In the heat transfer module, a constant convective heat flux from all surfaces using a given \$h\$ is set up, which for a real-life experiment may be either derived from experiments or in this case, using the placeholder value given in Table I. Setting up the initial values to the ambient temperature ensures that our final temperatures make sense. In the electric currents module, the relevant voltage boundary conditions of potential \$V\$ to heat the required pixel as applied by selecting the extreme faces of the electrode where the voltage input would be on the actual device.

Now that the electrical and thermal physics definitions have been set up, the coupling between the physics i.e. Joule heating, can be conveyed by using the COMSOL Multiphysics “Electromagnetic Heating” module. Selecting a “Normal” mesh size then allows one to solve for the temperature distribution or total crosstalk given desired input parameters. Furthermore, making a slight adjustment by directly applying temperature boundary conditions on the desired pixel in COMSOL using the “Heat Transfer in Solids” module allows us to investigate the pure thermal crosstalk, where there is no electrical coupling between the pixels.

Since the goal of the simulation is to get the temperature distribution through the device for a given desired pixel temperature \$T_{req}\$ to understand the thermal crosstalk, a connected problem is to determine \$V\$ such that \$T_p \approx T_{req}\$. To do this, we note that \$(T_p - T_\infty) \propto I \propto \frac{V^2}{R}\$, which gives us a trend:

$$T_p = A_T V^2 + T_\infty \quad (5)$$

Evaluating the model at a few random points allows one to approximate \$A_T\$ and find the required \$V\$ for \$T_p \approx T_{req}\$.

Referring to Fig. 4(a), the expected dependence of the total thermal crosstalk (\$C_{tot}\$) on the electrical conductivity ratio (\$\eta\$) predicted from Fig. 3(b) is seen. At low values of \$\eta\$, \$C_{tot} \gg 1\$, showing that the addressed pixel does not have the highest temperature in the array i.e. the correct pixel is not being addressed.

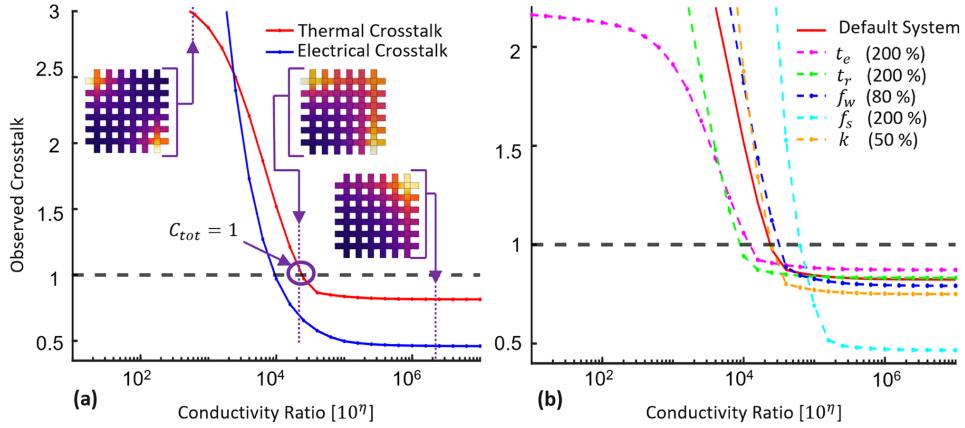


Fig. 4. (a) Effect of Conductivity Ratio on Thermal Crosstalk Distribution in device; (b) Effect of Structural and Thermal Parameter Variations on Crosstalk-Conductivity Ratio Curves.

TABLE II
SENSITIVITY OF DEVICE PARAMETERS ON CROSSTALK AND VALIDITY REQUIREMENTS

Parameter	Sensitivity of Validity Requirement			Sensitivity of Minimum Achievable Crosstalk		
	4 x 4	6 x 6	8 x 8	4 x 4	6 x 6	8 x 8
f _w	-0.0218	-0.0480	-0.0537	0.0594	0.0494	0.1272
f _s	0.0270	0.0602	0.0681	-0.2957	-0.2856	-0.2060
t _e	-0.1974	-0.2270	-0.2122	0.2172	0.1947	0.1728
t _r	-0.1834	-0.2141	-0.2027	0.0055	0.0099	0.0084
w _e	0.3462	0.3210	0.3102	-0.4347	-0.3703	-0.4020
k	-	-	-	0.2349	0.2026	0.1852
h	-	-	-	-0.2183	-0.1947	-0.1667

As η increased past some η_{cr} , since the associated electrical system has settled at the required voltages necessary to heat up the correct pixel, the corresponding total thermal crosstalk sees minimal change (visual at $\eta = 6.2$. This is reflected in the array as temperature hotspots which move from the pixel closer to application of voltage input, to the addressed pixel as η increases. Also, one can note from the figure that the electrical crosstalk C_{elec} leads C_{tot} , which is expected since, $C_{elec} < 1 \Rightarrow C_{tot} < 1$. At relatively higher electrical crosstalk, even if less than 1, the implication that the extreme pixels of the array may have similar heat sources attached to them, immediately means that the associated thermal crosstalk may still be greater than 1, depending on the possible routes of heat loss for the pixel.

Furthermore, in order to understand the effect of the choice of design parameters on the crosstalk curve, we focus on the local sensitivities of the validity requirement (η where $C_{tot} = 1$) and minimum achievable crosstalk (C_{tot} for $\eta > \eta_{cr}$) due to changes in the width and spacing factors, thermal conductivities, layer thicknesses and scale of the array from the nominal values in Table I (shown in Table II and Fig. 4(b)). It is noted that changes in the structure of the electrode layer which reduce the electrical/thermal resistance (decrease in f_w, t_e , increase in f_s) have competing effects, increasing the validity requirement but reducing the minimum crosstalk. However, increasing the high resistive layer thickness (t_r), which increases the electrical resistance of the heating element, since it can reduce the validity requirement with minimal effect on the minimum crosstalk. Similar effects are seen when the dimensional changes are seen

by scaling up the array by changing the pixel dimensions (w_e), where a significant drop in minimum thermal crosstalk as well as validity requirements can be seen. Additionally, reducing the thermal conductivity k (material modification) or increasing the convective heat flux coefficient h (environment modification) is also always beneficial since it reduces the minimum achievable crosstalk without affecting the validity requirement.

In the above curves, the crosstalk considered is the one seen from pixel (4,4) as opposed to other pixels, for the primary reason of validity, as discussed later. Defining crosstalk as in (1), one can easily notice that T_p is not defined to be any particular pixel, and any pixel can be used. Note that a coupling matrix relating $(\Delta T)_i = \sum c_{ji}(\Delta T)_{ii}$ as seen in [19] captures more information than a single value. However, since the goal is to compare multiple design's performances, a single value from any pixel may be used.

The most extreme pixel may be chosen in this regard as it has much harsher requirements as can be seen in Figs. 5 and 6. It may be argued that choosing a pixel in the interior of the array may be better since the smaller area available for heat dissipation results in a larger estimated thermal crosstalk, resulting in estimates for the upper bound for thermal crosstalk throughout the array. While this is true, selecting designs on the basis of this parameter may result in a design where, due to the electrical coupling, all pixels in the array are not addressable due to significant electrical crosstalk. As seen in Fig. 6, we can see a particular illustrating design with large spacing between pixels allowing for heat loss, where some pixels are addressable, but addressing the extreme pixel (4,4) is not possible.

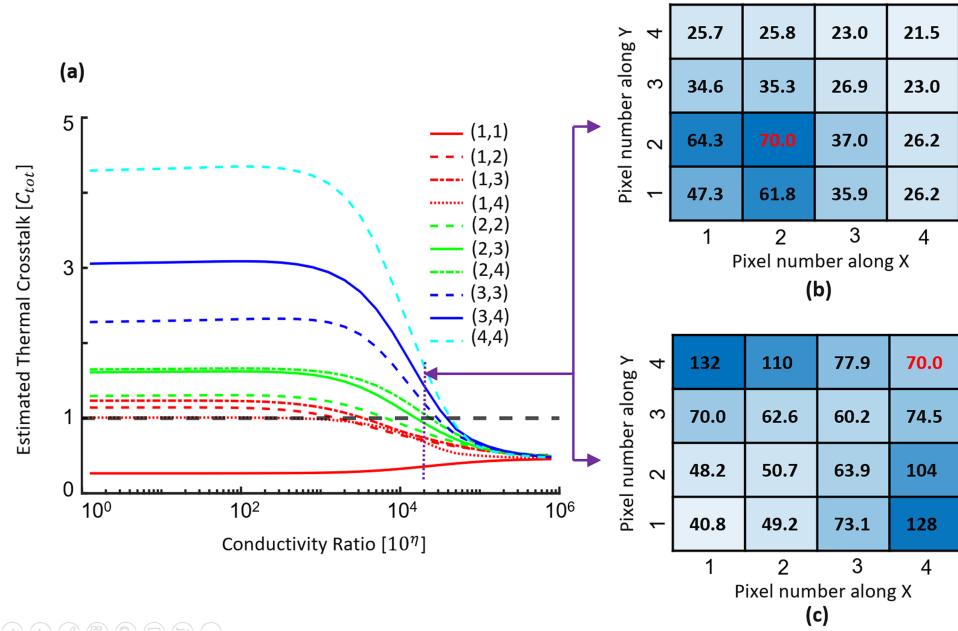


Fig. 5. (a) Crosstalk-Conductivity Ratio curves seen from addressing different pixels in the array; (b) Expected valid device's thermal distribution (at $\eta = 4.1$) seen from pixel (2,2); (c) Expected invalid device's thermal distribution (at $\eta = 4.1$) seen from pixel (4,4).

Effect of Active Pixel on Crosstalk Characterization

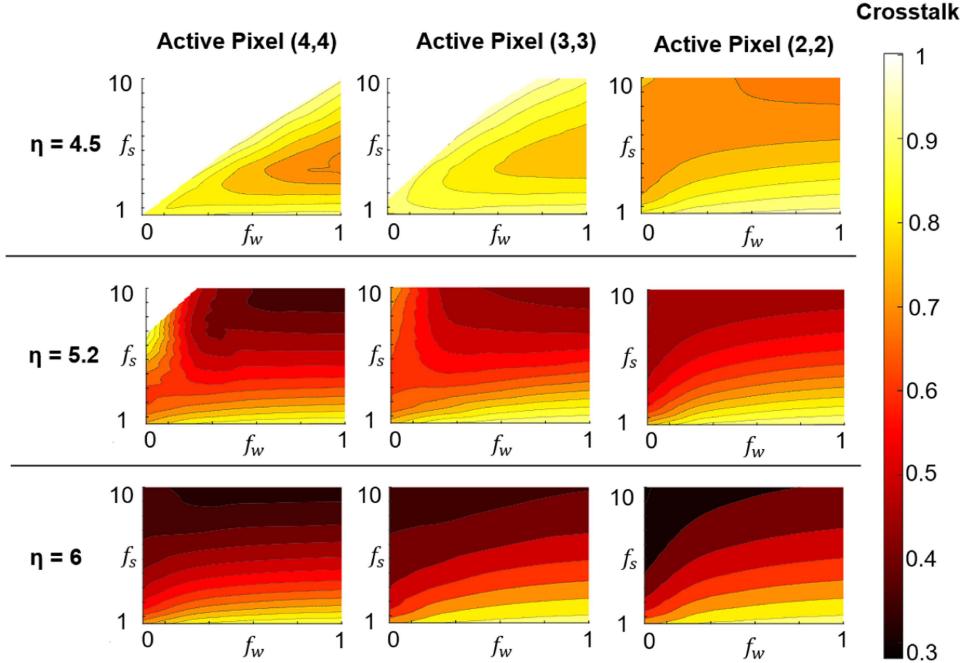


Fig. 6. Crosstalk Contours for swept values of $f_w \in (0, 1]$, $f_s \in [0.5, 10]$ displaying invalidity of device at low f_w , high f_s due to resistance ratio requirements on device.

In fact, this character can be more clearly seen in Fig. 6, where the choice of active pixel (4,4) is reflected in the crosstalk curves being much sharper, with much smaller regions of validity. White regions are where the device is considered invalid (crosstalk > 1). Thus, the most extreme pixel in the array furthest away from point of application of voltage is used to inform device design.

Another important aspect of such a device structure that can be seen in Fig. 7, is the predicted device invalidity at high values of f_s and low values of f_w . To understand why that is, consider a device of high width factor ($f_w = 1$), where the spacing factor is swept through some range ($f_s \in [1, 10]$) and investigate the different crosstalk parameters as seen in Fig. 7. As we increase f_s , the total thermal crosstalk seems to first decrease, and the

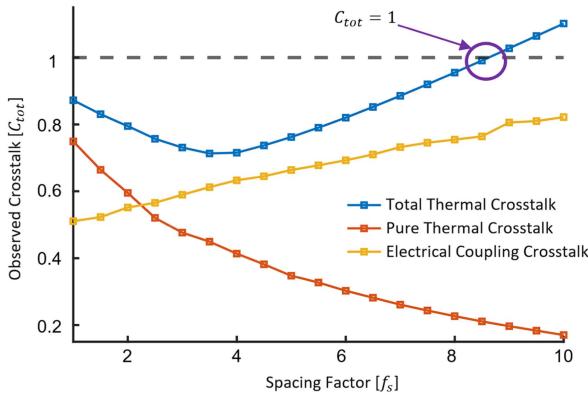


Fig. 7. Illustration of Trade-Offs in Device Design between Electrical and Thermal crosstalk.

increase past some $f_{s,\min}$ where the crosstalk is minimized for $f_w = 1$. However, if we consider the thermal model separately, we expect that the pure thermal crosstalk will continue decreasing until the pixels are effectively thermally decoupled. The reason is seen on observing the electrical crosstalk for the same device, where increasing the spacing factor corresponds to an increase in the electrical resistance of the electrode, thus corresponding to higher electrical crosstalk between the pixels. The increase of the electrical crosstalk eventually increases beyond the expected decrease in pure thermal crosstalk, imposing bounds on geometry on the basis of the total thermal crosstalk.

Given that the regions of validity that one sees in Fig. 6, one may guess that the electrical parameters that influence validity could be the total resistance ratio of the electrode vs the heating element / high resistive layer. To investigate this, f_w, f_s, t_r, M i.e. the factors affecting the geometry of the electrode and high resistive layer were varied to find the combinations of parameters that give $C_{tot} = 1$. Since the resistance ratio is expected to be the driving factor, consider the resistance of an electrode connective segment given by $R_e = \frac{f_s}{\sigma_e t_e f_w}$ and the resistance of one square of the resistive layer given by $R_{hr} = \frac{t_r}{\sigma_r w_e^2}$ as the parameters of interest. Plotting these parameters for the different combinations found (Fig. 8), allows one to see a linear relationship between these values for some value of M , suggesting a bound on this “resistance ratio” (given by the slope) below which the device is invalid. In fact, one might also notice that for larger arrays with a higher number of pixels, this slope increases quite drastically, which implies that as the number of pixels on the array increases this bound on resistance ratio becomes more severe, thus reducing the ranges of the design parameters for which the device is valid. Thus, we might define this parameter of interest for low R_e with a correction factor $c(M)$ as:

$$\left\{ V_s(M) = \frac{R'_{hr}}{R_e} \right. \\ \left. \text{where, } R'_{hr} = R_{hr} - c(M) \right. \quad (6)$$

In order to demonstrate the effect of resistance ratio on validity for such device arrays, we look at an example of a 16×16 resistive heating array where $t_e = 0.1$ mm, $t_r = 0.16$ mm, $w_e = 5$ mm and $f_s = 1.6$.

In such an array, the thermal crosstalk is reduced primarily by changing the width factor, whose reduction translates to the electrode segments which serve as thermal connective volumes between the pixels becoming thinner, increasing the thermal resistance of the connective segments. In this demonstration, consider a 16×16 design with $f_w = 1$ as a starting point. For this design, let η be the smallest value it can take after the thermal crosstalk has settled with further increases in η contributing no effect on the observed thermal crosstalk. The observed thermal crosstalk is 62% with a conductivity ratio of 6.6. If f_w is then decreased to the minimum it can take (based on manufacturing resolution, and structural integrity considerations) in order to reduce thermal crosstalk without ever changing the materials and thicknesses, we can see that the device fails to function properly (Fig. 9) due to the resistance ratio V_s not being high enough. We can then seek to change the resistance ratio by increasing the conductivity ratio to 7.6, after which increases in the conductivity ratio do not change the thermal crosstalk, thus allowing thermal crosstalk to reach 48%. Thus, we can see a nearly 22.5% decrease in crosstalk in the optimized design, albeit at the cost of a 72.5% increase in voltage requirements.

Thus, we can see that the conductivity ratio is an important factor that not only drives the power input to the device but also the feasibility of the device.

V. OPTIMIZATION OF RESISTIVE HEATING ARRAY TO REDUCE CROSSTALK

It can be seen in the earlier sections that the design parameter space can be related to a crosstalk surface, where the minimal points of crosstalk subject to some constraints can be connected to the optimized design. This connected optimization problem could be solved by any direct search method, since the gradients are not explicitly available unless its finite difference approximation is found, which may not be reliable. Pattern Search methods have been used in various problems, especially for those with multidimensional input with non-smooth outputs such as power system security analysis ([20]), actuator placement in morphing structures ([21]) as well as design of load bearing thermal insulation ([22]). In this paper especially, Pattern Search algorithm is considered due to the nonlinear crosstalk surface in response to changes in conductivity ratio. Even with the selection of a seed in a region of negligible gradient and non-optimal crosstalk, the algorithm is able to successfully reach an optimal value. Hence, for its reliability at the cost of more function evaluations, Pattern Search is chosen as the optimization algorithm.

For a device that may be considered to have no area constraints other than those due to the device structure, ignoring the required voltage input, one can try to find the optimal crosstalk possible, as we vary f_w, f_s, w_e, M , keeping all layers with the default thickness as in Table I as well as a fixed conductivity ratio. To understand each parameter’s effect, this optimal crosstalk is found by varying f_w, f_s for different sets of $w_e \in \{2 \text{ mm}, 3.5 \text{ mm}, 5 \text{ mm}\}$, $M \in \{4, 5, 6, 7, 8, 9\}$, using the Pattern Search Algorithm to find the optimal set of $f_{w,o}, f_{s,o}$ (Fig. 10(a), (b), (c)) using the following objective function to exclude all invalid devices:

$$J = \text{Min}(C_{tot}, 1) \quad (7)$$

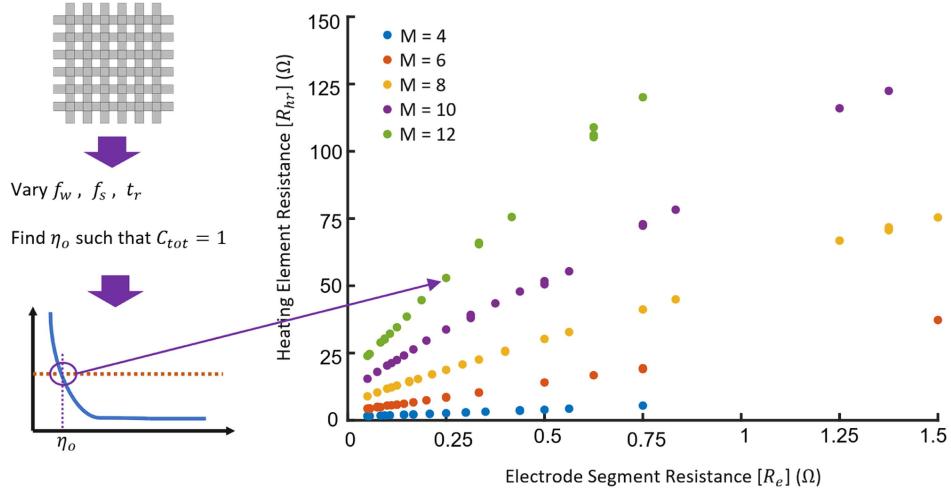


Fig. 8. Evaluation of trend in resistance ratio at validity boundary points found by varying structural and material properties.

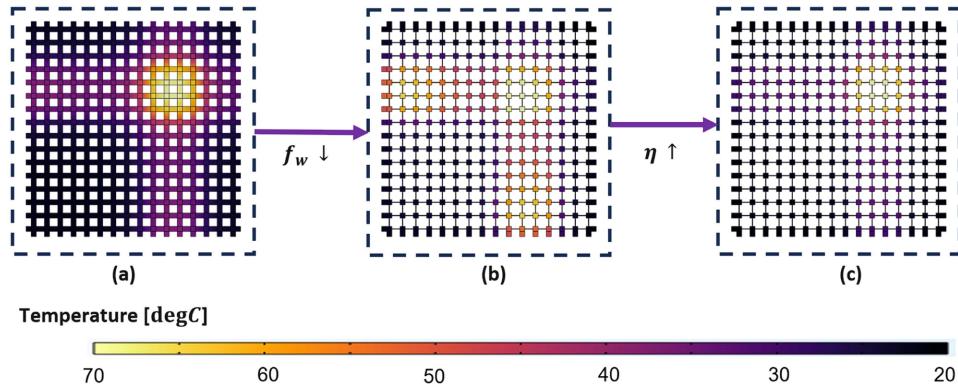


Fig. 9. Demonstration of conductivity ratio requirements on devices for reducing thermal crosstalk (a) High Crosstalk in device without altering width factor; (b) Alteration in width factor alone resulting in an infeasible device; (c) Device with lower crosstalk made feasible by increasing conductivity ratio.

Doing this, we notice a few key features. Without specifically adjusting layer thicknesses, as we increase the number of pixels in the array, there exists an upper bound on the device where all pixels are not addressed, even when the most crosstalk-optimal version of the device is considered. Also, even for a relatively small array of pixels, with the default layer geometries, the pixels cannot be completely thermally decoupled. This is again seen in the increasing electrical crosstalk due to the increasing requirement on validity given by $V_s = \frac{R_{hr}}{R_e}$ (6) as discussed in the previous section, resulting in a smaller valid region, and consequentially larger expected crosstalk. If compared to the purely thermal crosstalk at these optimal designs, the electrical crosstalk contributes almost an additional 0.1–0.2 increase in total thermal crosstalk from the pure thermal crosstalk or an increase of 5–10 °C. As a consequence of the shrinking region of validity, the optimal spacing factors also drop exponentially as the size of the array increases (Fig. 10(c)).

Thus, it is noted that a design's high resistive layer geometry must also be addressed i.e. R_{hr} must be increased, before increasing the scale of the array due to the direct effect of the validity region on the minimum global crosstalk.

For a more realistic device design problem, we consider a design with some given $M \in \{6, 8, 10\}$, $w_e = 3.5$ mm. Since

the objective is to minimize both crosstalk and the voltage input required, we consider the following weighted objective function, where $\alpha \in (0, 1)$ is the relative weighting given to crosstalk and V_{\max} is some maximum voltage considering device operation constraints:

$$J = \alpha \cdot \text{Min}(C_{tot}, 1) + (1 - \alpha) \cdot \text{Min}\left(\frac{V_{in}}{V_{\max}}, 1\right) \quad (8)$$

Varying the weight α between {0.1, 0.3, 0.5, 0.7, 0.9} with $V_{\max} = 60$ V then allows the exploration of the optimal trade-offs for such a design, also allowing us to explore the neighborhood of the case of the voltage input of 20 V. Furthermore, perturbing the array size slightly, we can see more interesting character in the trade-off curves generated (Fig. 10(d)). One can see the bounds on minimum achievable crosstalk at the crosstalk dominated sections of the trade-off curves where the 6×6 array is able to achieve $C_{tot} = 0.36$ for $V_{in} = 20$ V, but the 10×10 array is only able to achieve $C_{tot} = 0.48$ for the same voltage input. Furthermore, for the same achievable crosstalk, the smaller arrays have lower voltage input (going as low as 2 V for high thermal crosstalk for a 6×6 array) as well as lower requirements on the conductivity ratio. It can also be seen that increasing the requirements on voltage input, especially for

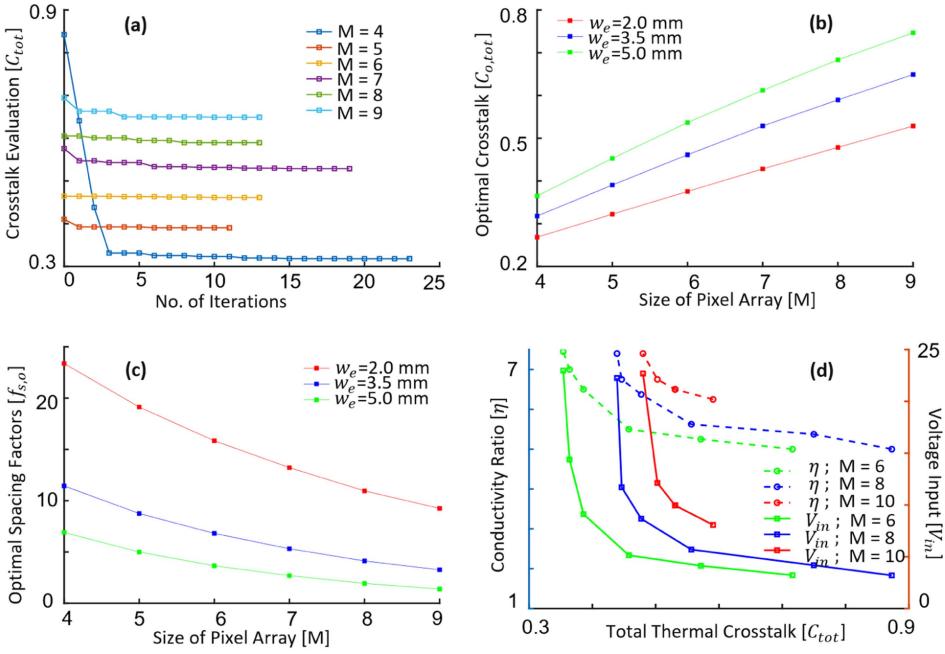


Fig. 10. (a) Pattern Search Optimization Convergence for a set of design constraints showing the increasing thermal crosstalk on array size; (b) Optimal Crosstalk values for w_e in {2 mm, 3.5 mm, 5 mm} and $M \in [4, 9]$; (c) Optimal Spacing Factor values for w_e in {2 mm, 3.5 mm, 5 mm} and $M \in [4, 9]$; (d) Pareto Fronts illustrating the trade-offs between voltage input and crosstalk affecting the conductivity ratio for a design problem involving area constraints.

larger array may result in designs lying outside the valid region, where pixels in the array may not be addressable. Thus, we can see that we are able to improve the crosstalk seen in the default 6×6 array (Table I) by 54.5% through this procedure. It must also be noted that such an optimization procedure can also be applied to an active matrix array (such as seen in [23]), in order to reduce crosstalk due to thermal diffusion by modifying the geometry of the electrode and resistive layer in the space between pixels.

VI. IMPLEMENTATION OF PROGRESSIVE SCAN USING SIMULINK-COMSOL

A matrix of devices cannot independently control the voltage to all pixels simultaneously. Consequently, the array is typically scanned by allowing current to flow into certain rows while setting the voltages on all of the columns simultaneously (similar to [4], [24], [14]). A few factors of interest in this method end up being the rate of cycling (which determines if the target pattern will be satisfied), the dependence of crosstalk on the target pattern, as well as the sets of pixels that the target pattern can be split into (which would affect the cycle length).

Using COMSOL as the means of testing the method and understanding the crosstalk in this case, COMSOL-Simulink Livelink (v6.1) was used, which allows the implementation of progressive scan on the Finite Element Model described in the earlier section. The inputs to the COMSOL Cosimulation Block are the voltages applied to each electrode, while the outputs are the temperatures at the surfaces of each pixel (the contact points at which an actuating layer may be placed). Taking a 5×5 pixel array ($M = 5$) as the testbed, one can find that the model is described by 10 ($2M$) inputs and 25 (M^2) outputs.

To implement progressive scan, a block diagram structure similar to Fig. 11 is used, where the “ $M \times M$ Resistive Heating Array Model” represents the pixel array to be controlled with $2M$ inputs and M^2 outputs. The output temperature feedback from the model is given to the “Reference Cycle Selector” block which then returns y , which represents the maximum pixel temperature of the set of pixels that the current part of the cycle is addressing. Since each sample time, a different part of the pattern is being addressed y can be seen to be changing the set of pixels that is refers each sample time and repeating this as a cycle finishes. Particularly note that this decomposes the corresponding MIMO control problem, to a chain of switching SISO controllers acting on different parts that the final shape can be decomposed into. This representative temperature y is compared against $T_{activated}$, which is the temperature threshold describing an active pixel. The compared error e is used as input to a discrete PI controller which gives the control input u' as a function of the error, where k refers to the sample index given some sampling time:

$$u'[k] = u'[k - 1] + C_1 e[k] + C_0 e[k - 1] \quad (9)$$

The output of the PI controller u' is constrained to the range $[0, \infty)$ which may be done by considering $u = \sqrt{u'}$, considering the input-output relationship in (5). This controlled voltage input is then used to inform the electrode voltage inputs in the block “Input Selector” for the array to address the correct pixel from where the temperature feedback has been taken. This voltage vector is then passed into the model to complete the control loop, which runs at a frequency of 50 Hz.

Now, in order to investigate the effects of such an addressing sequence on crosstalk/performance of the device, consider 3

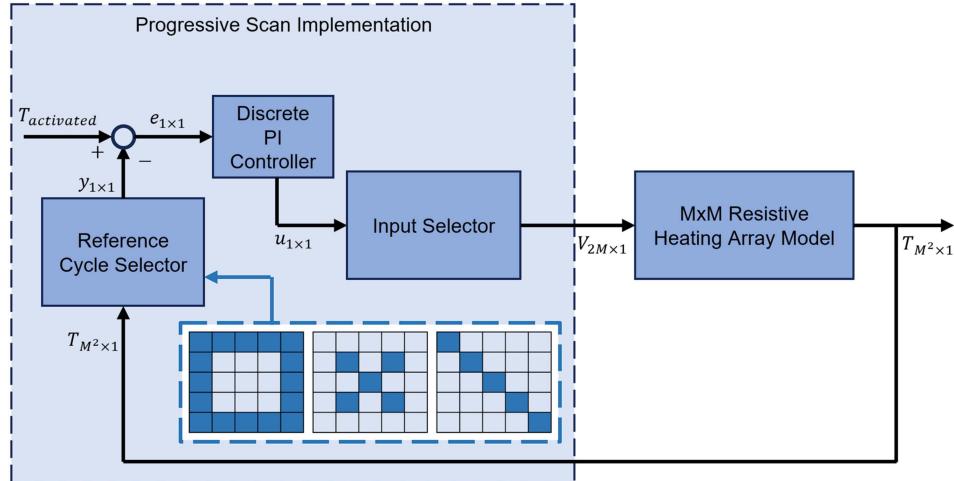


Fig. 11. Block Diagram Structure illustrating implemented progressive scan method in COMSOL-Simulink Livelink for shapes shown (left to right): Well shape, Cross shape, Diagonal shape.

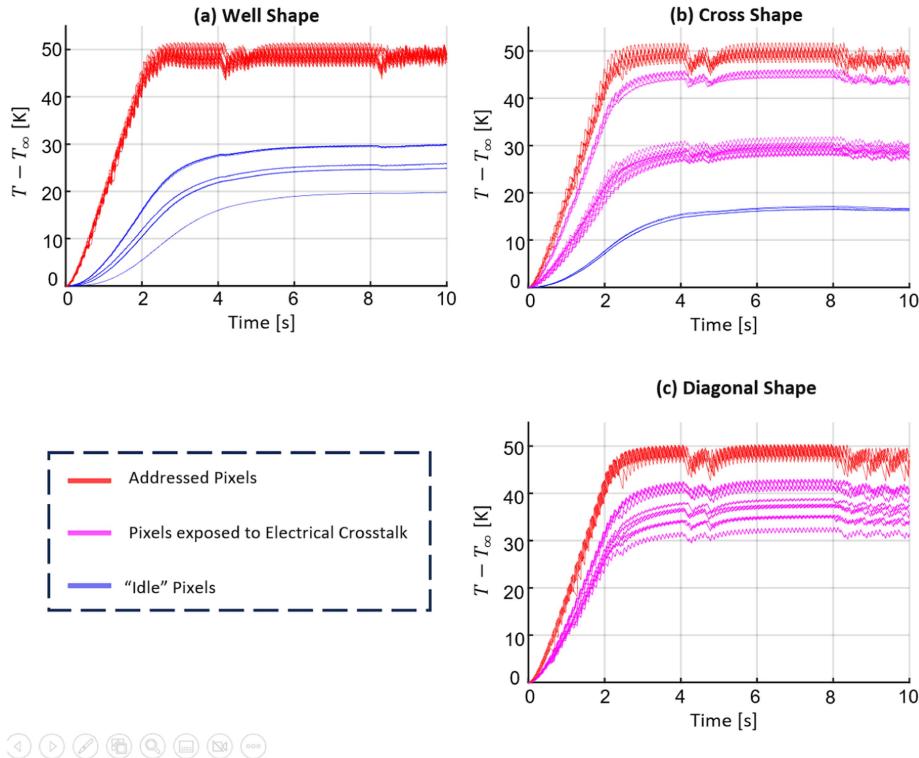


Fig. 12. Progressive Scan Results [Temperature Evolution over time].

different patterns shown in Fig. 11 for the following reasons of interest:

- 1) *Well shape*: All pixels in the pattern except the corner pieces can be addressed with constant voltage inputs (5 element cycle), and the addressing of the corner pieces results in electrical crosstalk along pixels which all fall in the subset of addressed pixels.
- 2) *Cross shape*: All 5pixels in this pattern have to be addressed individually (5 element cycle), and the pixels affected by the electrical crosstalk during this process have a subset which gets repeatedly exposed to this crosstalk

for the majority of the cycle duration. Note that not all pixels in the array get exposed to electrical crosstalk.

- 3) *Diagonal Shape*: All 5pixels in this pattern have to be addressed individually (5 element cycle), and the pixels affected by the electrical crosstalk during this process are only addressed for a part of the cycle duration. Note that all pixels in the array get exposed to electrical crosstalk at some time in the cycle.

Using a sampling time of 0.02 seconds and controller coefficients (7) $C_1 = 12$, $C_0 = -9.9$, the structure in Fig. 11 is implemented for the above target patterns to understand the

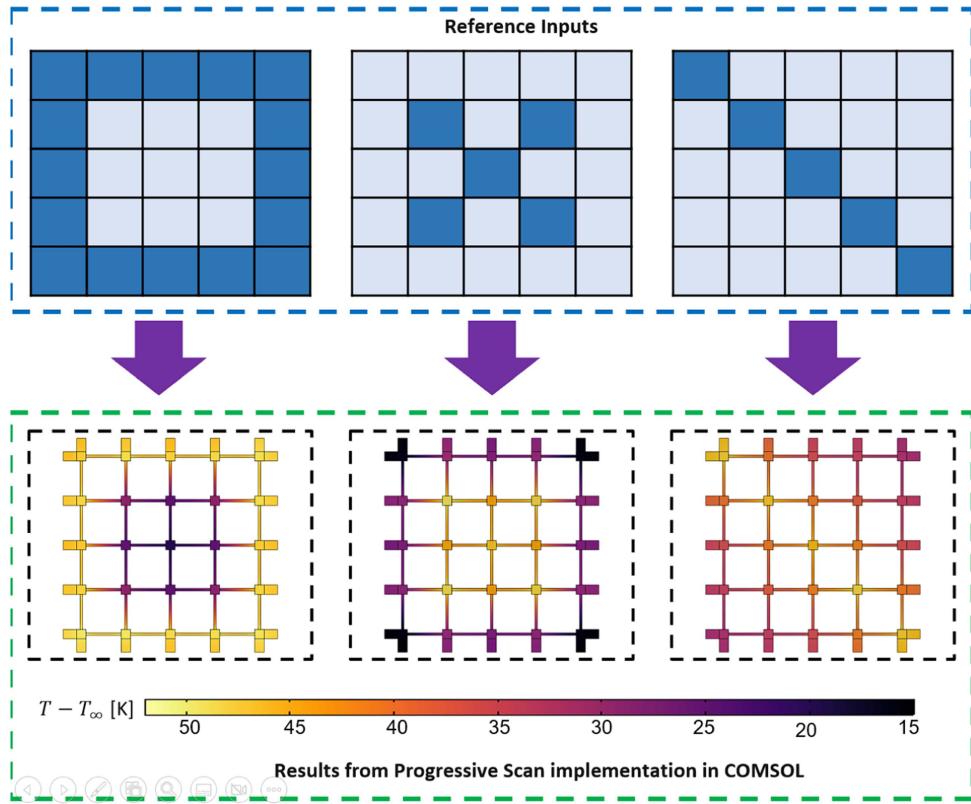


Fig. 13. Progressive Scan Results [COMSOL Visualization of Final Patterns] (left to right): Well Shape, Cross Shape, Diagonal Shape.

effect of target patterns and addressing methods on observed crosstalk.

Looking at the crosstalk in the device for the 3 designs obtained from COMSOL-Simulink simulations (Figs. 12 and 13), one may note the following:

- 1) *Well shape {Non-Addressed Pixel Temperature Range $\approx [40^\circ\text{C}, 50^\circ\text{C}]$ }*: Since all of the crosstalk in the device is localized to the pixels that also get addressed, the effect of electrical crosstalk is minimal as we can see in Figs. 12(a) and 13(a). However, since the boundary pixels get heated, the paths for heat loss are closed off resulting in a maximum thermal crosstalk near the edges at around 60%. Towards the center, the temperature is lower than the edges by a margin of around 30 °C.
- 2) *Cross shape {Non-Addressed Pixel Temperature Range $\approx [35^\circ\text{C}, 65^\circ\text{C}]$ }*: The pixels exposed to electrical crosstalk in this case can be split into 2 groups: central and boundary groups. The central group of pixels exposed to electrical crosstalk often get addressed multiple times in each cycle due to the pattern and addressing method resulting in a high crosstalk in this group at around 91%. The boundary elements exposed to electrical crosstalk get addressed fewer times each cycle, resulting in lower crosstalk in this group at around 60%. The corner pieces never get addressed and hence remain relatively colder compared to the rest of the array, as we can see in Figs. 12(b) and 13(b).
- 3) *Diagonal shape {Non-Addressed Pixel Temperature Range $\approx [50^\circ\text{C}, 62^\circ\text{C}]$ }*: Since all pixels get exposed

to electrical crosstalk, as we can see in Figs. 12(c) and 13(c), the maximum crosstalk in the array at around 80% is really close to the minimum crosstalk at around 60%.

Thus, one can see that the crosstalk seen in a particular non-addressed pixel (which could also be spatially different through the array) for an array depends not only on the device structure, but also on the addressing scheme and the interplay between the desired pattern and constraints imposed by the electrode coupling between pixels.

VII. CONCLUSION

As arrays of actuators in soft robotics and manipulation platforms have evolved to contain an increasing number of elements and increased requirements on the resolution of these arrays to achieve finer control to better affect the environment around it, it becomes increasingly important to find solutions which reduce the number of control inputs since addressing each pixel separately may not always be possible due to higher complexity of device design and control. Matrix addressing provides an elegant solution to this. In this study specifically, we consider passive matrix addressing over active matrix addressing due to reasons such as compatibility with large area fabrication methods and low-cost materials, which however comes with the non-negligible limitation of higher electrical coupling between pixels resulting in larger deviation from the ideal operation seen in a directly addressed array. A problem where such deviation may be acceptable is in the case of thermal actuator arrays where

the thermal array is used in conjunction with a thermally responsive material like Paraffin, where the material shows actuation only when the temperature applied is larger than a threshold temperature. This threshold temperature could directly translate to an upper limit in the possible crosstalk in the thermal array, suggesting that if neighboring pixels are at a temperature lower than this threshold, the thermal crosstalk might not be reflected in the mechanical behavior of the array. Hence, considering such application scenarios, the thermal crosstalk in a passively addressed $M \times M$ thermal actuator array with a laminated structure is analyzed.

In order to understand the thermal crosstalk, the key parameters of interest in such a laminated structure where intersecting arrays of electrodes sandwich a high resistive heating layer are considered to be the layer thicknesses, material electrical conductivities, electrode thermal conductivity, geometrical factors such as width of connective volumes and spacing between pixels, and finally the scale of array or the desired pixel dimensions. The effects of modification of these parameters was analyzed using Finite Element Analysis studies in COMSOL. Through these studies, a coupling between the thermal and electrical subsystem was noted, which resulted in a competing relationship between low crosstalk and low power requirements. In the structure of the thermal array studied in the paper, since the major form of thermal diffusion (which causes thermal crosstalk) is in the connective volumes of electrodes between the pixels, an immediate competition between increasing thermal resistance (to reduce thermal crosstalk) and increasing electrical resistance (which increases voltage requirements) can be noticed. This is why actions which seek to reduce thermal crosstalk may also end up increasing the voltage requirement, or even make the addressing structure invalid. This imposes constraints on the electrode geometry which directly translate to bounds on the thermal crosstalk between pixels in the device. The effects of such parameter variation is shown in a sample 16×16 array where appropriate changes in the width factor and material conductivity ratio improves the conductivity ratio by nearly 22.5% while simultaneously increasing the voltage requirements.

Taking this into consideration, the geometry of the electrode and material properties is optimized at different array scales and dimensions to notice trends in the designs with the lowest crosstalk. Optimizing the array with the weighted objective of reduction in crosstalk and simultaneous reduction in voltage input requirements further goes to show this competing relationship.

Furthermore, due to the electrical coupling between pixels, certain target patterns become unrealizable using constant voltage inputs for the device. Progressive scan is then employed to overcome these limitations, but further limitations on possible target shapes are found, which affects the spatial distributions of crosstalk in non-addressed pixels of the array, allowing the performance of the same device to be different for different target shapes. Thus, careful consideration of the the possible thermal patterns is also required in order to understand whether passive addressing is feasible for the task.

It must also be considered that the specific constraints on the parameters not only come from the addressing methodology studied but also the mode of application being considered.

Certain application modes might experience repetitive mechanical stresses which may give lower bounds on the layer thicknesses and width/spacing factors. The manufacturing method may also play a large role in the selection of materials, as well as the scale of the array. In addition, environmental factors such as humidity and temperature/wind fluctuations must also be considered in order to understand differences in operating behavior of the device. The device designer also has several more interesting choices in improving the performance of the device by considering other thermal management strategies such as fluid cooling of the inter-pixel spaces in the soft array. Another important choice is the array pattern and arrangement of pixels in itself. Despite using passive addressing, it may be possible to consider other shapes such as spirals or cylinders by changing the way in which the pixels are addressed. Yet another important choice is the definition of crosstalk itself, which could be altered depending on the level of exactness and detail, rather than lumping into one quantity. Additionally, another focus of future research could be the control method for achieving arbitrary shapes, where it might be possible to achieve better performance by changing the cycle time for a pixel based on its location (existence of nearby heat sources) and temperature or by considering more advanced control algorithms. Furthermore, the control method could be improved by explicitly considering the dynamic response of the pixel and using model-based methods. However, considering that this is a primarily computational study, the focus was on characterizing the behavior of thermal crosstalk and its dependence on possible design parameters which would be useful for a device designer who may opt to use passive matrix addressing in a resistive heating array. A similar procedure could also be applied to active heating matrices, in order to reduce the thermal crosstalk due to thermal diffusion.

In summary, the primary objective of this study was to understand the key design parameters in a laminated $M \times M$ resistive heating array. Due to the non-negligible electrical coupling, careful consideration of the design objectives is required to understand if passive addressing is a suitable method to control such an array.

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