1. Description

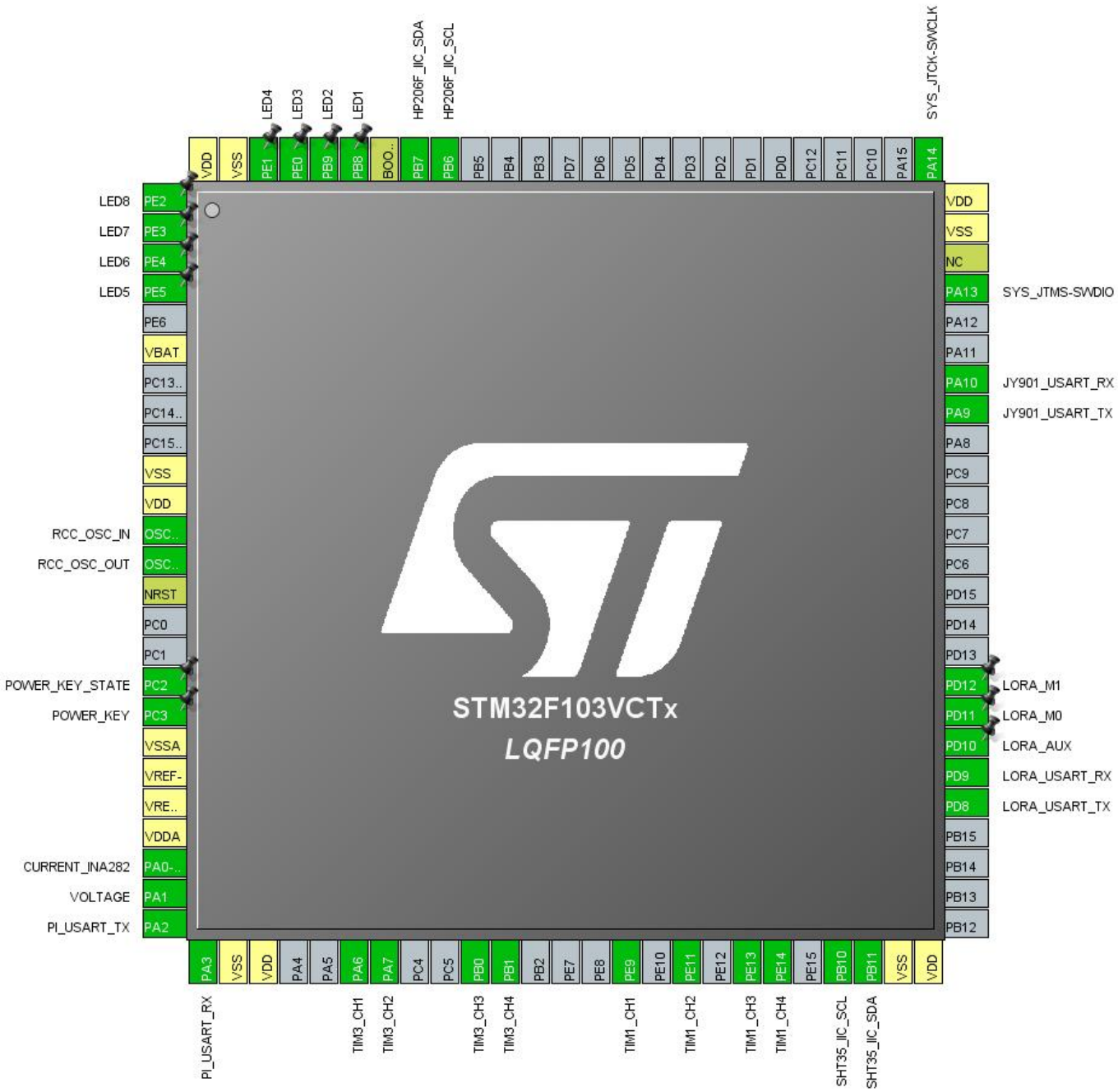
1.1. Project

Project Name	Fly_Vehicle
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	03/27/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



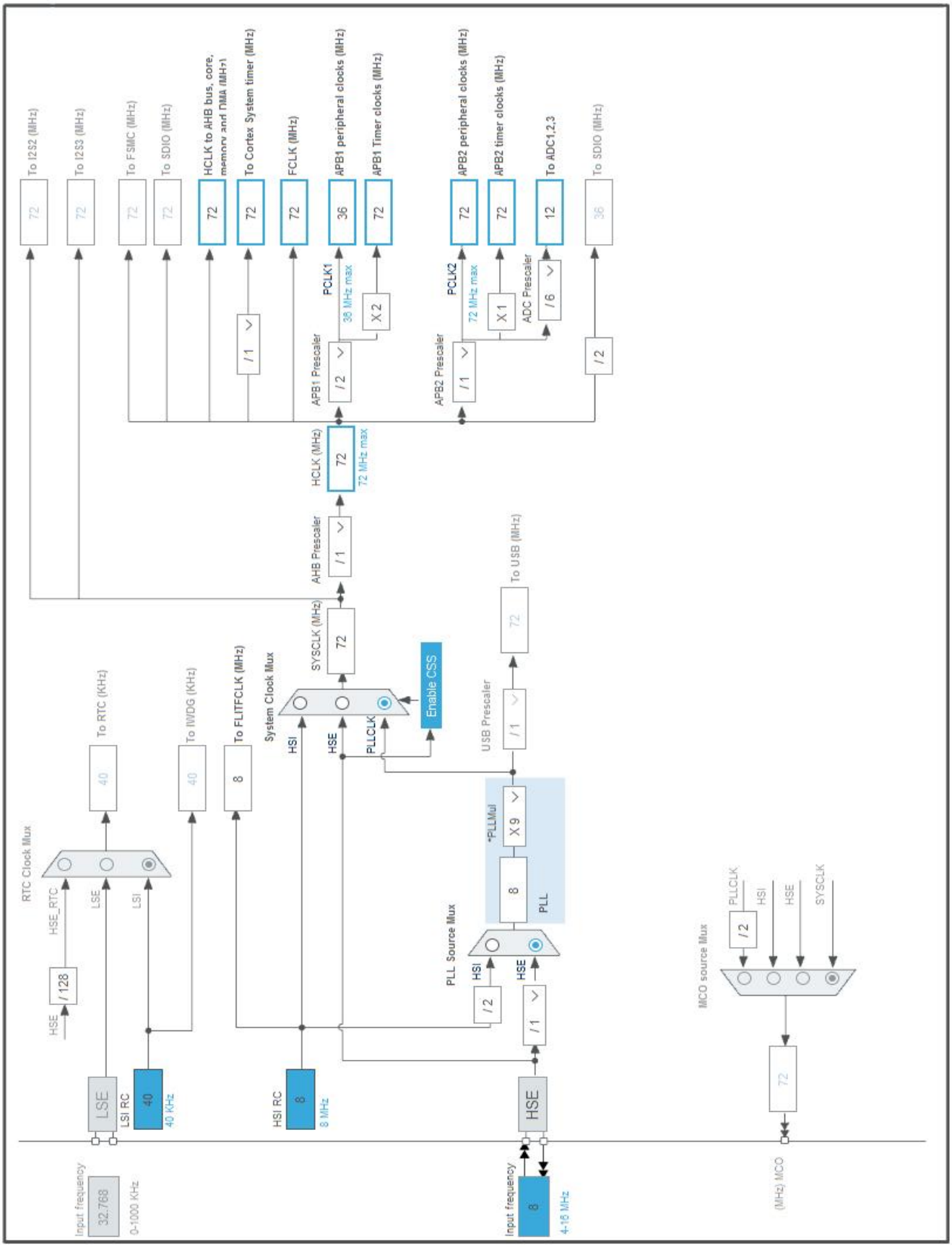
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	LED8
2	PE3 *	I/O	GPIO_Output	LED7
3	PE4 *	I/O	GPIO_Output	LED6
4	PE5 *	I/O	GPIO_Output	LED5
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	OSC_IN	I/O	RCC_OSC_IN	
13	OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
17	PC2 *	I/O	GPIO_Input	POWER_KEY_STATE
18	PC3 *	I/O	GPIO_Output	POWER_KEY
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	CURRENT_INA282
24	PA1	I/O	ADC1_IN1	VOLTAGE
25	PA2	I/O	USART2_TX	PI_USART_TX
26	PA3	I/O	USART2_RX	PI_USART_RX
27	VSS	Power		
28	VDD	Power		
31	PA6	I/O	TIM3_CH1	
32	PA7	I/O	TIM3_CH2	
35	PB0	I/O	TIM3_CH3	
36	PB1	I/O	TIM3_CH4	
40	PE9	I/O	TIM1_CH1	
42	PE11	I/O	TIM1_CH2	
44	PE13	I/O	TIM1_CH3	
45	PE14	I/O	TIM1_CH4	
47	PB10	I/O	I2C2_SCL	SHT35_IIC_SCL
48	PB11	I/O	I2C2_SDA	SHT35_IIC_SDA
49	VSS	Power		
50	VDD	Power		
55	PD8	I/O	USART3_TX	LORA_USART_TX
56	PD9	I/O	USART3_RX	LORA_USART_RX

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
57	PD10 *	I/O	GPIO_Output	LORA_AUX
58	PD11 *	I/O	GPIO_Output	LORA_M0
59	PD12 *	I/O	GPIO_Output	LORA_M1
68	PA9	I/O	USART1_TX	JY901_USART_TX
69	PA10	I/O	USART1_RX	JY901_USART_RX
72	PA13	I/O	SYS_JTMS-SWDIO	
73	NC	NC		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
92	PB6	I/O	I2C1_SCL	HP206F_IIC_SCL
93	PB7	I/O	I2C1_SDA	HP206F_IIC_SDA
94	BOOT0	Boot		
95	PB8 *	I/O	GPIO_Output	LED1
96	PB9 *	I/O	GPIO_Output	LED2
97	PE0 *	I/O	GPIO_Output	LED3
98	PE1 *	I/O	GPIO_Output	LED4
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Fly_Vehicle
Project Folder	F:\Items_ws\FLYER\Fly_Vehicle
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103VCTx
Datasheet	14611_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN1

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	**239.5 Cycles ***
Rank	**2 ***
Channel	Channel 0
Sampling Time	**239.5 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.3. I2C2

I2C: I2C

7.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.5. SYS

Debug: Serial Wire
Timebase Source: TIM7

7.6. TIM1

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**20000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM3

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**20000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***

Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**1500 ***
Fast Mode	Disable
CH Polarity	High

7.8. USART1

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.9. USART2

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.11. FREERTOS

Interface: CMSIS_V1

7.11.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8

USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**8192 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.11.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled

xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	CURRENT_INA282
	PA1	ADC1_IN1	Analog mode	n/a	n/a	VOLTAGE
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	n/a	**High ***	HP206F_IIC_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	n/a	**High ***	HP206F_IIC_SDA
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	n/a	**High ***	SHT35_IIC_SCL
	PB11	I2C2_SDA	Alternate Function Open Drain	n/a	**High ***	SHT35_IIC_SDA
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	n/a	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	n/a	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	n/a	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	n/a	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	n/a	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	n/a	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	JY901_USART_TX
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	JY901_USART_RX
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	**High ***	PI_USART_TX
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	PI_USART_RX
USART3	PD8	USART3_TX	Alternate Function Push Pull	n/a	**High ***	LORA_USART_TX
	PD9	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	LORA_USART_RX
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED8
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED6
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED5
	PC2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	POWER_KEY_STATE
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	POWER_KEY

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_AUX
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_M0
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_M1
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART3_RX	DMA1_Channel3	Peripheral To Memory	Low
USART3_TX	DMA1_Channel2	Memory To Peripheral	Low
ADC1	DMA1_Channel1	Peripheral To Memory	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal

Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel2 global interrupt	true	5	0
DMA1 channel3 global interrupt	true	5	0
DMA1 channel4 global interrupt	true	5	0
DMA1 channel5 global interrupt	true	5	0
DMA1 channel6 global interrupt	true	5	0
DMA1 channel7 global interrupt	true	5	0
USART1 global interrupt	true	5	0
USART3 global interrupt	true	5	0
TIM7 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART2 global interrupt	unused		

*** User modified value**

9. Software Pack Report