ststp

a Risc-V based processor implementation

Serves more for my own learning experiment than for any real-world use cases.

1 Device Overview

1.1 General Description

Ststp is a four stage (fetch, decode, execute, writeback) pipelined RISC-V processor utilizing a Harvard architectural design. It currently implements the base RV32I standard, and hopefully the multiply, floating point, and bit manipulation extensions soon.

1.2 Top-Level Block Diagram

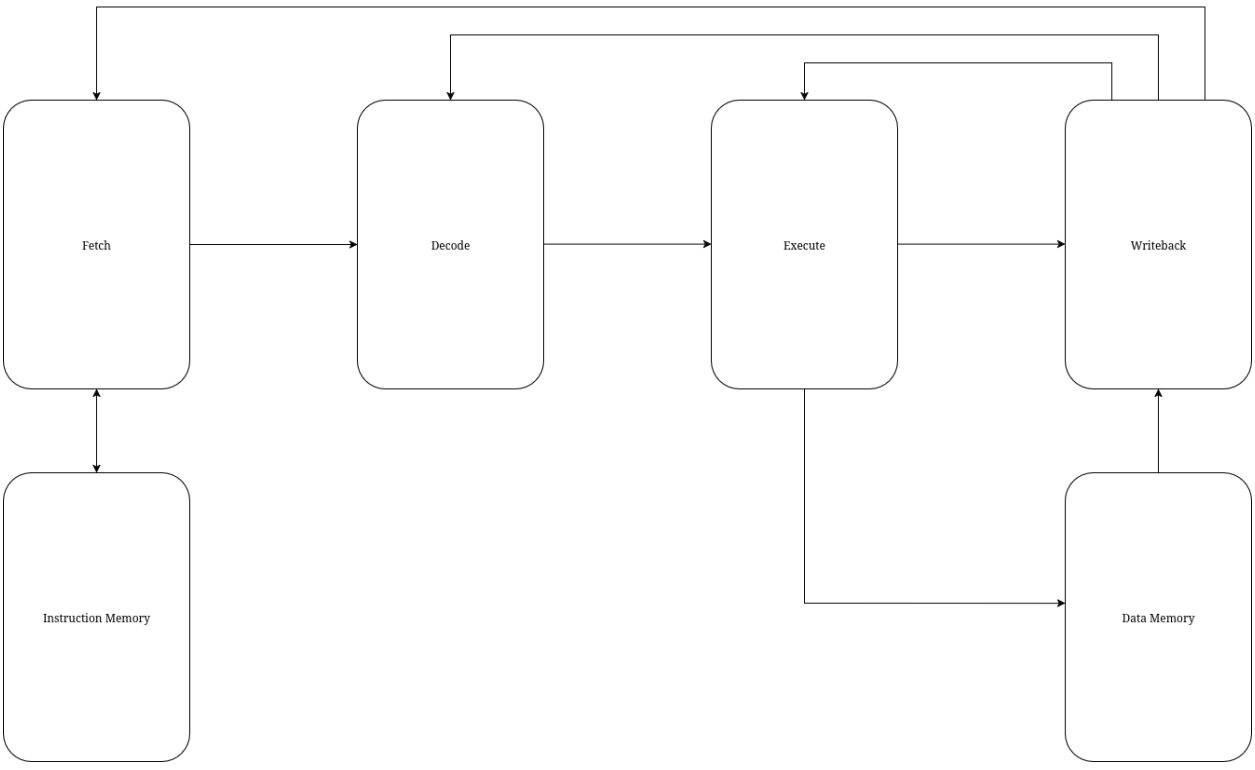

Figure 1: block diagram as of now