

CONG WANG

IEEE Student Member

Postgraduate Student ◇ School of Microelectronics

Southern University of Science and Technology (SUSTech)

12132472@mail.sustech.edu.cn

RESEARCH INTERESTS

Advanced simulation algorithms for Electronic Design Automation (EDA)

PUBLICATIONS

[C1] **Cong Wang**, Dongen Yang, Quan Chen, “EI-MOR: A Hybrid Exponential Integrator and Model Order Reduction Approach for Transient Power/Ground Network Analysis”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2022 (**Accepted**)

[J1] **Cong Wang**, Dongen Yang, Quan Chen, “On Model Order Reduction and Exponential Integrator for Transient Circuit Simulation”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), (**In preparation**)

EDUCATION BACKGROUND

Southern University of Science and Technology

Sept. 2021 - Present

➤ Master, School of Microelectronics

Supervisor : Prof. Quan CHEN

➤ Award: SUSTech Postgraduate Scholarship (2021, 2022)

Zhengzhou University

Sept. 2017 - Jul. 2021

➤ B.Eng. School of Information Engineering

➤ The average score: 80+ Rank: 20%

➤ Award: National Encouragement Scholarship (2019, 2020)(**3%**) The Third Prize Scholarship (2021)(**15%**)
Merit Student of Zhengzhou University (2019, 2020)(**10%**)

First Award of "Challenge Cup" National College Student Business Plan Competition in the university (2019)

First Award of Zhengzhou University in National Mathematics Competition for College Students (2020)

Second Award of Henan province in National Mathematics Competition for College Students (2020)

First Award of Zhengzhou University in “Qishi Cup” Mathematics Competition (2020)(**Rank the 1st**)

RESEARCH EXPERIENCE

“Research on Post-simulation Acceleration Technology of Analog Circuit Based on Exponential Integration”,

Research Project from National Natural Science Foundation of China (NSFC)

Jan. 2022 - Present

➤ Develop Exponential Integration-based methods to replace traditional SPICE for accelerating transient circuit simulation

➤ Position: key participant

“Model order reduction for large-scale circuit simulation”, Collaborative project with Hisilicon, Huawei

Jul. 2021 - Jul. 2022

➤ Develop industrial-grade C++ programs of passivity preserving model order reduction methods (PRIMA and BDSM)

➤ Position: first contributor

SELECTED HONORS AND SKILLS

Honors

Excellent Student Cadre (2019)

Advanced Individual of Social Work (2018)

Excellent Communist Party Member (2021)

Excellent Student Volunteer (2018)

Skills

Coding&Debug: C/C++, Matlab, Python (Numpy, Scipy)

English Level: IELTS(**7.0**)