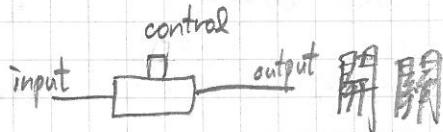
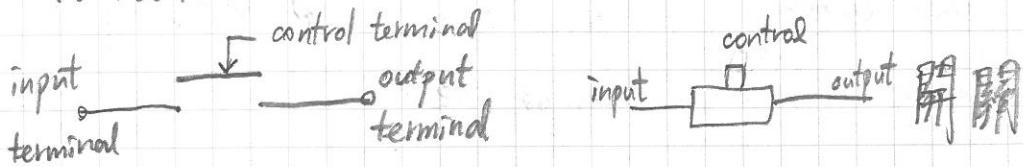


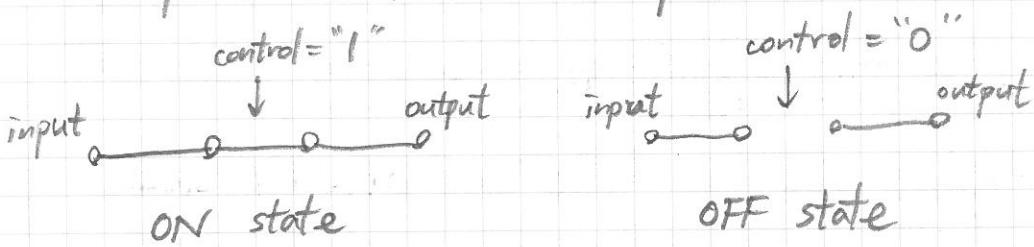
P54 ★ The MOSFET switch

(Metal Oxide Semiconductor Field-Effect Transistor)

A switch is a three-terminal element in a circuit.



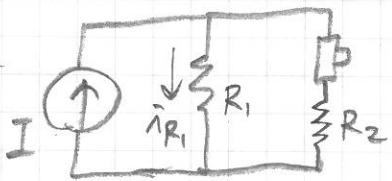
Ideally, input to the control terminal determines whether or not there is a short circuit between the input terminal and the output terminal:



(compare this with an ideal diode --- , P39)

Such a simple idea of a switch enables many ways to control the response of certain elements in a circuit. First, let's look at two examples showing how a switch may impact the response of another element in a circuit:

Example 1.

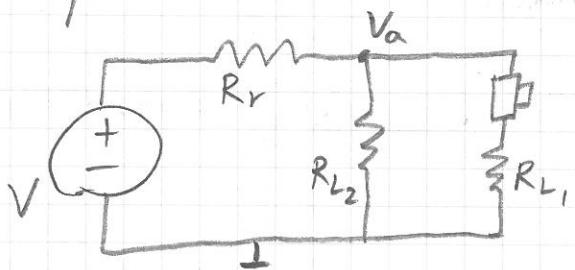


A switch connected in series with resistor R_2 will impact the current flowing through resistor R_1 .

$$\text{ON state: } i_{R_1} = I \times \frac{R_2}{R_1 + R_2}$$

$$\text{OFF state: } i_{R_1} = I$$

Example 2.



$$\text{ON state: } V_a = V \times \frac{R_{L_2} // R_{L_1}}{R_r + R_{L_2} // R_{L_1}}$$

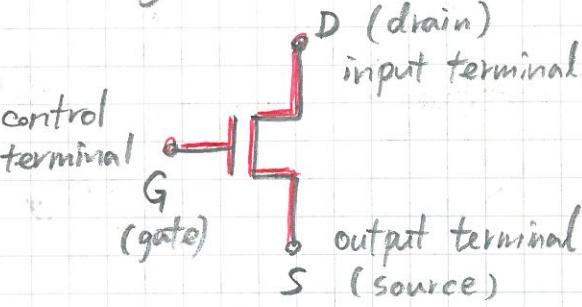
$$\text{OFF state: } V_a = V \times \frac{R_{L_2}}{R_r + R_{L_2}}$$

The voltage across the resistor R_{L_2} will drop if the switch is in the ON state, because of the existence of R_r .

Conceptually, by connecting two switches in series we may implement the AND logic; by connecting two switches in parallel, we may implement the OR logic. In both cases, the control terminals take the input logical values.

P56

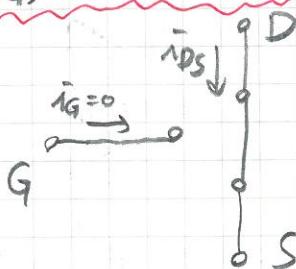
The symbol of a MOSFET



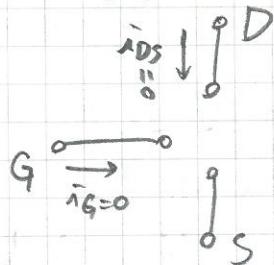
Let i_{DS} be the current flowing from the drain to the source, V_{GS} be the voltage across the gate and the source, and V_T be a threshold voltage.

In its simplest model (\underline{s} model), the MOSFET behaves as follows :

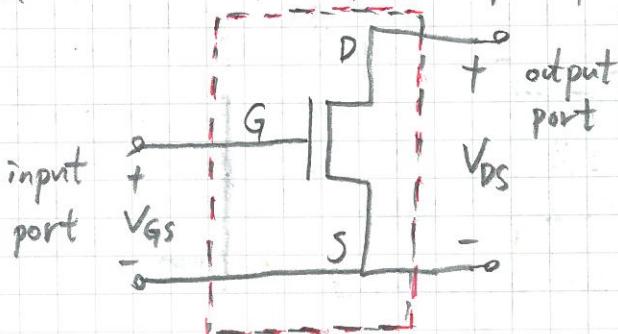
$$V_{GS} \geq V_T \Rightarrow \text{ON state}$$



$$V_{GS} < V_T \Rightarrow \text{OFF state}$$



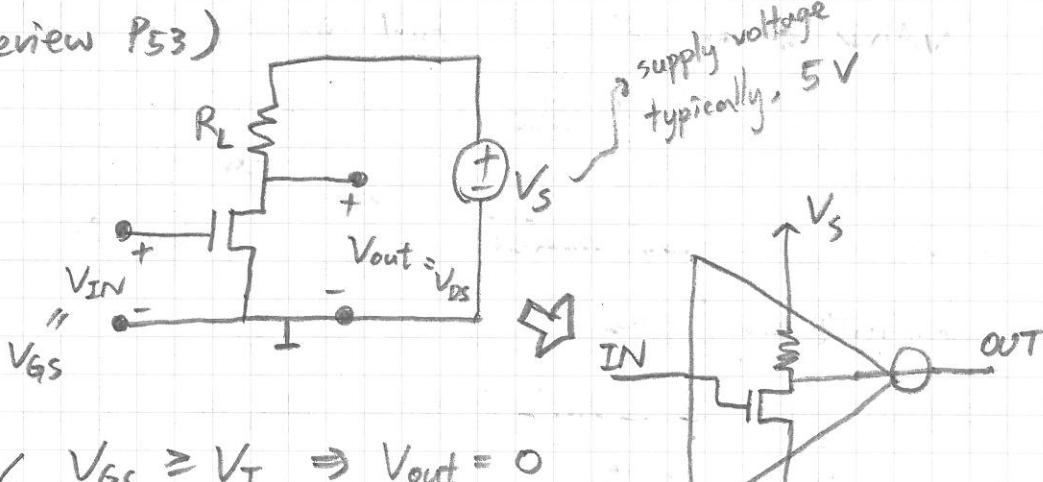
And in terms of input/output ports:



Later, we will study some more realistic models of MOSFET (for example, explicitly consider its internal resistance). For now, let's focus on the S model and its switching behavior. P57

We may use a MOSFET to construct a logical NOT gate $\rightarrow \text{D}\circlearrowleft$, so-called an "inverter":

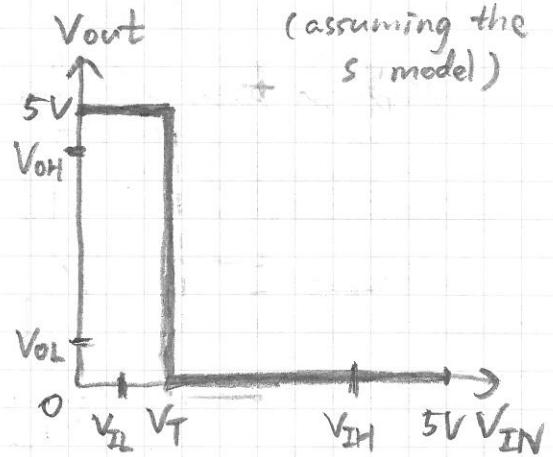
(review P53)



$$\left. \begin{array}{ll} V_{GS} \geq V_T \Rightarrow V_{out} = 0 \\ (\text{logic 1}) & (\text{logic 0}) \end{array} \right\}$$

$$\left. \begin{array}{ll} V_{GS} < V_T \Rightarrow V_{out} = V_S \\ (\text{logic 0}) & (\text{logic 1}) \end{array} \right\}$$

transfer characteristic of an inverter (assuming the S model)

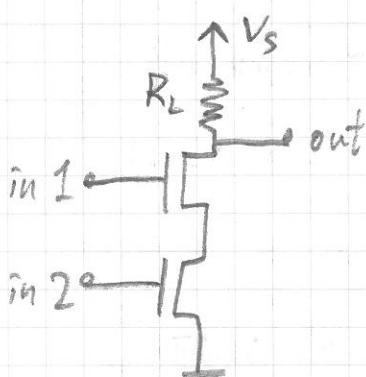


A valid mapping of voltage levels specified in the static discipline $\rightarrow V_{OL}$

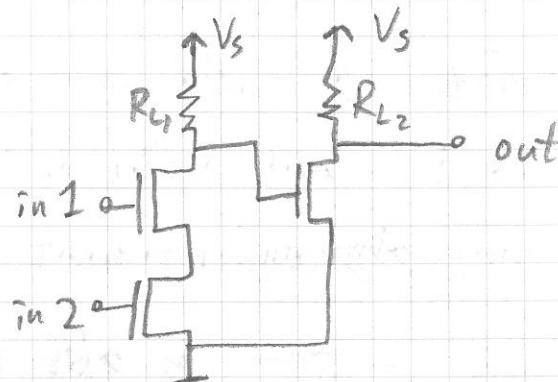
(review P52)

P58

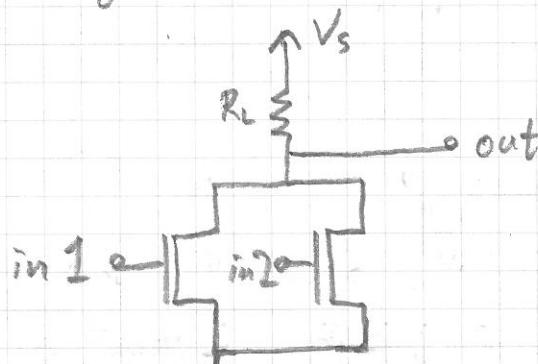
Similarly, we may use MOSFETs to construct other logic gates:



NAND gate



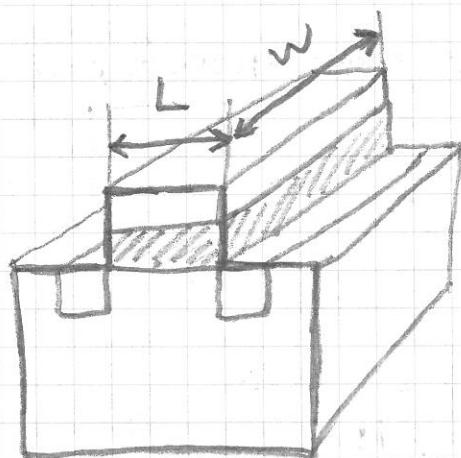
AND gate (NAND + NOT)



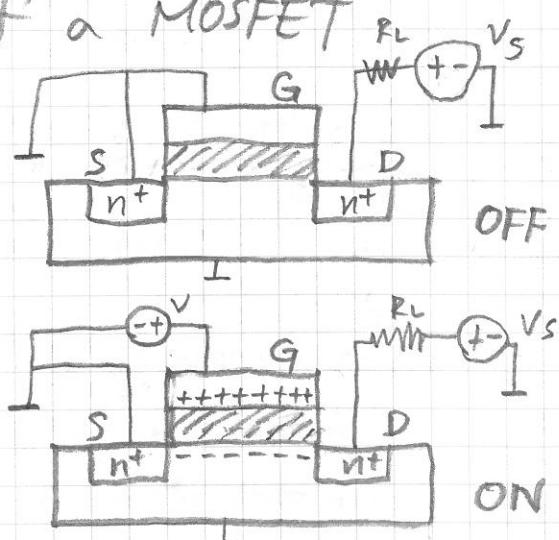
NOR gate

Exercise:
OR gate

★ Physical structure of a MOSFET



3D view



2D view

P59

When a positive voltage is applied at the control terminal G, a conducting channel will be built up between the two n^+ regions, and therefore some nontrivial current may flow from D to S. Read Section 6.7 in the textbook for a more detailed account.

The physical structure also implies that in the ON state there really will exist some resistance between D and S, and the value of the resistance is characterised by the dimensions of that conducting channel. Let R_N be the resistance per square of the channel, and L be the channel length and W the channel width.

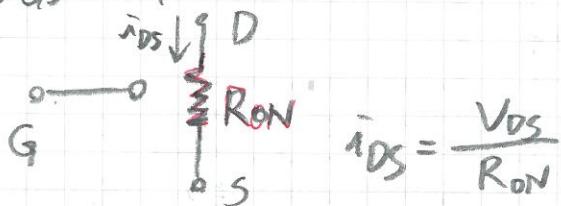
We have

$$R_{ON} = R_N \cdot \frac{L}{W} \quad (\text{review P6})$$

→ the resistance of the channel

The S model neglects R_{ON} . A more realistic model takes R_{ON} into account, and we call it the SR model:

$$V_{GS} \geq V_T \Rightarrow \text{ON state}$$



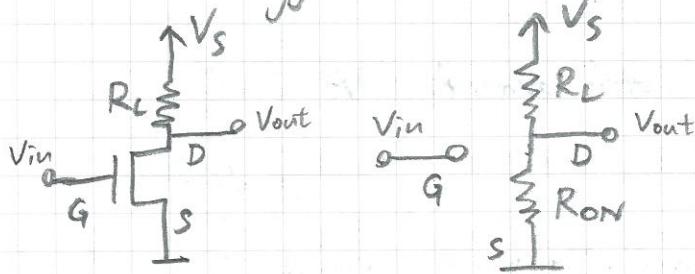
(the OFF state is same as that in the S model)

$$i_{DS} = \frac{V_{DS}}{R_{ON}}$$

P60 * Analyzing a MOSFET circuit using the SR model

Taking into account the impact from R_{ON} , the analysis may seem complicated, but it is still based on what we've learned so far.

Let's analyze an inverter to illustrate this:



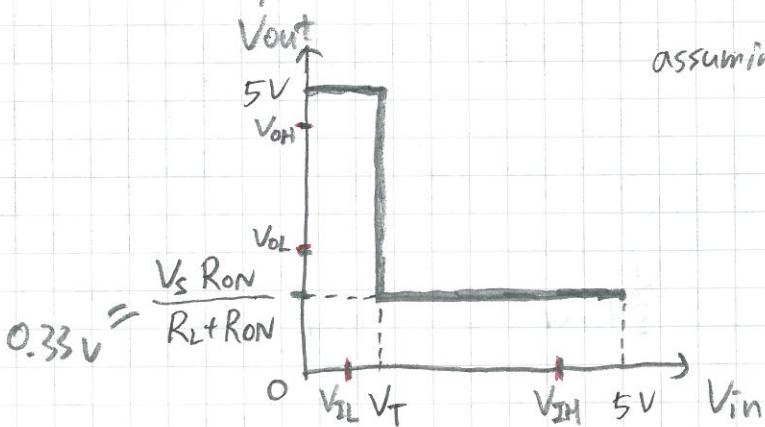
Because now we consider R_{ON} , the output voltage V_{out} will not be zero when $V_{GS} \geq V_T$;

instead,

$$V_{out} = V_s \times \frac{R_{on}}{R_L + R_{on}}$$

following the voltage-divider relationship.

And thus the transfer characteristic will become as follows (compare to one on P51):



assuming $V_s = 5V$

$$V_T = 1V$$

$$R_{on} = 1k\Omega$$

$$R_L = 14k\Omega$$

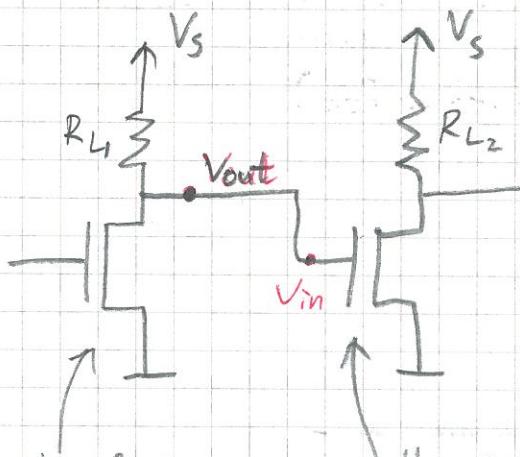
This change of V_{out} value has at least two impacts:

① To meet the static discipline, V_{out} needs to be lower than V_{OL} ; otherwise, we may observe that even though the magnitude of noise is within the specified margin, the value of V_{in} still exceeds V_{IL} .

→ solution A: redesign to reduce V_{out} .
(from the manufacturer's viewpoint)

→ solution B: replace by a compatible device.
(from the consumer's viewpoint)

② To drive another MOSFET, V_{out} in ON state needs to be lower than V_T , since V_{out} in OFF state equals $V_s \geq V_T$.
usually



(As another example,
see the AND gate)
on P58

the driving
MOSFET

the MOSFET whose ON/OFF state
is driven by the preceding MOSFET.

P62

study Examples 6.5 and 6.6 in the textbook.

In general, since $V_{out} = V_s \times \frac{R_{on}}{R_L + R_{on}}$,

to change V_{out} , we may {
① change V_s
② change R_L
③ change R_{on}

① \Rightarrow as a side-effect, it will also
change V_{out} in OFF state!

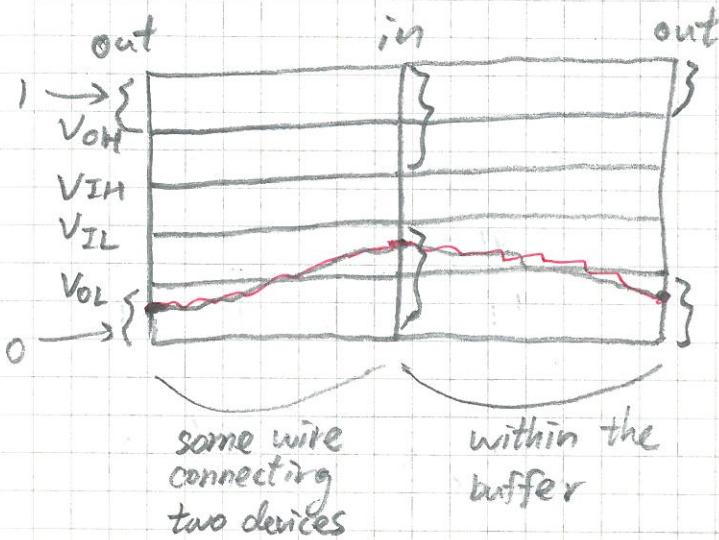
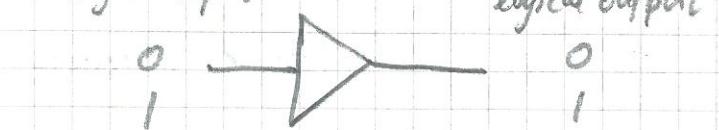
② \Rightarrow { larger resistance is hard to achieve in VLSI;
larger resistance would cause nontrivial
voltage drop in the presence of leakage current;

③ \Rightarrow may be achieved by changing the W/L ratio
of the MOSFET.

\Rightarrow An engineer's job often involves in finding
the best solution among "multiple" options !!

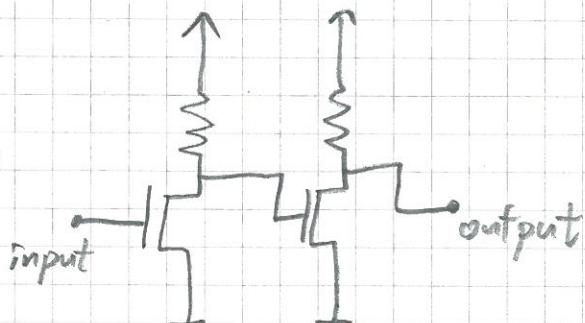
* Signal restoration, gain, and nonlinearity P63
(Section 6.9 in the textbook)

We may use a device called "buffer" to restore a distorted signal (distorted by noise, logical input logical output for example):



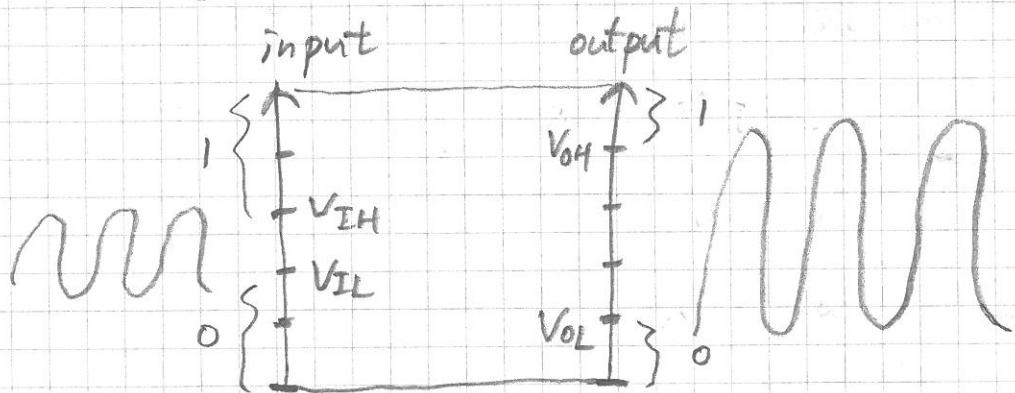
As long as the system follows the static discipline, the output of a buffer will be closer to the output of the device that precedes it.

A rough implementation
of a buffer:



P64

In order for an electronic device to satisfies the system's specification of the static discipline, it turns out that such a device must be capable of amplifying an input signal. Why? Because a signal may fluctuate between logic 0 and logic 1:

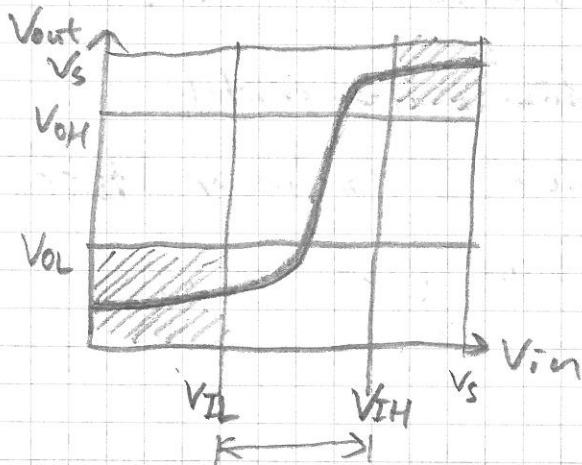


Definition :

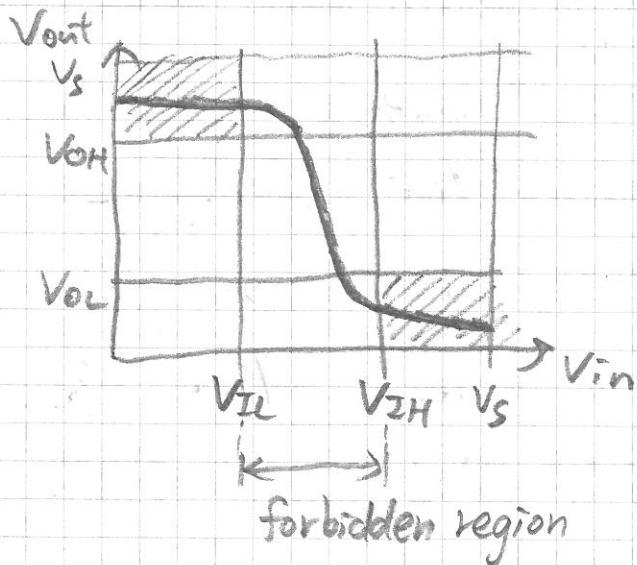
$$\text{Gain} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad \text{for } V_{IL} \rightarrow V_{IH} \text{ transition}$$

for example, if $V_{OH}=4$, $V_{IH}=3$, $V_{IL}=2$, $V_{OL}=1$
then the gain is 3.

The transfer characteristic of a buffer:



The transfer characteristic of an inverter:



In both cases, the shaded region represents the valid region for the transfer curve.

Note that since $V_{OL} < V_{IL}$ and $V_s - V_{OH} < V_s - V_{IH}$, the magnitude of the slope of the curve in the valid region is smaller than 1.

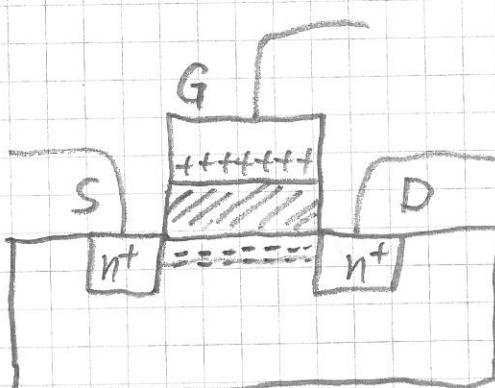
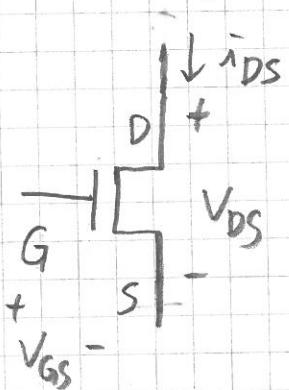
P66

So far, our discussion of MOSFET

include its behavior as a switch
(S model) as well as its linear $V_{DS} - i_{DS}$
relation in its ON state (SR model, with
resistor R_{ON}).

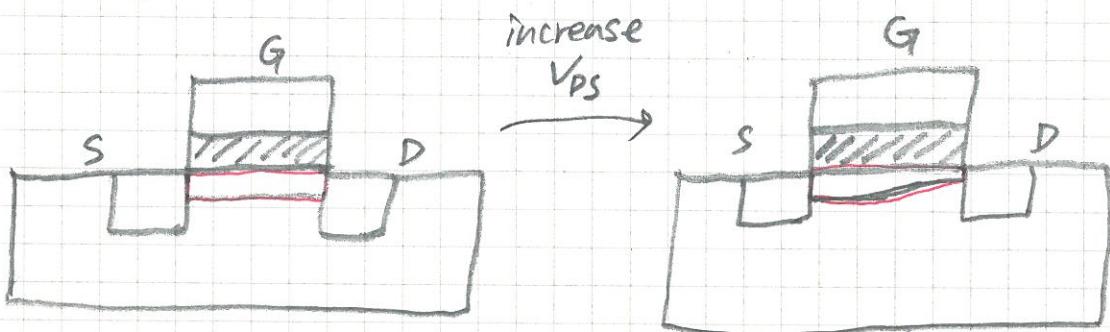
In science and engineering, we are often curious about how a system would behave should we increase/decrease the value of a certain parameter. We have seen that a MOSFET will go from OFF state to ON state as we increase voltage V_{GS} .

Now, let's consider what will happen if we gradually increase V_{DS} .

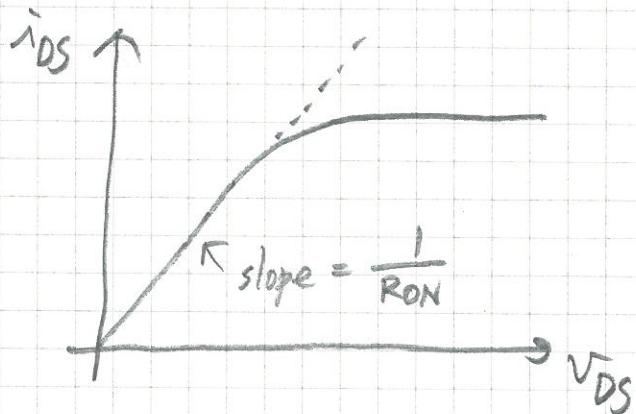


As we increase V_{DS} , the difference in electrical potentials between G and D decreases. → 電位差

This in turn will reduce the amount of free electrons near D, essentially shrinking the thickness of the conductible channel near D :



Therefore we will see a bending of the curve on the i_{DS} - V_{DS} plot :



電阻截面積 ↓
 \Rightarrow 電阻值 ↑
 \Rightarrow slope ↓