	1 1 1
2.0	solution
Name:)01-1

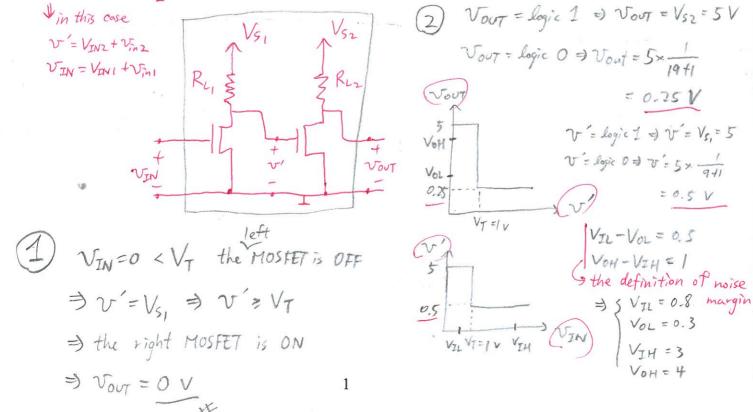
Student ID:

National Taiwan Normal University Department of Computer Science and Information Engineering CSU0007 - Basic Electronics Final Exam (June. 15, 2020)

Clearly state each step of your answer.

In the following questions, consider the circuit in Figure 1 (drawn on the blackboard).

- 1. (10 points) Consider the S model of the MOSFET. $V_{S1}=V_{S2}=5V$. $R_{L1}=R_{L2}=10$ k Ω . $V_{T}=1V$. Suppose that $v_{IN}=0V$. $v_{OUT}=?$
- 2. (10 points) Consider the SR model. We want to design a circuit such that if v_{IN} =logic 0, v_{OUT} will be logic 0, and that if v_{IN} =logic 1, v_{OUT} will be logic 1. Suppose V_T =1V, V_{S1} = V_{S2} =5V, V_{SN} =1 k Ω , V_{IL} =9 k Ω , V_{IL} =19 k Ω . And we want to have a noise margin of 0.5V for logic 0 and a noise margin of 1V for logic 1. Give a valid set of thresholds V_{OL} , V_{OH} , V_{IL} , and V_{IH} .
- 3. (10 points) Following Question 2, suppose that now V_{OL} = 0.5V, V_{OH} =4V, V_{IL} =0.9V, and V_{IH} =3V, and R_{ON} =2 k Ω , R_{L} =8 k Ω , V_{S1} =5 V, V_{T} =1V. What are the valid value ranges for R_{L1} and V_{S2} ?
- 4. (10 points) Again, consider the SR model. Suppose that we $V_{S1}=V_{S2}=5V$. $R_{L1}=10 \text{ k}\Omega$. $R_{ON}=2 \text{ k}\Omega$. $V_{T}=1V$. If we want $|v_{OUT}/v_{IN}|=0.5$, given $v_{IN}=0.5V$. What should be the value of resistance R_{L2} ?
- 5. (10 points) Following Question 5, but now consider the SCS model. If we still want |v_{OUT}/v_{IN}|=0.5, given v_{IN}=0.5V. Explain why in this case the right MOSFET will not operate in the saturation region.
- 6. (10 points) Following Question \$\frac{1}{5}\$, but now consider the SCS model. If $v_{IN}=1.8V$, find $v_{OUT}=?$
- 7. (10 points) Following Question 1 5, but now consider the SCS model. If $R_{L1}=8 \text{ k}\Omega$ and $R_{L2}=1.5 \text{ k}\Omega$. Find the maximum valid v_{IN} range for *both* MOSFETs to operate in the saturation region.
- 8. (10 points) Using graphical analysis to show that for a SCS model, if we increase R_{L2} and keep the same v_{IN} as before, then for the same v_{OUT} we will need to produce a smaller value of v'.
- 9. (10 points) Draw the small-signal model of the circuit in Figure 1.
- 10. (10 points) Following Question 9, suppose that we want to have the magnitude of the small-signal gain $|v_{out}/v_{in}|=0.5$, what should be the DC bias V_{IN1} ?





Sright MOSFET ON & Vour < 0.5 V

(note that if Riz=8Ksz, we'll have $V_{52} \times \frac{2}{8+2} < 0.5 = V_{52} < 2.5$, which conflicts to $V_{52} \times \frac{2}{8+2} < 0.5 = V_{52} < 2.5$, which conflicts to $V_{52} \times \frac{2}{8+2} < 0.5 = V_{52} < 2.5$, which conflicts to $V_{52} \times \frac{2}{8+2} < 0.5 = V_{52} < 2.5$ If you think of the left MOSFET inverter and the right MOSFET inverter as two components, you may write

$$| \frac{V_{OUT}}{V_{IN}} | = 0.5$$
 and $V_{IN} = 0.5V$ means we need $V_{OUT} = 0.25 V$
This suggests that the Vos of the right MOSFET is 0.25 V.
But $V_{IN} = 0.5V$ implies that VGs of the right MOSFET is 5V.
Thus we have $V_{GS} - V_T > V_{OS}$ and $V_{GS} > V_T$, which means that the right MOSFET is operating in the triode region.

 $V_{IN} > V_T$ suppose in saturation, then $v = V_{S_1} - \frac{k(V_{IN} - V_T)^2}{2}$. $R_{L_1} = 5 - \frac{10^3 \times 0.64}{2} \times 10 \times 10^3$

verify VIN-VT < 1.8 V, so indeed it operates in the saturation region. To compute Vout, apply the same procedure for the right MOSFET. Since I did not give the value of RLZ in this question, it's fine to just write voor = Vsz - K(V'-4)2 Rhz = 5 - 0.32×103 RLz

DA First, for the right MOSFET to operate in the saturation region,

(see Pages 358~359) in the textbook

$$\Rightarrow 1 \rightarrow \frac{-14\sqrt{1+2\times5\times1.5\times10^3\times10^3}}{1.5\times10^3\times10^3} + 1$$

> 1~3 v for v' this range dominates.

B) Then, for the left MOSFET, the maximum output range for the saturation region is

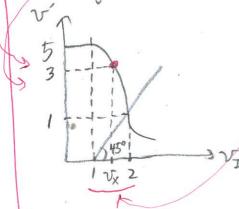
(again, see pages) 358~359

ララ~IV for で

Co Similarly, the maximum input range for the left MOSFET to operate in the saturation region is V7 > -1+JI+2Vsi·Ri·K + V7

+ 1~2 V for VIN

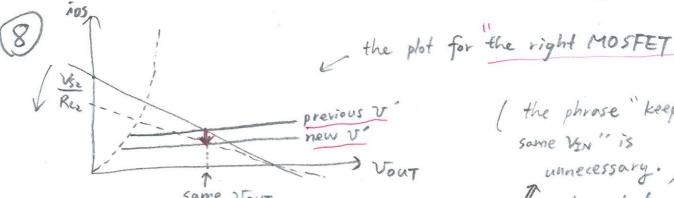
Combining A.B.C:



The maximum valid VIN range is

where 3=5- k(vx-4)2 RL

=> 1+505V & VIN = 2.V



open circuit Small-signed model

some VEN " is unnecessary.) for further study, that means we will need a larger value of RLI, and beware that Re, must not be too large to cause the left MOSFET to enter the triode region.

0.5 = | Vout | = K (VIN2 - VT) RL2 VINZ = VS1 - K(VINI) - VT) 2. RL => 5 VIN2 = 0.5 + VT VS1 - VINZ = KRLI (VINI-V7)2 => VINI = V7 + V(V5, -VINZ) - Z = V7 + \ \ \frac{2(Vs1 - V2N2)}{KRLI = V7 + \(\frac{2(V_{SI} - \frac{0.5}{KRL2} - V_{T})}{KRL2} \)

V= VIN2 + Vinz VIN = VINI + VIN1 our target I mistakenly circled this one on the blackboard ...

I the phrase "keep the