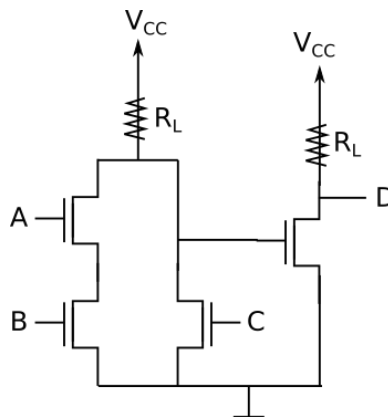


CSU0007 Basic Electronics, Homework 4

- Three questions in total. Submit your work via Moodle before 9PM, Dec 4th, 2020.
- Clearly state your reasoning to earn full score.
- Textbook coverage: Section 6.1 to Section 6.8 (before Section 6.8.1).
- The assignment for self-study: Section 6.8.1 in the textbook (no need to submit this assignment).

1. (30 points) Consider the S model. In the following circuit, suppose the input {A, B, C} corresponds to logical {0, 1, 0}. What would be the logical value output at D?



2. (40 points) Now, consider the SR model. Explain in your own words that under the static discipline,

1. (20 points) why we must have $V_{IL} < V_T$?
2. (20 points) why we must have $V_{OL} > V_{CC} \frac{R_{ON}}{R_{ON} + R_L}$?

3. (30 points) Consider the SR model and the following specification: The noise margin is 0.5V for logical 0 and 1V for logical 1. The forbidden region is from 1V to 1.5V. $V_T=1.2V$, $V_{cc}=3.3V$, and $R_N=5k\Omega$. Now, to build a MOSFET to meet this specification, what would be the minimum feasible value of ratio $\frac{L}{W}$? Assuming that $R_L=8k\Omega$.