FET113011

128X64

Evaluation Kit User Guide

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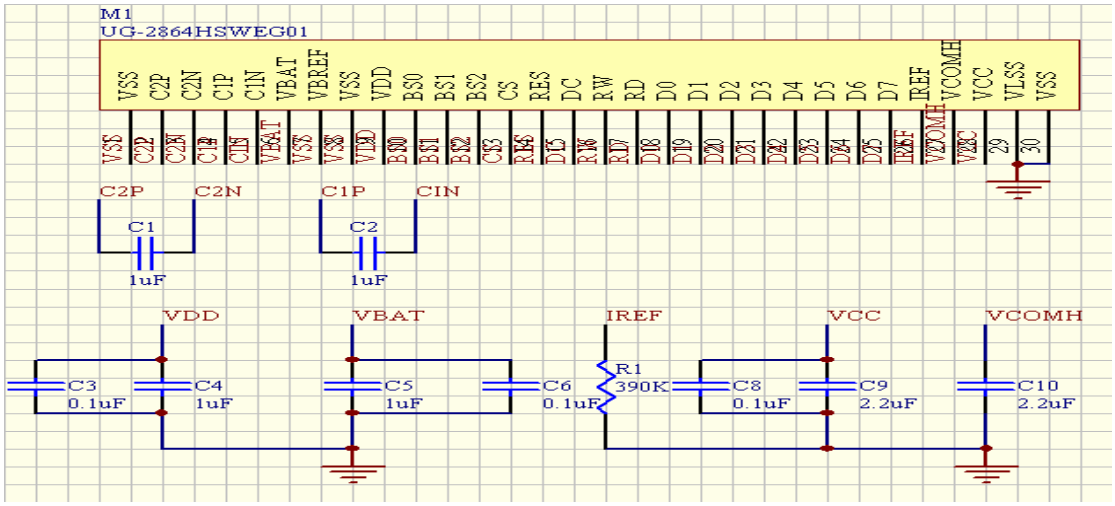
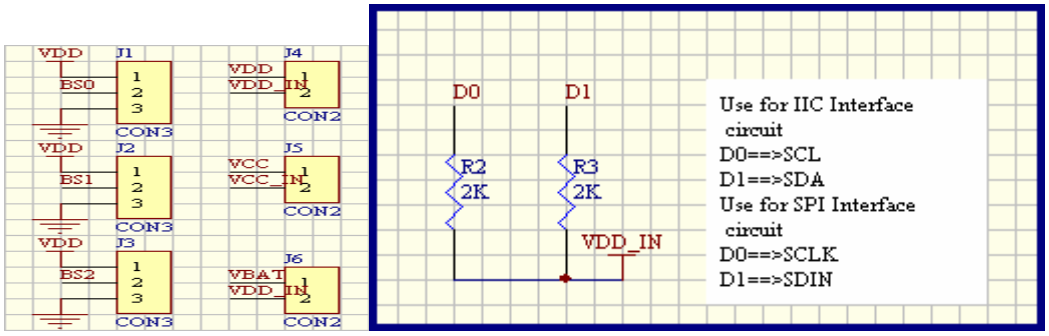
1. REVISION HISTORY

Date	Page	Contents	Version
2008/10/01		Preliminary	Preliminary 0.0

2. EVK Schematic





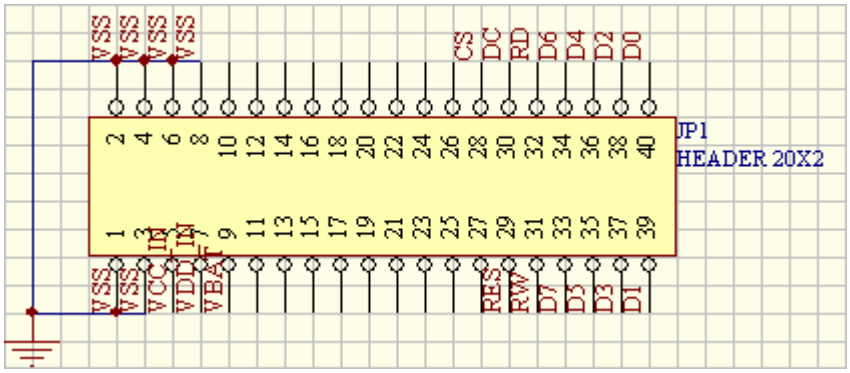


Table 7-1 : MCU Bus Interface Pin Selection

SSD1306 Pin Name	I²C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}

*** R1 should be replaced as 560kΩ while supplying 9V on VCC externally.**

3. Symbol define

VCC：Power supply for panel driving voltage.

VBAT：Power supply for panel driving voltage(Embedded Charge Pump).

VDD：Power supply for core logic operation.

VSS：This is ground pin.

BS0~BS2：MUC bus interface selection pin(Page 4 Table7-1).

CS：This pin is chip select input(active LOW).

RES：This pin is reset signal input(active LOW).

D/C：This is DATA/COMMAND control pin. When it is Pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register.

In I2C mode, this pin acts as SA0 for slave address select.

R/W：This is read/write control input pin connecting to the MCU interface.

When interface to a 6800-series microprocessor , Read mode will be carried out when this pin is pulled HIGH and write mode when low .

When interface to an 8080-microprocessor , this pin when be the data Write input.

When serial interface is selected, this pin must be connected to Vss.

E/RD：When interface to a 6800-series microprocessor , this pin will be used as the Enable(E) signal.

When interface to an 8080-microprocessor , this pin receives the Read(RD#)signal.

D0~D7：These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.

When serial interface mode is selected, D0(SCLK) will be the serial clock input,D1(SDIN) will be the serial data input,D2 should be left opened.

When I2C mode is selected,D1(SDA$_{in}$) AND D2(SDA$_{out}$) should be tied together,D0(SCL) is the I2Cclock input

IREF：This is segment output current reference pin.

VCOMH：This pin for COM signal deselected level voltage.

A capacitor should be connected between this pin and VSS.

VBAT: It should be connected to VDD (Charge Pump DISABLE) or could be connected to individual power voltage supply.

VBAT= 3.4~4.2V.(Charge Pump ENABLE)

C1P/C1N: It should be connected a capacitor.

C2P/C2N: It should be connected a capacitor.

VBREF : It should be connected VSS. It should be kept NC if it is not used.

BS[2:0]:MCU bus interface selection pins.

IREF:This is segment output current reference pin.
A resistor should be connected between this pin and VSS to maintain the IREF current at 12.5 uA.
FR: This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect.It should be kept NC if it is not used.
CL: This is external clock input pin.
When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to VSS. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS: This is internal clock enable pin. When it is pulled HIGH (i.e. connect to VDD), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#: This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to VDD) during normal operation.
CS#: This pin is the chip select input. (Active LOW)

4. IIC INTERFACES DESCRIPTIONS & TIMMING CHARACTERISTICS

4.1 80-Series MPU parallel Interface

WRITE CHARACTERISTICS

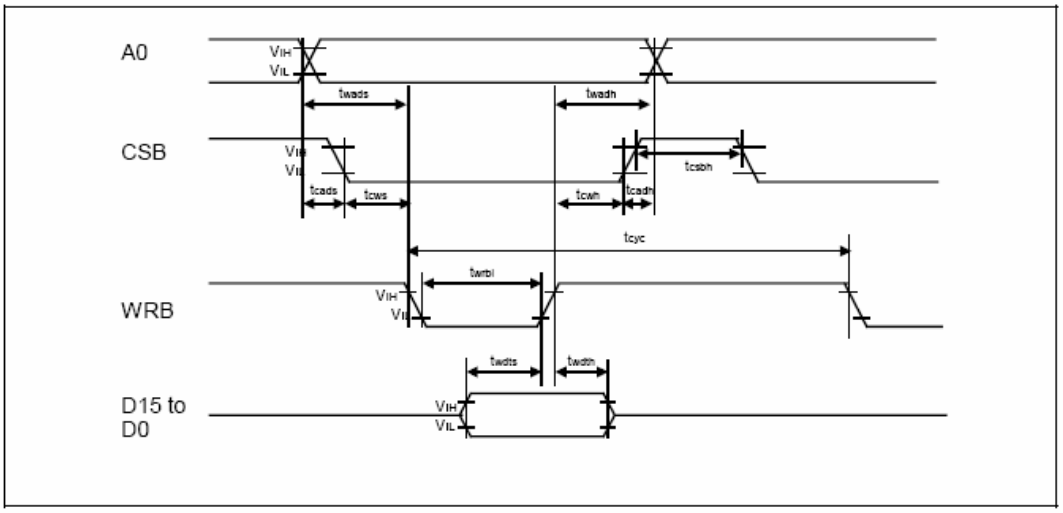


Figure 1 80-Series MPU parallel Interface Write Timing Diagram

(V_{DD} = 2.8V, Ta = 25 °C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{cyc}	Write cycle time	-	WRB	100	-	-	ns
t_{cads} t_{cadh}	Address and Select setup time Address and Select hold time	-	CSB,A0	0 0	- -	- -	ns
t_{wads} t_{wadh}	Address setup time Address hold time	-	A0	50 20	- -	- -	ns
t_{cws} t_{cwh}	Select setup time Select hold time	-	CSB	10 10	- -	- -	ns
t_{wrbl}	Write Low pulse width	-	WRB	30	-	-	ns
t_{csbh}	Select High pulse width	-	CSB	10	-	-	ns
t_{wdts} t_{wdth}	Data setup time Data hold time	-	D15 to D0	10 20	- -	- -	ns

Table 1 80-Series MPU parallel Interface Write Timing Characteristics

READ CHARACTERISTICS

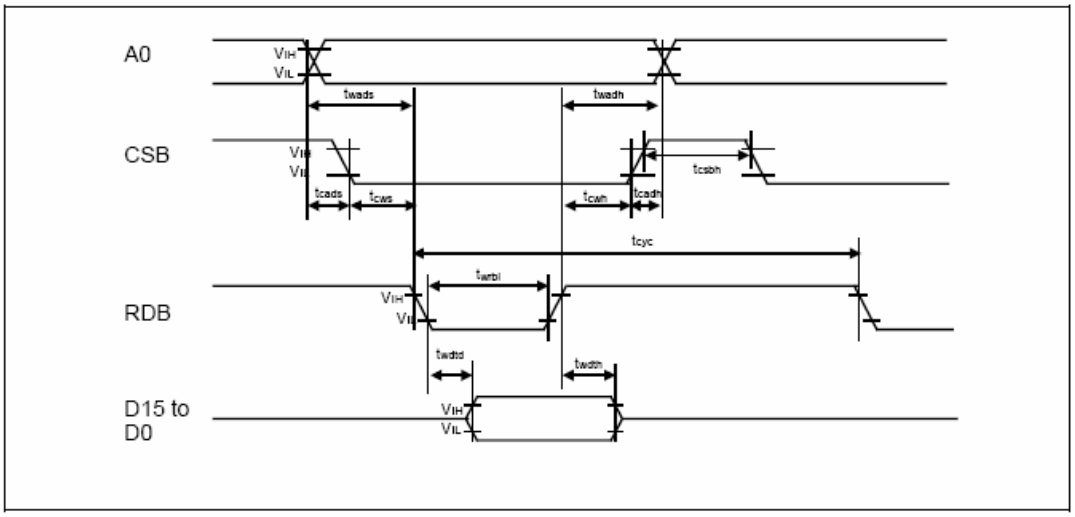


Figure 2 80-Series MPU parallel Interface Read Timing Diagram

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{cyc}	Read cycle time	-	RDB	500	-	-	ns
t_{cads} t_{cadh}	Address and Select setup time Address and Select hold time	-	CSB,A0	0 0	- -	- -	ns
t_{rads} t_{radh}	Address setup time Address hold time	-	A0	50 20	- -	- -	ns
t_{crs} t_{crh}	Select setup time Select hold time	-	CSB	10 10	- -	- -	ns
t_{rdbl}	Read Low pulse width	-	RDB	250	-	-	ns
t_{csbh}	Select High pulse width	-	CSB	10	-	-	ns
t_{rdtd} t_{rdth}	Data output delay time Data output hold time	CL = 100pF	D15 to D0	- 5	- -	200 -	ns

Table 2 80-Series MPU parallel Interface Read Timing Characteristics

4.2 6800-Series MPU parallel Interface

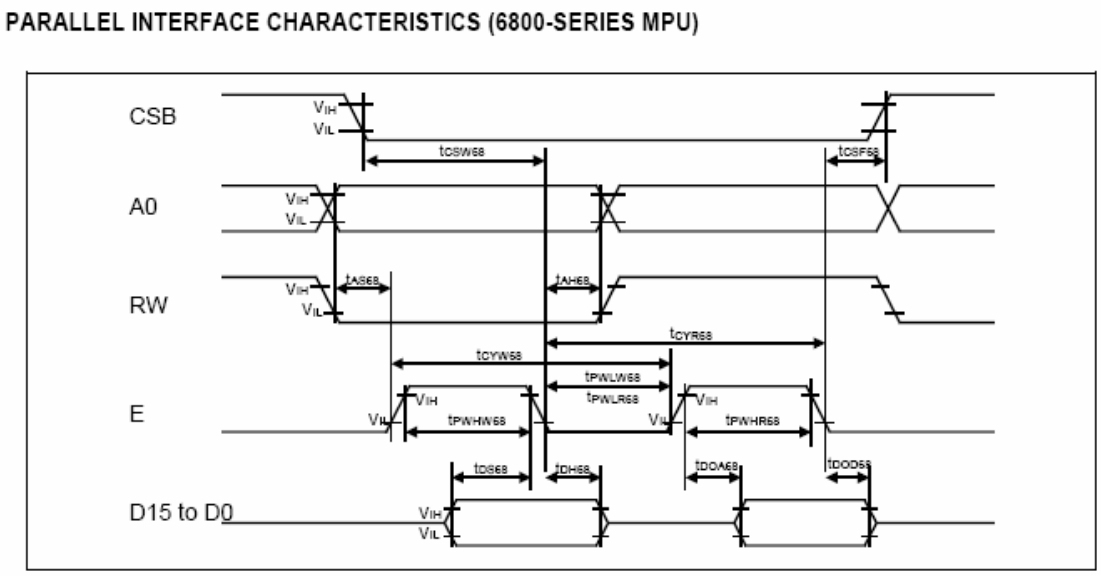


Figure 3 68-Series MPU parallel Interface Write Timing Diagram

(VSS=0V, VDD=2.8V,Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW68} t_{CSF68}	Chip select setup time Chip select hold time	-	CSB	10 10	- -	- -	ns
t_{AS68} t_{AH68}	Address setup time Address hold time	-	A0 RW	50 20	- -	- -	ns
t_{CYW68} t_{PWHW68} t_{PWLW68}	Write cycle time Write High Time Write Low Time	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	E	450 355 90	-	-	ns
t_{DS68} t_{DH68}	Data setup time Data hold time	-	D15 to D0	10 20	- -	- -	ns
t_{DOA68} t_{DOD68}	Data output access time Data output disable time	CL = 30pF		- 40	- -	40 80	ns

Table 3 68-Series MPU parallel Interface Write Timing Characteristics

4.3 SPI Interface

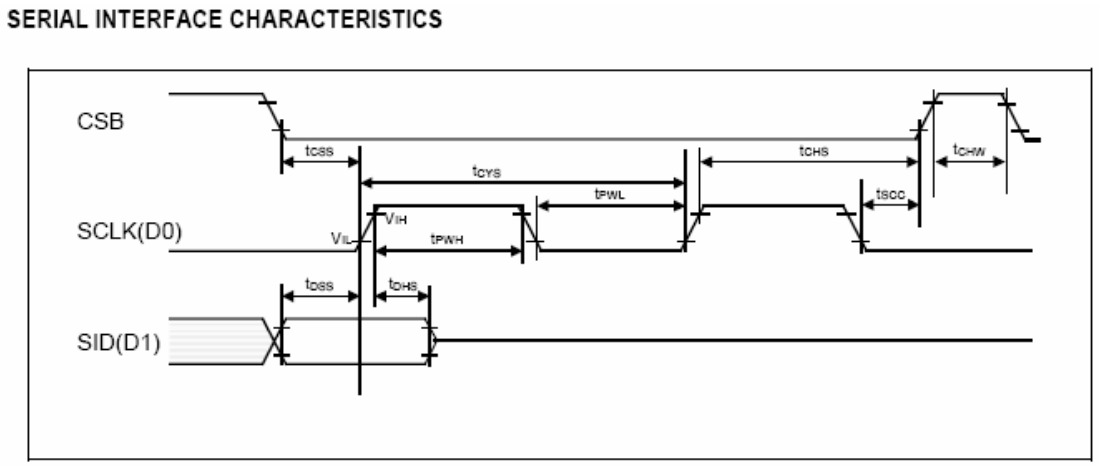


Figure 4 Serial peripheral interface Timing Diagram

(V_{SS}=0V, V_{DD}=2.8V, Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS}	Serial clock cycle	-	SCLK	160	-	-	ns
t_{WHS}	High pulse width			60	-	-	
t_{WLS}	Low pulse width			60			
t_{DSS}	Data setup time		SID (D1)	60	-	-	ns
t_{DHS}	Data hold time			60	-	-	
t_{CSS}	Chip select setup time	-	CSB	60	-	-	ns
t_{CHS}	Chip select hold time			65	-	-	
t_{CHW}	Chip select high pulse width			45	-	-	
t_{SCC}	SCLK to Chip select	-	SCLK, CSB	20	-	-	ns

Table 4 Serial peripheral interface Timing Characteristics

4.4 IIC Interface

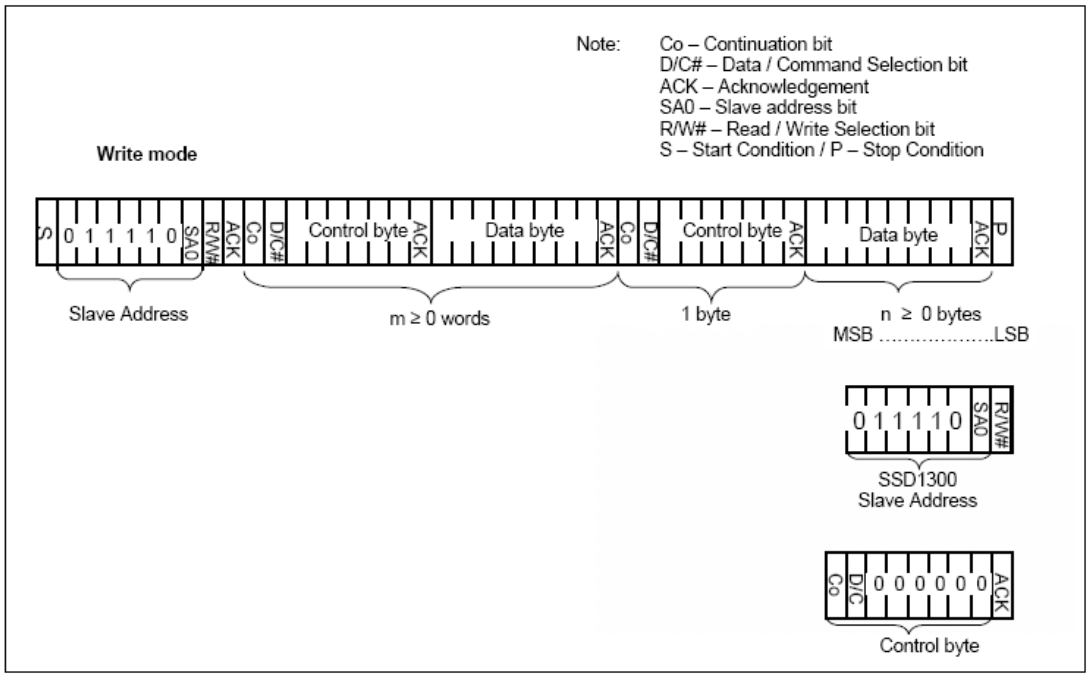
MPU I^2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/D_2 for output $/D_1$ and SDA_{IN} for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1300 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#
"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1300. D/C pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

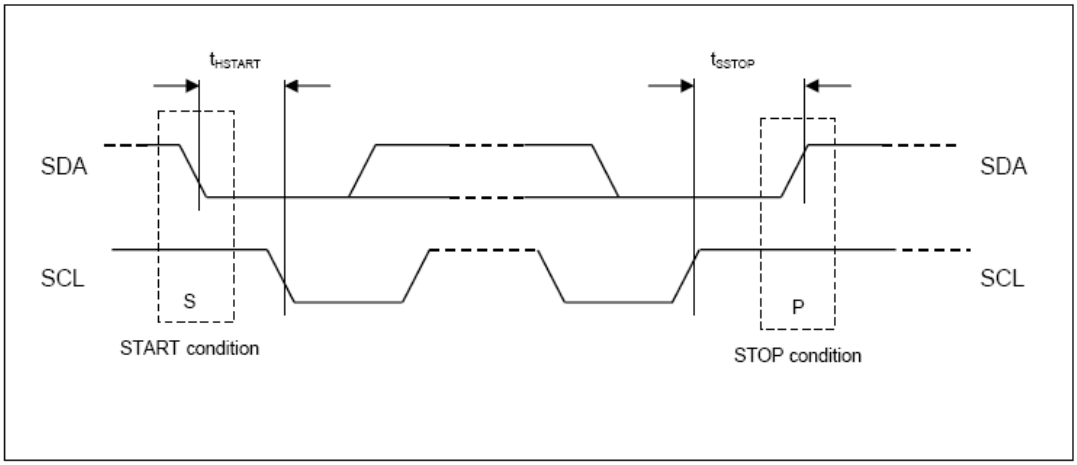
b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

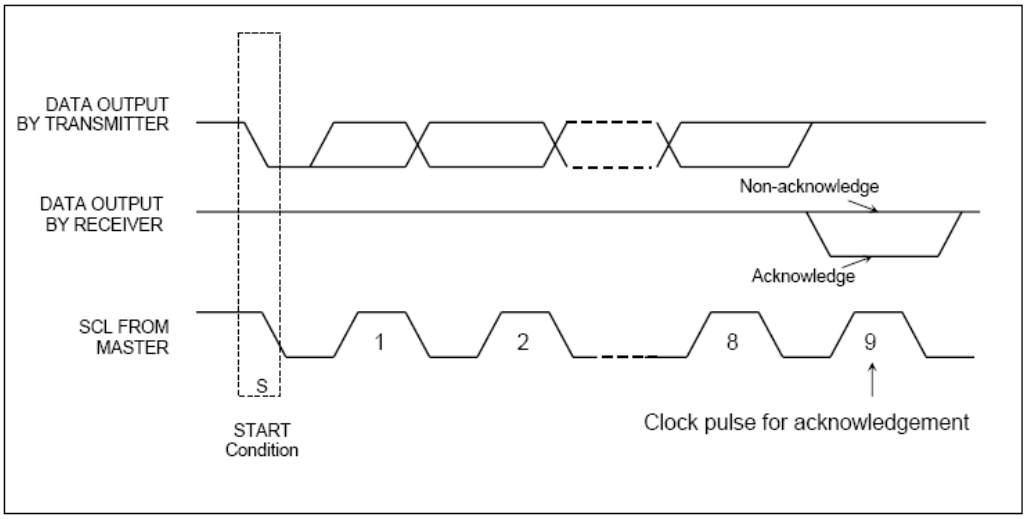
c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.



Write mode for I^2C

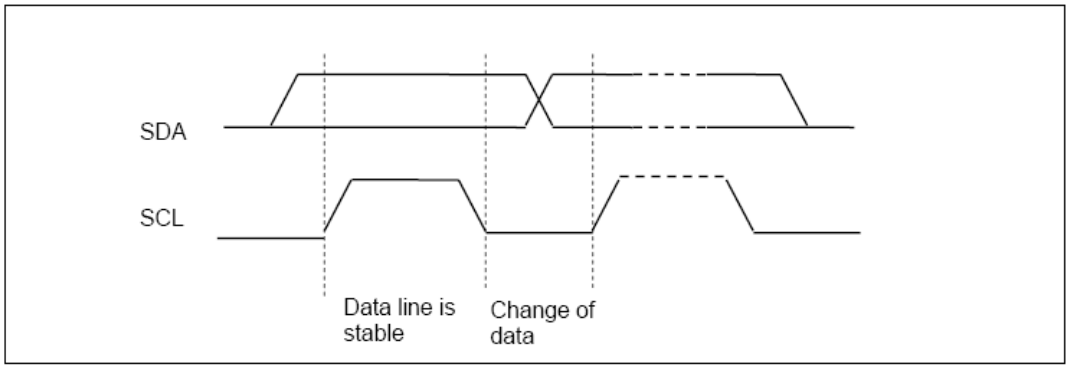
1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1300, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.





Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.



5.EVK use introduction

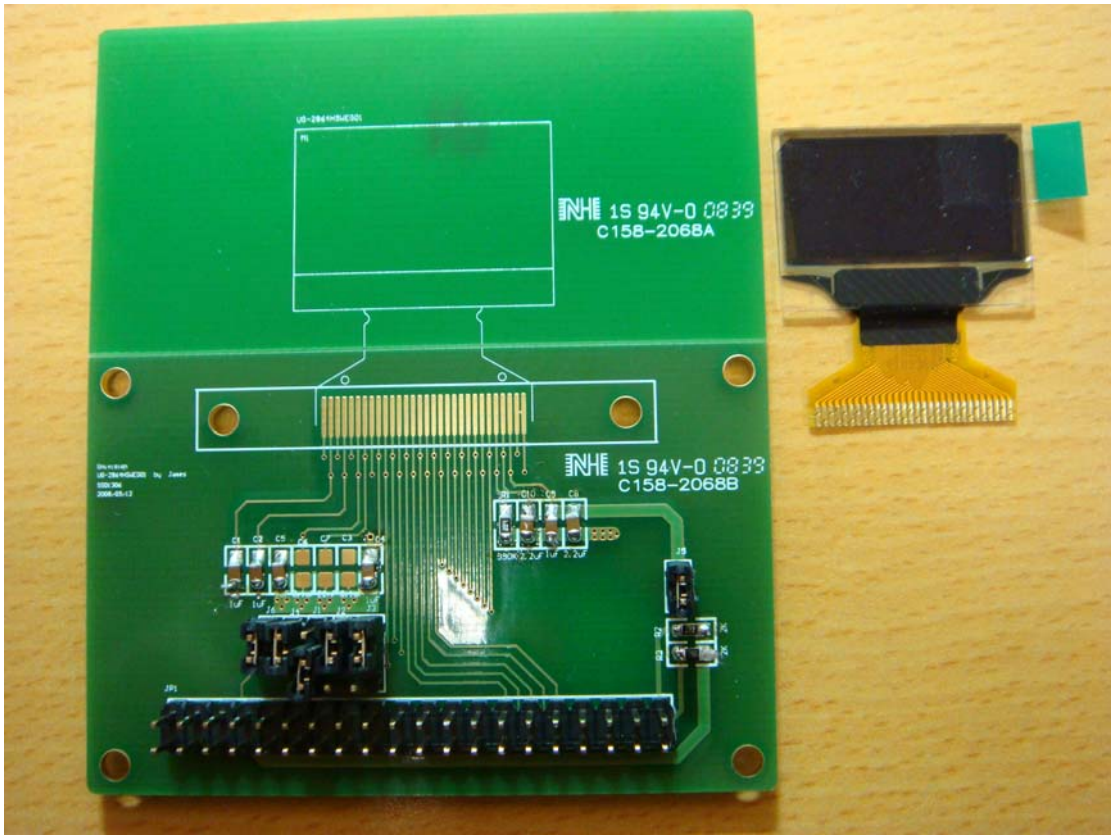


Figure1 EVK PCB and OLED Module

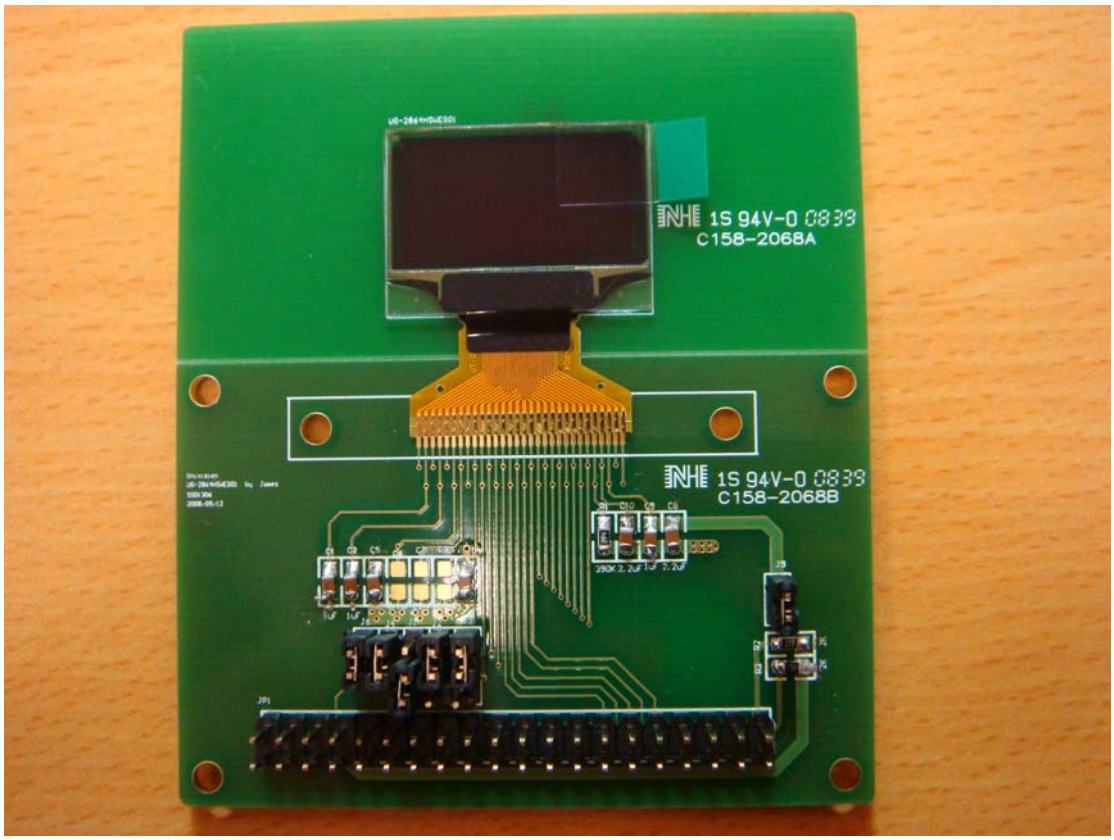


Figure2 The combination of the module and EVK

The SSD1306 is COG type package, that the connect pads are on the bottom of the module connector. When finished assembled the module and EVK, then push the locking pad to lock the module. See the Figure 1 and Figure2.

User can use leading wire to connect EVK with customer's system. The example shows as Figure 3

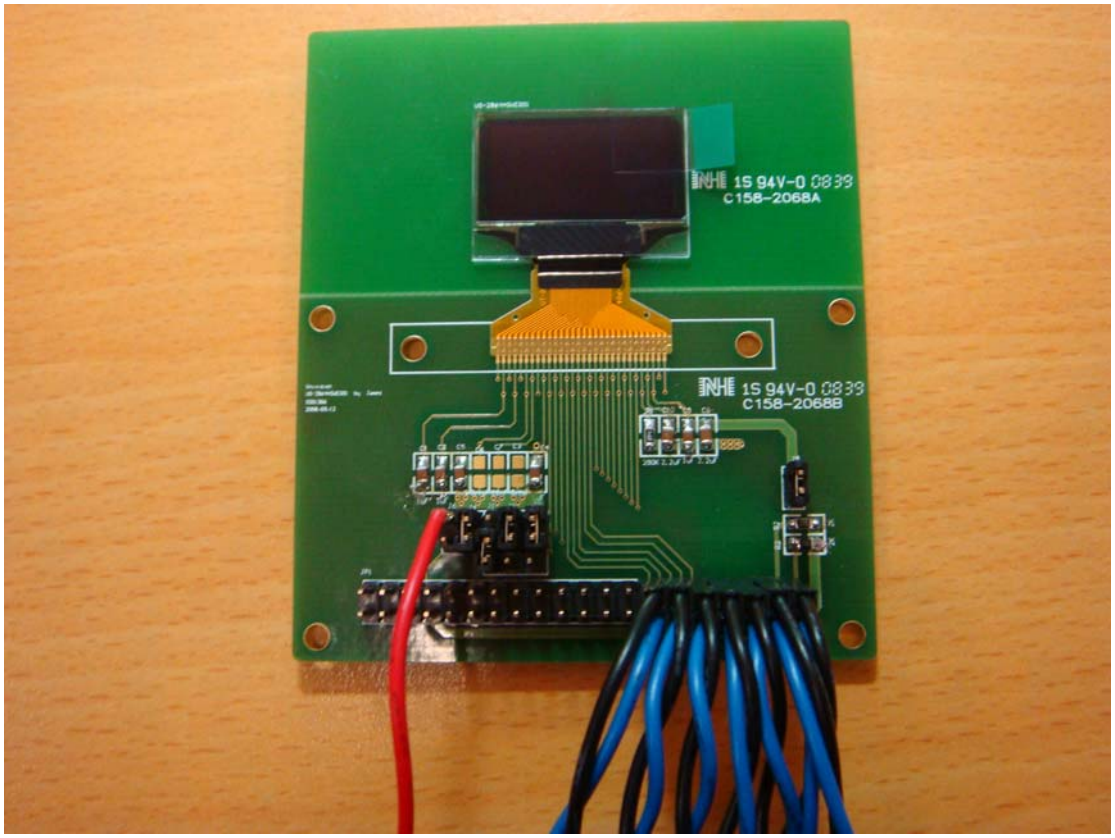


Figure3 EVK with test platform

Note 1：It is the internal most positive voltage supply. In this sample is connected to power supply.

Note 2：Those are leading wire connect to control board. Those are data pin.(D0-D7)

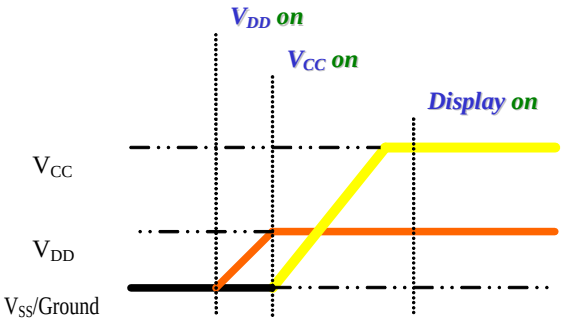
Note 3：Those are leading wire connect to control board. Those are control pin.
(DC, CS, RD, WR, RES)

6. Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

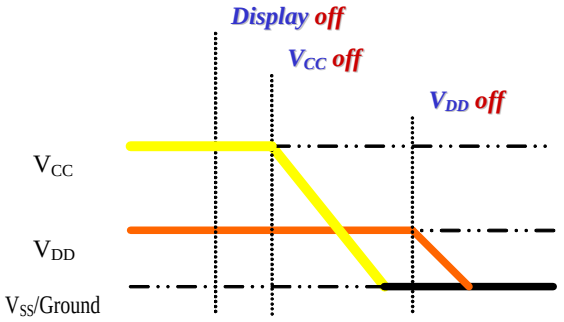
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up Vcc
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



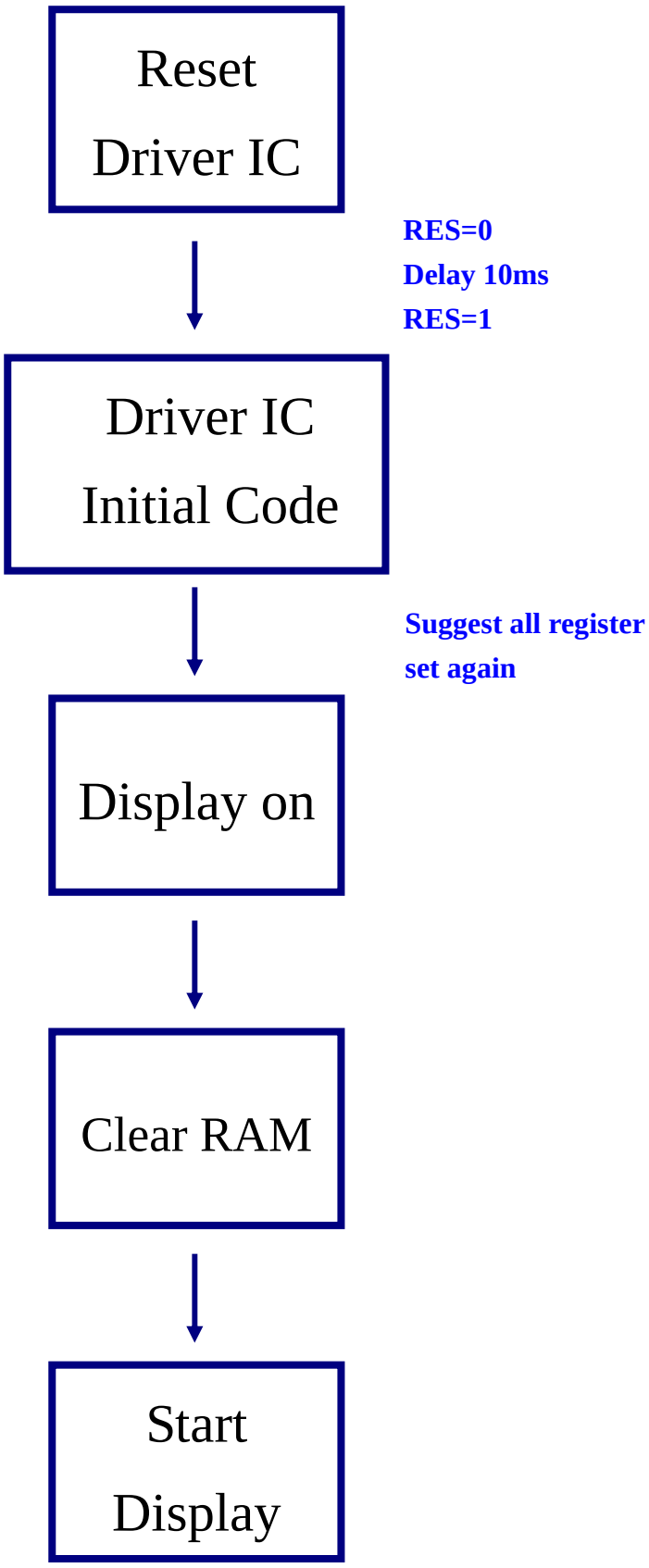
Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{cc} is reach 0 and
   panel is completely
   discharges)
4. Power down V_{DD}



7.How to use SSD1306 module

7.1 Initial Step Flow



RD recommends Initial Code:

Internal setting (Charge pump)

```
{
WRITE_COMMAND(0xae);//--turn off oled panel
WRITE_COMMAND(0x00);//---set low column address
WRITE_COMMAND(0x10);//---set high column address
WRITE_COMMAND(0x40);//--set start line address
WRITE_COMMAND(0x81);//--set contrast control register
WRITE_COMMAND(0xcf);
WRITE_COMMAND(0xa1);//--set segment re-map 95 to 0
WRITE_COMMAND(0xa6);//--set normal display
WRITE_COMMAND(0xa8);//--set multiplex ratio(1 to 64)
WRITE_COMMAND(0x3f);//--1/64 duty
WRITE_COMMAND(0xd3);//-set display offset
WRITE_COMMAND(0x00);//-not offset
WRITE_COMMAND(0xd5);//--set display clock divide ratio/oscillator frequency
WRITE_COMMAND(0x80);//--set divide ratio
WRITE_COMMAND(0xd9);//--set pre-charge period
WRITE_COMMAND(0xf1);
WRITE_COMMAND(0xda);//--set com pins hardware configuration
WRITE_COMMAND(0x12);
WRITE_COMMAND(0xdb);//--set vcomh
WRITE_COMMAND(0x40);
WRITE_COMMAND(0x8d);//--set Charge Pump enable/disable
WRITE_COMMAND(0x14);//--set(0x10) disable
WRITE_COMMAND(0xaf);//--turn on oled panel
}
```

External setting

```
{
WRITE_COMMAND(0xae);//--turn off oled panel
WRITE_COMMAND(0x00);//---set low column address
WRITE_COMMAND(0x10);//---set high column address
WRITE_COMMAND(0x40);//--set start line address
WRITE_COMMAND(0x81);//--set contrast control register
WRITE_COMMAND(0x8f);
WRITE_COMMAND(0xa1);//--set segment re-map 95 to 0
WRITE_COMMAND(0xa6);//--set normal display
WRITE_COMMAND(0xa8);//--set multiplex ratio(1 to 64)
WRITE_COMMAND(0x3f);//--1/64 duty
WRITE_COMMAND(0xd3);//-set display offset
WRITE_COMMAND(0x00);//-not offset
WRITE_COMMAND(0xd5);//--set display clock divide ratio/oscillator frequency
WRITE_COMMAND(0x80);//--set divide ratio
WRITE_COMMAND(0xd9);//--set pre-charge period
WRITE_COMMAND(0x22);
WRITE_COMMAND(0xda);//--set com pins hardware configuration
WRITE_COMMAND(0x12);
WRITE_COMMAND(0xdb);//--set vcomh
WRITE_COMMAND(0x40);
WRITE_COMMAND(0x8d);//--set Charge Pump enable/disable
WRITE_COMMAND(0x10);//--set(0x14) Enable
WRITE_COMMAND(0xaf);//--turn on oled panel
}
```