

Allegro®

PCB and Package Physical Layout

Command Reference Table of Contents

Series XL and GXL

Product Version 16.2
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Allegro PCB and Package Physical Layout Command Reference

Allegro[®] PCB and Package Physical Layout Command Reference

The command reference for the physical layout tools contains information on commands available in the following products:

- Allegro PCB Editor
- Allegro Package Designer (APD)
- Allegro Package SI (AP SI)
- Allegro PCB SI
- SiP Digital Architect/SiP Layout
- SiP RF Layout
- SiP Digital SI

To view all commands beginning with a specific letter, click the appropriate link, below. For example, to view/print information on `envcd`, click [E](#).

[A](#) [B](#) [C](#) [D](#) [E](#) [F](#) [G](#) [H](#) [I](#) [J](#) [K](#) [L](#) [M](#)
[N](#) [O](#) [P](#) [Q](#) [R](#) [S](#) [T](#) [U](#) [V](#) [W](#) [X](#) [Y](#) [Z](#)



Tip

Press the **F1** function key anywhere on your Cadence tool interface to display the Help topic for the command you are running!

For complete console window command-to-menu choice mapping for the products listed above, see [Command Mapping](#).

Allegro PCB and Package Physical Layout Command Reference

Allegro® PCB and Package Physical Layout Command Reference

Command Mapping

This document maps product menu choices to command window commands.

■ Allegro PCB Editor

- ☐ File
- ☐ Edit
- ☐ View
- ☐ Add
- ☐ Display
- ☐ Setup
- ☐ Shape
- ☐ Layout
- ☐ Logic
- ☐ Place
- ☐ Route
- ☐ Analyze
- ☐ Manufacture
- ☐ RF-PCB
- ☐ Tools
- ☐ Help

■ Allegro PCB SI

- ☐ File
- ☐ View
- ☐ Display
- ☐ Setup

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

- ☐ Logic
- ☐ Place
- ☐ Route
- ☐ Analyze
- ☐ Tools
- ☐ Help

■ APD/AP SI

- ☐ File
- ☐ Edit
- ☐ View
- ☐ Add
- ☐ Display
- ☐ Setup
- ☐ Layout
- ☐ Shape
- ☐ Generate
- ☐ Logic
- ☐ Place
- ☐ Route
- ☐ Analyze
- ☐ Manufacture
- ☐ Tools
- ☐ Help

■ SiP Digital Architect/SiP Layout

- ☐ File
- ☐ Edit
- ☐ View

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

- ☐ Add
- ☐ Display
- ☐ Setup
- ☐ Layout
- ☐ Shape
- ☐ Logic
- ☐ Place
- ☐ Route
- ☐ Analyze
- ☐ Manufacture
- ☐ RF-PCB
- ☐ Reports
- ☐ Tools
- ☐ Help

■ SiP RF Layout

- ☐ File
- ☐ Edit
- ☐ View
- ☐ Add
- ☐ Display
- ☐ Setup
- ☐ Layout
- ☐ Shape
- ☐ Logic
- ☐ Place
- ☐ Route
- ☐ Analyze

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

- ☐ Manufacture
- ☐ Reports
- ☐ Tools
- ☐ RF Module
- ☐ Help

■ SiP Digital SI

- ☐ File
- ☐ Edit
- ☐ View
- ☐ Add
- ☐ Display
- ☐ Setup
- ☐ Layout
- ☐ Logic
- ☐ Place
- ☐ Route
- ☐ Analyze
- ☐ Reports
- ☐ Tools
- ☐ Help

Allegro PCB Editor

The following diagram identifies the Allegro PCB Editor user interface toolbar icons, which execute the same console window commands corresponding to product menu choices. Your toolbar configuration may differ. You can also hover your cursor over each icon to display a data tip that identifies its function.

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Figure A-1 Allegro PCB Editor Toolbar Icons



The command mapping in Table A-1 lists the menu choices that can be found in the different modes (Layout and Symbol) of Allegro PCB Editor. If you are running a different product in the Allegro family (for example, PCB Design 220), some commands listed here might not be available.

Table A-1 Allegro PCB Editor Command Mapping

Menu Choice	Console Window Command
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Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

File

File – New	<u>new</u>
File – Open	<u>open</u>
File – Recent Designs	<u>opencd</u>
File – Save	<u>save</u>
File – Save As	<u>save as</u>
File – Create Symbol	<u>create symbol</u> (in Symbol Editor only)
File – Import – Logic	<u>netin param</u>
File – Import – Artwork	<u>load photoplot</u>
File – Import – Stream	<u>load stream</u>
File – Import – IPF	<u>load plot</u>
File – Import – DXF	<u>dxs in</u>
File – Import – IDF	<u>idf in</u>
File – Import – IFF	<u>iff in</u>
File – Import – Router	<u>specctra in</u>
File – Import – PADS	<u>pads in</u>
File – Import – PCAD	<u>pcad in</u>
File – Import – OrCAD Layout	<u>orcad in</u>
File – Import – Sub-Drawing	<u>clppaste</u>
File – Import – Techfile	<u>techfile in</u>
File – Import – Parameters	<u>param in</u>
File – Import – Active Times	<u>signal atimes</u>
File – Import – Placement	<u>plctxt in</u>
File – Import – Annotations	<u>annotation in</u>
File – Import – Pin Delay	<u>pin delay in</u>
File – Export – Logic	<u>feedback</u>

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Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

File – Export – Netlist w/Properties	<u>netout</u>
File – Export – IPF	<u>create plot</u>
File – Export – DXF	<u>dxs out</u>
File – Export – IDF	<u>idf out</u>
File – Export – Router	<u>specctra out</u>
File – Export – Sub-Drawing	<u>clpcopy</u>
File – Export – Libraries	<u>dlib</u>
File – Export – Techfile	<u>techfile out</u>
File – Export – Parameters	<u>param out</u>
File – Export – Placement	<u>plctxt out</u>
File – Export – Annotations	<u>annotation out</u>
File – Export – InterComm	<u>icm out</u>
File – Export – IPC 356	<u>ipc356 out</u>
File – Export – ODB ++ inside	<u>odb out</u>
File – Export – Save Design to 16.01	<u>downrev</u>
File – Export – Pin Delay	<u>pin delay out</u>
File – Viewlog	<u>viewlog</u>
File – File Viewer	No corresponding command
File – Plot Setup	<u>plot setup</u>
File – Plot Preview (Windows only)	<u>plot preview</u>
File – Plot	<u>plot</u>
File – Properties	<u>file property</u>
File – Change Editor	<u>toolswap</u>
File – Script	<u>script</u>
File – Exit	<u>exit</u>
Edit	
Edit – Undo	<u>undo</u>
Edit – Redo	<u>redo</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Edit – Move	<u>move</u>
Edit – Copy	<u>copy</u>
Edit – Mirror	<u>mirror</u>
Edit – Spin	<u>spin</u>
Edit – Change	<u>change</u>
Edit – Delete	<u>delete</u>
Edit – Z-Copy	<u>zcopy shape</u>
Edit – Split Plane – Parameters	<u>split plane param</u>
Edit – Split Plane – Create	<u>split plane create</u>
Edit – Vertex	<u>vertex</u>
Edit – Delete Vertex	<u>delete vertex</u>
Edit – Text	<u>text edit</u>
Edit – Groups	<u>groupedit</u>
Edit – Properties	<u>property edit</u>
Edit – Net Properties	<u>net properties</u>
View	
View – Zoom By Points	<u>zoom points</u>
View – Zoom Fit	<u>zoom fit</u>
View – Zoom In	<u>zoom in</u>
View – Zoom Out	<u>zoom out</u>
View – Zoom World	<u>zoom world</u>
View – Zoom Center	<u>zoom center</u>
View – Zoom Previous	<u>zoom previous</u>
View – Color View Save	<u>colorview create</u>
View – Color View Restore Last	<u>colorview restore</u>
View – Windows – Command	<u>showhide text</u>
View – Windows – World View	<u>showhide view</u>
View – Windows – Options	<u>showhide options</u>

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Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

View – Windows – Find	<u>showhide find</u>
View – Windows – Visibility	<u>showhide vis</u>
View – Windows – Show All	<u>show_allpanes</u>
View – Refresh	<u>redisplay</u>
View – Customization – Toolbar	No corresponding command
View – Reset UI to Cadence Default	<u>reset_dockwindows</u>
Add	
Add – Line	<u>add line</u>
Add – Arc w/Radius	<u>add rarc</u>
Add – 3pt Arc	<u>add arc</u>
Add – Circle	<u>add circle</u>
Add – Rectangle	<u>add rect</u>
Add – Frectangle	<u>add frect</u>
Add – Text	<u>add text</u>
Display	
Display – Color/Visibility	<u>color192</u>
Display – Layer Priority	<u>layer priority</u>
Display – Status	<u>status</u>
Display – Element	<u>show element</u>
Display – Measure	<u>show measure</u>
Display – Constraint	<u>cns show</u>
Display – Parasitic	<u>show parasitic</u>
Display – Property	<u>show property</u>
Display – Segments Over Voids	<u>highlight sov</u>
Display – Assign Color	<u>assign color</u>
Display – Highlight	<u>hilight</u>
Display – Dehighlight	<u>dehilight</u>
Display – Waive DRCs – Waive	<u>waive drc</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Display – Waive DRCs – Show	<u>show waived drcs</u>
Display – Waive DRCs – Blank	<u>blank waived drcs</u>
Display – Waive DRCs – Restore	<u>restore waived drc</u>
Display – Waive DRCs – Restore All	<u>restore waived drcs</u>
Display – Show Rats – All	<u>rats all</u>
Display – Show Rats – All Unbundled Rats	<u>rats unbundled show all</u>
Display – Show Rats – All Bundled Rats	<u>rats bundled show all</u>
Display – Show Rats – Unplanned Rats	<u>rats show unplanned</u>
Display – Show Rats – Components	<u>rats component</u>
Display – Show Rats – Net	<u>rats net</u>
Display – Show Rats – Of Selection	<u>rats show</u>
Display – Show – Bundles – All	<u>bundle show all</u>
Display – Show – Bundles – Selected	<u>bundle show</u>
Display – Show – Router Plan – All	<u>rplan show all</u>
Display – Show – Router Plan – All Bundles	<u>rplan bundled show</u>
Display – Show – Router Plan – All Random Logic	<u>rplan unbundled show all</u>
Display – Show – Router Plan – Of Selection	<u>rplan show</u>
Display – Show – Router Plan – Bundle Plan of Selection	<u>rplan bundled show</u>
Display – Blank Rats – All	<u>unrats all</u>
Display – Blank Rats – All Bundled Rats	<u>rats bundled blank all</u>
Display – Blank Rats – Components	<u>unrats component</u>
Display – Blank Rats – Nets	<u>unrats net</u>
Display – Blank Rats – Of Selection	<u>rats blank</u>
Display – Blank Bundles – All	<u>bundle blank all</u>
Display – Blank Bundles – Selected	<u>bundle blank</u>
Display – Blank Bundles – Unselected	<u>bundle blank unselected</u>
Display – Blank Router Plan – All	<u>rplan blank all</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Display – Blank Router Plan – All Bundles	<u>rplan bundled blank all</u>
Display – Blank Router Plan – All Random Logic	<u>rplan unbundled blank all</u>
Display – Blank Router Plan – Of Selection	<u>rplan blank</u>
Display – Blank Router Plan – Bundle Plan of Selection	<u>rplan bundled blank</u>
Setup	
Setup – Design Parameters	<u>prmed</u>
Setup – Application Mode – General Edit	<u>generaledit</u>
Setup – Application Mode – Place Mode	<u>placementedit</u>
Setup – Application Mode – Etch Edit	<u>etchedit</u>
Setup – Application Mode – Flow Planning	<u>ifp</u>
Setup – Application Mode – None	<u>noappmode</u>
Setup – Grids	<u>define grid</u>
Setup – Cross-section	<u>define lyrstack</u>
Setup – Unused Pads Suppression	<u>unused pads</u>
Setup – Subclasses	<u>define subclass</u>
Setup – Materials	<u>define materials</u>
Setup – Vias – Define B/B Via	<u>define bbvia</u>
Setup – Vias – Auto Define B/B Via	<u>auto define bbvia</u>
Setup – Enable On-Line DRC	<u>cns onlinedrc</u>
Setup – Constraints – Modes	<u>cns cmmodes</u>
Setup – Constraints – Electrical	<u>cmgr electrical</u>
Setup – Constraints – Physical	<u>cmgr physical</u>
Setup – Constraints – Spacing	<u>cmgr spacing</u>
Setup – Constraints – Physical Net Overrides	<u>property edit</u>
Setup – Constraints – Spacing Net Overrides	<u>property edit</u>
Setup – Constraints – DFA Constraint Spreadsheet	<u>dfa spreadsheet</u>
Setup – Constraints – Constraint Manager	<u>cmgr</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Setup – Property Definitions	<u>define property</u>
Setup – Define Lists	<u>define list</u>
Setup – Areas – Package Keepin	<u>keepin package</u>
Setup – Areas – Package Keepout	<u>keepout package</u>
Setup – Areas – Package Height	<u>package height</u>
Setup – Areas – Route Keepin	<u>keepin router</u>
Setup – Areas – Route Keepout	<u>keepout router</u>
Setup – Areas – Wire Keepout	<u>keepout wire</u>
Setup – Areas – Via Keepout	<u>keepout via</u>
Setup – Areas – Shape Keepout	<u>keepout shape</u>
Setup – Areas – Probe Keepout	<u>keepout probe</u>
Setup – Areas – Gloss Keepout	<u>keepout gloss</u>
Setup – Areas – Photoplot Outline	<u>keepin photo</u>
Setup – User Preferences	<u>enved</u>

Layout

Layout menu choices are available only in the Symbol Editor

Layout – Pins	<u>add pin</u>
Layout – Connections	<u>add connect</u>
Layout – Slide	<u>slide</u>
Layout – Labels – RefDes	<u>label refdes</u>
Layout – Labels – Device	<u>label device</u>
Layout – Labels – Value	<u>label value</u>
Layout – Labels – Tolerance	<u>label tolerance</u>
Layout – Labels – Part Number	<u>label part</u>

Shape

Shape – Polygon	<u>shape add</u>
Shape – Rectangular	<u>shape add rect</u>
Shape – Circular	<u>shape add circle</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Shape – Manual Void – Polygon	<u>shape void polygon</u>
Shape – Select Shape or Void	<u>shape select</u>
Shape – Manual Void – Rectangular	<u>shape void rectangle</u>
Shape – Manual Void – Circular	<u>shape void circle</u>
Shape – Manual Void – Delete	<u>shape void delete</u>
Shape – Manual Void – Element	<u>shape void element</u>
Shape – Manual Void – Move	<u>shape void move</u>
Shape – Manual Void – Copy	<u>shape void copy</u>
Shape – Edit Boundary	<u>shape edit boundary</u>
Shape – Delete Islands	<u>island delete</u>
Shape – Change Shape Type	<u>shape change type</u>
Shape – Merge Shapes	<u>shape merge shapes</u>
Shape – Check	<u>shape check</u>
Shape – Compose Shape	<u>compose shape</u>
Shape – Decompose Shape	<u>decompose shape</u>
Shape – Global Dynamic Params	<u>shape global param</u>
Logic	
Logic – Net Logic	<u>net logic</u>
Logic – Net Schedule	<u>net schedule</u>
Logic – Assign Differential Pair	<u>diff pairs</u>
Logic – Identify DC Nets	<u>identify nets</u>
Logic – Assign RefDes	<u>assign refdes</u>
Logic – Auto Rename RefDes – Rename	<u>rename param</u>
Logic – Auto Rename RefDes – Design	<u>rename area design</u>
Logic – Auto Rename RefDes – Room	<u>rename area room</u>
Logic – Auto Rename RefDes – Window	<u>rename area window</u>
Logic – Auto Rename RefDes – List	<u>rename area list</u>
Logic – Change Parts	<u>partedit</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Logic – Part Logic...	<u>partlogic</u>
Logic – Terminator Assignment	<u>ecl_param</u>
Place	
Place – Manually	<u>place manual</u>
Place – Quickplace	<u>quickplace</u>
Place – Router	<u>specctra</u>
Place – Autoplace – Insight	<u>place insight</u>
Place – Autoplace – Parameters	<u>place param</u>
Place – Autoplace – Top Grids	<u>place set topgrid</u>
Place – Autoplace – Bottom Grids	<u>place set bottomgrid</u>
Place – Autoplace – Design	<u>place area design</u>
Place – Autoplace – Room	<u>place area room</u>
Place – Autoplace – Window	<u>place area window</u>
Place – Autoplace – List	<u>place area list</u>
Place – Interactive	<u>place interactive</u>
Place – Swap – Pins	<u>swap pins</u>
Place – Swap – Functions	<u>swap functions</u>
Place – Swap – Components	<u>swap components</u>
Place – Autoswap – Parameters	<u>swap param</u>
Place – Autoswap – Design	<u>swap area design</u>
Place – Autoswap – Room	<u>swap area room</u>
Place – Autoswap – Window	<u>swap area window</u>
Place – Autoswap – List	<u>swap area list</u>
Place – Via Arrays – Via Array	<u>add viaarray</u>
Place – Via Arrays – Boundary Via Array	<u>add bviaarray</u>
Place – Via Arrays – Circular Via Array	<u>add cviaarray</u>
Place – Via Arrays – Cline Via Array	<u>add lviaarray</u>
Place – Via Arrays – Offset Via Array	<u>add oviaarray</u>

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Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Place – Update Symbols	<u>refresh symbol</u>
Place – Replace SQ Temporary – Devices	<u>replace temp device</u>
Place – Replace SQ Temporary – Symbols	<u>replace temp symbols</u>
Place – Design Partition – Create Partitions	<u>partition</u>
Place – Design Partition – Workflow Manager	<u>workflow</u>
Place – Design Partition – Guideports	<u>guideport</u>
Place – Design Partition – Soft Net Assignment	<u>soft net</u>
Route	
Route – Connect	<u>add connect</u>
Route – Slide	<u>slide</u>
Route – Delay Tune	<u>delay tune</u>
Route – Custom Smooth	<u>custom smooth</u>
Route – Create Fanout	<u>create fanout</u>
Route – Copy Fanout	<u>copy fanout</u>
Route – Define Via Structure	<u>define via structure</u>
Route – Convert Fanout – Mark	<u>mark fanout</u>
Route – Convert Fanout – Unmark	<u>unmark fanout</u>
Route – Fanout by Pick	<u>fanout by pick</u>
Route – Route Net(s) by Pick	<u>route by pick</u>
Route – Elongation by Pick	<u>elong by pick</u>
Route – Router Checks	<u>specctra checks</u>
Route – Optimize Rat Ts	<u>optimize ts</u>
Route – Route Automatic	<u>auto route</u>
Route – Custom	<u>custom route</u>
Route – Router Editor	<u>specctra</u>
Route – Miter by Pick	<u>miter by pick</u>
Route – Unmiter by Pick	<u>unmiter by pick</u>
Route – Spread Between Voids	<u>spread between voids</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Route – Line Fattening	<u>line fattening</u>
Route – Gloss – Add Fillet	<u>add fillet</u>
Route – Gloss – Delete Fillet	<u>delete fillet</u>
Route – Gloss – Parameters	<u>gloss param</u>
Route – Gloss – Design	<u>gloss area design</u>
Route – Gloss – Room	<u>gloss area room</u>
Route – Gloss – Window	<u>gloss area window</u>
Route – Gloss – Highlight	<u>gloss area highlight</u>
Route – Gloss – List	<u>gloss area list</u>

Analyze

Analyze – SI/EMI Sim – Initialize	<u>signal init</u>
Analyze – SI/EMI Sim – Library	<u>signal library</u>
Analyze – SI/EMI Sim – Model	<u>signal model</u>
Analyze – SI/EMI Sim – Model Dump/Refresh	<u>signal model refresh</u>
Analyze – SI/EMI Sim – Preferences	<u>signal prefs</u>
Analyze – SI/EMI Sim – Audit – Design Audit	<u>signal audit</u>
Analyze – SI/EMI Sim – Audit – Net Audit	<u>signal audit net</u>
Analyze – SI/EMI Sim – Audit – Audit One Library	<u>signal lib audit</u>
Analyze – SI/EMI Sim – Audit – Audit List of Libraries	<u>signal libs audit</u>
Analyze – SI/EMI Sim – Probe	<u>signal probe</u>
Analyze – SI/EMI Sim – Xtalk Table	<u>signal xtalktable</u>
Analyze – EMI Rule Checker	<u>emcontrol</u>
Analyze – Transmission Line Calculator	<u>tline calculator</u>

Manufacture

Manufacture – Dimension/Draft commands in the Layout Editor are accessed under the Dimension menu item in the Symbol Editor

Manufacture – Dimension/Draft – Parameters	<u>draft param</u>
Manufacture – Dimension/Draft – LineFont	<u>linefont</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Manufacture – Dimension/Draft – Linear Dim	<u>dimension linear</u>
Manufacture – Dimension/Draft – Datum Dim	<u>dimension datum</u>
Manufacture – Dimension/Draft – Angular Dim	<u>dimension angular</u>
Manufacture – Dimension/Draft – Leader Lines	<u>leader only</u>
Manufacture – Dimension/Draft – Diametral Leader	<u>leader diametral</u>
Manufacture – Dimension/Draft – Radial Leader	<u>leader radial</u>
Manufacture – Dimension/Draft – Balloon Leader	<u>leader balloon</u>
Manufacture – Dimension/Draft – Chamfer Leader	<u>leader chamfer</u>
Manufacture – Dimension/Draft – Chamfer	<u>draft chamfer</u>
Manufacture – Dimension/Draft – Fillet	<u>draft fillet</u>
Manufacture – Dimension/Draft – Create Detail	<u>create detail</u>
Manufacture – Artwork	<u>film param</u>
Manufacture – Stream Out	<u>stream out</u>
Manufacture – NC – Drill Customization	<u>ncdrill customization</u>
Manufacture – NC – Drill Legend	<u>ncdrill legend</u>
Manufacture – NC – Backdrill Setup and Analysis	<u>backdrill setup</u>
Manufacture – NC – NC Parameters	<u>ncdrill param</u>
Manufacture – NC – NC Drill	<u>nctape full</u>
Manufacture – NC – NC Route	<u>ncroute</u>
Manufacture – Cut Marks	<u>cut marks</u>
Manufacture – DFX Check (legacy)	<u>dfa</u>
Manufacture – Create Coupons	<u>create coupons</u>
Manufacture – Silkscreen	<u>silkscreen param</u>
Manufacture – Testprep – Automatic	<u>testprep automatic</u>
Manufacture – Testprep – Manual	<u>testprep manual</u>
Manufacture – Testprep – Properties	<u>testprep properties</u>
Manufacture – Testprep – Fix/unfix testpoints	<u>testprep fix</u>
Manufacture – Testprep – Create FIXTURE	<u>testprep createfixture</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

Manufacture – Testprep – Create NC drill data	<u>testprep ncdrill</u>
Manufacture – Testprep – Density Check	<u>testprep density</u>
Manufacture – Testprep – Resequence	<u>testprep resequence</u>
Manufacture – Thieving	<u>thieving</u>
Manufacture – Variants – Create Assembly Drawing	<u>variant assembly</u>
Manufacture – Variants – Create Bill of Materials	<u>variant bom</u>

RF-PCB

RF-PCB – Setup	<u>rf setup</u>
RF-PCB – Repackage	<u>rf repackage</u>
RF-PCB – Load Module	<u>rf load module</u>
RF-PCB – Place	<u>rf add component</u>
RF-PCB – Route – Add Connect	<u>rf route</u>
RF-PCB – Route – Direct Connect	<u>rf direct connect</u>
RF-PCB – Edit – Change	<u>rf change</u>
RF-PCB – Edit – Snap	<u>rf snap</u>
RF-PCB – Edit – Flip	<u>rf flip</u>
RF-PCB – Edit – Push	<u>rf push</u>
RF-PCB – Edit – Delete	<u>rf delete</u>
RF-PCB – Edit – Scaled Copy	<u>rf scaled copy</u>
RF-PCB – Edit – Modify Connectivity	<u>rf modify net</u>
RF-PCB – Edit – Copy	<u>rf group copy</u>
RF-PCB – Edit – VAR Edit	<u>rf varedit</u>
RF-PCB – Flexible Shape Editor – Edge Move	<u>fse edge move</u>
RF-PCB – Flexible Shape Editor – Edge Stretch	<u>fse edge stretch</u>
RF-PCB – Flexible Shape Editor – Edge Spread	<u>fse edge spread</u>
RF-PCB – Flexible Shape Editor – Tangent Segment	<u>fse seg tangent</u>
RF-PCB – Flexible Shape Editor – Arc Tangent	<u>fse arc tangent</u>
RF-PCB – Flexible Shape Editor – Line End Connect	<u>fse end connect</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-1 Allegro PCB Editor Command Mapping

RF-PCB – Flexible Shape Editor – Break and Delete	<u>fse break delete</u>
RF-PCB – Flexible Shape Editor – Vertex Insert	<u>fse vertex insert</u>
RF-PCB – Flexible Shape Editor – Vertex Convert	<u>fse vertex convert</u>
RF-PCB – Flexible Shape Editor – Shape Operations	<u>fse shape logicop</u>
RF-PCB – Flexible Shape Editor – Shape Corner Chamfer	<u>fse shape chamfer</u>
RF-PCB – Flexible Shape Editor – Shape Scale	<u>fse shape scale</u>
RF-PCB – Flexible Shape Editor – Multi-Layer Shape ZCopy	<u>fse shape zcopy</u>
RF-PCB – Flexible Shape Editor – Undo Multi-Layer ZCopy	<u>fse shape unzcopy</u>
RF-PCB – Display – Information	<u>rf display info</u>
RF-PCB – Display – Measurement	<u>rf measure</u>
RF-PCB – Display – New Components	<u>rf display newcomp</u>
RF-PCB – Convert – Tapered Pin Connect	<u>rf tapered connect</u>
RF-PCB – Convert – Chamfer	<u>rf chamfer</u>
RF-PCB – Convert – Shape to Component	<u>rf shape2component</u>
RF-PCB – Convert – Component to Shape	<u>rf component2shape</u>
RF-PCB – Convert – Cline to Tline Conversion	<u>rf cline convert</u>
RF-PCB – IFF Interface – Import	<u>rf iff import</u>
RF-PCB – IFF Interface – Export	<u>rf iff export</u>
RF-PCB – IFF Interface – SMT Library Translator	<u>rf libxlator</u>
Tools	
Tools – Create Module	<u>create module</u>
Tools – Padstack – Modify Design Padstack	<u>padeditdb</u>
Tools – Padstack – Modify Library Padstack	<u>padeditlib</u>
Tools – Padstack – Replace	<u>replace padstack</u>
Tools – Padstack – Group Edit	<u>multpadedit</u>
Tools – Padstack – Refresh	<u>refresh padstack</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

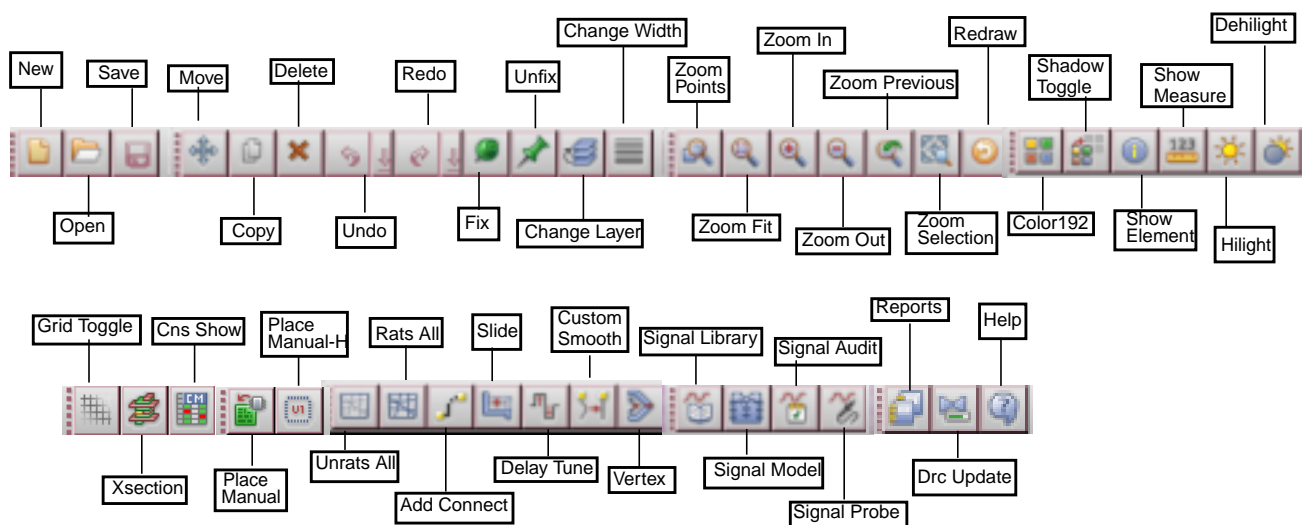
Table A-1 Allegro PCB Editor Command Mapping

Tools – Pad – Boundary	<u>editpad boundary</u>
Tools – Pad – Restore	<u>editpad restore</u>
Tools – Pad – Restore ALL	<u>editpad restore all</u>
Tools – Silkscreen	<u>silkscreen param</u>
Tools – Derive Connectivity	<u>derive connectivity</u>
Tools – Reports	<u>reports</u>
Tools – Technology File Compare	<u>techfile compare</u>
Tools – Setup Advisor	<u>setup advisor</u>
Tools – Database Check	<u>dbdoctor</u>
Tools – Update DRC	<u>drc update</u>
Help	
Help – Documentation	cdsdoc
Help – What's New	No corresponding command
Help – Message Detail	<u>smi message detail</u>
Help – Web Resources – KP&S	Web URL
Help – Web Resources – cdnUsers.org	Web URL
Help – Web Resources – Sourcelink	Web URL
Help – Web resources – Web Collaboration	Web URL
Help – Web Resources – Education Services	Web URL
Help – About	<u>about</u>

Allegro PCB SI

The following diagram identifies the Allegro PCB SI user interface toolbar icons, which execute the same console window commands corresponding to product menu choices. Your toolbar configuration may differ. You can also hover your cursor over each icon to display a datatip that identifies its function.

Figure A-2 Allegro PCB SI Toolbar Icons



The command mapping in Table [A-2](#) lists the menu choices in Allegro SI.

Table A-2 Allegro SI Command Mapping

Menu Choice	ConsoleWindow Command
File	
File – New	<u>n</u> ew
File – Open	<u>o</u> pen
File – Recent Designs	<u>o</u> pen <u>c</u> d
File – Save	<u>s</u> ave
File – Save As	<u>s</u> ave <u>a</u> s

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

File – Create Symbol	<u>create symbol</u> (in Symbol Editor only)
File – Import – Logic	<u>netin param</u>
File – Import – Router	<u>specctra in</u>
File – Import – Techfile	<u>techfile in</u>
File – Import – Active Times	<u>signal atimes</u>
File – Import – Timing	<u>import timing</u>
File – Export – Pin Delay	<u>pin delay in</u>
File – Import – Mentor	<u>import mentor</u>
File – Import – Board	<u>boardoutline import</u>
File – Export – Logic	<u>feedback</u>
File – Export – Netlist w/Properties	<u>netout</u>
File – Export – Pin Delay	<u>pin delay out</u>
File – Export – Router	<u>specctra out</u>
File – Export – Techfile	<u>techfile out</u>
File – Viewlog	<u>viewlog</u>
File – File Viewer	No corresponding command
File – Plot Setup	<u>plot setup</u>
File – Plot Preview	<u>plot preview</u>
File – Plot	<u>plot</u>
File – Properties	<u>file property</u>
File – Change Editor	<u>toolswap</u>
File – Script	<u>script</u>
File – Exit	<u>exit</u>
Edit	
Edit – Move	<u>move</u>
Edit – Copy	<u>copy</u>
Edit – Mirror	<u>mirror</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

Edit – Spin	<u>spin</u>
Edit – Change	<u>change</u>
Edit – Delete	<u>delete</u>
Edit – Vertex	<u>vertex</u>
Edit – Delete Vertex	<u>delete vertex</u>
Edit – Properties	<u>property edit</u>
Edit – Net Properties	<u>net properties</u>
Edit – Undo	<u>undo</u>
Edit – Redo	<u>redo</u>
View	
View – Zoom By Points	<u>zoom points</u>
View – Zoom Fit	<u>zoom fit</u>
View – Zoom In	<u>zoom in</u>
View – Zoom Out	<u>zoom out</u>
View – Zoom World	<u>zoom world</u>
View – Zoom Center	<u>zoom center</u>
View – Zoom Previous	<u>zoom previous</u>
View – Color View Save	<u>colorview create</u>
View – Color View Restore Last	<u>colorview restore</u>
View – Refresh	<u>redisplay</u>
View – Windows – Command	<u>showhide text</u>
View – Windows – World View	<u>showhide view</u>
View – Windows – Options	<u>showhide options</u>
View – Windows – Find	<u>showhide find</u>
View – Windows – Visibility	<u>showhide vis</u>
View – Windows – Show All	<u>show allpanes</u>
View – Customization – Display	<u>display param</u>
View – Customization – CustomizeToolbar	No corresponding command

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

View – Customization – Reset to Default	<u>reset_dockwindows</u>
Display	
Display – Color/Visibility	<u>color192</u>
Display – Color Priority	<u>color_priority</u>
Display – Element	<u>show_element</u>
Display – Measure	<u>show_measure</u>
Display – Property	<u>show_property</u>
Display – Parasitic	<u>show_parasitic</u>
Display – Segments Over Voids	<u>highlight_sov</u>
Display – Ratsnest	<u>ratsnest</u>
Display – Highlight/De-highlight	<u>view_hilite</u>
Display – Highlight By Pick	No corresponding command
Display – Dehighlight By Pick	No corresponding command
Display – Waive DRCs – Waive	<u>waive_drc</u>
Display – Waive DRCs – Show	<u>show_waived_drcs</u>
Display – Waive DRCs – Blank	<u>blank_waived_drcs</u>
Display – Waive DRCs – Restore	<u>restore_waived_drc</u>
Waive DRCs – Restore All	<u>restore_waived_drcs</u>
Display – Ratsnest	<u>ratsnest</u>
Display – Blank Rats All	<u>unrats_all</u>
Display – Show Rats All	<u>rats_all</u>
Setup	
Setup – Design Parameters	<u>prmed</u>
Setup – Cross-section	<u>define_lyrstack</u>
Setup – Materials	<u>define_materials</u>
Setup – Application Mode – General Edit	<u>generaledit</u>
Setup – Application Mode – Etch Edit	<u>etchedit</u>
Setup – Constraints – Modes	<u>cns_cmodes</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

Setup – Constraints – Electrical	<u>cmgr electrical</u>
Setup – Constraints – Physical	<u>cmgr physical</u>
Setup – Constraints – Spacing	<u>cmgr spacing</u>
Setup – Constraints – Physical Net Overrides	<u>property edit</u>
Setup – Constraints – Spacing Net Overrides	<u>property edit</u>
Setup – Constraints – Constraint Manager	<u>cmgr</u>
Setup – Property Definitions	<u>define property</u>
Setup – Define Lists	<u>define list</u>
Setup – Outlines – Room Outline	<u>room outline</u>
Setup – Outlines – Board Outline	<u>board outline</u>
Setup – Outlines – Keepout	<u>board keepout</u>
Setup – Outlines – Plane Outline	<u>board plane</u>
Setup – Notes	<u>edit note</u>
Setup – User Preferences	<u>enved</u>
Logic	
Logic – Parts List	<u>edit parts</u>
Logic – Edit Nets	<u>edit nets</u>
Logic – Net Schedule	<u>net schedule</u>
Logic – Assign Differential Pair	<u>diff pairs</u>
Logic – Identify DC Nets	<u>identify nets</u>
Logic – Create List of Nets	<u>create nets</u>
Logic – Identify Buses	<u>identify buses</u>
Logic – Room Assignment	<u>component assign</u>
Logic – Pin Type	<u>topology pinuse</u>
Logic – Define Terminators	<u>termination edit</u>
Logic – Package Terminators	<u>termination package</u>
Place	
Place – Manually	<u>place manual</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

Place – Quickplace	<u>quickplace</u>
Place – Fix Component Location	<u>component fix</u>
Place – Swap – Pins	<u>swap pins</u>
Place – Swap – Functions	<u>swap functions</u>
Place – Swap – Components	<u>swap components</u>
Route	
Route – Connect	<u>add connect</u>
Route – Slide	<u>slide</u>
Route – Delay Tune	<u>delay tune</u>
Route – Custom Smooth	<u>custom smooth</u>
Route – Fanout by Pick	<u>fanout by pick</u>
Route – Route Net(s) by Pick	<u>route by pick</u>
Route – Elongation by Pick	<u>elong by pick</u>
Route – Router Checks	<u>specctra checks</u>
Route – Optimize Rat Ts	<u>optimize ts</u>
Route – Custom	<u>custom route</u>
Route – Route Automatic	<u>auto route</u>
Route – Editor	<u>specctra</u>
Route – Miter by Pick	<u>miter by pick</u>
Route – Unmiter by Pick	<u>unmiter by pick</u>
Route – Spread Between Voids	<u>spread between voids</u>
Route – Gloss – Add Fillet	<u>add fillet</u>
Route – Gloss – Delete Fillet	<u>delete fillet</u>
Route – Gloss – Execute	<u>gloss param</u>
Route – Gloss – Design	<u>gloss area design</u>
Route – Gloss – Room	<u>gloss area room</u>
Route – Gloss – Window	<u>gloss area window</u>
Route – Gloss – Highlight	<u>gloss area highlight</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

Route – Gloss – List	<u>gloss area list</u>
Route – Define Net Priority	<u>route priority</u>
Analyze	
Analyze – SI/EMI Sim – Initialize	<u>signal init</u>
Analyze – SI/EMI Sim – Library	<u>signal library</u>
Analyze – SI/EMI Sim – Model	<u>signal model</u>
Analyze – SI/EMI Sim – Model Dump/Refresh	<u>signal model refresh</u>
Analyze – SI/EMI Sim – Preferences	<u>signal prefs</u>
Analyze – SI/EMI Sim – Audit – Design Audit	<u>signal audit</u>
Analyze – SI/EMI Sim – Audit – Net Audit	<u>signal audit net</u>
Analyze – SI/EMI Sim – Audit – Audit One Library	<u>signal lib audit</u>
Analyze – SI/EMI Sim – Audit – Audit List of Libraries	<u>signal libs audit</u>
Analyze – SI/EMI Sim – Probe	<u>signal probe</u>
Analyze – SI/EMI Sim – Xtalk Table	<u>signal xtalktable</u>
Analyze – SI/EMI Sim – Bus Setup	<u>signal bus setup</u>
Analyze – SI/EMI Sim – Bus Simulate	<u>signal bus sim</u>
Analyze – SI/EMI Sim – IR-Drop	<u>irdrop</u>
Analyze – EMI Rule Checker	<u>emcontrol</u>
Analyze – Transmission Line Calculator	<u>tline calculator</u>
Tools	
Tools – Reports	<u>reports</u>
Tools – Quick Reports	No associated command
Tools – Topology Editor	<u>sigxp</u>
Tools – Model Integrity	<u>model integrity</u>
Tools – Setup Advisor	<u>setup advisor</u>
Tools – Database Check	<u>dbdoctor</u>
Tools – Update DRC	<u>drc update</u>
Help	

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-2 Allegro SI Command Mapping

Help – Documentation	CDNSHelp
Help – Web Resources – KP&S	Web URL
Help – Web Resources – cdnUsers.org	Web URL
Help – Web Resources – Sourcelink	Web URL
Help – Web resources – Web Collaboration	Web URL
Help – Web Resources – Education Services	Web URL
Help – Web Resources – Design Communities	Web URL
Help – About	<u>about</u>

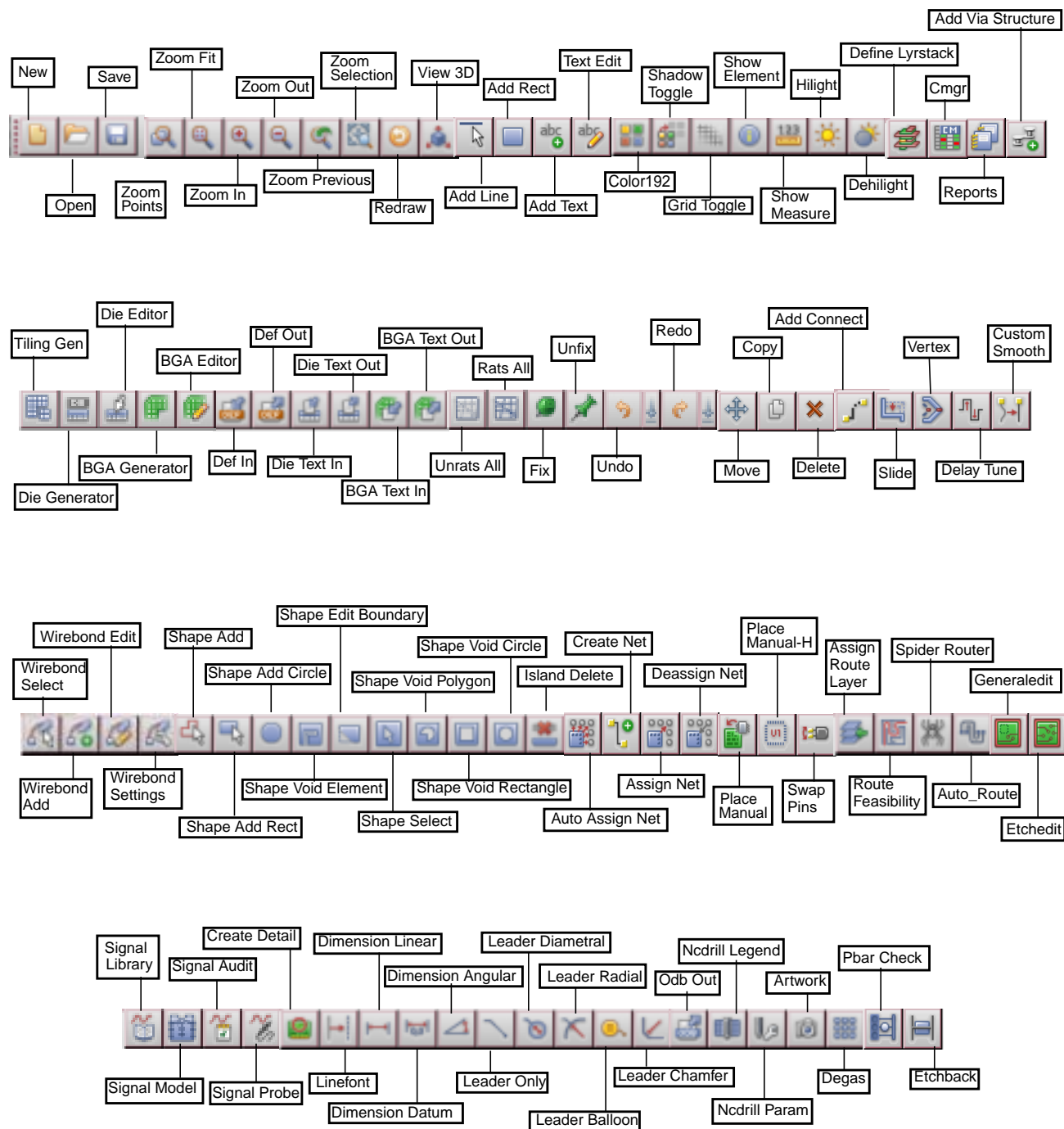
APD/AP SI

The following diagram identifies the APD/AP SI user interface toolbar icons, which execute the same console window commands corresponding to product menu choices. Your toolbar configuration may differ. You can also hover your cursor over each icon to display a datatip that identifies its function.

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Figure A-3 APD/AP SI Toolbar Icons



Allegro PCB and Package Physical Layout Command Reference

Command Mapping

The command mapping in Table A-3 lists the menu choices in the different modes (Layout and Symbol) of Allegro Package Designer (APD L and XL) and Allegro Package (AP SI L). Note that some commands may not be available in both products.

Table A-3 APD/AP SI Command Mapping

Menu Choice	Console Window Command
File	
File – New	<u>new</u>
File – Open	<u>open</u>
File – Save	<u>save</u>
File – Save As	<u>save as</u>
File – Create Symbol	<u>create symbol</u> (in Symbol Editor only)
File – Create Device	<u>create Device</u> (in Symbol Editor only)
File – Import – Netlist-In Wizard (APD XL and APSI)	<u>net list in</u>
File – Import – Logic	<u>netin param</u>
File – Import – NA2 (APD L and XL)	<u>na2 import</u>
File – Import – Artwork (APD L and XL)	<u>load photoplot</u>
File – Import – Stream (APD L and XL)	<u>load stream</u>
File – Import – IPF (APD L and XL)	<u>load plot</u>
File – Import – DXF	<u>dx f in</u>
File – Import – AIF	<u>aif in</u>
File – Import – IDF (APD L and XL)	<u>idf in</u>
File – Import – IFF (APD L and XL)	<u>iff in</u>
File – Import – Router	<u>specctr a in</u>
File – Import – Sub-Drawing (APD L and XL)	<u>clppaste</u>
File – Import – Techfile	<u>techfile in</u>
File – Import – Parameters	<u>param in</u>
File – Import – Active Times	<u>signal atimes</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

File – Import – Placement (APD L and XL)	<u>plctxt in</u>
File – Import – Paste Resistor (APD L and XL)	<u>film res</u>
File – Import – Annotations (APD L and XL)	<u>annotation in</u>
File – Import – Pin Delay	<u>pin delay in</u>
File – Export – BGA Text-Out Wizard	<u>bga text out</u>
File – Export – Die Text-Out Wizard	<u>die text out</u>
File – Export – DEF (Die Pins Only) APD XL only	<u>def out</u>
File – Export – OpenAccess (Die Pins Only) UNIX platforms only	<u>oa out</u>
File – Export – Update Co-Design Die Definition (APD XL only)	<u>update codesign die</u>
File – Export – Logic	<u>feedback</u>
File – Export – Netlist w/Properties	<u>netout</u>
File – Export – IPF (APD L and XL)	<u>create plot</u>
File – Export – DXF (APD L and XL)	<u>dxf out</u>
File – Export – IDF (APD L and XL)	<u>idf out</u>
File – Export – AIF	<u>aif out</u>
File – Export – Router	<u>specctra out</u>
File – Export – Sub-Drawing (APD L and XL)	<u>clpcopy</u>
File – Export – Libraries	<u>dlib</u>
File – Export – Techfile	<u>techfile out</u>
File – Export – Parameters	<u>param out</u>
File – Export – Placement (APD only)	<u>plctxt out</u>
File – Export – Board Level Component (APD L and XL)	<u>allegro component</u>
File – Export – Symbol Spreadsheet (APD L and XL)	<u>symbol to spreadsheet</u>
File – Export – Annotations (APD L and XL)	<u>annotation out</u>
File – Export – InterComm (APD L and XL)	<u>icm out</u>
File – Export – IPC 356 (APD L and XL)	<u>ipc356 out</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

File – Export – ODB ++ inside (APD L and XL)	<u>odb_out</u>
File – Export – Save Design to 16.1	<u>downrev</u>
File – Export – Pin Delay	<u>pin_delay_out</u>
File – Viewlog	<u>viewlog</u>
File – File Viewer	No corresponding command
File – Plot Setup	<u>plot_setup</u>
File – Plot	<u>plot</u>
File – Properties	<u>file_property</u>
File – Change Editor	<u>toolswap</u>
File – Script	<u>script</u>
File – Recent Designs	<u>opencd</u>
File – Exit	<u>exit</u>
Edit	
Edit – Undo	<u>undo</u>
Edit – Redo	<u>redo</u>
Edit – Move	<u>move</u>
Edit – Copy	<u>copy</u>
Edit – Mirror	<u>mirror</u>
Edit – Spin	<u>spin</u>
Edit – Change	<u>change</u>
Edit – Delete	<u>delete</u>
Edit – Z-Copy	<u>zcopy_shape</u>
Edit – Split Plane – Parameters (APD L and XL)	<u>split_plane_param</u>
Edit – Split Plane – Create (APD L and XL)	<u>split_plane_create</u>
Edit – Vertex	<u>vertex</u>
Edit – Delete Vertex	<u>delete_vertex</u>
Edit – Cline Change Width	<u>cline_change_width</u>
Edit – Text	<u>text_edit</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Edit – Groups	<u>grouppedit</u>
Edit – Properties	<u>property edit</u>
Edit – Net Properties	<u>net properties</u>
Edit – Die Properties	<u>die properties</u>
Edit – LEF Pin Parameters (APD XL only)	<u>lef pin param</u>
Edit – Die (APD XL only)	<u>die editor</u>
Edit – BGA	<u>bga editor</u>
View	
View – Zoom By Points	<u>zoom points</u>
View – Zoom Fit	<u>zoom fit</u>
View – Zoom In	<u>zoom in</u>
View – Zoom Out	<u>zoom out</u>
View – Zoom World	<u>zoom world</u>
View – Zoom Center	<u>zoom center</u>
View – Zoom Previous	<u>zoom previous</u>
View – Color View Save	<u>colorview create</u>
View – Color View Restore Last	<u>colorview restore</u>
View – 3D Model	<u>view 3d</u>
View – Redraw	<u>redisplay</u>
View – Windows – Command	No corresponding command
View – Windows – World View	No corresponding command
View – Windows – Options	No corresponding command
View – Windows – Find	No corresponding command
View – Windows – Visibility	No corresponding command
View – Windows – Show All	No corresponding command
View – Customize Toolbar	No corresponding command
View – Reset UI to Cadence Default	<u>reset docwindows</u>

Add

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Add – Line	<u>add line</u>
Add – Arc w/Radius	<u>add rarc</u>
Add – 3pt Arc	<u>add arc</u>
Add – Circle	<u>add circle</u>
Add – Rectangle	<u>add rect</u>
Add – Frectangle	<u>add frect</u>
Add – Text	<u>add text</u>
Add – Co-Design Die (APD XL only)	<u>add codesign die</u>
Add – Standard Die – DEF (Die Pins Only) (APD XL only)	<u>def in</u>
Add – Standard Die – Die Text-In Wizard	<u>die text in</u>
Add – Standard Die – Die Generator	<u>die generator</u>
Add – Standard Die – D.I.E Format	<u>die in</u>
Add – Standard Die – Tiled Die Generator (APD XL only)	<u>tiling gen</u>
Add – BGA – Text-In Wizard	<u>bga text in</u>
Add – BGA – BGA Generator	<u>bga generator</u>
Display	
Display – Color/Visibility	<u>color</u>
Display – Layer Priority	<u>layer priority</u>
Display – Status	<u>status</u>
Display – Element	<u>show element</u>
Display – Measure	<u>show measure</u>
Display – Constraint	<u>cns show</u>
Display – Parasitic	<u>show parasitic</u>
Display – Segments Over Voids (APD XL and AP SI)	<u>highlight sov</u>
Display – Property	<u>show property</u>
Display – Assign Color	<u>assign color</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Display – Highlight	<u>highlight</u>
Display – Dehighlight	<u>dehighlight</u>
Display – Waive DRCs – Waive	<u>waive drc</u>
Display – Waive DRCs – Show	<u>show waived drcs</u>
Display – Waive DRCs – Blank	<u>blank waived drcs</u>
Display – Waive DRCs – Restore	<u>restore waived drc</u>
Display – Waive DRCs – Restore All	<u>restore waived drcs</u>
Display – Pin Highlight	<u>pin highlight</u>
Display – Bond Finger Highlight	<u>bond finger hilite</u>
Display – Bond Finger Dehighlight	<u>bond finger dehilite</u>
Display – Rat Lines by Layer	<u>rats layer</u>
Display – Show Rat Lines – All	<u>rats all</u>
Display – Show Rat Lines – Components	<u>rats component</u>
Display – Show Rat Lines – Net	<u>rats net</u>
Display – Show Rat Lines – Of Selection	<u>rats show</u>
Display – Blank Rats – All	<u>unrats all</u>
Display – Blank Rats – Components	<u>unrats component</u>
Display – Blank Rats – Nets	<u>unrats net</u>
Setup	
Setup – Design Parameters	<u>prmed</u>
Setup – Grids	<u>define grid</u>
Setup – Subclasses (APD L and XL)	<u>define subclass</u>
Setup – Cross-section	<u>define lyrstack</u>
Setup – Unused Pads Suppresion	<u>unused pads</u>
Setup – Materials	<u>define materials</u>
Setup – Application Modes – General Edit	<u>generaledit</u>
Setup – Application Modes – Etch Edit	<u>etchedit</u>
Setup – Application Modes – Place Mode	<u>placementedit</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Setup – Application Modes – None	<u>noappmode</u>
Setup – Blind/Buried Via Definitions – Define B/B Via (APD L and XL)	<u>define bbvia</u>
Setup – Blind/Buried Via Definitions – Auto Define B/B Via (APD L and XL)	<u>auto define bbvia</u>
Setup – Enable On-Line DRC	<u>cns onlinedrc</u>
Setup – Constraints – Modes	<u>cns cmmodes</u>
Setup – Constraints – Electrical	<u>cmgr elec</u>
Setup – Constraints – Physical	<u>cmgr phys</u>
Setup – Constraints – Spacing	<u>cmgr spac</u>
Setup – Constraints – Same Net Spacing	<u>cmgr snspac</u>
Setup – Constraints – Physical Net Overrides	<u>property edit</u>
Setup – Constraints – Spacing Net Overrides	<u>property edit</u>
Setup – Constraints – DFA Constraint Spreadsheet	<u>dfa spreadsheet</u>
Setup – Constraints – Constraint Manager	<u>cmgr</u>
Setup – Property Definitions	<u>define property</u>
Setup – Define Lists	<u>define list</u>
Setup – LEF Libraries (APD L and XL)	<u>lef lib</u>
Setup – Areas – Component Keepin (APD L and XL)	<u>keepin component</u>
Setup – Areas – Component Keepout (APD L and XL)	<u>keepout component</u>
Setup – Areas – Component Height (APD L and XL)	<u>component height</u>
Setup – Areas – Route Keepin	<u>keepout router</u>
Setup – Areas – Route Keepout	<u>keepout router</u>
Setup – Areas – Wire Keepout (APD L and XL)	<u>keepout wire</u>
Setup – Areas – Via Keepout	<u>keepout via</u>
Setup – Areas – Shape Keepout	<u>keepout shape</u>
Setup – Areas – Probe Keepout (APD L and XL)	<u>keepout probe</u>
Setup – Areas – Gloss Keepout (APD L and XL)	<u>keepout gloss</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Setup – Areas – Photoplot Outline (APD L and XL)	<u>keepin photo</u>
Setup – User Preferences	<u>enved</u>
Layout	This menu is available only in the Symbol (Part) Editor
Layout – Pins	<u>add pin</u>
Layout – Pin RenNumbering	<u>rpn</u>
Layout – Connections	<u>add connect</u>
Layout – Slide	<u>slide</u>
Layout – Labels – RefDes	<u>label refdes</u>
Layout – Labels – Device	<u>label device</u>
Layout – Labels – Value	<u>label value</u>
Layout – Labels – Tolerance	<u>label tolerance</u>
Layout – Labels – Part Number	<u>label part</u>
Shape	
Shape – Polygon	<u>shape add</u>
Shape – Rectangular	<u>shape add rect</u>
Shape – Circular	<u>shape add circle</u>
Shape – Select Shape or Void	<u>shape select</u>
Shape – Manual Void – Polygon	<u>shape void polygon</u>
Shape – Manual Void – Rectangular	<u>shape void rectangle</u>
Shape – Manual Void – Circular	<u>shape void circle</u>
Shape – Manual Void – Delete	<u>shape void delete</u>
Shape – Manual Void – Element	<u>shape void element</u>
Shape – Manual Void – Move	<u>shape void move</u>
Shape – Manual Void – Copy	<u>shape void copy</u>
Shape – Edit Boundary	<u>shape edit boundary</u>
Shape – Delete Islands	<u>island delete</u>
Shape – Change Shape Type	<u>shape change type</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Shape – Merge Shapes	<u>shape merge shapes</u>
Shape – Check	<u>shape check</u>
Shape – Compose Shape (APD L and XL)	<u>compose shape</u>
Shape – Decompose Shape (APD L and XL)	<u>decompose shape</u>
Shape – Global Dynamic Params	<u>shape global param</u>
Generate	This menu is available only in APD L and APSI.
Generate – Die Generator	<u>die generator</u>
Generate – Die Text-In Wizard	<u>die text in</u>
Generate – BGA Generator	<u>bga generator</u>
Generate – BGA Text-In Wizard	<u>bga text in</u>
Generate – Offset Via Generator	<u>offset via gen</u>
Generate – Netlist-In Wizard	<u>net list in</u>
Generate – Power/Ground Ring Generator	<u>pring wizard</u>
Logic	
Logic – Auto Create Net	<u>auto create net</u>
Logic – Create Net	<u>create net</u>
Logic – Auto Assign Net	<u>auto assign net</u>
Logic – Assign Multiple Nets (APD XL only)	<u>assign multi nets</u>
Logic – Assign Net	<u>assign net</u>
Logic – Deassign Net (APD L and XL)	<u>deassign net</u>
Logic – Derive Assignment	<u>derive assignment</u>
Logic – Auto Assign Pin Use	<u>auto assign pinuse</u>
Logic – Purge Unused Nets	<u>purge unused nets</u>
Logic – Purge Unplaced Components	<u>purge unplaced comps</u>
Logic – Identify DC Nets	<u>identify nets</u>
Logic – Identify Buses (AP SI only)	<u>identify buses</u>
Logic – Net Logic	<u>net logic</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Logic – Net Schedule	<u>net schedule</u>
Logic – Assign Differential Pair	<u>diff pairs</u>
Logic – Assign RefDes (APD only)	<u>assign refdes</u>
Logic – Auto Rename RefDes – Rename (APD L and XL)	<u>rename param</u>
Logic – Auto Rename RefDes – Design (APD L and XL)	<u>rename area design</u>
Logic – Auto Rename RefDes – Room (APD L and XL)	<u>rename area room</u>
Logic – Auto Rename RefDes – Window (APD L and XL)	<u>rename area window</u>
Logic – Auto Rename RefDes – List (APD L and XL)	<u>rename area list</u>
Logic – Edit Parts List	<u>edit parts</u>
Logic – Pin Type (AP SI only)	<u>topology pinuse</u>
Logic – Terminator Assignment (APD L and XL)	<u>ec1 param</u>
Logic – Define Terminators (AP SI only)	<u>termination edit</u>
Logic – Package Terminators (AP SI only)	<u>termination package</u>
Place	
Place – Manually	<u>place manual</u>
Place – Autoplace – Insight (APD L and XL)	<u>place insight</u>
Place – Autoplace – Parameters (APD L and XL)	<u>place param</u>
Place – Autoplace – Top Grids (APD L and XL)	<u>place set topgrid</u>
Place – Autoplace – Bottom Grids (APD L and XL)	<u>place set bottomgrid</u>
Place – Autoplace – Design (APD L and XL)	<u>place area design</u>
Place – Autoplace – Room (APD L and XL)	<u>place area room</u>
Place – Autoplace – Window (APD L and XL)	<u>place area window</u>
Place – Autoplace – List (APD L and XL)	<u>place area list</u>
Place – Interactive (APD L and XL)	<u>place interactive</u>
Place – Quickplace (AP SI only)	<u>quickplace</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Place – Swap – Pins	<u>swap pins</u>
Place – Swap – Functions (APD L and XL)	<u>swap functions</u>
Place – Swap – Components (APD L and XL)	<u>swap components</u>
Place – Autoswap – Parameters (APD L and XL)	<u>swap param</u>
Place – Autoswap – Design (APD L and XL)	<u>swap area design</u>
Place – Autoswap – Room (APD L and XL)	<u>swap area room</u>
Place – Autoswap – Window (APD L and XL)	<u>swap area window</u>
Place – Autoswap – List (APD L and XL)	<u>swap area list</u>
Place – Update Symbols (APD L and XL)	<u>refresh symbol</u>
Place – Replace SI Temporary – Devices (APD L and XL)	<u>replace temp devices</u>
Place – Replace SI Temporary – Symbols (APD L and XL)	<u>replace temp symbols</u>
Place – Design Partition – Create Partitions (option)	<u>partition</u>
Place – Design Partition – Workflow Manager (option)	<u>workflow</u>
Place – Design Partition – Guideports (option)	<u>guideport</u>
Place – Design Partition – Soft Net Assignment (option)	<u>soft net</u>
Route	
Route – Connect	<u>add connect</u>
Route – Slide	<u>slide</u>
Route – Power/Ground Generator	<u>pring wizard</u>
Route – Wire Bond – Select	<u>wirebond select</u>
Route – Wire Bond – Add	<u>wirebond add</u>
Route – Wire Bond – Edit	<u>wirebond edit</u>
Route – Wire Bond – Modify	<u>wirebond modify</u>
Route – Wire Bond – Add/Edit Guide Paths	<u>wirebond manage guide paths</u>
Route – Wire Bond – Settings	<u>wirebond settings</u>
Route – Wire Bond – Purge Unused Groups	<u>wirebond purge groups</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Route – Wire Bond – Tack Point Move (APD L and XL)	<u>wirebond tack point</u>
Route – Wire Bond – Import (APD L and XL)	<u>wirebond import</u>
Route – Wire Bond – Export (APD L and XL)	<u>wirebond export</u>
Route – Wire Bond – Uprev	<u>wirebond uprev</u>
Route – Via Structure – Add	<u>add via structure</u>
Route – Via Structure – Replace	<u>replace via structure</u>
Route – Via Structure – Refresh	<u>refresh via structure</u>
Route – Offset Via Generator	<u>offset via gen</u>
Route – Flip-Chip Routing Estimation Layer (APD L and XL)	<u>layer estimation</u>
Route – Flip-Chip Die Escape Generator (APD L and XL)	<u>die escape gen</u>
Route – Wire Bond Via Estimation (APD L and XL)	<u>wire bond via estimation</u>
Route – Wire Bond Die Escape Generator (APD L and XL)	<u>wire bond escape</u>
Route – Routing Layer Assign	<u>assign route layer</u>
Route – Plating Layer Assign (APD L and XL)	<u>assign plating layer</u>
Route – Route Feasibility (APD XL only)	<u>route feasibility</u>
Route – Spider Router	<u>spider router</u>
Route – Custom Smooth	<u>custom smooth</u>
Route – Delay Tune	<u>delay tune</u>
Route – Define Short (APD L and XL)	<u>define shorting scheme</u>
Route – Create Short (APD L and XL)	<u>create short</u>
Route – ZRouter (APD L and XL)	<u>zrouter</u>
Route – Router – Route Radial	<u>radial router</u>
Route – Router – Fanout by Pick	<u>fanout by pick</u>
Route – Router – Route by Pick	<u>route by pick</u>
Route – Router – Elongation by Pick	<u>elong by pick</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Route – Router – Route Automatic	<u>auto route</u>
Route – Router – Router Checks	<u>specctr checks</u>
Route – Router – Interactive Editor	<u>specctr</u>
Route – Router – Miter by Pick	<u>miter by ppick</u>
Route – Router – Unmiter by Pick	<u>unmiter by pick</u>
Route – Router – Spread Clines	<u>spread clines</u>
Route – Router – Line Fattening	<u>line fattening</u>
Route – Add Fillet (APD L and XL)	<u>add fillet</u>
Route – Delete Fillet (APD L and XL)	<u>delete fillet</u>
Route – Gloss – Parameters (APD L and XL)	<u>gloss param</u>
Route – Gloss – Design (APD L and XL)	<u>gloss area design</u>
Route – Gloss – Room (APD L and XL)	<u>gloss area room</u>
Route – Gloss – Window (APD L and XL)	<u>gloss area window</u>
Route – Gloss – Highlight (APD L and XL)	<u>gloss area highlight</u>
Route – Gloss – List (APD L and XL)	<u>gloss area list</u>
Analyze	
Analyze – Initialize	<u>signal init</u>
Analyze – Library	<u>signal library</u>
Analyze – Model Assignment	<u>signal model</u>
Analyze – Model Dump/Refresh	<u>signal model refresh</u>
Analyze – Preferences	<u>signal prefs</u>
Analyze – Audit – Design Audit	<u>signal audit</u>
Analyze – Audit – Net Audit	<u>signal audit net</u>
Analyze – Audit – Audit One Library	<u>signal lib audit</u>
Analyze – Audit – Audit List of Libraries	<u>signal libs audit</u>
Analyze – Probe	<u>signal probe</u>
Analyze – Xtalk Table	<u>signal xtalktable</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Analyze – 3-D Package Model (In legacy products only)	<u>signal pkg model</u>
Analyze – 3-D Modeling (AP SI only)	<u>signal 3dmodel</u>
Analyze – Bus Setup (AP SI only)	<u>signal bus setup</u>
Analyze – Bus Simulate (AP SI only)	<u>signal bus sim</u>
Analyze – EMI Rule Checker	<u>emcontrol</u>
Manufacture	This menu is available in APD L and APD XL
Manufacture – Create Plating Bar	<u>pbar create</u>
Manufacture – Delete Plating Bar	<u>pbar delete</u>
Manufacture – Plating Bar Check	<u>pbar check</u>
Manufacture – Etch-back	<u>etchback</u>
Manufacture – Dimension/Draft commands in the Layout Editor are accessed under the Dimension menu item in the Symbol Editor	
Manufacture – Dimension/Draft – Parameters	<u>draft param</u>
Manufacture – Dimension/Draft – LineFont	<u>linefont</u>
Manufacture – Dimension/Draft – Linear Dim	<u>dimension linear</u>
Manufacture – Dimension/Draft – Datum Dim	<u>dimension datum</u>
Manufacture – Dimension/Draft – Angular Dim	<u>dimension angular</u>
Manufacture – Dimension/Draft – Leader Lines	<u>leader only</u>
Manufacture – Dimension/Draft – Diametral Leader	<u>leader diametral</u>
Manufacture – Dimension/Draft – Radial Leader	<u>leader radial</u>
Manufacture – Dimension/Draft – Balloon Leader	<u>leader balloon</u>
Manufacture – Dimension/Draft – Chamfer Leader	<u>leader chamfer</u>
Manufacture – Dimension/Draft – Chamfer	<u>draft chamfer</u>
Manufacture – Dimension/Draft – Fillet	<u>draft fillet</u>
Manufacture – Dimension/Draft – Create Detail	<u>create detail</u>
Manufacture – Stream Out	<u>stream out</u>
Manufacture – Artwork	<u>film param</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Manufacture – NC – Drill Customization	<u>ncdrill customization</u>
Manufacture – NC – Drill Legend	<u>ncdrill legend</u>
Manufacture – NC – NC Parameters	<u>ncdrill param</u>
Manufacture – NC – NC Drill	<u>nctape full</u>
Manufacture – NC – NC Route	<u>ncroute</u>
Manufacture – DFx Check (legacy)	<u>dfa</u>
Manufacture – Create Coupons	<u>create coupons</u>
Manufacture – Silkscreen	<u>silkscreen param</u>
Manufacture – Thieving	<u>thieving</u>
Manufacture – Shape Degassing	<u>degas</u>
Manufacture – Testprep – Automatic	<u>testprep automatic</u>
Manufacture – Testprep – Manual	<u>testprep manual</u>
Manufacture – Testprep – Properties	<u>testprep properties</u>
Manufacture – Testprep – Fix/unfix testpoints	<u>testprep fix</u>
Manufacture – Testprep – Create FIXTURE	<u>testprep createfixture</u>
Manufacture – Testprep – Create NC drill data	<u>testprep ncdrill</u>
Manufacture – Testprep – Parameters	<u>testprep prmed</u>
Manufacture – Create Bond Finger Soldermask	<u>wirebond soldermask create</u>
Manufacture – Documentation – Bond Finger Text	<u>bpa</u>
Manufacture – Documentation – Display Pin Text	<u>dpn</u>
Manufacture – Documentation – Package Report – Sorted by Die Pin	<u>dbp report die</u>
Manufacture – Documentation – Package Report – Sorted by Bond Finger	<u>dbp report bondfinger</u>
Manufacture – Documentation – Package Report – Sorted by Package Pin	<u>dbp report package</u>
Manufacture – Documentation – Package Report – Sorted by Netname	<u>dbp report net</u>

Reports

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Design Summary Report (APD XL)	<u>design summary report</u>
Net Delay Report (APD XL and APSI)	<u>net delay report</u>
Conductor Length Report (APD L and XL)	<u>cond length report</u>
Wire Bond Report (APD XL)	<u>wirebond reports</u>
Metal Usage Report (APD XL)	<u>metal usage report</u>
Reports	<u>reports</u>
Quick Reports	No corresponding command
Component Compare (APD XL only)	<u>compare comp</u>
Design Compare (APD L and XL)	<u>design compare</u>
Tools	
Tools – Create Module (APD only)	<u>create module</u>
Tools – Padstack – Modify Design Padstack (APD L and XL)	<u>padeditdb</u>
Tools – Padstack – Modify Library Padstack (APD L and XL)	<u>padeditlib</u>
Tools – Padstack – Replace (APD L and XL)	<u>replace padstack</u>
Tools – Padstack – Group Edit (APD L and XL)	<u>multpadedit</u>
Tools – Padstack – Refresh (APD L and XL)	<u>refresh padstack</u>
Tools – Pad – Boundary (APD L and XL)	<u>editpad boundary</u>
Tools – Pad – Restore (APD L and XL)	<u>editpad restore</u>
Tools – Pad – Restore ALL (APD L and XL)	<u>editpad restore all</u>
Tools – Derive Connectivity (APD L and XL)	<u>derive connectivity</u>
Tools – Compose Line	<u>compose line</u>
Tools – Database Diary	<u>db diary</u>
Tools – Topology Editor (AP SI only)	<u>sigxp</u>
Tools – Model Integrity (AP SI only)	<u>model integrity</u>
Tools – Technology File Compare	<u>techfile compare</u>
Tools – Setup Advisor	<u>setup advisor</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-3 APD/AP SI Command Mapping

Tools – Package Design Integrity	<u>package_integrity</u>
Tools – Database Check	<u>drbdocto</u>
Tools – Update DRC	<u>drc_update</u>
Tools – Utilities – Env Variables	<u>set</u>
Tools – Utilities – Aliases/Function Keys	<u>alias</u>
Tools – Utilities – Keyboard Commands	<u>helpcmd</u>
Tools – Utilities – Licenses Used	<u>license_use</u>
Tools – Utilities – Stroke Editor	<u>stroke_editor</u>
Help	
Help – Documentation	<u>cdsdoc</u>
Help – Message Detail	<u>smi_message_detail</u>
Help – Web Resources – KP&S	Web URL
Help – Web Resources – cdnsUsers.org	Web URL
Help – Web Resources – Sourcelink	Web URL
Help – Web Resources – Web Collaboration	Web URL
Help – Web Resources – Education Services	Web URL
Help – Web Resources – Design Communities (APSI)	Web URL
Help – About APD/AP SI	<u>about</u>

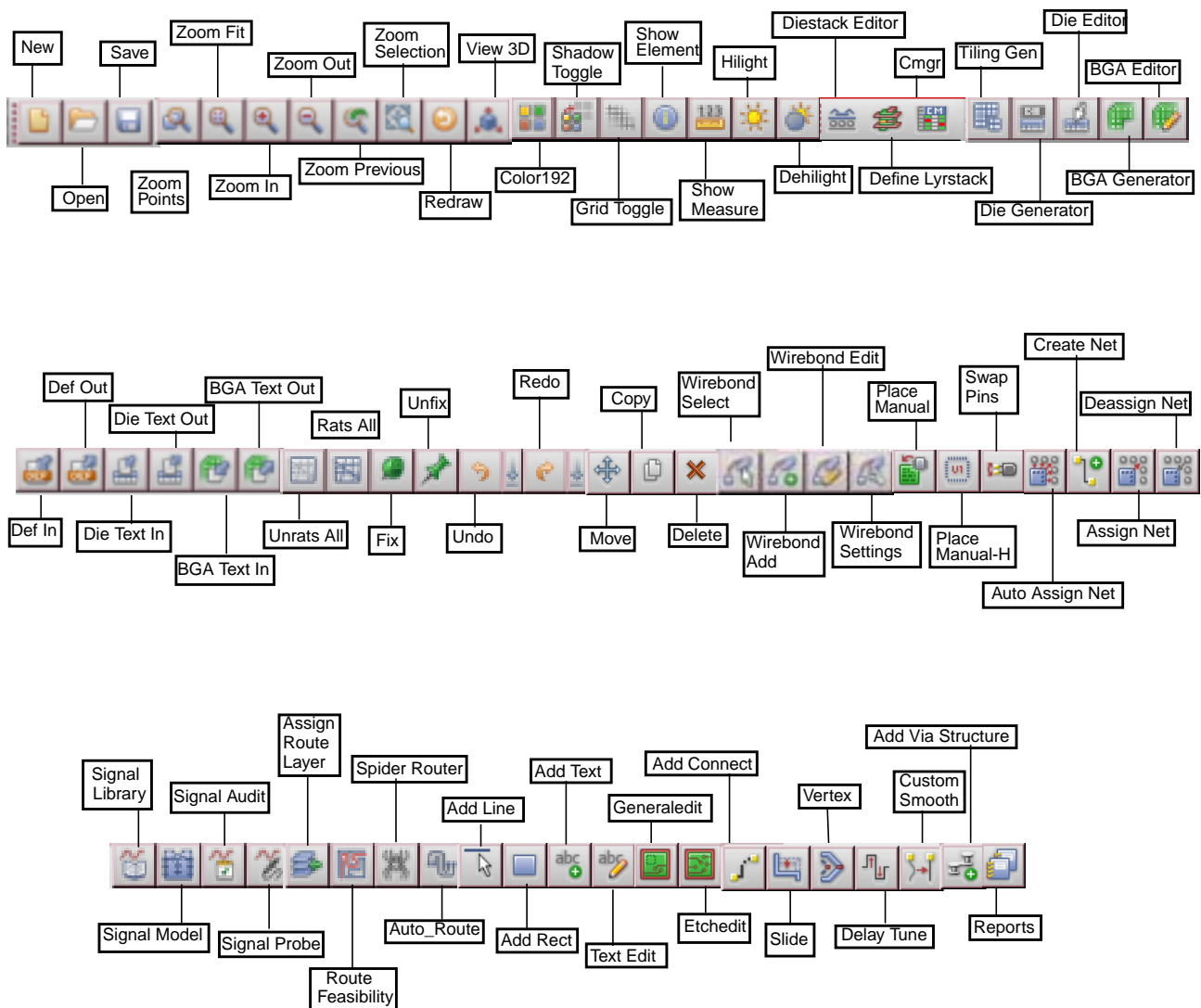
SiP Digital Architect/SiP Layout

The following diagram identifies the SiP Digital Architect/SiP Layout user interface toolbar icons, which execute the same console window commands corresponding to product menu choices. Your toolbar configuration may differ. You can also hover your cursor over each icon to display a datatip that identifies its function.

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Figure A-4 SiP Digital Architect/SiP Layout Toolbar Icons



The command mapping in Table A-4 lists the menu choices in the different modes (Layout and Symbol) of SiP Digital Architect and SiP Layout. Note that some commands may not be available in both products.

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Menu Choice
File

Console Window Command

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

File – New	<u>new</u>
File – Open	<u>open</u>
File – Save	<u>save</u>
File – Save As	<u>save as</u>
File – Create Symbol	<u>create symbol</u> (in Symbol Editor only)
File – Create Device	<u>create Device</u> (in Symbol Editor only)
File – Import – Netlist-In Wizard	<u>net list in</u>
File – Import – Logic	<u>netin param</u>
File – Import – MCM	<u>mcm import</u>
File – Import – NA2	<u>na2 import</u>
File – Import – DXF	<u>dxs in</u>
File – Import – Artwork (SiP Layout only)	<u>load photoplot</u>
File – Import – Stream (SiP Layout only)	<u>load stream</u>
File – Import – IDF (SiP Layout only)	<u>idf in</u>
File – Import – AIF	<u>aif in</u>
File – Import – IFF (SiP Layout only)	<u>iff in</u>
File – Import – Router	<u>specctra in</u>
File – Import – Sub-Drawing	<u>clppaste</u>
File – Import – Techfile	<u>techfile in</u>
File – Import – Parameters	<u>param in</u>
File – Import – Active Times	<u>signal atimes</u>
File – Import – Placement (SiP Layout only)	<u>plctxt in</u>
File – Import – Paste Resistor	<u>film res</u>
File – Import – Annotations (SiP Layout only)	<u>annotation in</u>
File – Import – Pin Delay	<u>pin delay in</u>
File – Export – BGA Text-Out Wizard	<u>bga text out</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

File – Export – Die Text-Out Wizard	<u>die text out</u>
File – Export – DEF (Die Pins Only)	<u>def out</u>
File – Export – OpenAccess (Die Pins Only) UNIX platforms only	<u>oa out</u>
File – Export – Logic	<u>feedback</u>
File – Export – Netlist w/Properties	<u>netout</u>
File – Export – MCM	<u>mcm export</u>
File – Export – DXF (SiP Layout only)	<u>dxs out</u>
File – Export – IDF (SiP Layout only)	<u>idf out</u>
File – Export – AIF	<u>aif out</u>
File – Export – Router	<u>specetra out</u>
File – Export – Sub-Drawing	<u>clpcopy</u>
File – Export – Libraries	<u>dlib</u>
File – Export – Techfile	<u>techfile out</u>
File – Export – Parameters	<u>param out</u>
File – Export – Placement (SiP Layout only)	<u>plctxt out</u>
File – Export – Board Level Component (SiP Layout only)	<u>allegro component</u>
File – Export – Symbol Spreadsheet (SiP Layout only)	<u>symbol to spreadsheet</u>
File – Export – Annotations (SiP Layout only)	<u>annotation out</u>
File – Export – InterComm (SiP Layout only)	<u>icm out</u>
File – Export – IPC 356 (SiP Layout only)	<u>ipc356 out</u>
File – Export – ODB ++ inside (SiP Layout only)	<u>odb out</u>
File – Export – Save Design to 16.1	<u>downrev</u>
File – Export – Pin Delay	<u>pin delay out</u>
File – Viewlog	<u>viewlog</u>
File – File Viewer	No corresponding command
File – Plot Setup	<u>plot setup</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

File – Plot	<u>plot</u>
File – Properties	<u>file property</u>
File – Change Editor	<u>toolswap</u>
File – Script	<u>script</u>
File – Recent Designs	<u>opencd</u>
File – Exit	<u>exit</u>
Edit	
Edit – Undo	<u>undo</u>
Edit – Redo	<u>redo</u>
Edit – Move	<u>move</u>
Edit – Copy	<u>copy</u>
Edit – Mirror	<u>mirror</u>
Edit – Spin	<u>spin</u>
Edit – Change	<u>change</u>
Edit – Delete	<u>delete</u>
Edit – Z-Copy	<u>zcopy shape</u>
Edit – Split Plane – Parameters (SiP Layout only)	<u>split plane param</u>
Edit – Split Plane – Create (SiP Layout only)	<u>split plane create</u>
Edit – Vertex	<u>vertex</u>
Edit – Delete Vertex	<u>delete vertex</u>
Edit – Cline Change Width	<u>cline change width</u>
Edit – Text	<u>text edit</u>
Edit – Groups	<u>groupedit</u>
Edit – Properties	<u>property edit</u>
Edit – Net Properties	<u>net properties</u>
Edit – LEF Pin Parameters	<u>lef pin param</u>
Edit – Die Properties	<u>die properties</u>
Edit – Die Stack	<u>diestack editor</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Edit – Die	<u>die editor</u>
Edit – BGA	<u>bga editor</u>
View	
View – Zoom By Points	<u>zoom points</u>
View – Zoom Fit	<u>zoom fit</u>
View – Zoom In	<u>zoom in</u>
View – Zoom Out	<u>zoom out</u>
View – Zoom World	<u>zoom world</u>
View – Zoom Center	<u>zoom center</u>
View – Zoom Previous	<u>zoom previous</u>
View – Color View Save	<u>colorview create</u>
View – Color View Restore Last	<u>colorview restore</u>
View – 3D Model	<u>view 3d</u>
View – Redraw	<u>redisplay</u>
View – Windows – Command	No corresponding command
View – Windows – World View	No corresponding command
View – Windows – Options	No corresponding command
View – Windows – Find	No corresponding command
View – Windows – Visibility	No corresponding command
View – Windows – Show All	No corresponding command
View – Customize Toolbar	No corresponding command
View – Reset UI to Cadence Default	<u>reset docwindows</u>
Add	
Add – Line	<u>add line</u>
Add – Arc w/Radius	<u>add rarc</u>
Add – 3pt Arc	<u>add arc</u>
Add – Circle	<u>add circle</u>
Add – Rectangle (in SiP Layout only)	<u>add rect</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Add – Frectangle (in SiP Layout only)	<u>add frect</u>
Add – Text	<u>add text</u>
Add – Interposer	<u>add interposer</u>
Add – Spacer	<u>add spacer</u>
Add – Co-Design Die	<u>add codesign die</u>
Add – Standard Die – DEF (Die Pins Only)	<u>def in</u>
Add – Standard Die – OA (Die Pins Only) – UNIX platforms only	<u>oa in</u>
Add – Standard Die – Die Text-In Wizard	<u>die text in</u>
Add – Standard Die – Die Generator	<u>die generator</u>
Add – Standard Die – Tiled Die Generator	<u>tiling gen</u>
Add – Standard Die – D.I.E Format	<u>die in</u>
Add – Standard Package – BGA – Text-In Wizard	<u>bga text in</u>
Add – Standard Package – BGA Generator	<u>bga generator</u>
Display	
Display – Color/Visibility	<u>color</u>
Display – Layer Priority	<u>layer priority</u>
Display – Status	<u>status</u>
Display – Element	<u>show element</u>
Display – Measure	<u>show measure</u>
Display – Constraint	<u>cns show</u>
Display – Parasitic	<u>show parasitic</u>
Display – Segments Over Voids	<u>highlight sov</u>
Display – Property	<u>show property</u>
Display – Assign Color	<u>assign color</u>
Display – Highlight	<u>hilight</u>
Display – Dehighlight	<u>dehilight</u>
Display – Waive DRCs – Waive	<u>waive drc</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Display – Waive DRCs – Show	<u>show waived drcs</u>
Display – Waive DRCs – Blank	<u>blank waived drcs</u>
Display – Waive DRCs – Restore	<u>restore waived drc</u>
Display – Waive DRCs – Restore All	<u>restore waived drcs</u>
Display – Pin Highlight	<u>pin highlight</u>
Display – Bond Finger Highlight	<u>bond finger hilite</u>
Display – Bond Finger Dehighlight	<u>bond finger dehilite</u>
Display – Rats by Layer	<u>rats layer</u>
Display – Show Rat Lines – All	<u>rats all</u>
Display – Show Rat Lines – Components	<u>rats component</u>
Display – Show Rat Lines – Net	<u>rats net</u>
Display – Show Rat Lines – Of Selection	<u>rats show</u>
Display – Blank Rats – All	<u>unrats all</u>
Display – Blank Rats – Components	<u>unrats component</u>
Display – Blank Rats – Nets	<u>unrats net</u>
Setup	
Setup – Design Parameters	<u>prmed</u>
Setup – Grids	<u>define grid</u>
Setup – Subclasses	<u>define subclass</u>
Setup – Cross-section	<u>define lyrstack</u>
Setup – Unused Pads Suppresion	<u>unused pads</u>
Setup – Materials	<u>define materials</u>
Setup – Application Modes – General Edit	<u>generaledit</u>
Setup – Application Modes – Placement Edit	<u>placementedit</u>
Setup – Application Modes – Etch Edit	<u>etchedit</u>
Setup – Application Modes – None	<u>noappmode</u>
Setup – Blind/Buried Via Definitions – Define B/B Via	<u>define bbvia</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Setup – Blind/Buried Via Definitions – Auto Define B/B Via	<u>auto define bbvia</u>
Setup – Enable On-Line DRC	<u>cns onlinedrc</u>
Setup – Constraints – Modes	<u>cns cmmodes</u>
Setup – Constraints – Electrical	<u>cmgr elec</u>
Setup – Constraints – Physical	<u>cmgr phys</u>
Setup – Constraints – Spacing	<u>cmgr spac</u>
Setup – Constraints – Same Net Spacing	<u>cmgr snspac</u>
Setup – Constraints – Physical Net Overrides	<u>property edit</u>
Setup – Constraints – Spacing Net Overrides	<u>property edit</u>
Setup – Constraints – DFA Constraint Spreadsheet	<u>dfa spreadsheet</u>
Setup – Constraints – Constraint Manager	<u>cmgr</u>
Setup – Property Definitions	<u>define property</u>
Setup – Define Lists	<u>define list</u>
Setup – LEF Libraries	<u>lef lib</u>
Setup – Areas – Component Keepin	<u>keepin component</u>
Setup – Areas – Component Keepout	<u>keepout component</u>
Setup – Areas – Component Height	<u>component height</u>
Setup – Areas – Route Keepin	<u>keepin router</u>
Setup – Areas – Route Keepout	<u>keepout router</u>
Setup – Areas – Wire Keepout	<u>keepout wire</u>
Setup – Areas – Via Keepout	<u>keepout via</u>
Setup – Areas – Shape Keepout	<u>keepout shape</u>
Setup – Areas – Probe Keepout	<u>keepout probe</u>
Setup – Areas – Gloss Keepout	<u>keepout gloss</u>
Setup – Areas – Photoplot Outline	<u>keepin photo</u>
Setup – User Preferences	<u>enved</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Layout	Layout menu choices are available only in the Symbol (Part) Editor
Layout – Pins	<u>add pin</u>
Layout – Pin RenNumbering	<u>rpn</u>
Layout – Connections	<u>add connect</u>
Layout – Slide	<u>slide</u>
Layout – Labels – RefDes	<u>label refdes</u>
Layout – Labels – Device	<u>label device</u>
Layout – Labels – Value	<u>label value</u>
Layout – Labels – Tolerance	<u>label tolerance</u>
Layout – Labels – Part Number	<u>label part</u>
Shape	This menu is available only in SiP Digital Layout.
Shape – Polygon	<u>shape add</u>
Shape – Rectangular	<u>shape add rect</u>
Shape – Circular	<u>shape add circle</u>
Shape – Select Shape or Void	<u>shape select</u>
Shape – Manual Void – Polygon	<u>shape void polygon</u>
Shape – Manual Void – Rectangular	<u>shape void rectangle</u>
Shape – Manual Void – Circular	<u>shape void circle</u>
Shape – Manual Void – Delete	<u>shape void delete</u>
Shape – Manual Void – Element	<u>shape void element</u>
Shape – Manual Void – Move	<u>shape void move</u>
Shape – Manual Void – Copy	<u>shape void copy</u>
Shape – Edit Boundary	<u>shape edit boundary</u>
Shape – Delete Islands	<u>island delete</u>
Shape – Change Shape Type	<u>shape change type</u>
Shape – Merge Shapes	<u>shape merge shapes</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Shape – Check	<u>shape check</u>
Shape – Compose Shape	<u>compose shape</u>
Shape – Decompose Shape	<u>decompose shape</u>
Shape – Global Dynamic Params	<u>shape global param</u>
Logic	
Logic – Auto Create Net	<u>auto create net</u>
Logic – Create Net	<u>create net</u>
Logic – Auto Assign Net	<u>auto assign net</u>
Logic – Assign Multiple Nets	<u>assign multi nets</u>
Logic – Assign Net	<u>assign net</u>
Logic – Deassign Net	<u>deassign net</u>
Logic – Derive Assignment	<u>derive assignment</u>
Logic – Auto Assign Pin Use	<u>auto assign pinuse</u>
Logic – Purge Unused Nets	<u>purge unused nets</u>
Logic – Purge Unplaced Components	<u>purge unplaced comps</u>
Logic – Identify DC Nets	<u>identify nets</u>
Logic – Identify Buses	<u>identify buses</u>
Logic – Net Logic	<u>net logic</u>
Logic – Net Schedule	<u>net schedule</u>
Logic – Assign Differential Pair	<u>diff pairs</u>
Logic – Assign RefDes	<u>assign refdes</u>
Logic – Auto Rename RefDes – Rename	<u>rename param</u>
Logic – Auto Rename RefDes – Design	<u>rename area design</u>
Logic – Auto Rename RefDes – Room	<u>rename area room</u>
Logic – Auto Rename RefDes – Window	<u>rename area window</u>
Logic – Auto Rename RefDes – List	<u>rename area list</u>
Logic – Edit Parts List	<u>edit parts</u>

Place

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Place – Manually	<u>place manual</u>
Place – Autoplace – Insight (SiP Layout only)	<u>place insight</u>
Place – Autoplace – Parameters (SiP Layout only)	<u>place param</u>
Place – Autoplace – Top Grids (SiP Layout only)	<u>place set topgrid</u>
Place – Autoplace – Bottom Grids (SiP Layout only)	<u>place set bottomgrid</u>
Place – Autoplace – Design (SiP Layout only)	<u>place area design</u>
Place – Autoplace – Room (SiP Layout only)	<u>place area room</u>
Place – Autoplace – Window (SiP Layout only)	<u>place area window</u>
Place – Autoplace – List (SiP Layout only)	<u>place area list</u>
Place – Interactive (SiP Layout only)	<u>place interactive</u>
Place – Swap – Pins	<u>swap pins</u>
Place – Swap – Functions (SiP Layout only)	<u>swap functions</u>
Place – Swap – Components (SiP Layout only)	<u>swap components</u>
Place – Autoswap – Parameters (SiP Layout only)	<u>swap param</u>
Place – Autoswap – Design (SiP Layout only)	<u>swap area design</u>
Place – Autoswap – Room (SiP Layout)	<u>swap area room</u>
Place – Autoswap – Window (SiP Layout only)	<u>swap area window</u>
Place – Autoswap – List (SiP Layout only)	<u>swap area list</u>
Place – Update Symbols	<u>refresh symbol</u>
Place – Replace SI Temporary – Devices	<u>replace temp device</u>
Place – Replace SI Temporary – Symbols	<u>replace temp symbols</u>
Place – Design Partition – Create Partitions	<u>partition</u>
Place – Design Partition – Workflow Manager	<u>workflow</u>
Place – Design Partition – Guideports	<u>guideport</u>
Place – Design Partition – Soft Net Assignment	<u>soft net</u>
Route	
Route – Connect	<u>add connect</u>
Route – Slide	<u>slide</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Route – Power/Ground Ring Generator	<u>pring wizard</u>
Route – Wire Bond – Select	<u>wirebond select</u>
Route – Wire Bond – Add	<u>wirebond add</u>
Route – Wire Bond – Edit	<u>wirebond edit</u>
Route – Wire Bond – Modify	<u>wirebond modify</u>
Route – Wire Bond – Add/Edit Guide Paths	<u>wirebond manage guide paths</u>
Route – Wire Bond – Settings	<u>wirebond settings</u>
Route – Wire Bond – Purge Unused Groups	<u>wirebond purge groups</u>
Route – Wire Bond –Tack Point Move (SiP Layout only)	<u>wirebond tack point</u>
Route – Wire Bond – Import	<u>wirebond import</u>
Route – Wire Bond – Export	<u>wirebond export</u>
Route – Wire Bond – Uprev	<u>wirebond uprev</u>
Route – Via Structure – Add	<u>add via structure</u>
Route – Via Structure – Replace	<u>replace via structure</u>
Route – Via Structure – Refresh	<u>refresh via structure</u>
Route – Offset Via Generator	<u>offset via gen</u>
Route – Flip-Chip Routing Estimation Layer (SiP Layout only)	<u>layer estimation</u>
Route – Flip-Chip Die Escape Generator (SiP Layout only)	<u>die escape gen</u>
Route – Wire Bond Via Estimation (SiP Layout only)	<u>wire bond via estimation</u>
Route – Wire Bond Die Escape Generator (SiP Layout only)	<u>wire bond escape</u>
Route – Routing Layer Assign	<u>assign route layer</u>
Route – Plating Layer Assign (SiP Layout only)	<u>assign plating layer</u>
Route – Define Net Priority	<u>route priority</u>
Route – Route Feasibility	<u>route feasibility</u>
Route – Spider Router	<u>spider router</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Route – Custom Smooth	<u>custom smooth</u>
Route – Delay Tune	<u>delay tune</u>
Route – Define Short	<u>define shorting scheme</u>
Route – Create Short	<u>create short</u>
Route – ZRouter	<u>zrouter</u>
Route – Router – Route Radial	<u>radial router</u>
Route – Router – Fanout by Pick	<u>fanout by pick</u>
Route – Router – Route by Pick	<u>route by pick</u>
Route – Router – Elongation by Pick	<u>elong by pick</u>
Route – Router – Route Automatic	<u>auto route</u>
Route – Router – Router Checks	<u>specctra checks</u>
Route – Router – Interactive Editor	<u>specctra</u>
Route – Router – Miter by Pick	<u>miter by ppick</u>
Route – Router – Unmiter by Pick	<u>unmiter by pick</u>
Route – Router – Spread Clines (SiP Layout only)	<u>spread clines</u>
Route – Router – Line Fattening	<u>line fattening</u>
Route – Add Fillet (SiP Layout only)	<u>add fillet</u>
Route – Delete Fillet (SiP Layout only)	<u>delete fillet</u>
Route – Gloss – Parameters (SiP Layout only)	<u>gloss param</u>
Route – Gloss – Design (SiP Layout only)	<u>gloss area design</u>
Route – Gloss – Room (SiP Layout only)	<u>gloss area room</u>
Route – Gloss – Window (SiP Layout only)	<u>gloss area window</u>
Route – Gloss – Highlight (SiP Layout only)	No corresponding command
Route – Gloss – List (SiP Layout only)	<u>gloss area list</u>
Analyze	
Analyze – Initialize	<u>signal init</u>
Analyze – Library	<u>signal library</u>
Analyze – Model Assignment	<u>signal model</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Analyze – Model Dump/Refresh	<u>signal model refresh</u>
Analyze – Preferences	<u>signal prefs</u>
Analyze – Audit – Design Audit	<u>signal audit</u>
Analyze – Audit – Net Audit	<u>signal audit net</u>
Analyze – Audit – Audit One Library	<u>signal lib audit</u>
Analyze – Audit – Audit List of Libraries	<u>signal libs audit</u>
Analyze – Probe	<u>signal probe</u>
Analyze – Xtalk Table	<u>signal xtalktable</u>
Analyze – EMI Rule Checker	<u>emcontrol</u>
Analyze – 3-D Package Model (In legacy products only)	<u>signal pkg model</u>
Analyze – 3-D Modeling (SiP Architect only)	<u>signal 3dmodel</u>
Analyze – Bus Setup (SiP Architect only)	<u>signal bus setup</u>
Analyze – Bus Simulate (SiP Architect only)	<u>signal bus sim</u>
Manufacture	This menu is available only in SiP Layout.
Manufacture – Create Plating Bar	<u>pbar create</u>
Manufacture – Delete Plating Bar	<u>pbar delete</u>
Manufacture – Plating Bar Check	<u>pbar check</u>
Manufacture – Etch-back	<u>etchback</u>
Manufacture – Assembly Rule Checker	<u>assemrules standard</u>
Manufacture – Dimension/Draft commands in the Layout Editor are accessed under the Dimension menu item in the Symbol Editor	
Manufacture – Dimension/Draft – Parameters	<u>draft param</u>
Manufacture – Dimension/Draft – LineFont	<u>linefont</u>
Manufacture – Dimension/Draft – Linear Dim	<u>dimension linear</u>
Manufacture – Dimension/Draft – Datum Dim	<u>dimension datum</u>
Manufacture – Dimension/Draft – Angular Dim	<u>dimension angular</u>
Manufacture – Dimension/Draft – Leader Lines	<u>leader only</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Manufacture – Dimension/Draft – Diametral Leader	<u>leader diametral</u>
Manufacture – Dimension/Draft – Radial Leader	<u>leader radial</u>
Manufacture – Dimension/Draft – Balloon Leader	<u>leader balloon</u>
Manufacture – Dimension/Draft – Chamfer Leader	<u>leader chamfer</u>
Manufacture – Dimension/Draft – Chamfer	<u>draft chamfer</u>
Manufacture – Dimension/Draft – Fillet	<u>draft fillet</u>
Manufacture – Dimension/Draft – Create Detail	<u>create detail</u>
Manufacture – Stream Out	<u>stream out</u>
Manufacture – Artwork	<u>film param</u>
Manufacture – NC – Drill Customization	<u>ncdrill customization</u>
Manufacture – NC – Drill Legend	<u>ncdrill legend</u>
Manufacture – NC – NC Parameters	<u>ncdrill param</u>
Manufacture – NC – NC Drill	<u>nctape full</u>
Manufacture – NC – NC Route	<u>ncroute</u>
Manufacture – DFX Check (legacy)	<u>dfa</u>
Manufacture – Thieving	<u>thieving</u>
Manufacture – Shape Degassing	<u>degas</u>
Manufacture – Create Bond Finger Soldermask	<u>wirebond soldermask create</u>
Manufacture – Documentation – Bond Finger Text	<u>bpa</u>
Manufacture – Documentation – Display Pin Text	<u>dpn</u>
Manufacture – Documentation – Package Report – Sorted by Die Pin	<u>dbp report die</u>
Manufacture – Documentation – Package Report – Sorted by Bond Finger	<u>dbp report bondfinger</u>
Manufacture – Documentation – Package Report – Sorted by Package Pin	<u>dbp report package</u>
Manufacture – Documentation – Package Report – Sorted by Netname	<u>dbp report net</u>

Reports

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Design Summary Report	<u>design summary report</u>
Net Delay Report	<u>net delay report</u>
Conductor Length Report	<u>cond length report</u>
Wire Bond Report	<u>wirebond reports</u>
Metal Usage Report	<u>metal usage report</u>
Reports	<u>reports</u>
Quick Reports	No corresponding command
Component Compare	<u>compare comp</u>
Design Compare	<u>design compare</u>
Tools	
Tools – Create Module	<u>create module</u>
Tools – Padstack – Modify Design Padstack	<u>padeditdb</u>
Tools – Padstack – Modify Library Padstack	<u>padeditlib</u>
Tools – Padstack – Replace	<u>replace padstack</u>
Tools – Padstack – Group Edit	<u>multpadedit</u>
Tools – Padstack – Refresh	<u>refresh padstack</u>
Tools – Pad – Boundary	<u>editpad boundary</u>
Tools – Pad – Restore	<u>editpad restore</u>
Tools – Pad – Restore ALL	<u>editpad restore all</u>
Tools – Derive Connectivity	<u>derive connectivity</u>
Tools – Compose Line	<u>compose line</u>
Tools – Topology Editor (available only in Architect)	<u>sigxp</u>
Tools – Model Integrity (available only in Architect)	<u>model integrity</u>
Tools – Database Diary	<u>db diary</u>
Tools – Technology File Compare	<u>techfile compare</u>
Tools – Setup Advisor	<u>setup advisor</u>
Tools – Package Design Integrity	<u>package integrity</u>
Tools – Database Check	<u>drbdocto</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-4 SiP Digital Architect/SiP Layout Command Mapping

Tools – Update DRC	<u>drc update</u>
Tools – Utilities – Env Variables	<u>set</u>
Tools – Utilities – Aliases/Function Keys	<u>alias</u>
Tools – Utilities – Keyboard Commands	<u>helpcmd</u>
Tools – Utilities – Licenses Used	<u>license use</u>
Tools – Utilities – Stroke Editor	<u>stroke editor</u>
Help	
Help – Documentation	<u>cdsdoc</u>
Help – Message Detail	<u>smi message detail</u>
Help – SiP Solution Overview	
Help – Web Resources – KP&S	Web URL
Help – Web Resources – cdnsUsers.org	Web URL
Help – Web Resources – Sourcelink	Web URL
Help – Web Resources – Web Collaboration	Web URL
Help – Web Resources – Education Services	Web URL
Help – About Cadence SiP Layout	<u>about</u>

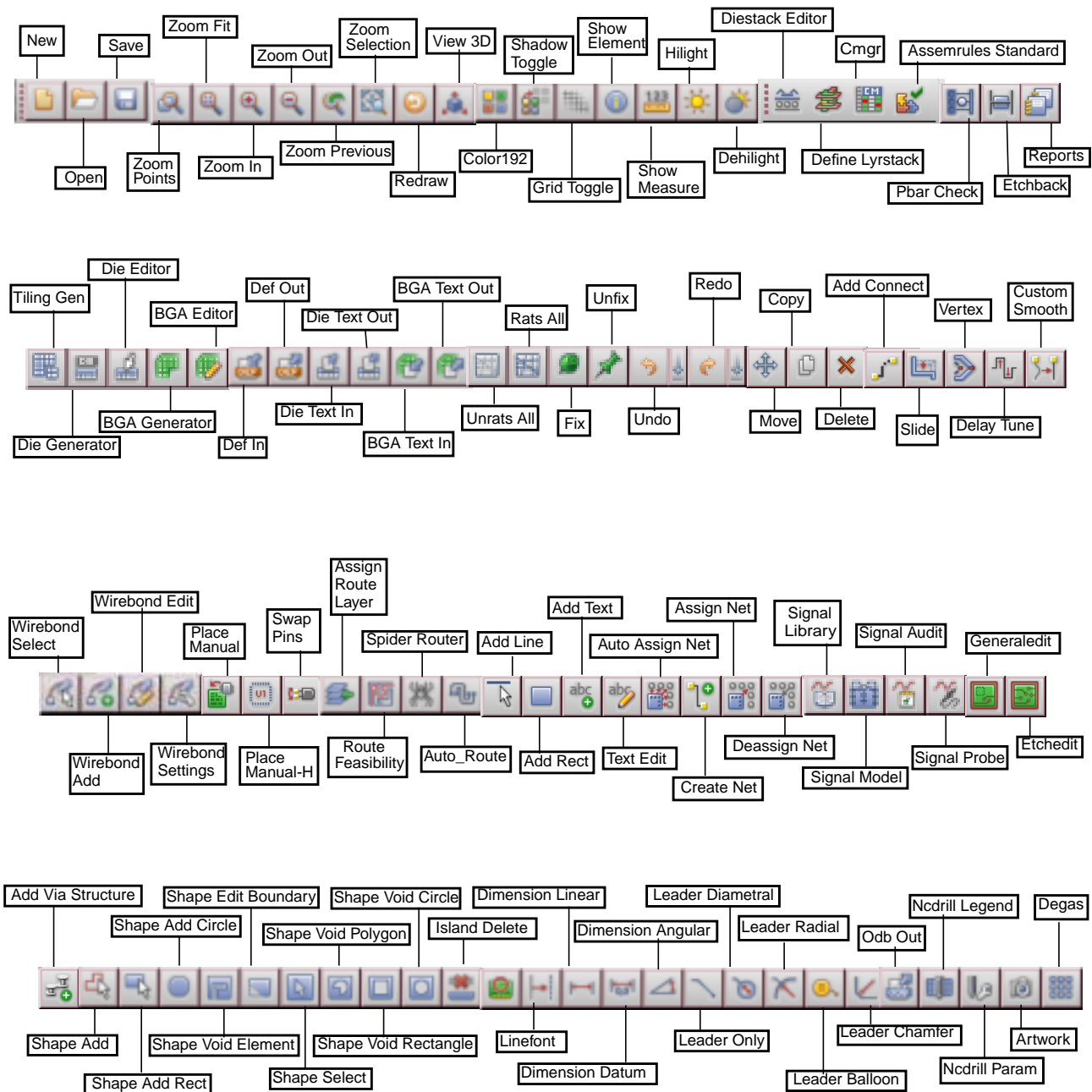
SiP RF Layout

The following diagram identifies the SiP RF Layout user interface toolbar icons, which execute the same console window commands corresponding to product menu choices. Your toolbar configuration may differ. You can also hover your cursor over each icon to display a datatip that identifies its function.

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Figure A-5 SiP RF Layout Toolbar Icons



The command mapping in Table A-5 lists the menu choices and corresponding commands for SiP RF Layout.

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Menu Choice	Console Window Command
File	
File – New	<u>new</u>
File – Open	<u>open</u>
File – Save	<u>save</u>
File – Save As	<u>save as</u>
File – Create Symbol	<u>create symbol</u> (in Symbol Editor only)
File – Create Device	<u>create Device</u> (in Symbol Editor only)
File – Import – Netlist-In Wizard	<u>net list in</u>
File – Import – Logic	<u>netin param</u>
File – Import – MCM	<u>mcm import</u>
File – Import – NA2	<u>na2 import</u>
File – Import – DXF	<u>dx f in</u>
File – Import – Artwork	<u>load photoplot</u>
File – Import – Stream	<u>load stream</u>
File – Import – IDF	<u>idf in</u>
File – Import – AIF	<u>aif in</u>
File – Import – IFF	<u>iff in</u>
File – Import – Router	<u>specctra in</u>
File – Import – Sub-Drawing	<u>clppaste</u>
File – Import – Techfile	<u>techfile in</u>
File – Import – Parameters	<u>param in</u>
File – Import – Active Times	<u>signal atimes</u>
File – Import – Placement	<u>plctxt in</u>
File – Import – Paste Resistor	<u>film res</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

File – Import – Annotations	<u>annotation in</u>
File – Import – Pin Delay	<u>pin delay in</u>
File – Export – BGA Text-Out Wizard	<u>bga text out</u>
File – Export – Die Text-Out Wizard	<u>die text out</u>
File – Export – DEF (Die Pins Only)	<u>def out</u>
File – Export – OpenAccess (Die Pins Only) UNIX platforms only	<u>oa out</u>
File – Export – Logic	<u>feedback</u>
File – Export – Netlist w/Properties	<u>netout</u>
File – Export – MCM	<u>mcm export</u>
File – Export – DXF	<u>dxs out</u>
File – Export – IDF	<u>idf out</u>
File – Export – AIF	<u>aif out</u>
File – Export – Router	<u>specetra out</u>
File – Export – Sub-Drawing	<u>clpcopy</u>
File – Export – Libraries	<u>dlib</u>
File – Export – Techfile	<u>techfile out</u>
File – Export – Parameters	<u>param out</u>
File – Export – Placement	<u>plctxt out</u>
File – Export – Board Level Component	<u>allegro component</u>
File – Export – Symbol Spreadsheet	<u>symbol to spreadsheet</u>
File – Export – Annotations	<u>annotation out</u>
File – Export – InterComm	<u>icm out</u>
File – Export – IPC 356	<u>ipc356 out</u>
File – Export – ODB ++ inside	<u>odb out</u>
File – Export – Save Design to 16.1	<u>downrev</u>
File – Export – Pin Delay	<u>pin delay out</u>
File – Viewlog	<u>viewlog</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

File – File Viewer	No corresponding command
File – Plot Setup	<u>plot_setup</u>
File – Plot	<u>plot</u>
File – Properties	<u>file_property</u>
File – Change Editor	<u>toolswap</u>
File – Script	<u>script</u>
File – Recent Designs	<u>opencd</u>
File – Exit	<u>exit</u>
Edit	
Edit – Undo	<u>undo</u>
Edit – Redo	<u>redo</u>
Edit – Move	<u>move</u>
Edit – Copy	<u>copy</u>
Edit – Mirror	<u>mirror</u>
Edit – Spin	<u>spin</u>
Edit – Change	<u>change</u>
Edit – Delete	<u>delete</u>
Edit – Z-Copy	<u>zcopy_shape</u>
Edit – Split Plane – Parameters	<u>split_plane_param</u>
Edit – Split Plane – Create	<u>split_plane_create</u>
Edit – Vertex	<u>vertex</u>
Edit – Delete Vertex	<u>delete_vertex</u>
Edit – Cline Change Width	<u>cline_change_width</u>
Edit – Text	<u>text_edit</u>
Edit – Groups	<u>groupedit</u>
Edit – Properties	<u>property_edit</u>
Edit – Net Properties	<u>net_properties</u>
Edit – LEF Pin Parameters	<u>lef_pin_param</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Edit – Die Properties	<u>die properties</u>
Edit – Die Stack	<u>diestack editor</u>
Edit – Die	<u>die editor</u>
Edit – BGA	<u>bga editor</u>
View	
View – Zoom By Points	<u>zoom points</u>
View – Zoom Fit	<u>zoom fit</u>
View – Zoom In	<u>zoom in</u>
View – Zoom Out	<u>zoom out</u>
View – Zoom World	<u>zoom world</u>
View – Zoom Center	<u>zoom center</u>
View – Zoom Previous	<u>zoom previous</u>
View – Color View Save	<u>colorview create</u>
View – Color View Restore Last	<u>colorview restore</u>
View – 3D Model	<u>view 3d</u>
View – Redraw	<u>redisplay</u>
View – Windows – Command	No corresponding command
View – Windows – World View	No corresponding command
View – Windows – Options	No corresponding command
View – Windows – Find	No corresponding command
View – Windows – Visibility	No corresponding command
View – Windows – Show All	No corresponding command
View – Customize Toolbar	No corresponding command
View – Reset UI to Cadence Default	<u>reset docwindows</u>
Add	
Add – Line	<u>add line</u>
Add – Arc w/Radius	<u>add rarc</u>
Add – 3pt Arc	<u>add arc</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Add – Circle	<u>add circle</u>
Add – Rectangle	<u>add rect</u>
Add – Frectangle	<u>add frect</u>
Add – Text	<u>add text</u>
Add – Interposer	<u>add interposer</u>
Add – Spacer	<u>add spacer</u>
Add – Co-Design Die	<u>add codesign die</u>
Add – Standard Die – DEF (Die Pins Only)	<u>def in</u>
Add – Standard Die – OA (Die Pins Only) – UNIX platforms only	<u>oa in</u>
Add – Standard Die – Die Text-In Wizard	<u>die text in</u>
Add – Standard Die – Die Generator	<u>die generator</u>
Add – Standard Die – Tiled Die Generator	<u>tiling gen</u>
Add – Standard Die – D.I.E Format	<u>die in</u>
Add – Standard Package – BGA – Text-In Wizard	<u>bga text in</u>
Add – Standard Package – BGA Generator	<u>bga generator</u>

Display

Display – Color/Visibility	<u>color</u>
Display – Layer Priority	<u>layer priority</u>
Display – Status	<u>status</u>
Display – Element	<u>show element</u>
Display – Measure	<u>show measure</u>
Display – Constraint	<u>cns show</u>
Display – Parasitic	<u>show parasitic</u>
Display – Segments Over Voids	<u>highlight sov</u>
Display – Property	<u>show property</u>
Display – Assign Color	<u>assign color</u>
Display – Highlight	<u>hilight</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Display – Dehighlight	<u>dehighlight</u>
Display – Waive DRCs – Waive	<u>waive drc</u>
Display – Waive DRCs – Show	<u>show waived drcs</u>
Display – Waive DRCs – Blank	<u>blank waived drcs</u>
Display – Waive DRCs – Restore	<u>restore waived drc</u>
Display – Waive DRCs – Restore All	<u>restore waived drcs</u>
Display – Pin Highlight	<u>pin highlight</u>
Display – Bond Finger Highlight	<u>bond finger hilite</u>
Display – Bond Finger Dehighlight	<u>bond finger dehilite</u>
Display – Rats by Layer	<u>rats layer</u>
Display – Show Rat Lines – All	<u>rats all</u>
Display – Show Rat Lines – Components	<u>rats component</u>
Display – Show Rat Lines – Net	<u>rats net</u>
Display – Show Rat Lines – Of Selection	<u>rats show</u>
Display – Blank Rats – All	<u>unrats all</u>
Display – Blank Rats – Components	<u>unrats component</u>
Display – Blank Rats – Nets	<u>unrats net</u>
Setup	
Setup – Design Parameters	<u>prmed</u>
Setup – Grids	<u>define grid</u>
Setup – Subclasses	<u>define subclass</u>
Setup – Cross-section	<u>define lyrstack</u>
Setup – Materials	<u>define materials</u>
Setup – Application Modes – General Edit	<u>generaledit</u>
Setup – Application Mode – Place Mode	<u>placementedit</u>
Setup – Application Modes – Etch Edit	<u>etchedit</u>
Setup – Application Modes – None	<u>noappmode</u>
Setup – Blind/Buried Via Definitions – Define B/B Via	<u>define bbvia</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Setup – Blind/Buried Via Definitions – Auto Define B/B Via	<u>auto define bbvia</u>
Setup – Enable On-Line DRC	<u>cns onlinedrc</u>
Setup – Constraints – Modes	<u>cns cmmodes</u>
Setup – Constraints – Electrical	<u>cmgr elec</u>
Setup – Constraints – Physical	<u>cmgr phys</u>
Setup – Constraints – Spacing	<u>cmgr spac</u>
Setup – Constraints – Same Net Spacing	<u>cmgr snspac</u>
Setup – Constraints – Physical Net Overrides	<u>property edit</u>
Setup – Constraints – Spacing Net Overrides	<u>property edit</u>
Setup – Constraints – DFA Constraint Spreadsheet	<u>dfa spreadsheet</u>
Setup – Constraints – Constraint Manager	<u>cmgr</u>
Setup – Property Definitions	<u>define property</u>
Setup – Define Lists	<u>define list</u>
Setup – LEF Libraries	<u>lef lib</u>
Setup – Areas – Component Keepin	<u>keepin component</u>
Setup – Areas – Component Keepout	<u>keepout component</u>
Setup – Areas – Component Height	<u>component height</u>
Setup – Areas – Route Keepin	<u>keepin router</u>
Setup – Areas – Route Keepout	<u>keepout router</u>
Setup – Areas – Wire Keepout	<u>keepout wire</u>
Setup – Areas – Via Keepout	<u>keepout via</u>
Setup – Areas – Shape Keepout	<u>keepout shape</u>
Setup – Areas – Probe Keepout	<u>keepout probe</u>
Setup – Areas – Gloss Keepout	<u>keepout gloss</u>
Setup – Areas – Photoplot Outline	<u>keepin photo</u>
Setup – User Preferences	<u>enved</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Layout	Layout menu choices are available only in the Symbol (Part) Editor
Layout – Pins	<u>add pin</u>
Layout – Pin RenNumbering	<u>rpn</u>
Layout – Connections	<u>add connect</u>
Layout – Slide	<u>slide</u>
Layout – Labels – RefDes	<u>label refdes</u>
Layout – Labels – Device	<u>label device</u>
Layout – Labels – Value	<u>label value</u>
Layout – Labels – Tolerance	<u>label tolerance</u>
Layout – Labels – Part Number	<u>label part</u>
Shape	
Shape – Polygon	<u>shape add</u>
Shape – Rectangular	<u>shape add rect</u>
Shape – Circular	<u>shape add circle</u>
Shape – Select Shape or Void	<u>shape select</u>
Shape – Manual Void – Polygon	<u>shape void polygon</u>
Shape – Manual Void – Rectangular	<u>shape void rectangle</u>
Shape – Manual Void – Circular	<u>shape void circle</u>
Shape – Manual Void – Delete	<u>shape void delete</u>
Shape – Manual Void – Element	<u>shape void element</u>
Shape – Manual Void – Move	<u>shape void move</u>
Shape – Manual Void – Copy	<u>shape void copy</u>
Shape – Edit Boundary	<u>shape edit boundary</u>
Shape – Delete Islands	<u>island delete</u>
Shape – Change Shape Type	<u>shape change type</u>
Shape – Merge Shapes	<u>shape merge shapes</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Shape – Check	<u>shape check</u>
Shape – Compose Shape	<u>compose shape</u>
Shape – Decompose Shape	<u>decompose shape</u>
Shape – Global Dynamic Params	<u>shape global param</u>
Logic	
Logic – Auto Create Net	<u>auto create net</u>
Logic – Create Net	<u>create net</u>
Logic – Auto Assign Net	<u>auto assign net</u>
Logic – Assign Multiple Nets	<u>assign multi nets</u>
Logic – Assign Net	<u>assign net</u>
Logic – Deassign Net	<u>deassign net</u>
Logic – Derive Assignment	<u>derive assignment</u>
Logic – Auto Assign Pin Use	<u>auto assign pinuse</u>
Logic – Purge Unused Nets	<u>purge unused nets</u>
Logic – Purge Unplaced Components	<u>purge unplaced comps</u>
Logic – Identify DC Nets	<u>identify nets</u>
Logic – Identify Buses	<u>identify buses</u>
Logic – Net Logic	<u>net logic</u>
Logic – Net Schedule	<u>net schedule</u>
Logic – Assign Differential Pair	<u>diff pairs</u>
Logic – Assign RefDes	<u>assign refdes</u>
Logic – Auto Rename RefDes – Rename	<u>rename param</u>
Logic – Auto Rename RefDes – Design	<u>rename area design</u>
Logic – Auto Rename RefDes – Room	<u>rename area room</u>
Logic – Auto Rename RefDes – Window	<u>rename area window</u>
Logic – Auto Rename RefDes – List	<u>rename area list</u>
Logic – Edit Parts List	<u>edit parts</u>

Place

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Place – Manually	<u>place manual</u>
Place – Autoplace – Insight	<u>place insight</u>
Place – Autoplace – Parameters	<u>place param</u>
Place – Autoplace – Top Grids	<u>place set topgrid</u>
Place – Autoplace – Bottom Grids	<u>place set bottomgrid</u>
Place – Autoplace – Design	<u>place area design</u>
Place – Autoplace – Room	<u>place area room</u>
Place – Autoplace – Window	<u>place area window</u>
Place – Autoplace – List	<u>place area list</u>
Place – Interactive	<u>place interactive</u>
Place – Swap – Pins	<u>swap pins</u>
Place – Swap – Functions	<u>swap functions</u>
Place – Swap – Components	<u>swap components</u>
Place – Autoswap – Parameters	<u>swap param</u>
Place – Autoswap – Design	<u>swap area design</u>
Place – Autoswap – Room	<u>swap area room</u>
Place – Autoswap – Window	<u>swap area window</u>
Place – Autoswap – List	<u>swap area list</u>
Place – Update Symbols	<u>refresh symbol</u>
Place – Replace SI Temporary – Devices	<u>replace temp device</u>
Place – Replace SI Temporary – Symbols	<u>replace temp symbols</u>
Place – Design Partition – Create Partitions	<u>partition</u>
Place – Design Partition – Workflow Manager	<u>workflow</u>
Place – Design Partition – Guideports	<u>guideport</u>
Place – Design Partition – Soft Net Assignment	<u>soft net</u>
Route	
Route – Connect	<u>add connect</u>
Route – Slide	<u>slide</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Route – Power/Ground Ring Generator	<u>pring wizard</u>
Route – Wire Bond – Select	<u>wirebond select</u>
Route – Wire Bond – Add	<u>wirebond add</u>
Route – Wire Bond – Edit	<u>wirebond edit</u>
Route – Wire Bond – Modify	<u>wirebond modify</u>
Route – Wire Bond – Add/Edit Guide Paths	<u>wirebond manage guide paths</u>
Route – Wire Bond – Settings	<u>wirebond settings</u>
Route – Wire Bond – Purge Unused Groups	<u>wirebond purge groups</u>
Route – Wire Bond –Tack Point Move	<u>wirebond tack point</u>
Route – Wire Bond – Import	<u>wirebond import</u>
Route – Wire Bond – Export	<u>wirebond export</u>
Route – Wire Bond – Uprev	<u>wirebond uprev</u>
Route – Via Structure – Add	<u>add via structure</u>
Route – Via Structure – Replace	<u>replace via structure</u>
Route – Via Structure – Refresh	<u>refresh via structure</u>
Route – Offset Via Generator	<u>offset via gen</u>
Route – Flip-Chip Routing Estimation Layer	<u>layer estimation</u>
Route – Flip-Chip Die Escape Generator	<u>die escape gen</u>
Route – Wire Bond Via Estimation	<u>wire bond via estimation</u>
Route – Wire Bond Die Escape Generator	<u>wire bond escape</u>
Route – Routing Layer Assign	<u>assign route layer</u>
Route – Plating Layer Assign	<u>assign plating layer</u>
Route – Define Net Priority	<u>route priority</u>
Route – Route Feasibility	<u>route feasibility</u>
Route – Spider Router	<u>spider router</u>
Route – Custom Smooth	<u>custom smooth</u>
Route – Delay Tune	<u>delay tune</u>
Route – Define Short	<u>define shorting scheme</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Route – Create Short	<u>create short</u>
Route – ZRouter	<u>zrouter</u>
Route – Router – Route Radial	<u>radial router</u>
Route – Router – Fanout by Pick	<u>fanout by pick</u>
Route – Router – Route by Pick	<u>route by pick</u>
Route – Router – Elongation by Pick	<u>elong by pick</u>
Route – Router – Route Automatic	<u>auto route</u>
Route – Router – Router Checks	<u>specctra checks</u>
Route – Router – Interactive Editor	<u>specctra</u>
Route – Router – Miter by Pick	<u>miter by ppick</u>
Route – Router – Unmiter by Pick	<u>unmiter by pick</u>
Route – Router – Spread Clines	<u>spread clines</u>
Route – Add Fillet	<u>add fillet</u>
Route – Delete Fillet	<u>delete fillet</u>
Route – Gloss – Parameters	<u>gloss param</u>
Route – Gloss – Design	<u>gloss area design</u>
Route – Gloss – Room	<u>gloss area room</u>
Route – Gloss – Window	<u>gloss area window</u>
Route – Gloss – Highlight	No corresponding command
Route – Gloss – List	<u>gloss area list</u>
Analyze	
Analyze – Initialize	<u>signal init</u>
Analyze – Library	<u>signal library</u>
Analyze – Model Assignment	<u>signal model</u>
Analyze – Model Dump/Refresh	<u>signal model refresh</u>
Analyze – Preferences	<u>signal prefs</u>
Analyze – Audit – Design Audit	<u>signal audit</u>
Analyze – Audit – Net Audit	<u>signal audit net</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Analyze – Audit – Audit One Library	<u>signal lib audit</u>
Analyze – Audit – Audit List of Libraries	<u>signal libs audit</u>
Analyze – Probe	<u>signal probe</u>
Analyze – Xtalk Table	<u>signal xtalktable</u>
Analyze – EMI Rule Checker	<u>emcontrol</u>
Analyze – 3-D Package Model (In legacy products only)	<u>signal pkg model</u>
Manufacture	
Manufacture – Create Plating Bar	<u>pbar create</u>
Manufacture – Delete Plating Bar	<u>pbar delete</u>
Manufacture – Plating Bar Check	<u>pbar check</u>
Manufacture – Etch-back	<u>etchback</u>
Manufacture – Assembly Rule Checker	<u>assemrules standard</u>
Manufacture – Dimension/Draft commands in the Layout Editor are accessed under the Dimension menu item in the Symbol Editor	
Manufacture – Dimension/Draft – Parameters	<u>draft param</u>
Manufacture – Dimension/Draft – LineFont	<u>linefont</u>
Manufacture – Dimension/Draft – Linear Dim	<u>dimension linear</u>
Manufacture – Dimension/Draft – Datum Dim	<u>dimension datum</u>
Manufacture – Dimension/Draft – Angular Dim	<u>dimension angular</u>
Manufacture – Dimension/Draft – Leader Lines	<u>leader only</u>
Manufacture – Dimension/Draft – Diametral Leader	<u>leader diametral</u>
Manufacture – Dimension/Draft – Radial Leader	<u>leader radial</u>
Manufacture – Dimension/Draft – Balloon Leader	<u>leader balloon</u>
Manufacture – Dimension/Draft – Chamfer Leader	<u>leader chamfer</u>
Manufacture – Dimension/Draft – Chamfer	<u>draft chamfer</u>
Manufacture – Dimension/Draft – Fillet	<u>draft fillet</u>
Manufacture – Dimension/Draft – Create Detail	<u>create detail</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Manufacture – Stream Out	<u>stream out</u>
Manufacture – Artwork	<u>film param</u>
Manufacture – NC – Drill Customization	<u>ncdrill customization</u>
Manufacture – NC – Drill Legend	<u>ncdrill legend</u>
Manufacture – NC – NC Parameters	<u>ncdrill param</u>
Manufacture – NC – NC Drill	<u>nctape full</u>
Manufacture – NC – NC Route	<u>ncroute</u>
Manufacture – DFX Check (legacy)	<u>dfa</u>
Manufacture – Thieving	<u>thieving</u>
Manufacture – Shape Degassing	<u>degas</u>
Manufacture – Create Bond Finger Soldermask	<u>wirebond soldermask create</u>
Manufacture – Documentation – Bond Finger Text	<u>bpa</u>
Manufacture – Documentation – Display Pin Text	<u>dpn</u>
Manufacture – Documentation – Package Report – Sorted by Die Pin	<u>dbp report die</u>
Manufacture – Documentation – Package Report – Sorted by Bond Finger	<u>dbp report bondfinger</u>
Manufacture – Documentation – Package Report – Sorted by Package Pin	<u>dbp report package</u>
Manufacture – Documentation – Package Report – Sorted by Netname	<u>dbp report net</u>

Reports

Reports – Design Summary Report	<u>design summary report</u>
Reports – Net Delay Report	<u>net delay report</u>
Reports – Conductor Length Report	<u>cond length report</u>
Reports – Wire Bond Report	<u>wirebond reports</u>
Metal Usage Report	<u>metal usage report</u>
Reports – Reports	<u>reports</u>
Quick Reports	No corresponding command

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Reports – Component Compare	<u>compare comp</u>
Reports – Design Compare	<u>design compare</u>
Tools	
Tools – Create Module	<u>create module</u>
Tools – Padstack – Modify Design Padstack	<u>padeditdb</u>
Tools – Padstack – Modify Library Padstack	<u>padeditlib</u>
Tools – Padstack – Replace	<u>replace padstack</u>
Tools – Padstack – Group Edit	<u>multpadeit</u>
Tools – Padstack – Refresh	<u>refresh padstack</u>
Tools – Pad – Boundary	<u>editpad boundary</u>
Tools – Pad – Restore	<u>editpad restore</u>
Tools – Pad – Restore ALL	<u>editpad restore all</u>
Tools – Derive Connectivity	<u>derive connectivity</u>
Tools – Compose Line	<u>compose line</u>
Tools – Database Diary	<u>db diary</u>
Tools – Technology File Compare	<u>techfile compare</u>
Tools – Setup Advisor	<u>setup advisor</u>
Tools – Package Design Integrity	<u>package integrity</u>
Tools – Database Check	<u>drbdocto</u>
Tools – Update DRC	<u>drc update</u>
Tools – Utilities – Env Variables	<u>set</u>
Tools – Utilities – Aliases/Function Keys	<u>alias</u>
Tools – Utilities – Keyboard Commands	<u>helpcmd</u>
Tools – Utilities – Licenses Used	<u>license use</u>
Tools – Utilities – Stroke Editor	<u>stroke editor</u>
RF Module	
Edit RF Components	<u>rfedit</u>
Place RF Shape	<u>rfplace</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-5 SiP RF Layout Command Mapping

Re-Place Pcells	<u>rfreplace ripup</u>
Graphic Edit	<u>graphic edit</u>
Export chips & connectivity	<u>export chips</u>
RF Route – Create Route	<u>rfsip route</u>
Add Ruler	<u>add ruler</u>
Delete All Rulers	<u>delete all rulers</u>
Help	
Help – Documentation	cdsdoc
Help – Message Detail	<u>smi message detail</u>
Help – SiP Solution Overview	
Help – Web Resources – KP&S	Web URL
Help – Web Resources – cdnsUsers.org	Web URL
Help – Web Resources – Sourcelink	Web URL
Help – Web Resources – Web Collaboration	Web URL
Help – Web Resources – Education Services	Web URL
Help – About Cadence SiP Layout	<u>about</u>

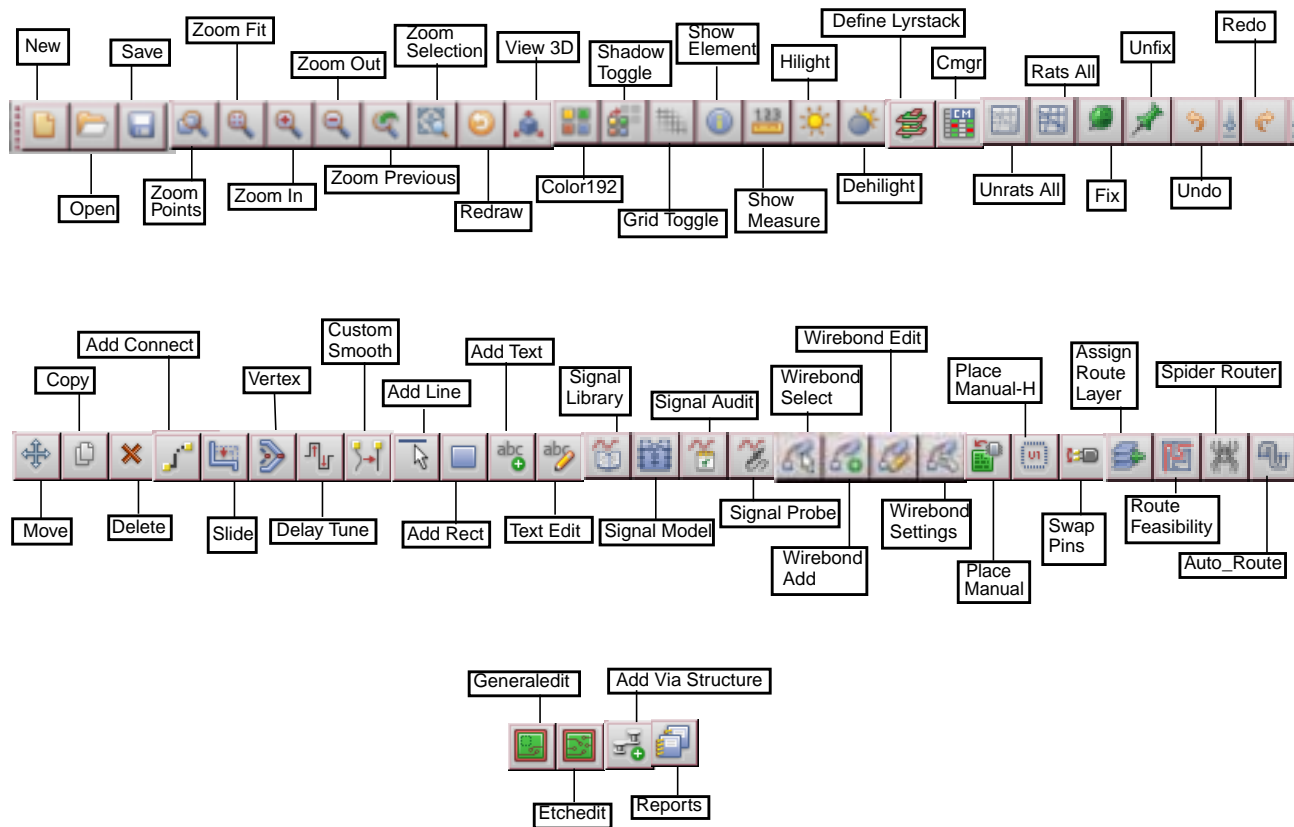
SiP Digital SI

The following diagram identifies the SiP Digital SI user interface toolbar icons, which execute the same console window commands corresponding to product menu choices. Your toolbar configuration may differ. You can also hover your cursor over each icon to display a datatip that identifies its function.

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Figure A-6 SiP Digital SI Toolbar Icons



The command mapping in Table A-6 lists the menu choices and corresponding commands for SiP Digital SI.

Table A-6 SiP Digital SI Command Mapping

Menu Choice	Console Window Command
File	
File – New	<u>new</u>
File – Open	<u>open</u>
File – Save	<u>save</u>
File – Save As	<u>save_as</u>
File – Create Symbol	<u>create_symbol</u> (in Symbol Editor only)

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-6 SiP Digital SI Command Mapping

File – Create Device	<u>create Device</u> (in Symbol Editor only)
File – Import – Netlist-In Wizard	<u>net list in</u>
File – Import – Logic	<u>netin param</u>
File – Import – MCM	<u>mcm import</u>
File – Import – Router	<u>specctra in</u>
File – Import – Sub-Drawing	<u>clppaste</u>
File – Import – Techfile	<u>techfile in</u>
File – Import – Active Times	<u>signal atimes</u>
File – Import – Pin Delay	<u>pin delay in</u>
File – Export – Logic	<u>feedback</u>
File – Export – Netlist w/Properties	<u>netout</u>
File – Export – MCM	<u>mcm export</u>
File – Export – Router	<u>specctra out</u>
File – Export – Sub-Drawing	<u>clpcopy</u>
File – Export – Libraries	<u>dlib</u>
File – Export – Techfile	<u>techfile out</u>
File – Export – Save Design to 16.1	<u>downrev</u>
File – Export – Pin Delay (SiP Layout only)	<u>pin delay out</u>
File – Viewlog	<u>viewlog</u>
File – File Viewer	No corresponding command
File – Plot Setup	<u>plot setup</u>
File – Plot	<u>plot</u>
File – Properties	<u>file property</u>
File – Change Editor	<u>toolswap</u>
File – Script	<u>script</u>
File – Recent Designs	<u>opencd</u>
File – Exit	<u>exit</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-6 SiP Digital SI Command Mapping

Edit

Edit – Undo	<u>undo</u>
Edit – Redo	<u>redo</u>
Edit – Move	<u>move</u>
Edit – Copy	<u>copy</u>
Edit – Mirror	<u>mirror</u>
Edit – Spin	<u>spin</u>
Edit – Change	<u>change</u>
Edit – Delete	<u>delete</u>
Edit – Z-Copy	<u>zcopy shape</u>
Edit – Vertex	<u>vertex</u>
Edit – Delete Vertex	<u>delete vertex</u>
Edit – Cline Change Width	<u>cline change width</u>
Edit – Text	<u>text edit</u>
Edit – Groups	<u>groupedit</u>
Edit – Properties	<u>property edit</u>
Edit – Net Properties	<u>net properties</u>

View

View – Zoom By Points	<u>zoom points</u>
View – Zoom Fit	<u>zoom fit</u>
View – Zoom In	<u>zoom in</u>
View – Zoom Out	<u>zoom out</u>
View – Zoom World	<u>zoom world</u>
View – Zoom Center	<u>zoom center</u>
View – Zoom Previous	<u>zoom previous</u>
View – Color View Save	<u>colorview create</u>
View – Color View Restore Last	<u>colorview restore</u>
View – 3D Model	<u>view 3d</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-6 SiP Digital SI Command Mapping

View – Redraw	<u>redisplay</u>
View – Windows – Command	No corresponding command
View – Windows – World View	No corresponding command
View – Windows – Options	No corresponding command
View – Windows – Find	No corresponding command
View – Windows – Visibility	No corresponding command
View – Windows – Show All	No corresponding command
View – Customize Toolbar	No corresponding command
View – Reset UI to Cadence Default	<u>reset_docwindows</u>
Add	
Add – Line	<u>add_line</u>
Add – Arc w/Radius	<u>add_rarc</u>
Add – 3pt Arc	<u>add_arc</u>
Add – Circle	<u>add_circle</u>
Add – Text	<u>add_text</u>
Display	
Display – Color/Visibility	<u>color</u>
Display – Layer Priority	<u>layer_priority</u>
Display – Status	<u>status</u>
Display – Element	<u>show_element</u>
Display – Measure	<u>show_measure</u>
Display – Constraint	<u>cns_show</u>
Display – Parasitic	<u>show_parasitic</u>
Display – Segments Over Voids	<u>highlight_sov</u>
Display – Property	<u>show_property</u>
Display – Assign Color	<u>assign_color</u>
Display – Highlight	<u>hilight</u>
Display – Dehighlight	<u>dehilight</u>

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Command Mapping

Table A-6 SiP Digital SI Command Mapping

Display – Waive DRCs – Waive	<u>waive drc</u>
Display – Waive DRCs – Show	<u>show waived drcs</u>
Display – Waive DRCs – Blank	<u>blank waived drcs</u>
Display – Waive DRCs – Restore	<u>restore waived drc</u>
Display – Waive DRCs – Restore All	<u>restore waived drcs</u>
Display – Pin Highlight	<u>pin highlight</u>
Display – Rats by Layer	<u>rats layer</u>
Display – Show Rat Lines – All	<u>rats all</u>
Display – Show Rat Lines – Components	<u>rats component</u>
Display – Show Rat Lines – Net	<u>rats net</u>
Display – Blank Rats – Of Selection	<u>rats blank</u>
Display – Blank Rat Lines – All	<u>unrats all</u>
Display – Blank Rat Lines – Components	<u>unrats component</u>
Display – Blank Rat Lines – Nets	<u>unrats net</u>
Setup	
Setup – Design Parameters	<u>prmed</u>
Setup – Grids	<u>define grid</u>
Setup – Subclasses	<u>define subclass</u>
Setup – Cross-section	<u>define lyrstack</u>
Setup – Materials	<u>define materials</u>
Setup – Application Modes – General Edit	<u>generaledit</u>
Setup – Application Modes – Etch Edit	<u>etchedit</u>
Setup – Application Modes – None	<u>noappmode</u>
Setup – Constraints – Modes	<u>cns cmmodes</u>
Setup – Constraints – Electrical	<u>cmgr elec</u>
Setup – Constraints – Physical	<u>cmgr phys</u>
Setup – Constraints – Spacing	<u>cmgr spac</u>
Setup – Constraints – Same Net Spacing	<u>cmgr snspac</u>

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Command Mapping

Table A-6 SiP Digital SI Command Mapping

Setup – Constraints – Physical Net Overrides	<u>property edit</u>
Setup – Constraints – Spacing Net Overrides	<u>property edit</u>
Setup – Constraints – Constraint Manager	<u>cmgr</u>
Setup – Property Definitions	<u>define property</u>
Setup – Define Lists	<u>define list</u>
Setup – User Preferences	<u>enved</u>
Layout	Layout menu choices are available only in the Symbol (Part) Editor
Layout – Pins	<u>add pin</u>
Layout – Pin RenNumbering	<u>rpn</u>
Layout – Connections	<u>add connect</u>
Layout – Slide	<u>slide</u>
Layout – Labels – RefDes	<u>label refdes</u>
Layout – Labels – Device	<u>label device</u>
Layout – Labels – Value	<u>label value</u>
Layout – Labels – Tolerance	<u>label tolerance</u>
Layout – Labels – Part Number	<u>label part</u>
Shape – Check	<u>shape check</u>
Shape – Compose Shape	<u>compose shape</u>
Shape – Decompose Shape	<u>decompose shape</u>
Shape – Global Dynamic Params	<u>shape global param</u>
Logic	
Logic – Auto Assign Pin Use	<u>auto assign pinuse</u>
Logic – Identify DC Nets	<u>identify nets</u>
Logic – Pin Type	<u>topology pinuse</u>
Logic – Define Terminators	<u>termination edit</u>
Logic – Package Terminators	<u>termination package</u>

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-6 SiP Digital SI Command Mapping

Logic – Terminator Assignment	<u>ecl_param</u>
Place	
Place – Manually	<u>place_manual</u>
Place – Interactive	<u>place_interactive</u>
Place – Swap –Pins	<u>swap_pins</u>
Place – Design Partition – Create Partitions	<u>partition</u>
Place – Design Partition – Workflow Manager	<u>workflow</u>
Place – Design Partition – Guideports	<u>guideport</u>
Place – Design Partition – Soft Net Assignment	<u>soft_net</u>
Route	
Route – Connect	<u>add_connect</u>
Route – Slide	<u>slide</u>
Route – Wire Bond – Select	<u>wirebond_select</u>
Route – Wire Bond – Add	<u>wirebond_add</u>
Route – Wire Bond – Edit	<u>wirebond_edit</u>
Route – Wire Bond – Modify	<u>wirebond_modify</u>
Route – Wire Bond – Settings	<u>wirebond_settings</u>
Route – Wire Bond – Purge Unused Groups	<u>wirebond_purge_groups</u>
Route – Wire Bond – Uprev	<u>wirebond_uprev</u>
Route – Via Structure – Add	<u>add_via_structure</u>
Route – Via Structure – Replace	<u>replace_via_structure</u>
Route – Via Structure – Refresh	<u>refresh_via_structure</u>
Route – Offset Via Generator	<u>offset_via_gen</u>
Route – Routing Layer Assign	<u>assign_route_layer</u>
Route – Define Net Priority	<u>route_priority</u>
Route – Route Feasibility	<u>route_feasibility</u>
Route – Spider Router	<u>spider_router</u>
Route – Custom Smooth	<u>custom_smooth</u>

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Command Mapping

Table A-6 SiP Digital SI Command Mapping

Route – Delay Tune	<u>delay tune</u>
Route – ZRouter	<u>zrouter</u>
Route – Router – Route Radial	<u>radial router</u>
Route – Router – Fanout by Pick	<u>fanout by pick</u>
Route – Router – Route by Pick	<u>route by pick</u>
Route – Router – Elongation by Pick	<u>elong by pick</u>
Route – Router – Route Automatic	<u>auto route</u>
Route – Router – Router Checks	<u>specctra checks</u>
Route – Router – Interactive Editor	<u>specctra</u>
Route – Router – Miter by Pick	<u>miter by ppick</u>
Route – Router – Unmiter by Pick	<u>unmiter by pick</u>
Analyze	
Analyze – Initialize	<u>signal init</u>
Analyze – Library	<u>signal library</u>
Analyze – Model Assignment	<u>signal model</u>
Analyze – Model Dump/Refresh	<u>signal model refresh</u>
Analyze – Preferences	<u>signal prefs</u>
Analyze – Audit – Design Audit	<u>signal audit</u>
Analyze – Audit – Net Audit	<u>signal audit net</u>
Analyze – Audit – Audit One Library	<u>signal lib audit</u>
Analyze – Audit – Audit List of Libraries	<u>signal libs audit</u>
Analyze – Probe	<u>signal probe</u>
Analyze – Xtalk Table	<u>signal xtalktable</u>
Analyze – EMI Rule Checker	<u>emcontrol</u>
Analyze – 3-D Modeling	<u>signal 3dmodel</u>
Analyze – Bus Setup	<u>signal bus setup</u>
Analyze – Bus Simulate	<u>signal bus sim</u>

Reports

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Command Mapping

Table A-6 SiP Digital SI Command Mapping

Reports – Design Summary Report	<u>design summary report</u>
Reports – Net Delay Report	<u>net delay report</u>
Reports – Conductor Length Report	<u>cond length report</u>
Reports – Reports	<u>reports</u>
Reports – Quick Reports	No corresponding command
Reports – Design Compare	<u>design compare</u>
Tools	
Tools – Compose Line	<u>compose line</u>
Tools – Topology Editor	<u>sigxp</u>
Tools – Model Integrity	<u>model integrity</u>
Tools – Technology File Compare	<u>techfile compare</u>
Tools – Setup Advisor	<u>setup advisor</u>
Tools – Package Design Integrity	<u>package integrity</u>
Tools – Database Check	<u>drbdocto</u>
Tools – Update DRC	<u>drc update</u>
Tools – Utilities – Env Variables	<u>set</u>
Tools – Utilities – Aliases/Function Keys	<u>alias</u>
Tools – Utilities – Keyboard Commands	<u>helpcmd</u>
Tools – Utilities – Licenses Used	<u>license use</u>
Tools – Utilities – Stroke Editor	<u>stroke editor</u>
Help	
Help – Documentation	<u>cdsdoc</u>
Help – Message Detail	<u>smi message detail</u>
Help – SiP Solution Overview	
Help – Web Resources – KP&S	Web URL
Help – Web Resources – cdnUsers.org	Web URL
Help – Web Resources – Sourcelink	Web URL
Help – Web Resources – Web Collaboration	Web URL

Allegro PCB and Package Physical Layout Command Reference

Command Mapping

Table A-6 SiP Digital SI Command Mapping

Help – Web Resources – Education Services	Web URL
Help – About Cadence SiP SI	<u>about</u>
