PCI Trace Routing Guidelines
Parameter

Length matching between single ended signals

Transfer Rate @ 33MHz

Maximum data and control signal length allowance for the COM Express Carrier Board.	10 inches
Maximum clock signal length allowance for the COM Express Carrier Board.	8.88 inches
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between signals (inter-signal) (S)	7mils (microstrip routing) (*)

Trace Routing

132 MB/sec

Max. 200mils

Length matching between clock signals Max 200mils Min. 40mils Spacing from edge of plane Reference plane GND referenced preferred Try to minimize number of vias Via Usage Decoupling capacitors for each PCI slot. Min. 1x22µF, 2x 100nF @ VCC 5V Min. 2x22uF, 4x 100nF @ VCC 3.3V Min. 1x22µF, 2x 100nF @ +12V (if used) Min. 1x22µF, 2x 100nF @ -12V (if used) The decoupling capacitors for the power rails should be placed as close as possible to the slot power pins, connected with wide traces.