PCI Express 1.1 Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate / PCIe Lane	2.5 GBit/s
Maximum signal line length (coupled traces)	TX and RX path: 21.0 inches
Signal length allowance on the COM Express Carrier Board	TX and RX path: 15.85 inches @ 0.28dB/GHz/inch to PCIe device 9.00 inches @ 0.28dB/GHz/inch to PCIe slot
Differential Impedance	92 Ω +/-10% (covers Gen1 100 Ω +/-20% and Gen2 85 Ω +/-20% requirements)
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	4 mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.