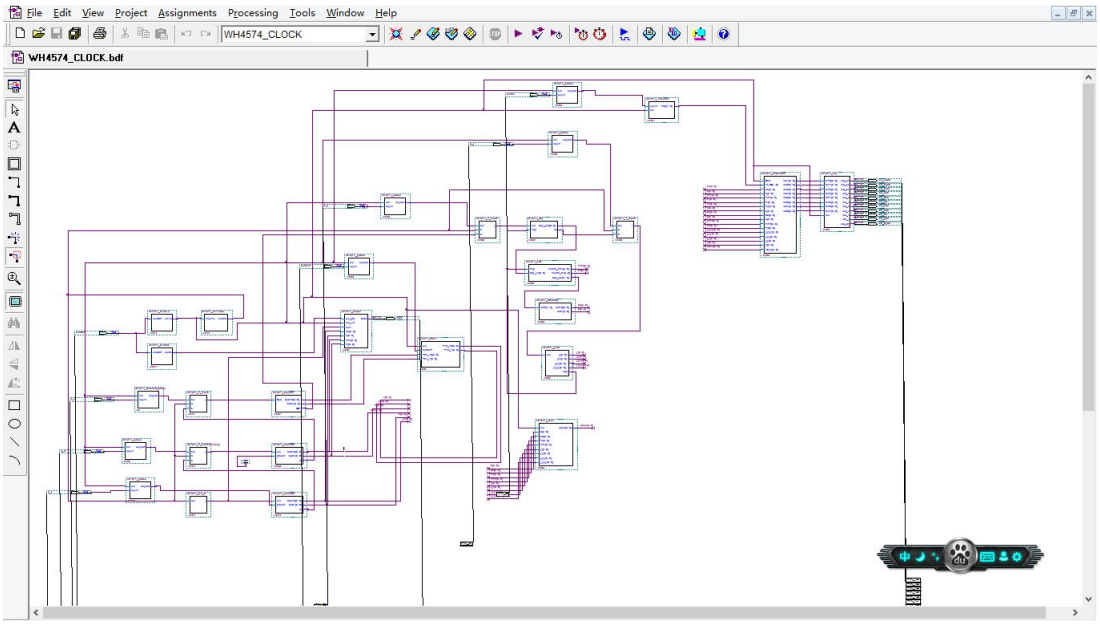
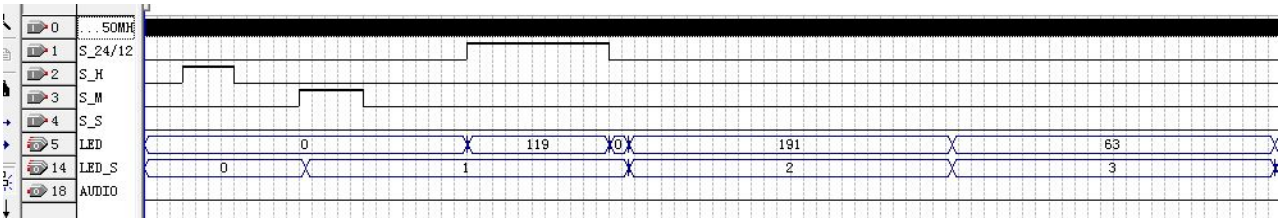
附录

一、12/24 小时数字时钟 VHDL 设计

1，系统顶层逻辑图：



时序仿真波形

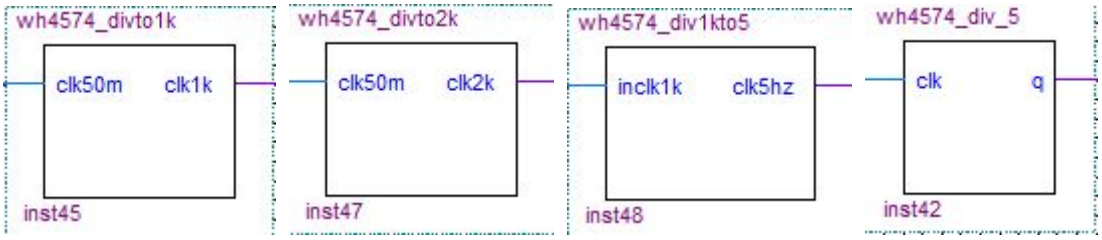


管脚定义以及锁定

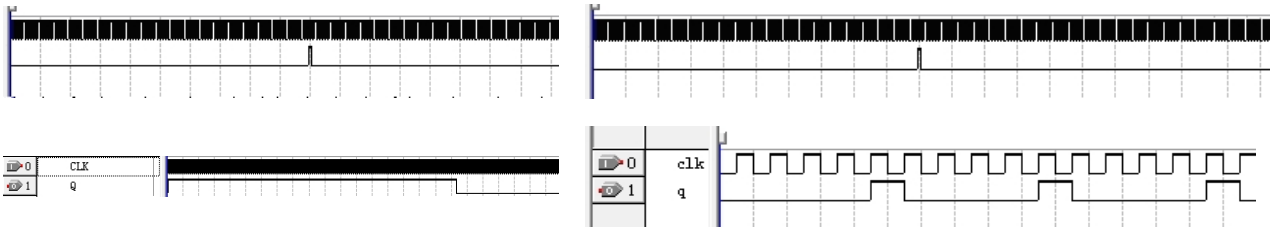
	Node Name	Direction	Location	I/O Bank
1	buzz	Output	PIN_112	7
2	clk50m	Input	PIN_22	1
3	led_a32	Output	PIN_129	8
4	led_b33	Output	PIN_128	8
5	led_c34	Output	PIN_127	7
6	led_d35	Output	PIN_126	7
7	led_dp39	Output	PIN_120	7
8	led_e36	Output	PIN_125	7
9	led_f37	Output	PIN_124	7
10	led_g38	Output	PIN_121	7
11	led_sa29	Output	PIN_132	8
12	led_sb30	Output	PIN_133	8
13	led_sc31	Output	PIN_135	8
14	s_d	Input	PIN_25	2
15	s_h	Input	PIN_91	6
16	s_m	Input	PIN_90	6
17	s_s	Input	PIN_89	5
18	s_y	Input	PIN_24	2
19	switch	Input	PIN_88	5
20	switchP	Input	PIN_23	1
21	<<new node>>			

2，分频模块。

①各个分频模块的模块图：



②，分别对应的仿真波形：



③50mhz 分频至 1k 模块代码：

```
library ieee;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_1164.all;
entity wh4574_divto1k is
 port(clk50m:in std_logic;
        clk1k:out std_logic);
end wh4574_divto1k;
architecture behav of wh4574_divto1k is
 signal count1:std_logic_vector(14 downto
0);
 signal count2:std_logic;
 signal co:std_logic;
          begin
  process(clk50m)
    begin
    if clk50m'event and clk50m='1' then
     if count1="110000110100111" then
          count1<="000000000000000";
          co<='1';
          else
          count1<=count1+'1';
          co<='0';
     end if;
    end if;
  end process;
   process(co)
     begin
     if co'event and co='1' then
      count2<=not count2;
     end if;
   end process;
   clk1k<=count2;
end behav;
```

50mhz 分频至 2k 模块代码：

```
library ieee;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_1164.all;
entity wh4574_divto2k is
 port(clk50m:in std_logic;
        clk2k:out std_logic);
end wh4574_divto2k;
architecture behav of wh4574_divto2k is
 signal count1:std_logic_vector(13 downto
0);
 signal count2:std_logic;
 signal co:std_logic;
          begin
  process(clk50m)
```

```
    begin
    if clk50m'event and clk50m='1' then
     if count1="11000011010011" then
         count1<="00000000000000";
         co<='1';
         else
         count1<=count1+'1';
         co<='0';
      end if;
    end if;
  end process;
    process(co)
       begin
       if co'event and co='1' then
        count2<=not count2;
       end if;
    end process;
    clk2k<=count2;
end behav;
```

1k 分频至 5hz 代码：

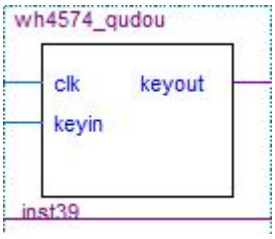
```
library ieee;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_1164.all;
entity wh4574_div1kto5 is
 port(inclk1k:in std_logic;
        clk5hz:out std_logic);
end wh4574_div1kto5;
architecture behav of wh4574_div1kto5 is
 signal count1:std_logic_vector(6 downto
0);
 signal count2:std_logic;
 signal co:std_logic;
          begin
  process(inclk1k)
    begin
    if inclk1k'event and inclk1k='1' then
     if count1="1100011" then
         count1<="0000000";
         co<='1';
         else
         count1<=count1+'1';
         co<='0';
      end if;
    end if;
  end process;
    process(co)
       begin
       if co'event and co='1' then
        count2<=not count2;
       end if;
    end process;
    clk5hz<=count2;
end behav;
```

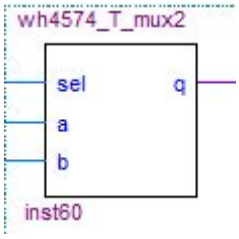
5 分频代码：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_div_5 is
 port(clk:in std_logic;
        q:out std_logic);
end wh4574_div_5;
architecture behav of wh4574_div_5 is
 signal count:std_logic_vector(2 downto 0);
 begin
 process(clk)
  begin
   if clk'event and clk='1' then
    if count="100"then
         count<="000";
         q<='1';
    else
         count<=count+1;
         q<='0';
    end if;
   end if;
  end process;
 end behav;
```

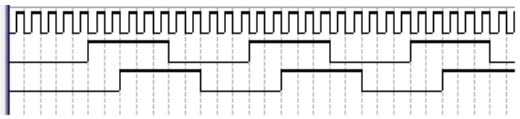
3，按键去抖动模块，二选一模块。

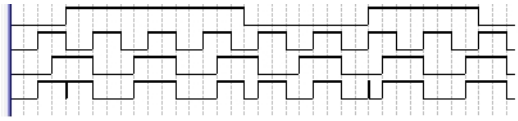
① 模块图：





② 时序仿真波形依次为：





③ 源代码：

按键去抖动：

```
library ieee;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_1164.all;
entity wh4574_qudou is
 port(clk,keyin :in std_logic;
        keyout:out std_logic);
end wh4574_qudou;
architecture behav of wh4574_qu
dou is
  begin
   process(clk)
   variable count1,count2:std_logic
_vector(3 downto 0);
    begin
    if clk'event and clk='1' then
     if keyin='0' then
       if count1="0101" then
          keyout<='0';
       else count1:=count1+1;
       end if;

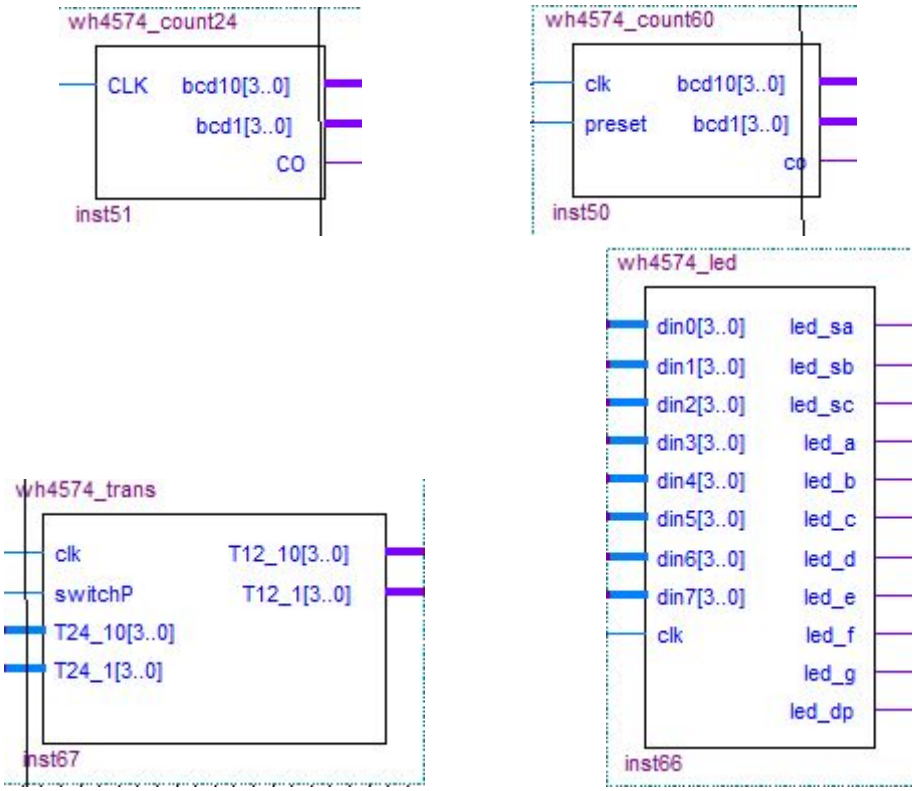
     elsif keyin='1' then
         if count2="0101" then
          keyout<='1';
         else count2:=count2+1;
       end if;
       end if;
       end if;
       end process;
       end behav;
```

二选一数选器：

```
library ieee;
use ieee.std_logic_1164.all;
entity wh4574_T_mux2 is
port(sel,a,b:in std_logic;
          q:out std_logic);
end wh4574_T_mux2;
architecture bav of wh4574_T_mux2 is
begin
 process(sel,a,b)
  begin
   if sel='1' then
    q<=a;
   else
    q<=b;
   end if;
  end process;
end bav;
```

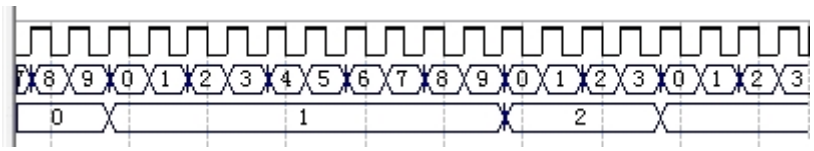
4，24,60 进制计数器模块，24 小时转 12 小时模块，动态译码显示模块。

① 模块图：

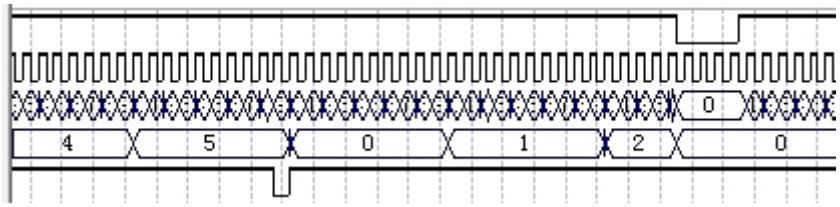


② 时序仿真波形图。

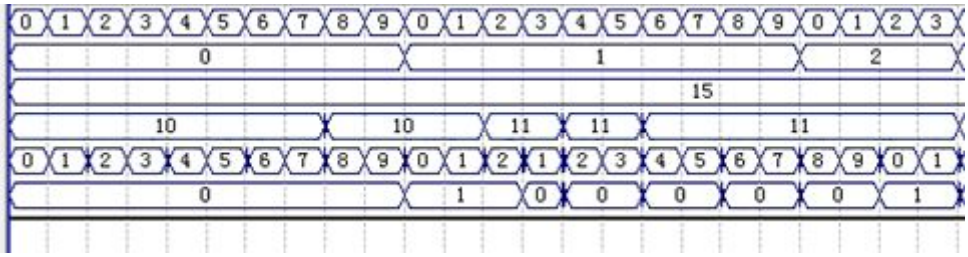
24 进制计数波形：



60 进制仿真波形：



24 小时制转 12 小时制：



③ ，程序源代码.

24 进制计数器：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity wh4574_count24 is
port(CLK:in std_logic;
     bcd10,bcd1:buffer std_logic_vector(3
downto 0);
     CO:OUT STD_LOGIC);
end wh4574_count24;

architecture behav of wh4574_count24 is
 begin
   process(CLK,bcd10)
   begin
     if CLK'EVENT AND CLK='1' THEN
      if bcd10="0010"and bcd1="0011" th
en
        bcd1<="0000";
        CO<='1';
      elsif bcd1="1001" then
          bcd1<="0000";
          CO<='0';
      else
        bcd1<=bcd1+'1';
        CO<='0';
      end if;
     end if;
   end process;

   process(CLK,bcd1)
    begin
     if CLK'event and CLK='1' then
      if bcd1="0011"and bcd10="0010" th
en
        bcd10<="0000";
      elsif bcd1="1001" then
        bcd10<=bcd10+'1';
      end if;
     end if;
   end process;
   end behav;
```

60 进制：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_count60 is
port(clk:in std_logic;
     bcd10,bcd1:buffer std_logic_vector(3
downto 0);
     preset:in std_logic;
     co:out std_logic);
end wh4574_count60;
architecture rtl of wh4574_count60 is
signal co_1:std_logic;
 begin
  process(clk,preset)
   begin
    if preset='0' then
     bcd1<="0000";
    else
     if clk='1'and clk'event then
      if bcd1="1001" then
       bcd1<="0000";
      else
       bcd1<=bcd1+'1';
      end if;
     end if;
    end if;
   end process;
  process(clk,preset,bcd1)
   begin
    if preset='0' then
     bcd10<="0000";
     co_1<='0';
    else
     if clk='1'and clk'event then
      if bcd1="1000"and bcd10="0101" th
en
        co_1<='1';
       elsif bcd1="1001"and bcd10="0101"
 then
        bcd10<="0000";
```

```
          co_1<='0';
         elsif bcd1="1001" then
          bcd10<=bcd10+'1';
          co_1<='0';
         end if;
        end if;
       end if;
     end process;
     co<=not co_1;
     end rtl;
```

24 转换 12

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_trans is
   port(clk:in std_logic;
          switchP:in std_logic;
          T24_10,T24_1:in std_logic_vector(3
downto 0);
          T12_10,T12_1:buffer std_logic_vect
or(3 downto 0));
end wh4574_trans;
architecture behav of wh4574_trans is
 begin
    process(T24_10,T24_1)
       begin

        case switchP&T24_10&T24_1 is
         when "100000000"=>T12_10<="000
0";T12_1<="0000";
         when "100000001"=>T12_10<="000
0";T12_1<="0001";
         when "100000010"=>T12_10<="000
0";T12_1<="0010";
         when "100000011"=>T12_10<="000
0";T12_1<="0011";
         when "100000100"=>T12_10<="000
0";T12_1<="0100";
         when "100000101"=>T12_10<="000
0";T12_1<="0101";
         when "100000110"=>T12_10<="000
0";T12_1<="0110";
         when "100000111"=>T12_10<="000
0";T12_1<="0111";
         when "100001000"=>T12_10<="000
0";T12_1<="1000";
         when "100001001"=>T12_10<="000
0";T12_1<="1001";
         when "100010000"=>T12_10<="000
1";T12_1<="0000";
         when "100010001"=>T12_10<="000
1";T12_1<="0001";
         when "100010010"=>T12_10<="000
0";T12_1<="0000";
         when "100010011"=>T12_10<="000
0";T12_1<="0001";
         when "100010100"=>T12_10<="000
0";T12_1<="0010";
         when "100010101"=>T12_10<="000
0";T12_1<="0011";
         when "100010110"=>T12_10<="000
0";T12_1<="0100";
         when "100010111"=>T12_10<="000
0";T12_1<="0101";
         when "100011000"=>T12_10<="000
0";T12_1<="0110";
         when "100011001"=>T12_10<="000
0";T12_1<="0111";
         when "100100000"=>T12_10<="000
0";T12_1<="1000";
         when "100100001"=>T12_10<="000
0";T12_1<="1001";
         when "100100010"=>T12_10<="000
1";T12_1<="0000";
         when "100100011"=>T12_10<="000
1";T12_1<="0001";
         when "100100100"=>T12_10<="000
0";T12_1<="0000";
         when "000000000"=>T12_10<="000
0";T12_1<="0000";
         when "000000001"=>T12_10<="000
0";T12_1<="0001";
         when "000000010"=>T12_10<="000
0";T12_1<="0010";
         when "000000011"=>T12_10<="000
0";T12_1<="0011";
         when "000000100"=>T12_10<="000
```

```
0";T12_1<="0100";
        when "000000101"=>T12_10<="000
0";T12_1<="0101";
        when "000000110"=>T12_10<="000
0";T12_1<="0110";
        when "000000111"=>T12_10<="000
0";T12_1<="0111";
        when "000001000"=>T12_10<="000
0";T12_1<="1000";
        when "000001001"=>T12_10<="000
0";T12_1<="1001";
        when "000010000"=>T12_10<="000
1";T12_1<="0000";
        when "000010001"=>T12_10<="000
1";T12_1<="0001";
        when "000010010"=>T12_10<="000
1";T12_1<="0010";
        when "000010011"=>T12_10<="000
1";T12_1<="0011";
        when "000010100"=>T12_10<="000
1";T12_1<="0100";
        when "000010101"=>T12_10<="000
1";T12_1<="0101";
        when "000010110"=>T12_10<="000
1";T12_1<="0110";
        when "000010111"=>T12_10<="000
1";T12_1<="0111";
        when "000011000"=>T12_10<="000
1";T12_1<="1000";
        when "000011001"=>T12_10<="000
1";T12_1<="1001";
        when "000100000"=>T12_10<="001
0";T12_1<="0000";
        when "000100001"=>T12_10<="001
0";T12_1<="0001";
        when "000100010"=>T12_10<="001
0";T12_1<="0010";
        when "000100011"=>T12_10<="001
0";T12_1<="0011";
        when "000100100"=>T12_10<="001
0";T12_1<="0100";
        when others=>T12_10<="ZZZZ";T12
_1<="ZZZZ";
      end case;
    end process;
  end behav;
```

动态译码显示模块

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_led is
port(din0,din1,din2,din3,din4,din5,din6,din7:i
n std_logic_vector(3 downto 0);
      clk:in std_logic;
      led_sa,led_sb,led_sc:out std_logic;
      led_a,led_b,led_c,led_d,led_e,led_f,led
_g,led_dp:out std_logic);
 end entity;

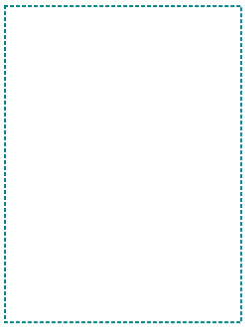
 architecture behav of wh4574_led is
 signal seg:std_logic_vector(6 downto 0);
 signal sel:std_logic_vector( 2 downto 0);
 signal num:std_logic_vector(3 downto 0);
 signal s:std_logic_vector(2 downto 0);
 begin
 led_sa<=sel(0);
 led_sb<=sel(1);
 led_sc<=sel(2);
 led_a<=seg(0);
 led_b<=seg(1);
 led_c<=seg(2);
 led_d<=seg(3);
 led_e<=seg(4);
 led_f<=seg(5);
 led_g<=seg(6);
 process(clk)
begin
if rising_edge(clk) then
 if s="111" then
     s<="000";
     else s<=s+'1';
 end if;
 end if;
 end process;
 process(s,din0,din1,din2,din3,din4,din5,din6,
din7)
```

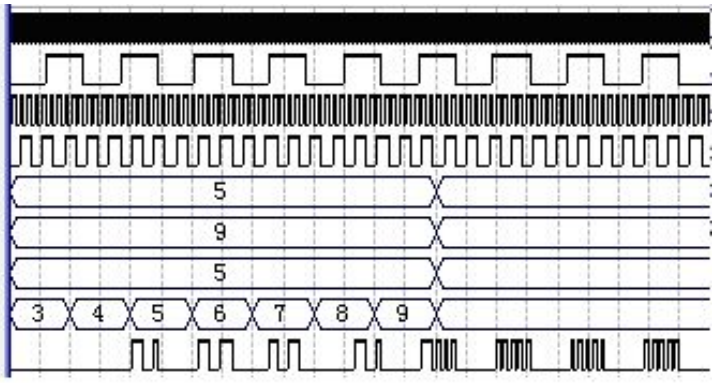
```
begin
if s="000" then
sel<="000";
num<=din0;
led_dp<='0';
elsif s="001" then
sel<="001" ;num<=din1;
led_dp<='0';
elsif s="010" then
sel<="010" ;num<=din2;
led_dp<='1';
elsif s="011" then
sel<="011" ;num<=din3;
led_dp<='0';
elsif s="100" then
sel<="100" ;num<=din4;
led_dp<='1';
elsif s="101" then
sel<="101" ;num<=din5;
led_dp<='0';
elsif s="110" then
sel<="110";num<=din6;
led_dp<='0';
else
sel<="111";num<=din7;
led_dp<='0';
end if;
end process;

seg<="0111111" when num=0 else
      "0000110" when num=1 else
      "1011011" when num=2 else
      "1001111" when num=3 else
      "1100110" when num=4 else
      "1101101" when num=5 else
      "1111101" when num=6 else
      "0000111" when num=7 else
      "1111111" when num=8 else
      "1101111" when num=9 else
      "1110111" when num=10 else
      "1111100" when num=11 else
      "0111001" when num=12 else
      "1011110" when num=13 else
      "ZZZZZZZ" when num=14 else
      "1110001" when num=15 else
      "ZZZZZZZ";
end behav;
```

5，整点报时模块：

①，模块图：②，时序仿真波形





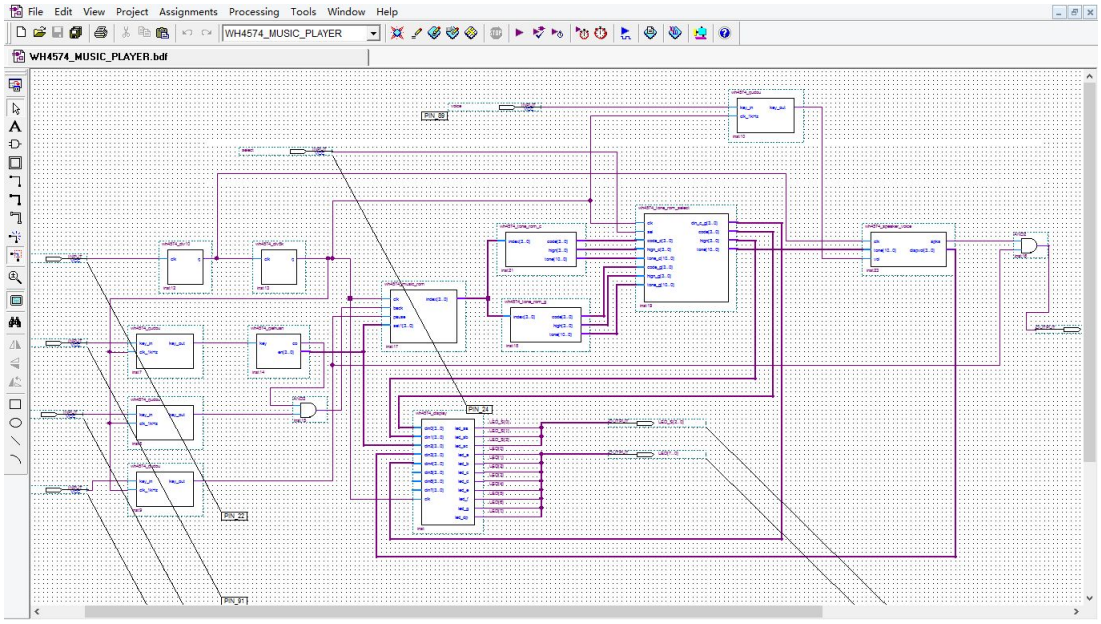
③，源代码：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_chuck is
   port(clk_2K,clk_1K,clk1:in std_logic;
        ss,s,mm,m:in std_logic_vector(3 do
wnto 0);
        buzz:out std_logic);
end wh4574_chuck;
architecture behav of wh4574_chuck is
signal buzz_1:std_logic;
   begin
process(ss,s,mm,m,clk_2K,clk_1K,clk1)
 begin
    if (mm="0101" and m="1001") and (ss
="0101") and (s>4) and (s<=9) then

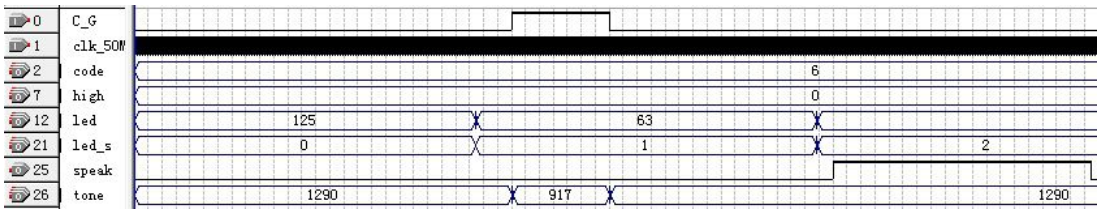
          if clk1='1' then
              buzz_1<=clk_1K;
          else
              buzz_1<='Z';
          end if;
    elsif (mm="0000" and m="0000") and
(ss="0000") and (s="0000") then
          if clk1='1' then
              buzz_1<=clk_2K;
          else
              buzz_1<='Z';
          end if;
    else
       buzz_1<='Z';
    end if;
   buzz<=buzz_1;
 end process;
end behav;
```

二 乐曲播放电路设计

1 电路系统逻辑顶层图：



时序仿真波形：

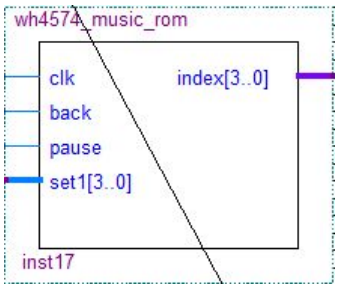


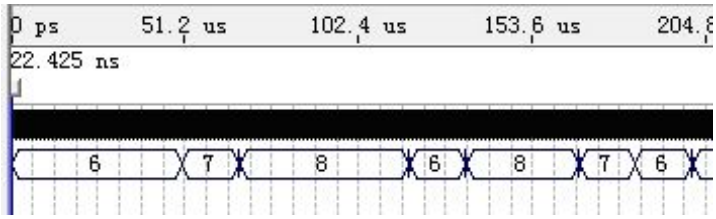
管脚定义锁定表：

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	C_G	Input	PIN_23	1	B1_N0	2.5 V (default)	
2	clk_50MHz	Input	PIN_22	1	B1_N0	2.5 V (default)	
3	led[0]	Output	PIN_129	8	B8_N0	2.5 V (default)	
4	led[1]	Output	PIN_128	8	B8_N0	2.5 V (default)	
5	led[2]	Output	PIN_127	7	B7_N0	2.5 V (default)	
6	led[3]	Output	PIN_126	7	B7_N0	2.5 V (default)	
7	led[4]	Output	PIN_125	7	B7_N0	2.5 V (default)	
8	led[5]	Output	PIN_124	7	B7_N0	2.5 V (default)	
9	led[6]	Output	PIN_121	7	B7_N0	2.5 V (default)	
10	led[7]	Output	PIN_120	7	B7_N0	2.5 V (default)	
11	led_s[0]	Output	PIN_132	8	B8_N0	2.5 V (default)	
12	led_s[1]	Output	PIN_133	8	B8_N0	2.5 V (default)	
13	led_s[2]	Output	PIN_135	8	B8_N0	2.5 V (default)	
14	speak	Output	PIN_112	7	B7_N0	2.5 V (default)	

2 乐曲节拍发生器模块：

①，模块图及时序仿真波形：





②，程序源代码：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;
entity wh4574_music_rom is
  port(clk,back,pause: in std_logic;
       index: out std_logic_vector(3 downto 0);
       set1: in std_logic_vector(3 downto 0));
end wh4574_music_rom;
architecture behav of wh4574_music_rom is
  subtype word is integer range 0 to 15;
  type memory is array(0 to 523) of word;
  signal rom: memory;
  signal clk_cnt: integer range 0 to 249;
  signal clk_4Hz: std_logic;
  signal adr: integer range 0 to 523;
  begin
divide: process(clk)
          begin
            if (clk'event and clk ='1') then
                if clk_cnt=249 then

clk_cnt<=0;clk_4Hz<='1';
                else

clk_cnt<=clk_cnt+1;clk_4Hz<='0';
                end if;
              end if;
          end process;
cnt:process(clk_4Hz,back,pause)
       begin
          if pause='1' then
                if adr=523 then
                    adr<=0;
                elsif (back='0') then
                     adr<=0;
                elsif (clk_4Hz'event and clk_4Hz='1'and back='1') then
                     adr<=adr+1;
                     end if;
                     else
                     null;
                     end if;
          end process;

  music:process(set1)
begin
   if set1="0011" then
index<=conv_std_logic_vector(rom(adr),4);
rom(0)<=0;rom(1)<=0;rom(2)<=0;rom(3)<=5;
rom(4)<=8;rom(5)<=5;rom(6)<=8;rom(7)<=9;
rom(8)<=11;rom(9)<=11;rom(10)<=10;rom(11)
<=9;
rom(12)<=9;rom(13)<=10;rom(14)<=10;rom(1
5)<=0;
rom(16)<=0;rom(17)<=0;rom(18)<=0;rom(19)
<=5;
rom(20)<=8;rom(21)<=5;rom(22)<=8;rom(23)
<=9;
rom(24)<=11;rom(25)<=11;rom(26)<=10;rom(
27)<=9;
rom(28)<=9;rom(29)<=10;rom(30)<=9;rom(31)
<=8;
rom(32)<=8;rom(33)<=8;rom(34)<=0;rom(35)
<=0;
```

rom(36)<=0;rom(37)<=5;rom(38)<=8;rom(39)<=9;
rom(40)<=11;rom(41)<=11;rom(42)<=9;rom(43)<=8;
rom(44)<=8;rom(45)<=6;rom(46)<=6;rom(47)<=5;
rom(48)<=5;rom(49)<=5;rom(50)<=5;rom(51)<=5;
rom(52)<=0;rom(53)<=0;rom(54)<=0;rom(55)<=0;
rom(56)<=0;rom(57)<=0;rom(58)<=0;rom(59)<=5;
rom(60)<=8;rom(61)<=5;rom(62)<=8;rom(63)<=9;
rom(64)<=11;rom(65)<=11;rom(66)<=10;rom(67)<=9;
rom(68)<=9;rom(69)<=10;rom(70)<=10;rom(71)<=0;
rom(72)<=0;rom(73)<=0;rom(74)<=0;rom(75)<=5;
rom(76)<=8;rom(77)<=5;rom(78)<=8;rom(79)<=9;
rom(80)<=11;rom(81)<=11;rom(82)<=10;rom(83)<=9;
rom(84)<=9;rom(85)<=10;rom(86)<=9;rom(87)<=8;
rom(88)<=8;rom(89)<=8;rom(90)<=0;rom(91)<=13;
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rom(104)<=8;rom(105)<=8;rom(106)<=8;rom(107)<=8;
rom(108)<=9;rom(109)<=10;rom(110)<=10;rom(111)<=9;
rom(112)<=9;rom(113)<=9;rom(114)<=9;rom(115)<=9;
rom(116)<=0;rom(117)<=7;rom(118)<=8;rom(119)<=7;
rom(120)<=6;rom(121)<=6;rom(122)<=6;rom(123)<=12;
rom(124)<=12;rom(125)<=12;rom(126)<=13;rom(127)<=13;
rom(128)<=12;rom(129)<=12;rom(130)<=11;rom(131)<=11;
rom(132)<=10;rom(133)<=10;rom(134)<=10;rom(135)<=10;
rom(136)<=11;rom(137)<=10;rom(138)<=11;rom(139)<=11;
rom(140)<=8;rom(141)<=8;rom(142)<=8;rom(143)<=8;
rom(148)<=9;rom(149)<=10;rom(150)<=10;rom(151)<=10;
rom(152)<=10;rom(153)<=10;rom(154)<=0;rom(155)<=7;
rom(156)<=8;rom(157)<=7;rom(158)<=6;rom(159)<=6;
rom(160)<=6;rom(161)<=8;rom(162)<=8;rom(163)<=8;
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rom(412)<=0;rom(413)<=0;rom(414)<=0;rom(
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rom(420)<=0;rom(421)<=0;rom(422)<=0;rom(
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rom(424)<=0;rom(425)<=0;rom(426)<=0;rom(
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rom(428)<=0;rom(429)<=0;rom(430)<=0;rom(
431)<=0;
rom(432)<=0;rom(433)<=0;rom(434)<=0;rom(
435)<=0;
rom(436)<=0;rom(437)<=0;rom(438)<=0;rom(
439)<=0;
rom(440)<=0;rom(441)<=0;rom(442)<=0;rom(
443)<=0;
rom(444)<=0;rom(445)<=0;rom(446)<=0;rom(
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rom(448)<=0;rom(449)<=0;rom(450)<=0;rom(
451)<=0;
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rom(468)<=0;rom(469)<=0;rom(470)<=0;rom(
471)<=0;

   elsif set1="0001" then
index<=conv_std_logic_vector(rom(adr),4);
rom(0)<=8;rom(1)<=8;rom(2)<=7;rom(3)<=8;
rom(4)<=12;rom(5)<=12;rom(6)<=12;rom(7)<
=12;
rom(8)<=8;rom(9)<=8;rom(10)<=7;rom(11)<=
8;
rom(12)<=10;rom(13)<=10;rom(14)<=10;rom(
15)<=10;
rom(16)<=8;rom(17)<=8;rom(18)<=7;rom(19)
<=8;
rom(20)<=5;rom(21)<=5;rom(22)<=10;rom(23)
<=10;
rom(24)<=9;rom(25)<=6;rom(26)<=7;rom(27)
<=8;
rom(28)<=9;rom(29)<=9;rom(30)<=9;rom(31)
<=9;
rom(32)<=8;rom(33)<=8;rom(34)<=7;rom(35)
<=8;
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rom(40)<=13;rom(41)<=13;rom(42)<=14;rom(
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rom(44)<=10;rom(45)<=10;rom(46)<=10;rom(
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rom(48)<=13;rom(49)<=13;rom(50)<=14;rom(
51)<=15;
rom(52)<=12;rom(53)<=12;rom(54)<=10;rom(
55)<=10;
rom(56)<=11;rom(57)<=10;rom(58)<=6;rom(5
9)<=9;
rom(60)<=8;rom(61)<=8;rom(62)<=8;rom(63)
<=8;
rom(64)<=8;rom(65)<=8;rom(66)<=7;rom(67)
<=8;
rom(68)<=12;rom(69)<=12;rom(70)<=12;rom(
71)<=12;
rom(72)<=8;rom(73)<=8;rom(74)<=7;rom(75)
<=8;
rom(76)<=10;rom(77)<=10;rom(78)<=10;rom(
79)<=10;
rom(80)<=8;rom(81)<=8;rom(82)<=7;rom(83)
<=8;
rom(84)<=5;rom(85)<=5;rom(86)<=10;rom(87)
<=10;
rom(88)<=9;rom(89)<=6;rom(90)<=7;rom(91)
<=8;
```

rom(92)<=9;rom(93)<=9;rom(94)<=9;rom(95)<=9;
rom(96)<=8;rom(97)<=8;rom(98)<=7;rom(99)<=8;
rom(100)<=12;rom(101)<=12;rom(102)<=12;rom(103)<=12;
rom(104)<=13;rom(105)<=13;rom(106)<=14;rom(107)<=15;
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rom(252)<=9;rom(253)<=9;rom(254)<=15;rom(255)<=15;
rom(256)<=14;rom(257)<=14;rom(258)<=12;rom(259)<=12;
rom(260)<=8;rom(261)<=8;rom(262)<=7;rom(263)<=8;
rom(264)<=12;rom(265)<=12;rom(266)<=12;rom(267)<=12;

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rom(276)<=8;rom(277)<=8;rom(278)<=7;rom(279)<=8;
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rom(292)<=8;rom(293)<=8;rom(294)<=7;rom(295)<=8;
rom(296)<=12;rom(297)<=12;rom(298)<=12;rom(299)<=12;
rom(300)<=13;rom(301)<=13;rom(302)<=14;rom(303)<=15;
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rom(336)<=8;rom(337)<=8;rom(338)<=8;rom(339)<=8;
rom(340)<=13;rom(341)<=13;rom(342)<=14;rom(343)<=15;
rom(344)<=15;rom(345)<=15;rom(346)<=15;rom(347)<=10;
rom(348)<=11;rom(349)<=10;rom(350)<=6;rom(351)<=9;
rom(352)<=9;rom(353)<=9;rom(354)<=8;rom(355)<=8;
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rom(364)<=0;rom(365)<=0;rom(366)<=0;rom(367)<=0;
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rom(380)<=0;rom(381)<=0;rom(382)<=0;rom(383)<=0;
rom(384)<=0;rom(385)<=0;rom(386)<=0;rom(387)<=0;
rom(388)<=0;rom(389)<=0;rom(390)<=0;rom(391)<=0;
rom(392)<=0;rom(393)<=0;rom(394)<=0;rom(395)<=0;
rom(396)<=0;rom(397)<=0;rom(398)<=0;rom(399)<=0;
rom(400)<=0;rom(401)<=0;rom(402)<=0;rom(403)<=0;
rom(404)<=0;rom(405)<=0;rom(406)<=0;rom(407)<=0;
rom(408)<=0;rom(409)<=0;rom(410)<=0;rom(411)<=0;
rom(412)<=0;rom(413)<=0;rom(414)<=0;rom(415)<=0;
rom(416)<=0;rom(417)<=0;rom(418)<=0;rom(419)<=0;
rom(420)<=0;rom(421)<=0;rom(422)<=0;rom(423)<=0;
rom(424)<=0;rom(425)<=0;rom(426)<=0;rom(427)<=0;
rom(428)<=0;rom(429)<=0;rom(430)<=0;rom(431)<=0;
rom(432)<=0;rom(433)<=0;rom(434)<=0;rom(435)<=0;
rom(436)<=0;rom(437)<=0;rom(438)<=0;rom(439)<=0;
rom(440)<=0;rom(441)<=0;rom(442)<=0;rom(443)<=0;

```
rom(444)<=0;rom(445)<=0;rom(446)<=0;rom(
447)<=0;
rom(448)<=0;rom(449)<=0;rom(450)<=0;rom(
451)<=0;
rom(452)<=0;rom(453)<=0;rom(454)<=0;rom(
455)<=0;
rom(456)<=0;rom(457)<=0;rom(458)<=0;rom(
459)<=0;
rom(460)<=0;rom(461)<=0;rom(462)<=0;rom(
463)<=0;
rom(464)<=0;rom(465)<=0;rom(466)<=0;rom(
467)<=0;
rom(468)<=0;rom(469)<=0;rom(470)<=0;rom(
471)<=0;


  elsif set1="0010"then

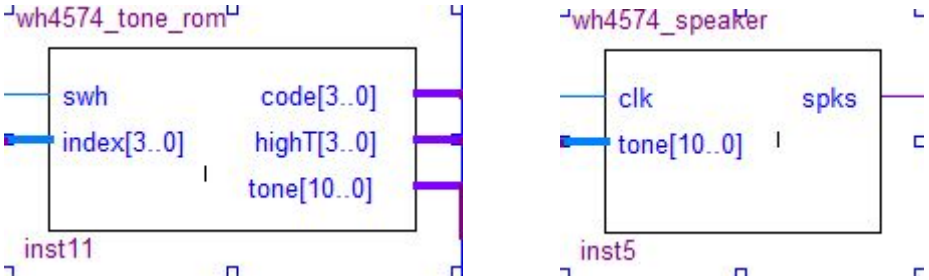
index<=conv_std_logic_vector(rom(adr),4);
rom(0)<=5;rom(1)<=11;rom(2)<=10;rom(3)<=
10;
rom(4)<=0;rom(5)<=10;rom(6)<=11;rom(7)<=
10;
rom(8)<=9;rom(9)<=8;rom(10)<=9;rom(11)<=
10;
rom(12)<=11;rom(13)<=10;rom(14)<=10;rom(
15)<=10;
rom(16)<=0;rom(17)<=6;rom(18)<=11;rom(19)
<=11;
rom(20)<=0;rom(21)<=11;rom(22)<=12;rom(2
3)<=11;
rom(24)<=9;rom(25)<=10;rom(26)<=11;rom(2
7)<=11;
rom(28)<=11;rom(29)<=10;rom(30)<=10;rom(
31)<=10;
rom(32)<=0;rom(33)<=8;rom(34)<=12;rom(35)
<=12;
rom(36)<=0;rom(37)<=12;rom(38)<=13;rom(3
9)<=12;
rom(40)<=11;rom(41)<=10;rom(42)<=10;rom(
43)<=11;
rom(44)<=9;rom(45)<=8;rom(46)<=14;rom(47)
<=14;
rom(48)<=0;rom(49)<=13;rom(50)<=12;rom(5
1)<=11;
rom(52)<=6;rom(53)<=7;rom(54)<=10;rom(55)
<=10;
rom(56)<=9;rom(57)<=8;rom(58)<=8;rom(59)
<=8;
rom(60)<=8;rom(61)<=8;rom(62)<=8;rom(63)
<=8;
rom(64)<=5;rom(65)<=11;rom(66)<=10;rom(6
7)<=10;
rom(68)<=0;rom(69)<=10;rom(70)<=11;rom(7
1)<=10;
rom(72)<=9;rom(73)<=8;rom(74)<=9;rom(75)
<=10;
rom(76)<=11;rom(77)<=10;rom(78)<=10;rom(
79)<=10;
rom(80)<=0;rom(81)<=6;rom(82)<=11;rom(83)
<=11;
rom(84)<=0;rom(85)<=11;rom(86)<=12;rom(8
7)<=11;
rom(88)<=9;rom(89)<=10;rom(90)<=11;rom(9
1)<=11;
rom(92)<=11;rom(93)<=10;rom(94)<=10;rom(
95)<=10;
rom(96)<=0;rom(97)<=8;rom(98)<=12;rom(99)
<=12;
rom(100)<=0;rom(101)<=12;rom(102)<=13;ro
m(103)<=12;
rom(104)<=11;rom(105)<=10;rom(106)<=10;r
om(107)<=11;
rom(108)<=9;rom(109)<=7;rom(110)<=14;ro
m(111)<=14;
rom(112)<=0;rom(113)<=13;rom(114)<=12;ro
m(115)<=11;
rom(116)<=6;rom(117)<=8;rom(118)<=10;ro
m(119)<=10;
rom(120)<=9;rom(121)<=8;rom(122)<=8;rom(
123)<=8;
rom(124)<=8;rom(125)<=8;rom(126)<=0;rom(
127)<=8;
rom(128)<=11;rom(129)<=12;rom(130)<=12;r
om(131)<=13;
rom(132)<=11;rom(133)<=10;rom(134)<=9;ro
m(135)<=0;
rom(136)<=6;rom(137)<=10;rom(138)<=11;ro
```

m(139)<=11;
rom(140)<=11;rom(141)<=12;rom(142)<=10;rom(143)<=9;
rom(144)<=8;rom(145)<=0;rom(146)<=4;rom(147)<=9;
rom(148)<=10;rom(149)<=10;rom(150)<=10;rom(151)<=11;
rom(152)<=11;rom(153)<=6;rom(154)<=7;rom(155)<=7;
rom(156)<=8;rom(157)<=9;rom(158)<=8;rom(159)<=8;
rom(160)<=8;rom(161)<=8;rom(162)<=9;rom(163)<=10;
rom(164)<=0;rom(165)<=8;rom(166)<=10;rom(167)<=12;
rom(168)<=12;rom(169)<=13;rom(170)<=11;rom(171)<=10;
rom(172)<=9;rom(173)<=0;rom(174)<=15;rom(175)<=14;
rom(176)<=15;rom(177)<=15;rom(178)<=12;rom(179)<=13;
rom(180)<=12;rom(181)<=11;rom(182)<=10;rom(183)<=0;
rom(184)<=8;rom(185)<=11;rom(186)<=12;rom(187)<=12;
rom(188)<=12;rom(189)<=13;rom(190)<=13;rom(191)<=8;
rom(192)<=8;rom(193)<=8;rom(194)<=7;rom(195)<=7;
rom(196)<=8;rom(197)<=8;rom(198)<=8;rom(199)<=8;
rom(200)<=8;rom(201)<=8;rom(202)<=5;rom(203)<=11;
rom(204)<=10;rom(205)<=10;rom(206)<=0;rom(207)<=10;
rom(208)<=11;rom(209)<=10;rom(210)<=9;rom(211)<=8;
rom(212)<=9;rom(213)<=10;rom(214)<=11;rom(215)<=10;
rom(216)<=10;rom(217)<=10;rom(218)<=0;rom(219)<=6;
rom(220)<=11;rom(221)<=11;rom(222)<=0;rom(223)<=11;
rom(224)<=12;rom(225)<=11;rom(226)<=9;rom(227)<=10;
rom(228)<=11;rom(229)<=11;rom(230)<=11;rom(231)<=10;
rom(232)<=10;rom(233)<=10;rom(234)<=0;rom(235)<=8;
rom(236)<=12;rom(237)<=12;rom(238)<=0;rom(239)<=12;
rom(240)<=13;rom(241)<=12;rom(242)<=11;rom(243)<=10;
rom(244)<=10;rom(245)<=11;rom(246)<=9;rom(247)<=8;
rom(248)<=14;rom(249)<=14;rom(250)<=0;rom(251)<=13;
rom(252)<=12;rom(253)<=11;rom(254)<=6;rom(255)<=7;
rom(256)<=10;rom(257)<=10;rom(258)<=9;rom(259)<=8;
rom(260)<=8;rom(261)<=8;rom(262)<=8;rom(263)<=8;
rom(264)<=8;rom(265)<=8;rom(266)<=8;rom(267)<=8;
rom(268)<=0;rom(269)<=0;rom(270)<=0;rom(271)<=0;
rom(272)<=0;rom(273)<=0;rom(274)<=0;rom(275)<=0;
rom(276)<=0;rom(277)<=0;rom(278)<=0;rom(279)<=0;
rom(280)<=0;rom(281)<=0;rom(282)<=0;rom(283)<=0;
rom(284)<=0;rom(285)<=0;rom(286)<=0;rom(287)<=0;
rom(288)<=0;rom(289)<=0;rom(290)<=0;rom(291)<=0;
rom(292)<=0;rom(293)<=0;rom(294)<=0;rom(295)<=0;
rom(296)<=0;rom(297)<=0;rom(298)<=0;rom(299)<=0;
rom(300)<=0;rom(301)<=0;rom(302)<=0;rom(303)<=0;
rom(304)<=0;rom(305)<=0;rom(306)<=0;rom(307)<=0;
rom(308)<=0;rom(309)<=0;rom(310)<=0;rom(311)<=0;
rom(312)<=0;rom(313)<=0;rom(314)<=0;rom(

```
315)<=0;
rom(316)<=0;rom(317)<=0;rom(318)<=0;rom(
319)<=0;
rom(320)<=0;rom(321)<=0;rom(322)<=0;rom(
323)<=0;
rom(324)<=0;rom(325)<=0;rom(326)<=0;rom(
327)<=0;
rom(328)<=0;rom(329)<=0;rom(330)<=0;rom(
331)<=0;
rom(332)<=0;rom(333)<=0;rom(334)<=0;rom(
335)<=0;
rom(336)<=0;rom(337)<=0;rom(338)<=0;rom(
339)<=0;
rom(340)<=0;rom(341)<=0;rom(342)<=0;rom(
343)<=0;
rom(344)<=0;rom(345)<=0;rom(346)<=0;rom(
347)<=0;
rom(348)<=0;rom(349)<=0;rom(350)<=0;rom(
351)<=0;
rom(352)<=0;rom(353)<=0;rom(354)<=0;rom(
355)<=0;
rom(356)<=0;rom(357)<=0;rom(358)<=0;rom(
359)<=0;
rom(360)<=0;rom(361)<=0;rom(362)<=0;rom(
363)<=0;
rom(364)<=0;rom(365)<=0;rom(366)<=0;rom(
367)<=0;
rom(368)<=0;rom(369)<=0;rom(370)<=0;rom(
371)<=0;
rom(372)<=0;rom(373)<=0;rom(374)<=0;rom(
375)<=0;
rom(376)<=0;rom(377)<=0;rom(378)<=0;rom(
379)<=0;
rom(380)<=0;rom(381)<=0;rom(382)<=0;rom(
383)<=0;
rom(384)<=0;rom(385)<=0;rom(386)<=0;rom(
387)<=0;
rom(388)<=0;rom(389)<=0;rom(390)<=0;rom(
391)<=0;
rom(392)<=0;rom(393)<=0;rom(394)<=0;rom(
395)<=0;
rom(396)<=0;rom(397)<=0;rom(398)<=0;rom(
399)<=0;
rom(400)<=0;rom(401)<=0;rom(402)<=0;rom(
403)<=0;
rom(404)<=0;rom(405)<=0;rom(406)<=0;rom(
407)<=0;
rom(408)<=0;rom(409)<=0;rom(410)<=0;rom(
411)<=0;
rom(412)<=0;rom(413)<=0;rom(414)<=0;rom(
415)<=0;
rom(416)<=0;rom(417)<=0;rom(418)<=0;rom(
419)<=0;
rom(420)<=0;rom(421)<=0;rom(422)<=0;rom(
423)<=0;
rom(424)<=0;rom(425)<=0;rom(426)<=0;rom(
427)<=0;
rom(428)<=0;rom(429)<=0;rom(430)<=0;rom(
431)<=0;
rom(432)<=0;rom(433)<=0;rom(434)<=0;rom(
435)<=0;
rom(436)<=0;rom(437)<=0;rom(438)<=0;rom(
439)<=0;
rom(440)<=0;rom(441)<=0;rom(442)<=0;rom(
443)<=0;
rom(444)<=0;rom(445)<=0;rom(446)<=0;rom(
447)<=0;
rom(448)<=0;rom(449)<=0;rom(450)<=0;rom(
451)<=0;
rom(452)<=0;rom(453)<=0;rom(454)<=0;rom(
455)<=0;
rom(456)<=0;rom(457)<=0;rom(458)<=0;rom(
459)<=0;
rom(460)<=0;rom(461)<=0;rom(462)<=0;rom(
463)<=0;
rom(464)<=0;rom(465)<=0;rom(466)<=0;rom(
467)<=0;
rom(468)<=0;rom(469)<=0;rom(470)<=0;rom(
471)<=0;
  else
       index<="0000";
       end if;
    end process;
end behav;
```

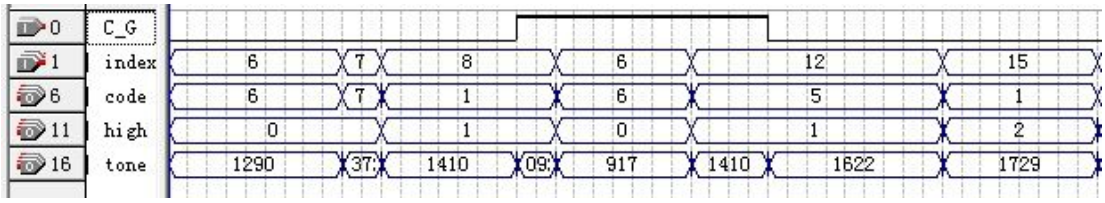
3,音符查表及简谱产生电路模块，音频输出模块

①，模块图

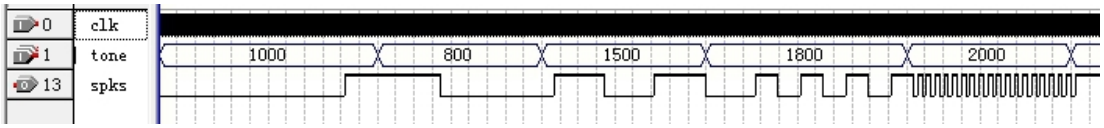


②，时序仿真波形：

音符查表及简谱产生电路模块仿真波形：



音频输出模块仿真波形;



③，程序源代码：

音符查表及简谱产生电路代码

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;
entity wh4574_tone_rom is
  port(swh:in std_logic;
       index:in std_logic_vector(3 downto 0);
       code: out std_logic_vector(3 downto 0);
       highT: out std_logic_vector(3 downto 0);
       tone: out std_logic_vector(10 downto 0));
end entity wh4574_tone_rom ;
architecture one of wh4574_tone_rom is
signal index1:integer range 0 to 15;
signal tone1: integer range 0 to 16#7FF#;
signal code1:integer range 0 to 15;
begin
  index1<=conv_integer(index);
  tone<=conv_std_logic_vector(tone1,11);
  code<=conv_std_logic_vector(code1,4);
  search:process(index)
  begin
```

```
 if swh='0' then
   case index1 is
     when 0=>tone1<=2047;code1<=0;highT<="0000";
     when 1=>tone1<=773;code1<=1;highT<="0000";
     when 2=>tone1<=912;code1<=2;highT<="0000";
     when 3=>tone1<=1036;code1<=3;highT<="0000";
     when 4=>tone1<=1092;code1<=4;highT<="0000";
     when 5=>tone1<=1197;code1<=5;highT<="0000";
     when 6=>tone1<=1290;code1<=6;highT<="0000";
     when 7=>tone1<=1372;code1<=7;highT<="0000";
     when 8=>tone1<=1410;code1<=1;highT<="0001";
     when 9=>tone1<=1480;code1<=2;highT<="0001";
     when 10=>tone1<=1542;code1<=3;highT<="0001";
     when 11=>tone1<=1570;code1<=4;highT<="0001";
     when 12=>tone1<=1622;code1<=5;highT<="0001";
     when 13=>tone1<=1669;code1<=6;highT<="0001";
     when 14=>tone1<=1710;code1<=7;highT<="0001";
     when 15=>tone1<=1729;code1<=1;highT<="0010";
     when others=>null;
   end case;
 elsif swh='1' then
   case index1 is
     when 0=>tone1<=2047;code1<=0;highT<="0000";
     when 1=>tone1<=137;code1<=1;highT<="0000";
     when 2=>tone1<=345;code1<=2;highT<="0000";
     when 3=>tone1<=531;code1<=3;highT<="0000";
     when 4=>tone1<=616;code1<=4;highT<="0000";
     when 5=>tone1<=772;code1<=5;highT<="0000";
     when 6=>tone1<=912;code1<=6;highT<="0000";
     when 7=>tone1<=1036;code1<=7;highT<="0000";
     when 8=>tone1<=1092;code1<=1;highT<="0001";
     when 9=>tone1<=1197;code1<=2;highT<="0001";
     when 10=>tone1<=1290;code1<=3;highT<="0001";
     when 11=>tone1<=1332;code1<=4;highT<="0001";
     when 12=>tone1<=1410;code1<=5;highT<="0001";
     when 13=>tone1<=1480;code1<=6;highT<="0001";
     when 14=>tone1<=1542;code1<=7;highT<="0001";
     when 15=>tone1<=1570;code1<=1;highT<="0010";
     when others=>null;
   end case;
 end if;
 end process;
end one;
```

音频输出模块代码：

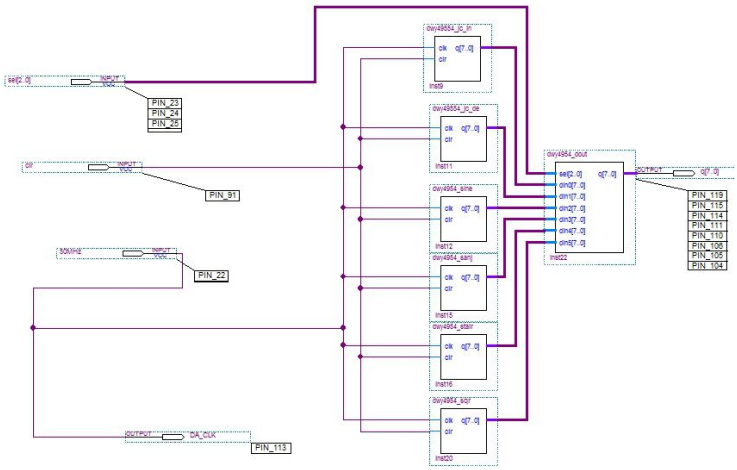
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
entity wh4574_speaker is
  port(clk:in std_logic;
          tone:in std_logic_vector(10 downto 0);
          spks:out std_logic);
end wh4574_speaker;
architecture one of wh4574_speaker is
  signal preclk:std_logic;
  signal fullspks:std_logic;
  signal tone1:integer range 0 to 16#7FF# ;
begin
  tone1<=conv_integer(tone);
  divdeclk:process(clk)
    variable count4:integer range 0 to 15;
  begin
    preclk<='0';
    if count4>=5 then
      preclk<='1';
      count4:=0;
    elsif clk'event and clk='1' then
      count4:=count4+1;
    end if;
  end process;
  genspks:process(preclk,tone1)
  variable count11:integer range 0 to 16#7FF#;
  begin
    if preclk'event and preclk='1' then
      if count11=16#7FF# then
        count11:=tone1;
        fullspks<='1';
        else count11:=count11+1;
                fullspks<='0';
      end if;
    end if;
  end process;
  delayspks:process(fullspks)
  variable count2:std_logic;
  begin
    if fullspks'event and fullspks='1' then
      count2:=not count2;
```

```
      if count2='1' then
        spks<='1';
          else spks<='0';
      end if;
   end if;
 end process;
end one;
```

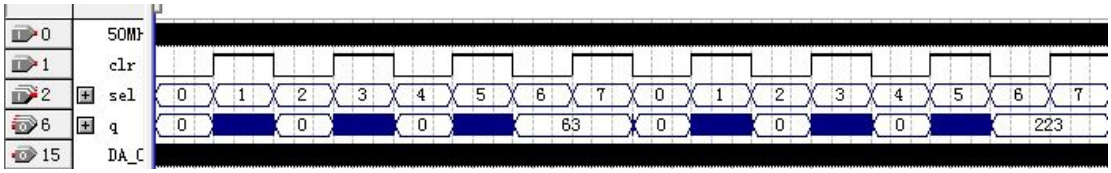
4，动态译码 LED 显示模块与分频模块与设计一《12/24 小时数字时钟 VHDL 设计》一致，这里不赘述。

三，函数信号发生器设计

1，系统顶层电路：



时序仿真波形：

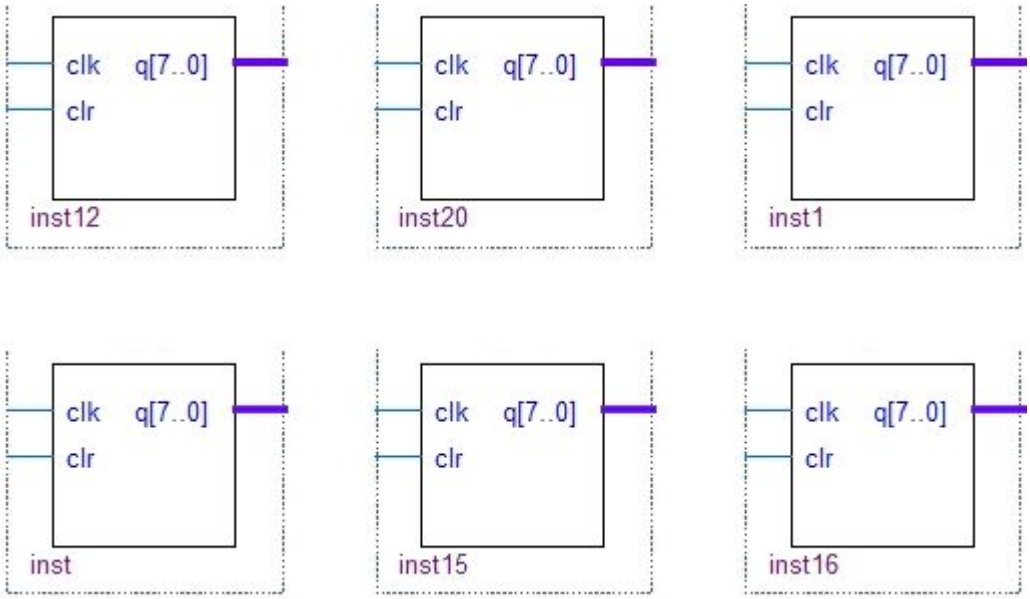


管脚定义及锁定：

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard
1	50MHz	Input	PIN_22	1	B1_N0	2.5 V (default)
2	clr	Input	PIN_91	6	B6_N0	2.5 V (default)
3	DA_CLK	Output	PIN_113	7	B7_N0	2.5 V (default)
4	q[0]	Output	PIN_104	6	B6_N0	2.5 V (default)
5	q[1]	Output	PIN_105	6	B6_N0	2.5 V (default)
6	q[2]	Output	PIN_106	6	B6_N0	2.5 V (default)
7	q[3]	Output	PIN_110	7	B7_N0	2.5 V (default)
8	q[4]	Output	PIN_111	7	B7_N0	2.5 V (default)
9	q[5]	Output	PIN_114	7	B7_N0	2.5 V (default)
10	q[6]	Output	PIN_115	7	B7_N0	2.5 V (default)
11	q[7]	Output	PIN_119	7	B7_N0	2.5 V (default)
12	sel[0]	Input	PIN_23	1	B1_N0	2.5 V (default)
13	sel[1]	Input	PIN_24	2	B2_N0	2.5 V (default)
14	sel[2]	Input	PIN_25	2	B2_N0	2.5 V (default)

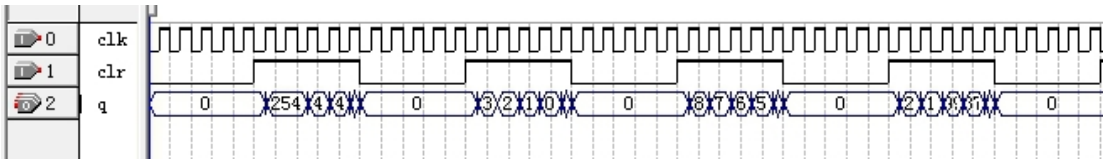
2，正弦(sine)，方波(sqr)，锯齿波(jc_de 和 jc_in 两种)，三角波(sanj)和阶梯波(stair)信号模块。

①，模块图：

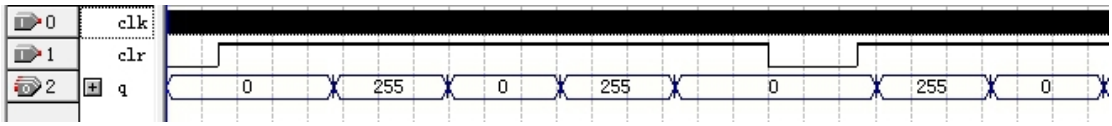


②，时序仿真波形：

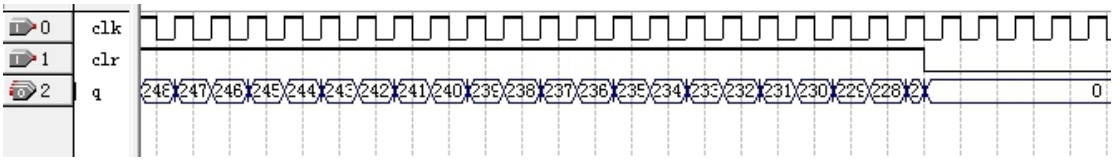
正弦信号：



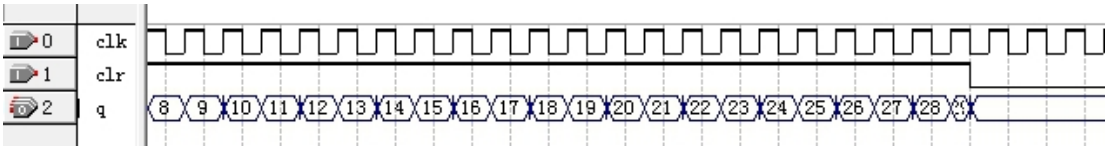
方波信号：



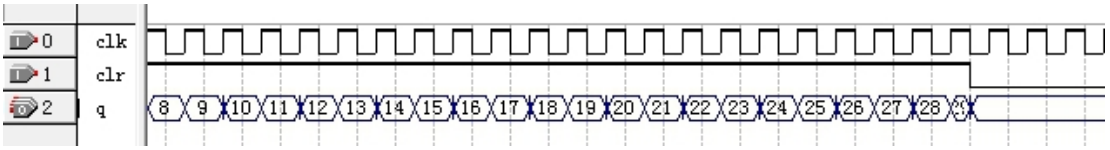
锯齿波递增信号：



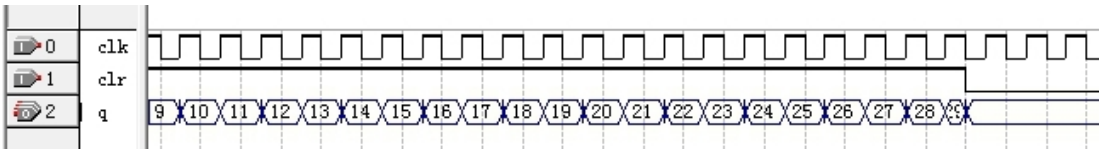
锯齿波递减信号：



阶梯波信号：



三角波信号：



③，源代码：

正弦信号

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_sine is
   port(clk,clr:in std_logic;
          q:out integer range 0 to 255);
end wh4574_sine;
architecture behav of wh4574_sine is
   signal a:bit;
begin
   process(clk,clr)
      variable temp:integer range 0 to 63;
   begin
      if clr='0'then
         q<=0;
      elsif(clk'event and clk='1')then
        if temp=63 then
            temp:=0;
        else
            temp:=temp+1;
        end if;
        case temp is
when 00=>q<=255;
when 001=>q<=254;when 02=>q<=254;
when 03=>q<=249;when 04=>q<=245;
when 05=>q<=239;when 06=>q<=233;
when 07=>q<=225;when 08=>q<=217;
when 09=>q<=207;when 10=>q<=197;
when 11=>q<=186;when 12=>q<=174;
when 13=>q<=162;when 14=>q<=150;
when 15=>q<=137;when 16=>q<=124;
when 17=>q<=112;when 18=>q<=99;
when 19=>q<=87;when 20=>q<=75;
when 21=>q<=64;when 22=>q<=53;
when 23=>q<=43;when 24=>q<=34;
when 25=>q<=26;when 26=>q<=19;
when 27=>q<=13;when 28=>q<=8;
when 29=>q<=4;
when 30=>q<=1;
when 31=>q<=0;when 32=>q<=0;
when 33=>q<=1;when 34=>q<=4;
when 35=>q<=8;when 36=>q<=13;
when 37=>q<=19;when 38=>q<=26;
when 39=>q<=34;when 40=>q<=43;
when 41=>q<=53;when 42=>q<=64;
when 43=>q<=75;when 44=>q<=87;
when 45=>q<=99;when 46=>q<=112;
when 47=>q<=124;when 48=>q<=137;
when 49=>q<=150;when 50=>q<=162;
when 51=>q<=174;when 52=>q<=186;
when 53=>q<=197;when 54=>q<=207;
when 55=>q<=217;when 56=>q<=225;
when 57=>q<=233;when 58=>q<=239;
when 59=>q<=245;when 60=>q<=249;
when 61=>q<=252;when 62=>q<=254;
when 63=>q<=255;when others=>null;
          end case;
       end if;
   end process;
end behav;
```

方波信号：

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITYwh4574_sqr IS
  PORT(clk,clr:IN STD_LOGIC;
    q:OUT INTEGER RANGE 0 TO 255);
ENDwh4574_sqr;
```

```
ARCHITECTURE bhv OFwh4574_sqr IS
SIGNAL a:BIT;
BEGIN
 PROCESS(clk,clr)
 VARIABLE cnt:INTEGER RANGE 0 TO 255;
 BEGIN
  IF clr='0' THEN
    a<='0';
  ELSIF clk'EVENT AND clk='1' THEN
    IF cnt<63 THEN
      cnt:=cnt+1;
    ELSE
      cnt:=0;
      a<=NOT a;
    END IF;
  END IF;
 END PROCESS;

 PROCESS(clk,a)
 BEGIN
  IF clk'EVENT AND clk='1' THEN
    IF a='1' THEN
      q<=255;
    ELSE
      q<=0;
    END IF;
  END IF;
 END PROCESS;
END bhv;
```

锯齿波递增信号：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh45744_jc_in is
port(clk,clr:in std_logic;
       q:out std_logic_vector(7 downto 0));
end wh4574_jc_in;
architecture behav of wh4574_jc_in is
begin
   process(clk,clr)
      variable temp:std_logic_vector(7 downto
0);
   begin
      if clr='0' then
          temp:="00000000";
      elsif(clk'event and clk='1')then
          if(temp="00000000")then
              temp:="11111111";
          else
              temp:=temp-1;
          end if;
      end if;
      q<=temp;
   end process;
end behav;
```

锯齿波递减信号：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_jc_de is
port(clk,clr:in std_logic;
       q:out std_logic_vector(7 downto 0));
end wh4574_jc_de;
architecture behav of wh4574_jc_de is
begin
   process(clk,clr)
      variable temp:std_logic_vector(7 downto
0);
   begin
      if clr='0' then
          temp:="00000000";
      elsif(clk'event and clk='1')then
          if(temp="11111111")then
              temp:="00000000";
          else
              temp:=temp+1;
          end if;
      end if;
      q<=temp;
   end process;
end behav;
```

三角波信号：

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_sanj is
   port(clk,clr:in std_logic;
        q:out std_logic_vector(7 downto 0));
end wh45744_sanj;
architecture behav of wh4574_sanj is
begin
   process(clk,clr)
      variable temp1:std_logic_vector(7
downto 0);
      variable temp2:std_logic;
   begin
      if clr='0'then
         temp1:="00000000";
      elsif(clk'event and clk='1')then
         if temp2='0'then
            if(temp1="11111110")then
               temp1:="11111111";
               temp2:='1';
            else
               temp1:=temp1+1;
            end if;
         else
            if(temp1="00000001")then
               temp1:="00000000";
               temp2:='0';
            else
               temp1:=temp1-1;
            end if;
         end if;
      end if;
         q<=temp1;
   end process;
end behav;
```

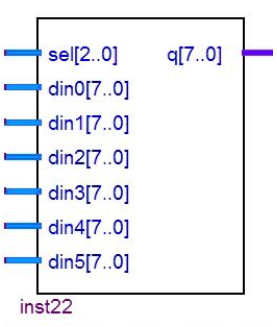
阶梯波：

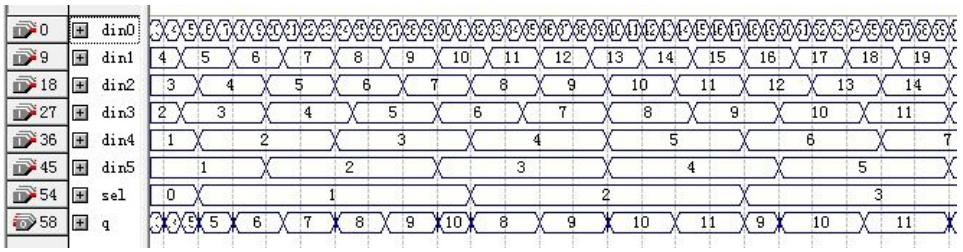
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity wh4574_stair is
port(clk,clr:in std_logic;
      q:out std_logic_vector(7 downto 0));
end wh4574_stair;
architecture behav of wh4574_stair is
begin
   process(clk,clr)
      variable temp1:std_logic_vector(7
downto 0);
      variable temp2:std_logic;
   begin
      if clr='0'then
         temp1:="00000000";
      elsif(clk'event and clk='1')then
         if temp2='0'then
            if(temp1="11111111")then
               temp1:="00000000";
               temp2:='1';
            else
               temp1:=temp1+32;
               temp2:='1';
            end if;
         else
            temp2:='0';
         end if;
      end if;
      q<=temp1;
   end process;
end behav;
```

3，信号数据选择输出模块：

①，模块图：

②，时序仿真波形：





③，源代码：

```
library ieee;
use ieee.std_logic_1164.all;
entity wh4574_dout is
port(sel:in std_logic_vector(2 downto 0);
      din0,din1,din2,din3,din4,din5:in
std_logic_vector(7 downto 0);
      q:out std_logic_vector(7 downto 0));
end entity;
architecture behav of wh4574_dout is
begin
  process(sel)
  begin
    case sel is
      when"000"=>q<=din0;
      when"001"=>q<=din1;
      when"010"=>q<=din2;
      when"011"=>q<=din3;
      when"100"=>q<=din4;
      when"101"=>q<=din5;
      when others=>null;
    end case;
  end process;
end behav;
```