Efficient Algorithms for Device Placement
of DNN Graph Operators

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Abstract

Modern machine learning workloads use large models, with complex structures, that are very expensive to execute. The devices that execute complex models are becoming increasingly heterogeneous as we see a flourishing of domain-specific accelerators being offered as hardware accelerators in addition to CPUs. These trends necessitate distributing the workload across multiple devices. Recent work has shown that significant gains can be obtained with *model parallelism*, i.e, partitioning a neural network's computational graph onto multiple devices. In particular, this form of parallelism assumes a *pipeline* of devices, which is fed a stream of samples and yields high throughput for training and inference of DNNs. However, for such settings (large models and multiple heterogeneous devices), we require automated algorithms and toolchains that can partition the ML workload across devices. In this paper, we identify and isolate the *structured optimization problem* at the core of device placement of DNN operators, for both inference and training, especially in modern pipelined settings. We then provide algorithms that solve this problem to optimality. We demonstrate the applicability and efficiency of our approaches using several contemporary DNN computation graphs.

1   Introduction

Deep Neural Networks (DNNs) have been effective across a range of applications, including image classification [KSH12, SZ14, HZRS15a], translation [WSC+16], language modeling [MKS17], and video captioning [VRD+15]. The proliferation of heterogeneous hardware accelerators [JYP+17, SPM+16] coupled with the dramatic growth in the size and the structural complexity of DNNs has bolstered the importance of *model parallelism*, where for both inference and training, the model is distributed across devices.

DNN inference in the "single-stream" setting [mlp], where only one inference request is issued at a time, is *latency-sensitive*. To achieve low latency, model parallel executions split the model across many accelerators [CKES16, FOP+18, CFO+18]. Model-parallel inference is beneficial due to three primary reasons. First, such splits are mandated by the memory-capacity (size) limitations of accelerators that cannot fit a single DNN model. Current DNN models have billions of parameters and require multiple GBs of space to store the weights and intermediate activations. Second, wide branching in recent DNN structures, as well as in the operator-granularity graphs for established DNNs, opens up the potential of executing data-independent sections of the computation in parallel to reduce latency. Third, the model needs to be split across multiple types of devices when a subset of operators in the graph are better suited or only supported to execute on certain devices.

DNN training, on the other hand, is *throughput-bound*, as is DNN inference for the "offline" setting where many inputs can be serviced together [mlp]. Model parallelism has been proposed for training for the very same motivational reasons listed for inference above [KSH12, Kri14]. Early influential systems

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such as DistBelief [DCM⁺12] and Project Adam [CSAK14] split models to operate on commodity CPU clusters and out of CPU caches. In such a setting, operators in a DNN model are partitioned across the available devices, with each device evaluating and performing updates only on a subset of the model's parameters for all inputs. While traditional model parallel training suffers from problems of low hardware utilization, as only a single accelerator is active at any given time, **pipelined model parallelism** overcomes this deficiency. The amount of data communicated in pipelined training is the size of intermediate outputs (and corresponding gradients), which need to be sent across accelerators, and is much lower than the size of data communicated in data-parallel training. In particular, for a range of existing models that fit on a single GPU, PipeDream [HNP⁺18, NHP⁺19] uses pipelined model-parallelism to achieve much faster training time to advertised accuracy than data-parallelism. Similarly, GPipe [HCC⁺18, HCB⁺19] uses pipelined model-parallel training for very large models whose total training memory footprint exceeds the memory capacity of a single accelerator.

Given the importance of model-parallel inference and training, in this paper we present efficient algorithms to answer the following general question: *For a DNN model and a deployment scenario (a set of accelerators and their memory and interconnect constraints), how can we effectively partition the model to optimize the metric of interest, such as latency or throughput, relevant to the inference or training task at hand?*

We provide novel algorithmic approaches to tackle the problem of partitioning the model in both model-parallel inference and training scenarios, optimizing for their corresponding metrics of interest:

- Inference – (i) Model-Parallel Inference, optimized for "single-stream" latency (Fig. 2a), (ii) Pipelined Inference, optimized for "offline" throughput (Fig. 5a).

- Training, optimized for throughput – (i) Model-Parallel Training (Fig. 2b), (ii) Pipeline-Parallel Training with PipeDream and GPipe schedules (Fig. 7).

In particular, for both non-pipelined and pipelined settings, we identify the combinatorial optimization problem at the core of the device placement question, whose solution will yield the *optimal* partition. We then show how to solve this problem to optimality via Integer Programming (IP) and Dynamic Programming (DP) based algorithms. Our methods are general as they can be applied either to coarse-granularity layer graphs or to more complex fine-granularity operator graphs. We support graph partitions where accelerators can hold a *non-contiguous* fragment of the graph. We evaluate our partitioning algorithms for different scenarios described above for a variety of modern DNN workloads (7 DNNs, 16 layer and operator graphs). We find that the placements are efficient and result in non-trivial optimal splits; non-contiguous splits outperform all the techniques, with an improvement of up to 2× over expert (average 1.46×), 2.08× over local search (average 1.29×) [MKA07], 1.21× over PipeDream (average 1.10×) [NHP⁺19], 7.69× over Scotch (average 1.50×) [Pel09].

Outline. This paper is organized as follows. We discuss related work in Section 2. In Section 3 we define our model of DNN computation, as well as the input/output specification for the problem of finding the best split. Next, in Sections 4 and 5 we focus on the latency objective (feeding one sample) and throughput objective (pipelining multiple samples), respectively. We present efficient algorithms that find optimal splits for both objectives. In Sections 6 and 7 we present our evaluation results for the throughput objective and the latency objective, respectively.

2 Related Work

In the context of DNN workloads, model partitioning across different devices has mostly been a manual process driven by human experts. Most prior work on *automated* device placement falls into two broad categories.

The first category comprises methods that treat the objective function (i.e., latency or throughput) as a black box. These works use heuristics, mostly based on reinforcement learning, to find partitions for a given workload (Mirhoseini et al. [MPL⁺17, MGP⁺18], Spotlight [GCL18]) or learn a placement policy that

can then be adjusted for new workloads via transfer learning (Placeto [ABVG⁺19], GDP [ZRA⁺19]) or used to bootstrap a genetic algorithm (REGAL [PGN⁺20]). Unfortunately, these methods are computationally expensive, as they need to evaluate large numbers of placements, each of which entails a reconfiguration of the deployed devices (for a new DNN split) and measuring the runtime of several inference/training steps. For instance, [MPL⁺17] requires 12–27 hours of training time *on the target system* to partition modern workloads; [MGP⁺18] requires 12 GPU hours. For this reason, some systems (Placeto [ABVG⁺19], FlexFlow [JZA19]) resort to implementing a simulator to evaluate the objective.

Works in the second category – including ours – build a cost model that closely reflects real performance, and then algorithmically solve the resulting "offline" optimization problem of finding good partitions and schedules. This includes classic results in scheduling on multiple machines/devices [LLKS93, Gra66, KL70, PY90, SW99, ST93], as well as modern DNN scheduling works (OptCNN [JLQA18], PipeDream's [NHP⁺19] optimizer). Such algorithms use *profiled* compute time of each node (layer or operator) and data-transfer requirements between nodes in a graph, and the target deployment system infrastructure such as machine and network properties (e.g. measured bandwidths). Such techniques do not evaluate the performance of splits in an online fashion. Nevertheless, it has been demonstrated that for well-defined cost models the objective function closely matches real performance (PipeDream [NHP⁺19, Figure 15], FlexFlow [JZA19, Figure 11], OptCNN [JLQA18, Table 4]). Our throughput maximization model in Section 5 generalizes the cost model used in PipeDream [NHP⁺19], and our latency minimization objective (Section 4) is similar to the cost model of FlexFlow's simulator [JZA19]. In terms of approach, both OptCNN [JLQA18] and FlexFlow [JZA19] optimize over different dimensions than our methods, opting for more local parallelization strategies.

Pipelining. GPipe [HCB⁺19] and PipeDream [NHP⁺19] introduce *pipelined* model-parallelism for training. Given that this prior work has already shown the efficacy of pipeline parallel training on statistical efficiency (training progress compared to data-parallel training), the focus of this paper is instead on efficient algorithms to effectively partition DNN models across accelerators. For finding good DNN splits, GPipe presents no algorithm, and PipeDream proposes a method limited to layer graphs that are linear (i.e., a path). Efficiently finding optimal splits for pipelined execution in a general-DAG setting for both training and inference is a central contribution of this paper.

3 Computational Model

Input. We consider a heterogeneous system with k DNN hardware accelerators and ℓ CPUs. For simplicity of exposition we assume all accelerators to be of the same type (such as GPU, FPGA, or TPU) for a single input. Every such accelerator has a capacity limit for its associated memory, denoted by M. We refer to both CPUs and accelerators as *devices*. The rest of the input to our algorithms consists of a directed acyclic graph (DAG) $G = (V, E)$ with associated weights:

- The set V of nodes represents operators such as `MatMul`, `Add`, `ReLu`, etc. (for operator graphs), or layers such as `MaxPool2d` or `LSTM` (for layer graphs). Each node v has an associated time p_v^{cpu} required to process v on a CPU, as well as the processing time p_v^{acc} of v on an accelerator.[1] Each node also has a size m_v: the memory usage of its associated weights and activations.

- The set E of directed edges encodes dependency/precedence constraints: an edge (u, v) implies that the operation v depends on the result of u. Each node u has a communication cost c_u, which corresponds to the time required to transfer u's output between CPU DRAM (henceforth referred to as RAM) and the accelerator's memory, say through a PCIE bus. Crucially, this cost is paid only if u and v are placed on different devices: if u is on an accelerator, it needs to write this output to RAM, and if v is on an accelerator, it needs to read this input from RAM. We ignore the cost of reading or writing to RAM from CPUs.

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[1]If v is not supported on the accelerator, we set $p_v^{\mathrm{acc}} = \infty$.

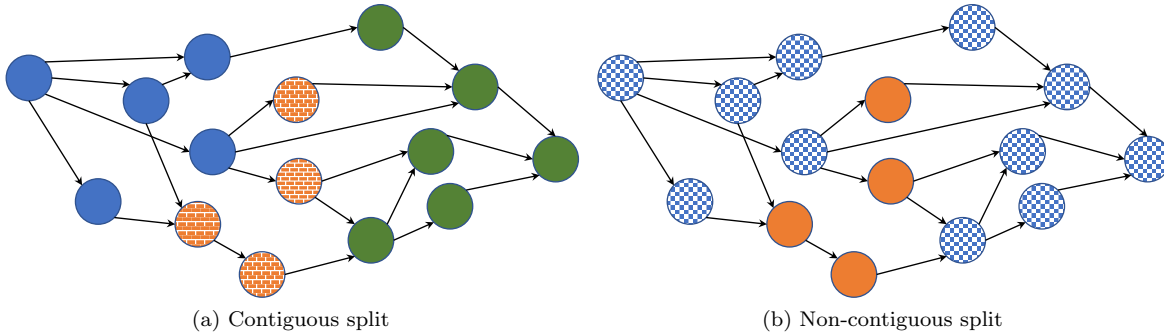(a) Contiguous split   (b) Non-contiguous split

Figure 1: (a) Contiguous and (b) non-contiguous splits. Note that the brick-patterned orange nodes in (a) form a contiguous subgraph despite not being connected, and checked blue nodes in (b) form a non-contiguous subgraph despite being connected.

(a) Model-parallel inference schedule   (b) Model-parallel training schedule
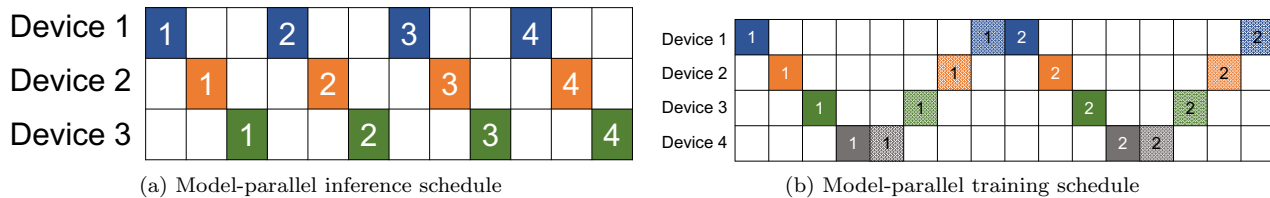
Figure 2: (a) Single-stream model-parallel inference and (b) Model-parallel training schedule with darker shades for forward pass and lighter for backward. The x-axis is time, and numbers 1–4 are input minibatch identifiers. Different colors represent different devices.

Output. We seek to assign each node in the graph to exactly one device so that for every accelerator the sum of sizes m_v of nodes assigned to it does not exceed its capacity M. Out of all feasible partitions we want to select one that optimizes a metric of interest (latency or throughput).

Contiguous and non-contiguous subgraphs of computation. By default, we desire every device to hold a contiguous fragment of the DNN:

Definition 3.1. *We say that a set $S \subseteq V$ is* contiguous *if there do **not** exist nodes $u \in S$, $v \in V \setminus S$, and $w \in S$ such that v is reachable from u and w is reachable from v.*

See Fig. 1 for an example. This property enables subgraphs to be invoked in an uninterrupted way: all required inputs can be transferred to the accelerator at one time, after which it performs computations and produces all its outputs. This allows for simpler system implementations and less interactivity with the accelerator.[2]

However, in this work we also explore non-contiguous splits, where the subgraphs placed on an accelerator can be arbitrary. In particular, we explain how to build a pipelined schedule for executing such a split for a stream of many samples, and how to find an optimal split of this more general form.

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\begin{aligned}
\min \quad & \text{TotalLatency} \\
\text{s.t.} \quad & \sum\nolimits_{i=0}^{k} x_{vi} = 1 && (\forall v) && (1) \\
& \text{subgraph } \{v \in V : x_{vi} = 1\} \text{ is contiguous} && (\forall i = 1, ..., k) && (2) \\
& M \geq \sum\nolimits_{v} m_v \cdot x_{vi} && (\forall i = 1, ..., k) && (3) \\
& \text{CommIn}_{ui} \geq x_{vi} - x_{ui} && (\forall (u, v) \in E)\ (\forall i = 1, ..., k) && (4) \\
& \text{CommOut}_{ui} \geq x_{ui} - x_{vi} && (\forall (u, v) \in E)\ (\forall i = 1, ..., k) && (5) \\
& \text{TotalLatency} \geq \text{Latency}_v && (\forall v) \\
& \text{SubgraphStart}_i \geq \text{Latency}_v \cdot \text{CommIn}_{vi} && (\forall v)\ (\forall i = 1, ..., k) && (6) \\
& \text{SubgraphFinish}_i = \text{SubgraphStart}_i + \sum\nolimits_{v} \text{CommIn}_{vi} \cdot c_v \\
& \qquad\qquad + \sum\nolimits_{v} x_{vi} \cdot p_v^{\text{acc}} + \sum\nolimits_{v} \text{CommOut}_{vi} \cdot c_v && (\forall i = 1, ..., k) && (7) \\
& \text{Latency}_v \geq x_{v0} \cdot p_v^{\text{cpu}} && (\forall v) && (8) \\
& \text{Latency}_v \geq x_{v0} \cdot p_v^{\text{cpu}} + \text{Latency}_u && (\forall (u, v) \in E) && (9) \\
& \text{Latency}_v \geq x_{vi} \cdot \text{SubgraphFinish}_i && (\forall v)\ (\forall i = 1, ..., k) && (10) \\
& x_{vi} \in \{0, 1\} && (\forall v)\ (\forall i = 0, ..., k)
\end{aligned}
$$

Figure 3: A schema of the Integer Program for latency minimization

4   Inference and Latency Minimization

In this section we focus on the task of DNN inference in the non-pipelined setting, i.e., when one sample is fed at a time (see Fig. 2). The objective here is latency, i.e., the time to produce the final output. Here, model parallelism is required and/or assists in the following two ways. First, the model might not fit in the memory of a single accelerator, making the split necessary. Second, it enables us to exploit the parallelism inherent in the model: if two operators are independent, they can be processed simultaneously if placed on different devices. We present an *Integer Programming* based solution for this setting.

Mode of computation.   In the setting of latency minimization, we assume the way of invoking contiguous subgraphs of computation that we mentioned above (in Section 3). Specifically, an accelerator, which is assigned a subgraph $S \subseteq V$ of nodes, can be *invoked* when all of its required inputs are ready in DRAM (these are outputs of nodes not in S but with an edge to S). Once invoked, the accelerator transfers this data to its memory. Next, it processes operations $v \in S$ (in some sequential order). Finally, it transfers the results back to DRAM (these are outputs of nodes in S with an edge leaving S). This uninterrupted mode of execution is made possible by S being contiguous.

Another mild assumption we make to streamline the Integer Programming formulation is that the number ℓ of CPU cores is no smaller than the *width* of G, i.e., the maximum number of nodes that can feasibly be processed in parallel.[3]

Our formulation.   Our IP formulation is presented in Fig. 3. Devices/subgraphs of accelerators are indexed $i = 1, ..., k$, and the special index $i = 0$ denotes all CPU cores together. We use binary variables x_{vi} to denote

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[2]In particular, this way of invoking subgraphs of computation on accelerators is motivated by production systems at Microsoft [FOP+18, CFO+18], where there is no state maintained across any two subgraph invocations other than subgraph model parameters.

[3]Formally, ℓ is larger than any *antichain*: a set $A \subseteq V$ of nodes such that for any $u, v \in A$, u is not reachable from v.

whether node v should be placed on device/subgraph i, and continuous variables Latency_v to denote the time at which node v has finished executing and its output (or that of the subgraph where it is placed) is available in RAM. The objective TotalLatency is the maximum of Latency_v over all nodes v. All variables except x_{vi} are bound to be non-negative (i.e., not necessarily integral). We explain the remaining variables and constraints below:

- The variable CommIn_{ui} is intended to be 1 if u is not in subgraph i, but has an edge to it (and 0 otherwise). In this case its output needs to be transferred to the corresponding accelerator's memory. This is encoded by constraint (4).

- Similarly CommOut_{ui} should be 1 if u is in subgraph i and has an edge going out of i. In this case its output needs to be transferred from the corresponding accelerator to RAM. This is encoded by constraint (5).

- For a subgraph i, SubgraphStart_i is the time at which all its inputs are ready in RAM (not the accelerator's memory). This is encoded by constraint (6). SubgraphFinish_i is the time at which all its outputs are ready and have been transferred to RAM. Constraint (7) relates the two by taking into account the in-transfer, processing inside the subgraph, and the out-transfer.

- Constraint (1) means that every node should be assigned to exactly one subgraph (or a CPU).

- Constraint (3) encodes the requirement that the sum of sizes of nodes on accelerator i should be at most M.

- Constraints (8) and (9) encode that node v can start processing once all of its predecessors u are finished. If v is placed on a CPU, then its processing takes p_v^{cpu} time. Otherwise, its processing time is taken into account in constraint (7) of the subgraph i where it is placed; the outputs of i are available at time SubgraphFinish_i, and constraint (10) will set Latency_v to that value.

Note that the formulation as presented in Fig. 3 is not yet a Mixed-Integer Program (MIP) – but can be made so.

Lemma 4.1. *The constraints* (2), (6) *and* (10) *can be reformulated as linear constraints.*

Proof. To reformulate (6), take H to be a very large number (guaranteed to be larger than Latency_v in any considered solution) and write

$$\text{SubgraphStart}_i \geq \text{Latency}_v - (1 - \text{CommIn}_{vi}) \cdot H \,.$$

If $\text{CommIn}_{vi} = 1$, then we recover the original constraint. Otherwise, if $\text{CommIn}_{vi} = 0$, the right-hand side is negative and the constraint becomes vacuous. Constraint (10) can be rewritten analogously.

To formulate the contiguity constraint (2), we use extra variables z_{vi}, with the following linear constraints:

$$z_{vi} \geq x_{vi} \qquad\qquad (\forall v)\ (\forall i = 1, ..., k) \qquad\qquad (11)$$
$$z_{vi} \leq z_{ui} \qquad\qquad (\forall (u,v) \in E)\ (\forall i = 1, ..., k) \qquad\qquad (12)$$
$$z_{vi} \leq x_{vi} - x_{ui} + 1 \qquad\qquad (\forall (u,v) \in E)\ (\forall i = 1, ..., k) \qquad\qquad (13)$$

Intuitively, one can think of $z_{\cdot i}$ as being a non-increasing sequence that lays above $x_{\cdot i}$.

Fix i. We claim that the subgraph $S = \{v \in V : x_{vi} = 1\}$ is contiguous if and only if there exists a vector $(z_{vi})_{v \in V}$ satisfying constraints (11)–(13).

"Only if" direction: for every v define $z_{vi} = 1$ if any node in S is reachable from v, and 0 otherwise. Constraints (11) and (12) are clearly satisfied. For constraint (13), the only interesting case is when $x_{vi} = 0$ and $x_{ui} = 1$; then the constraint becomes $z_{vi} \leq 0$. This is indeed satisfied as no node $w \in S$ can be reachable from v; if it were, then the triple (u, v, w) would contradict the contiguity of S (cf. Theorem 3.1).

"If" direction: towards a contradiction assume that there are nodes $u \in S$, $v \notin S$ and $w \in S$ such that v is reachable from u and w is reachable from v. Without loss of generality assume that $(u, v) \in E$. Then $z_{vi} \leq 0$ by constraint (13). By following the path from v to w and repeatedly applying constraint (12) we get $z_{wi} \leq z_{vi}$, thus $z_{wi} \leq 0$. But by constraint (11) we must also have $z_{wi} \geq 1$ since $w \in S$, a contradiction. $\square$

$$\min \quad \text{TotalLatency}$$

$$\text{s.t.} \quad \sum_{j=0}^{kq} x_{vj} = 1 \qquad (\forall v) \qquad (1)$$

$$\text{subgraph } \{v \in V : x_{vj} = 1\} \text{ is contiguous} \qquad (\forall j > 0) \qquad (2)$$

$$M \geq \sum_v m_v \cdot \sum_{j=(i-1)q+1}^{iq} x_{vj} \qquad (\forall i = 1, ..., k) \qquad (3^*)$$

$$\text{CommIn}_{uj} \geq x_{vj} - x_{uj} \qquad (\forall(u,v) \in E) \ (\forall j > 0) \qquad (4)$$

$$\text{CommOut}_{uj} \geq x_{uj} - x_{vj} \qquad (\forall(u,v) \in E) \ (\forall j > 0) \qquad (5)$$

$$\text{TotalLatency} \geq \text{Latency}_v \qquad (\forall v)$$

$$\text{SubgraphStart}_j \geq \text{Latency}_v \cdot \text{CommIn}_{vj} \qquad (\forall v) \ (\forall j > 0) \qquad (6)$$

$$\text{SubgraphFinish}_j = \text{SubgraphStart}_j + \sum_v \text{CommIn}_{vj} \cdot c_v$$

$$+ \sum_v x_{vj} \cdot p_v^{\text{acc}} + \sum_v \text{CommOut}_{vj} \cdot c_v \qquad (\forall j > 0) \qquad (7)$$

$$\text{Latency}_v \geq x_{v0} \cdot p_v^{\text{cpu}} \qquad (\forall v) \qquad (8)$$

$$\text{Latency}_v \geq x_{v0} \cdot p_v^{\text{cpu}} + \text{Latency}_u \qquad (\forall(u,v) \in E) \qquad (9)$$

$$\text{Latency}_v \geq x_{vj} \cdot \text{SubgraphFinish}_j \qquad (\forall v) \ (\forall j > 0) \qquad (10)$$

$$\text{SubgraphStart}_j \geq \text{SubgraphFinish}_{j-1} \qquad (\forall j > 0, j \neq 1 \bmod q) \qquad (14)$$

$$x_{vj} \in \{0, 1\} \qquad (\forall v) \ (\forall j)$$

Figure 4: A schema of the Integer Program for latency minimization (non-contiguous splits: q contiguous subgraphs per accelerator).

Our formulation has $O(|V| \cdot k)$ variables and $O((|V| + |E|) \cdot k)$ constraints.

4.1 Non-contiguous splits

Our formulation can be extended to allow every accelerator to hold up to some number q of contiguous subgraphs. We then need to ensure that their processing times in our schedule do not overlap.

We use a modified Integer Program that provides for a customizable extent of non-contiguity. Here, an accelerator can be assigned several subsets of nodes $S \subseteq V$, each of which we will call a *subgraph*. The mode of computation described at the beginning of Section 4 is used for every subgraph. We require every subgraph to be a contiguous set S of nodes.

We index devices/subgraphs as follows. For each accelerator $i = 1, ..., k$ we create q subgraph slots indexed $j = (i-1)q+1, (i-1)q+2, ..., iq$, where q is a customizable degree of non-contiguity that can be adjusted for the workload at hand. The special index $j = 0$ will denote all CPU cores together.

The modified IP formulation is given in Fig. 4.

We discuss the constraints that differ from the contiguous version:

- Constraint (3^*) encodes the requirement that the sum of sizes of nodes in all subgraphs that are placed on accelerator i should be at most M.

- Constraint (14) arises because an accelerator i cannot process more than one subgraph at a time. Therefore we order its subgraphs $j = (i-1)q+1, ..., iq$ by the time when they are processed.

Finally, if collocation constraints are required (e.g. for training), then they should be expressed in terms of devices rather than subgraphs. That is, for two nodes u and v that should be collocated, we write $x_{u0} = x_{v0}$ and for $i = 1, ..., k$, $\sum_{j=(i-1)q+1}^{iq} x_{uj} = \sum_{j=(i-1)q+1}^{iq} x_{vj}$.

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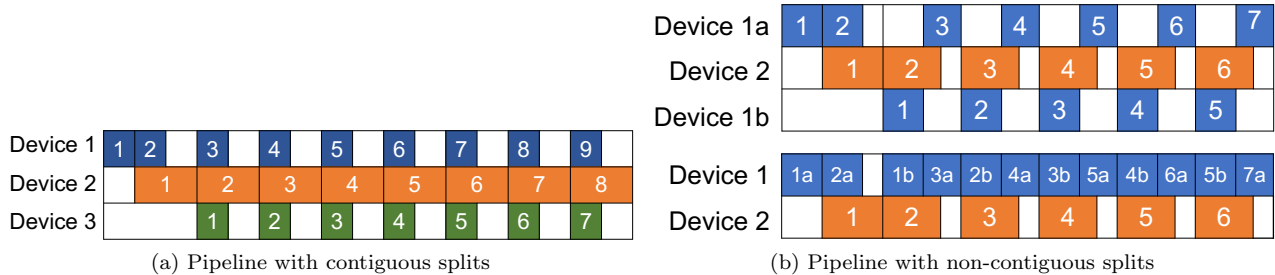(a) Pipeline with contiguous splits (b) Pipeline with non-contiguous splits

Figure 5: Pipelined inference. In these figures x-axis is time, rectangle widths are device loads (processing times for a sample), and numbers 1–9 are input sample/minibatch identifiers. The average time spent per sample is decided by the most loaded and always-busy device. In (b) the non-contiguous subgraph of device 1 can be split into two contiguous subgraphs and thought to be assigned to virtual sub-devices 1a and 1b (that can never be executing at same time). The top and bottom figures in (b) present two equivalent ways to view this schedule.

Our formulation has $O(|V| \cdot q \cdot k)$ variables and $O((|V| + |E|) \cdot q \cdot k)$ constraints.

4.2 Non-pipelined model-parallel training

The algorithm described above can be directly applied to the traditional setting of model-parallel *training* with no pipelining (one sample at a time, as shown in Fig. 2b). In this case the computation graph contains a forward-pass part followed by a backward-pass part. A natural extra requirement is that corresponding forward and backward nodes be placed on the same device, as they operate on the same set of weights. It is easy to express this co-location constraint: for forward and corresponding backward nodes u and v we require $x_{ui} = x_{vi}$ for all i. The contiguity constraint (see Section 4.1 below) should be enforced separately for the forward and the backward parts.

5 Throughput Maximization

The next goal of this work is to provide an algorithm for the setting where the DNN handles a steady stream of samples and the metric of interest is *throughput*. For simplicity we think that there are $n \to \infty$ samples to be processed offline. A schedule of choice in this scenario is model parallelism with *pipelining*. Without pipelining, only one device is active at any given time (see Figs. 2a and 2b), which leads to under-utilization of resources. We remark that pipelining *schedules* that we discuss are essentially due to prior works [HCB+19, NHP+19], which discuss their implementation aspects, statistical efficiency, and demonstrate large real-world gains in time-to-accuracy. Here we focus on *algorithms* to find optimal *splits* for this mode of execution.

We begin by introducing our techniques in the setting of *pipelined inference*, as it is simpler yet allows us to present the main ideas. Next, we will extend them to handle *training* workloads.

5.1 Inference and throughput maximization

Imagine a DNN that has already been contiguously split into subgraphs per device. The question we ask is: How do we schedule the execution of many samples so as to maximize the throughput, or equivalently, minimize the average Time-Per-Sample? To do so, we use pipelined inference, i.e, we build a pipeline out of devices (in the order in which the subgraphs are arranged in the DNN), and we insert consecutive samples into it (see Fig. 5a). Time can be viewed as divided into rounds: each sample spends one round on every device. After a short ramp-up period, the pipeline reaches a steady state, in which the duration of every round is determined by the slowest (most loaded) device. With a batch of n samples, the average Time-Per-Sample

becomes just the maximum load of a device (plus a vanishing $O(1/n)$ term for the ramp-up and ramp-down periods). We remark that this schedule is optimal, in the sense that that this average time cannot be lower: the bottleneck device would need to spend at least ($n \times$ its load) time to process n samples in *any* schedule.

The above discussion shows that the best split is one that minimizes the maximum load of a device. Under this *min-max* objective, it is optimal to balance the load among devices, in contrast to the *min-sum*-like objective of latency minimization. Another difference is that here, when searching for the best split, we do not need to simultaneously optimize for the best schedule (which was done for latency minimization using the Latency$_v$ variables in Section 4) – pipelining gives this for free. Without this scheduling aspect, we are left with a partitioning problem, which is easier to solve.

5.1.1 Dynamic Programming solution

The two main ideas behind our Dynamic Programming (DP) solution are described below. First, if we want contiguous splits, then we can carve out successive device-subgraphs starting from the beginning of the network. At all times, the already-partitioned region will be a downward-closed set that we henceforth call an *ideal*.

Definition 5.1. *We call a set $I \subseteq V$ of nodes an* ideal *if for any $(u, v) \in E$ with $v \in I$ we have $u \in I$.*

It turns out that, going from ideal to ideal, we can obtain every possible contiguous subgraph:

Fact 5.2. *A set $S \subseteq V$ of nodes is contiguous (see Theorem 3.1) if and only if it is the difference of two ideals: $S = I \setminus I'$ where $I' \subseteq I$.*

Proof. **"Only if" direction:** we take $I = \{v \in V : \text{ some node in } S \text{ is reachable from } v\}$ and $I' = I \setminus S$. Clearly I is an ideal and $S = I \setminus I'$; it remains to show that I' is an ideal. For this, take any edge $(u, v) \in E$ with $v \in I'$; we need to show that $u \in I'$. Since $v \in I$, we also have $u \in I$. It remains to show that $u \notin S$. Assume otherwise, i.e., that $u \in S$. Since $v \in I$, some node $w \in S$ is reachable from v. But $v \notin S$; thus the triple (u, v, w) contradicts the contiguity of S.

"If" direction: towards a contradiction assume that there are nodes $u \in S$, $v \notin S$ and $w \in S$ such that v is reachable from u and w is reachable from v. We have $w \in S \subseteq I$ and I is an ideal, so $v \in I$. Since $v \notin S = I \setminus I'$, we must have $v \in I'$. Since I' is an ideal, also $u \in I'$. However, $u \in S = I \setminus I'$, a contradiction. $\square$

General DAGs can contain exponentially many ideals (the worst case being a graph with no edges). Our second insight is that the operator graphs of most modern DNNs, while less and less linear in structure, still contain a manageable amount of branching. This topology ensures a limited number of ideals. Thus, we can consider all possible contiguous sets via Dynamic Programming.

The Dynamic Program. We fill a DP table of dimensions $(k + 1) \times (\ell + 1) \times$ (number of ideals in G), where the cell $\text{dp}[I][k'][\ell']$ is intended to hold the optimal (i.e. smallest) maximum load of a device if we use k' accelerators and ℓ' CPUs to partition the set $I \subseteq V$ of nodes. The initialization, which is $(k', \ell') = (0, 0)$, is easy: the only ideal that we can partition using 0 devices is the empty set, so we have $\text{dp}[I][0][0] = 0$ if $I = \emptyset$ and ∞ otherwise. For $(k', \ell') \neq (0, 0)$ and any I, we iterate over all choices of the subgraph being placed on the last device (which is either a CPU or an accelerator), which are contiguous sets of the form $I \setminus I'$ for an ideal $I' \subseteq I$:

$$\text{dp}[I][k'][\ell'] = \min_{\text{ideal} I' \subseteq I} \min[\max\left(\text{dp}[I'][k' - 1][\ell'], \text{acc}(I \setminus I')\right), \max\left(\text{dp}[I'][k'][\ell' - 1], \text{cpu}(I \setminus I')\right)]$$

with the caveat that if $k' = 0$ or $\ell' = 0$, then we should skip the corresponding branch of the second min. By $\text{cpu}(S)$ and $\text{acc}(S)$ we denote the total load of the corresponding device holding the contiguous set S; thus $\text{cpu}(S) = \sum_{v \in S} p_v^{\text{cpu}}$, and $\text{acc}(S)$ comprises: the incoming communication costs of S ($\sum_v c_v$ over $v \notin S$

with an edge to S), the processing cost $\sum_{v \in S} p_v^{\mathrm{acc}}$, and the outgoing communication costs of S ($\sum_v c_v$ over $v \in S$ with an edge to $V \setminus S$). If S would not fit on an accelerator, i.e., $\sum_{v \in S} m_v > M$, then we instead set $\mathrm{acc}(S) = \infty$.

Runtime and memory usage. The DP table dominates the memory usage, which is $O(\mathcal{I} \cdot (k+1) \cdot (\ell+1))$, where by $\mathcal{I}$ we denote the number of ideals in G. It takes $O(\mathcal{I})$ time to fill one entry of the table. The entire DP solution can be implemented to run in time $O(\mathcal{I}^2 \cdot [(k+1) \cdot (\ell+1) + |V| + |E|])$, where the additional term $\mathcal{I}^2 \cdot (|V| + |E|)$ arises due to computing the costs $\mathrm{cpu}(I \setminus I')$ and $\mathrm{acc}(I \setminus I')$.

Extensions. A similar DP solution is used in PipeDream [NHP$^+$19], albeit only for layer-granularity graphs that are linear (i.e., a path). That work also considers two extensions: replication (where a single subgraph is replicated on multiple devices, creating a hybrid model-parallel/data-parallel split) and hierarchical accelerator topologies (e.g. clusters of GPUs connected internally with faster interconnects). Both of these extensions can also be handled by our DP algorithm, at the costs of $O(k + \ell)$ and $O(\mathcal{I})$ factors in the runtime, respectively. See Appendix C for more details.

5.1.2 Dynamic Programming Solution – Linearization Heuristic (DPL)

The $\mathcal{I}^2$ term in the running time can make the DP solution inefficient for certain DNN workloads that are both large and strongly branching. To deal with this, one can reduce the search space by adding artificial edges to the graph. In particular, we use the following version of this technique: find a Hamiltonian path (in other words, a linear/topological ordering) of the input DAG using a Depth-First Search (DFS) traversal, and add this path of artificial edges. This yields the largest possible reduction of the search space: the resulting graph has only one topological ordering, and thus the number $\mathcal{I}$ of ideals becomes the number $|V|$ of nodes plus 1, giving an $O(|V|^2)$ term instead of $O(\mathcal{I}^2)$. The algorithm so obtained is polynomial-time, but it may not return the optimal solution. In Section 6 we show that it is very close to optimal for most workloads and provides a compelling trade-off between solution quality and runtime. We denote it by DPL in that section.

5.1.3 Integer Programming solution

Our IP formulation is presented in Fig. 6. We index devices as follows: accelerators are assigned indices $i = 1, ..., k$ and CPUs are indexed $i = k + 1, ..., k + \ell$. As in Section 4, we use binary variables x_{vi} to denote whether node v should be placed on device i. The variables CommIn_{vi}, $\mathrm{CommOut}_{vi}$ and constraints (15)–(19) are also analogous to those used in the latency-minimization IP. However, this IP is simpler as, thanks to the maximum-load objective, no scheduling aspect is present. The objective MaxLoad is the maximum over Load_i for all devices i, which is given by constraint (20) for accelerators and (21) for CPUs.

5.2 Non-contiguous splits

Suppose we are given a non-contiguous split of a DNN. We go back to the question from Section 5.1: how to best schedule our workload? Clearly, we still cannot obtain a smaller average time per sample than the max-load.[4] Fortunately, we can still match the max-load using a variant of pipelining. A challenge here is that the device-subgraphs may no longer have a linear or acyclic ordering induced from the input DNN (e.g. in Fig. 1b, neither subgraph comes fully before the other). One possible solution (see Fig. 5b for an example) is to split non-contiguous subgraphs into smaller ones, so that all subgraphs can be topologically ordered, and mentally place them on *virtual devices*; then we build a pipeline of virtual devices. Now we can build a round-based schedule as before, keeping in mind that virtual devices belonging to the same real device cannot process concurrently. The bottleneck device will be the one whose total load (of all virtual devices) is maximal.[5] See Fig. 5b for an example.

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[4]However, the optimal max-load of a non-contiguous split can be lower than the best contiguous one.

[5]This quantity is the original load of that device, independent of the split into virtual devices.

$$\min \quad \text{MaxLoad}$$

$$\text{s.t.} \quad \sum_{i=1}^{k+\ell} x_{vi} = 1 \qquad\qquad (\forall v) \qquad (15)$$

the subgraph $\{v \in V : x_{vi} = 1\}$ is contiguous **(optional)** $\qquad (\forall i) \qquad (16)$

$$M \geq \sum_v m_v \cdot x_{vi} \qquad\qquad (\forall i = 1, ..., k) \qquad (17)$$

$$\text{CommIn}_{ui} \geq x_{vi} - x_{ui} \qquad\qquad (\forall (u,v) \in E) \ (\forall i = 1, ..., k) \qquad (18)$$

$$\text{CommOut}_{ui} \geq x_{ui} - x_{vi} \qquad\qquad (\forall (u,v) \in E) \ (\forall i = 1, ..., k) \qquad (19)$$

$$\text{MaxLoad} \geq \text{Load}_i \qquad\qquad (\forall i)$$

$$\text{Load}_i = \sum_v \text{CommIn}_{vi} \cdot c_v + \sum_v x_{vi} \cdot p_v^{\text{acc}} + \sum_v \text{CommOut}_{vi} \cdot c_v \quad (\forall i = 1, ..., k) \qquad (20)$$

$$\text{Load}_i = \sum_v x_{vi} \cdot p_v^{\text{cpu}} \qquad\qquad (\forall i = k+1, ..., k+\ell) \qquad (21)$$

$$x_{vi} \in \{0, 1\} \qquad\qquad (\forall v) \ (\forall i)$$

Figure 6: A schema of the Integer Program for max-load minimization (throughput maximization). See Theorem 4.1 on how to reformulate constraint (16) to obtain an Integer Program.

(a) GPipe schedule (batch with 4 microbatches).   (b) PipeDream's 1F1B schedule.
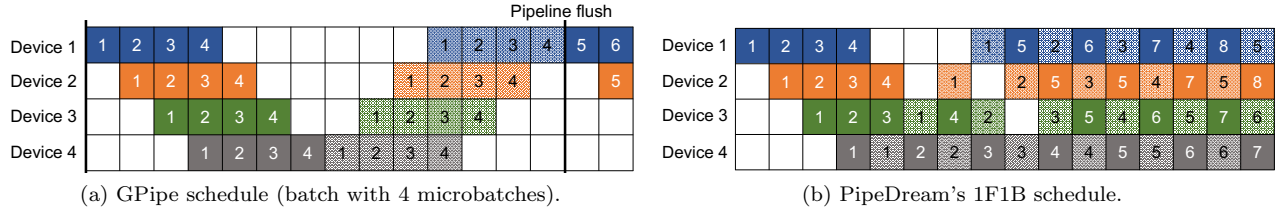
Figure 7: Pipeline-parallel training schedules. For simplicity the load is drawn as equal for all devices and for the forward (darker color) and backward passes (lighter color).

The above discussion shows that our max-load objective does not change when dealing with non-contiguous splits. Our IP solution (Section 5.1.3) "natively supports" the non-contiguous setting, by just removing the contiguity constraint.

5.3   Training and throughput maximization

Pipeline parallelism can be applied to training as well, where the task of processing large numbers of samples (and maximizing throughput) is especially relevant. As discussed at the end of Section 4, computation graphs for training consist of a forward-pass part and a backward-pass part. Certain backward nodes operate on the same state (weights/parameters) as their corresponding forward nodes, and so they must be colocated. Contiguity, if desired, should be enforced separately for the forward and the backward parts; i.e., a device i would hold a contiguous subgraph of the forward part and a contiguous subgraph of the backward part. Let FW_i and BW_i denote their respective loads/costs.

Objective. GPipe [HCB+19] and PipeDream [NHP+19] propose two different pipeline schedules. Our max-load objective function is appropriate for both these schedules. In **PipeDream** – see Fig. 7b – after a short ramp-up period, every device starts alternating between processing a forward sample and a backward sample, which together takes $\text{FW}_i + \text{BW}_i$ time. As before, the device i that maximizes this quantity, i.e., the

load, is the bottleneck that decides the throughput of the system. The **GPipe** schedule, shown in Fig. 7a, first processes all forward samples in a batch, pipelined as they would be for inference; the average time taken for a sample in this pass is $\max_i \text{FW}_i$ (ignoring an $O(1/n)$ term). The backward pass then takes place, with an average time of $\max_i \text{BW}_i$. We thus get the objective $\max_i \text{FW}_i + \max_i \text{BW}_i$; the difference between this and the objective $\max_i \text{FW}_i + \text{BW}_i$ is insignificant, as we argue in Appendix A. For *non-contiguous splits*, both types of schedules can be modified in the same vein as in Section 5.2.

Next we describe how to extend our algorithms from Section 5.1 for training workloads.

Integer Programming: Our IP solution handles training graphs out-of-the-box; the only required modification is that we apply the contiguity constraint (16) separately for the forward and the backward parts (if desired).

Dynamic Programming: Our DP algorithm can only find contiguous splits, but now most devices need to be assigned two contiguous subgraphs (backward and forward). Our solution is to run the DP only on the forward part, but taking the corresponding backward nodes together with every considered contiguous subgraph (we also count their cost). Some care is required to make sure that we assign those backward nodes that do not have a corresponding forward node, and that we only consider those contiguous subgraphs on the forward side whose corresponding backward nodes also form contiguous subgraphs. See Appendix B for more details.

6 Experiments – Throughput Maximization

In this section we evaluate our throughput maximization algorithms on the following modern DNN models for inference and training: BERT (with 3, 6, 12, and 24 Transformer layers), ResNet50, Inception-v3, and GNMT. The results for latency minimization can be found in Section 7.

We reiterate that we do not evaluate a particular pipelining system, but *algorithms* to find high-quality splits for pipelined executions. However, we remark that our max-load objective function (cost model) is a natural generalization of that of PipeDream, which has been shown [NHP+19, Figure 15] to closely reflect real performance.

The code and workloads used for evaluations are available at
`https://github.com/msr-fiddle/dnn-partitioning`.

Inputs (workloads). We evaluate our algorithms on diverse and widely used deep learning workloads ranging from transformer models (BERT) and convolutional neural networks (ResNet, Inception) to translation LSTM-based models (GNMT). We exported BERT [VSP+17] and ResNet [HZRS15b] operator graphs through the ONNX Runtime library [ONN20]. It allows exporting the operator graph topology for deep learning models by taking as input their forward pass and appending the corresponding backward pass to generate an output in ONNX format. We obtained all the layer graphs from previous work [HNP+18].

Our inputs correspond to the following deployment scenarios for these workloads. The DNN workloads are split across 6 accelerators of the same type (GPU for layer graphs, a hardware accelerator representing TPUs or FPGAs for operator graphs). We use 3 accelerators in case of the smaller BERT-3 and BERT-6 models. Each accelerator has 16 GB of DRAM and is connected to the CPU over a PCIE 3.0 interconnect. To assign a cost to each node and edge in the graph, we profile the workloads on GPU for layer workloads, and we estimate the numbers for the operator graphs for the hardware accelerator. We then convert the topology of each graph to a JSON format, comprising all the relevant information about the graph that is required of an input instance of our algorithms (see Section 3). For our Dynamic Programming solution, we run several preprocessing steps before we can apply our basic method; see Appendix B for more details.

Algorithm execution setup. All our experiments are executed (that is, the optimization algorithms that we develop are run) on a machine with an Intel Xeon E5-2673 v4 CPU and 64 GB of RAM running Ubuntu

Workload	Nodes	DP (contiguous)			IP (contiguous)		IP (non-contiguous)			DPL	Expert	Local search	PipeDream	Scotch
		Ideals	Runtime	TPS	Runtime	TPS	Runtime	TPS	Gain	TPS	TPS	TPS	TPS	TPS
Operator-granularity graphs, pipelined inference														
BERT-3	235	1428	**1s**	27.92	**1s**	27.92	2s	21.91	27%	27.92	-	24.32	-	35.94
BERT-6	418	1923	5s	29.58	**4s**	29.58	54s (3s*)	28.33	4%	29.58	-	42.52	-	49.80
BERT-12	783	2906	**19s**	147.48	11m (1m*)	147.48	>20m (18s*)	130.03	13%	147.48	-	257.38	-	230.12
ResNet50	604	241	**0s**	124.35	15s	124.35	1m (10s*)	124.35	0%	124.35	-	250.08	-	197.84
Operator-granularity graphs, pipelined training														
BERT-3	600	2774	8s	65.30	2s	65.30	**1s**	54.21	20%	65.30	-	66.17	-	416.97
BERT-6	1071	3776	25s	72.86	**6s**	72.86	13m (2s*)	71.64	1%	79.50	-	94.86	-	130.20
BERT-12	2012	2938	**1m**	438.00	>20m (1m*)	438.00	>20m (1m*)	373.42	17%	438.00	-	737.99	-	800.79
ResNet50	1243	258	**2s**	255.19	2m (28s*)	255.19	7s	255.19	0%	255.19	-	530.95	-	379.21
Layer-granularity graphs, pipelined inference														
BERT-24	32	30	**0s**	17.79	1s	17.79	>20m (1s*)	17.71	0.4%	17.79	20.08	17.80	17.79	18.03
ResNet50	177	242	**0s**	33.77	48s	33.77	14s	33.31	1.3%	33.77	43.92	35.63	39.38	34.50
InceptionV3	326	36596	32m	51.55	3m	51.55	**19s**	51.52	0%	51.55	102.48	54.03	60.42	54.01
GNMT	96	17914	29s	32.91	**4s**	32.91	9s	31.68	4%	32.91	46.21	31.75	33.03	34.92
Layer-granularity graphs, pipelined training														
BERT-24	64	30	**0s**	41.75	1s	41.75	9s	39.79	5%	41.75	49.40	39.93	41.75	42.01
ResNet50	354	242	**1s**	78.63	45s	78.63	15s	76.65	3%	78.65	112.11	81.32	83.67	80.10
InceptionV3	652	36596	58m	122.76	8m	123.35	**43s**	117.72	5%	123.93	213.65	122.80	128.32	128.32
GNMT	192	17914	42s	107.00	4s	107.00	**1s**	88.47	21%	107.00	137.15	91.52	107.35	107.00

Table 1: Pipelined workloads for maximization of throughput / minimization of Time-Per-Sample (TPS, equal to max-load). We run the IP optimizer until it guarantees a solution within 1% of the optimum, but no longer than 20 minutes. The parenthesized times with asterisks denote the time it took the optimizer to find the solution of the final value (though it could not yet guarantee its near-optimality). DPL stands for the DP with the Linearization heuristic (see Section 5.1.2), which always runs under 3 seconds. The fastest non-DPL runtime for every input is in bold.

18.04. The Dynamic Programming solution is implemented in C++ and compiled with gcc 7.4 using the `-O3` optimization flag; it is a sequential (single-threaded) implementation. The Integer Programming formulations are solved using Gurobi 8.1 [GO19], which runs on 4 CPU cores. The IP models are constructed using Gurobi bindings for Python; the runtime of this construction is insignificant.

Baselines used for comparison. We use the following baselines to compare our solutions:

- **Hand-crafted placements**, similar to [MGP+18, GCL18, ABVG+19]. This is still a widely used means for device placement. We perform expert splits only for layer graphs, as the operator graphs with their much stronger branching are infeasible to split manually. In line with prior work [SVL14, WSC+16], for GNMT we place each LSTM layer on a separate GPU, and then balance between 6 devices. We proceed similarly with BERT-24. In ResNet50 and Inception-v3, we split the convolution, batch normalization, and ReLu layers equally among all devices.

- **Scotch** [Pel09], a graph partitioning software used for mapping computation graphs onto devices in a balanced way, taking communication costs between dependent nodes into account. The output splits are not guaranteed to be contiguous.

- **Local search** [MKA07] is a heuristic that starts from a random split and repeatedly makes the best single-node reassignment until a local optimum is reached. We restart 10 times and take the best solution. Note that this almost always yields a non-contiguous split.

- **PipeDream** [NHP+19]'s optimizer only supports layer graphs, thus we only run it on our layer workloads. It requires the input to be a linear path, thus it contracts all branchings to single nodes.

Workload	DP	IP (contiguous)	IP (non-contiguous)	DPL	Expert	Local search	PipeDream	Scotch
Operator-granularity graphs, pipelined inference								
BERT-3	1.00×	1.00×	1.27×	1.00×	-	1.15×	-	0.78×
BERT-6	1.00×	1.00×	1.04×	1.00×	-	0.70×	-	0.59×
BERT-12	1.00×	1.00×	1.13×	1.00×	-	0.57×	-	0.64×
ResNet50	1.00×	1.00×	1.00×	1.00×	-	0.50×	-	0.63×
Operator-granularity graphs, pipelined training								
BERT-3	1.00×	1.00×	1.20×	1.00×	-	0.99×	-	0.16×
BERT-6	1.00×	1.00×	1.02×	0.92×	-	0.77×	-	0.56×
BERT-12	1.00×	1.00×	1.17×	1.00×	-	0.59×	-	0.55×
ResNet50	1.00×	1.00×	1.00×	1.00×	-	0.48×	-	0.67×
Layer-granularity graphs, pipelined inference								
BERT-24	1.00×	1.00×	1.00×	1.00×	0.89×	1.00×	1.00×	0.99×
ResNet50	1.00×	1.00×	1.01×	1.00×	0.77×	0.95×	0.86×	0.98×
InceptionV3	1.00×	1.00×	1.00×	1.00×	0.50×	0.95×	0.85×	0.95×
GNMT	1.00×	1.00×	1.04×	1.00×	0.71×	1.04×	1.00×	0.94×
Layer-granularity graphs, pipelined training								
BERT-24	1.00×	1.00×	1.05×	1.00×	0.85×	1.05×	1.00×	0.99×
ResNet50	1.00×	1.00×	1.03×	1.00×	0.70×	0.97×	0.94×	0.98×
InceptionV3	1.00×	1.00×	1.04×	0.99×	0.57×	1.00×	0.96×	0.96×
GNMT	1.00×	1.00×	1.21×	1.00×	0.78×	1.17×	1.00×	1.00×

Table 2: Throughput maximization results, same as in Table 1 in Section 6, but presented in terms of throughput improvement in relation to the DP (Dynamic Program, contiguous splits) being 1×. For example, on BERT-3 inference operator-graph, the best non-contiguous split offers 1.27× the throughput of the best contiguous one, and Scotch gives 0.78× the throughput of the best contiguous one. In addition, we show the single-accelerator throughput (placing the entire DNN workload on one accelerator). See Figure 8 for a graphical representation of data in this table.

6.1 Results

Table 1 shows each workload, the number of nodes (operators or layers) in the graph, runtimes of our algorithms, and the average Time-Per-Sample (TPS) – that is, the maximum device load, which is inversely proportional to throughput – of the found splits. We also report the gain of best non-contiguous splits over best contiguous splits, and the TPS of the baselines. For better understanding of the DP runtimes we show the number of ideals in the forward part of each DNN. We also present the same results in an equivalent form, displaying the throughput advantages obtained by our algorithms with respect to baselines. See Table 2 on page 14 and Fig. 8 on page 15. Also, see Fig. 9 for an illustration of an example pair of optimal contiguous (top) and non-contiguous (bottom) splits of an operator-level graph (BERT-3) that are returned by our algorithms.

Below we discuss the main takeaways.

DP vs. IP (optimality, efficiency). DP and IP (contiguous) both return the optimal split, so their TPS/max-load values are equal (up to a 1% IP optimality threshold). The optimization problems we solve are computationally hard, and our algorithms are exponential-time in general; however, we see that their runtimes are reasonable on real-life DNN inputs due to their workload structure. For our IP solution we used a commercial-grade solver [GO19] that ran on 4 CPU cores. The efficiency of free software solvers is much worse. It is worth noting that most of the runtime is often spent on certifying the near-optimality of the found solution; it would therefore be reasonable to cut the computation much sooner, still obtaining high-quality solutions. For the DP solution we created a single-core, self-contained implementation. Its runtimes are very competitive with those of the IP, except for the most branching models such as Inception-v3. We remark that

(a) Operator graphs, inference

(b) Operator graphs, training

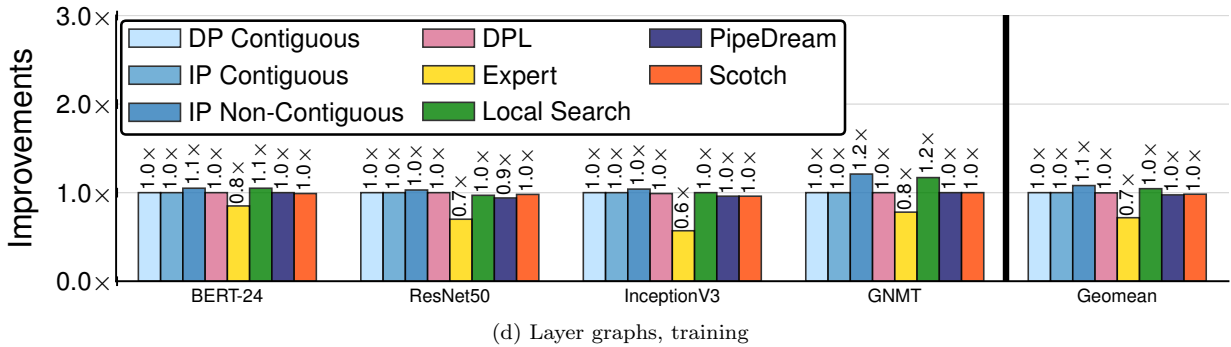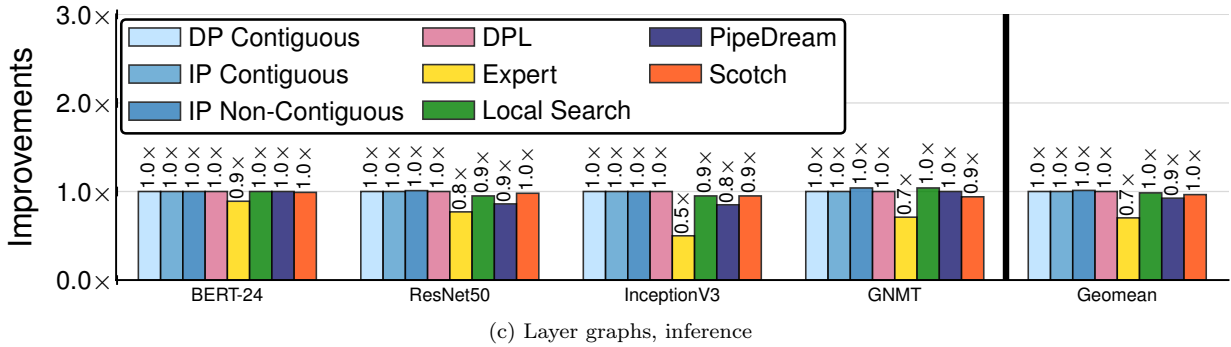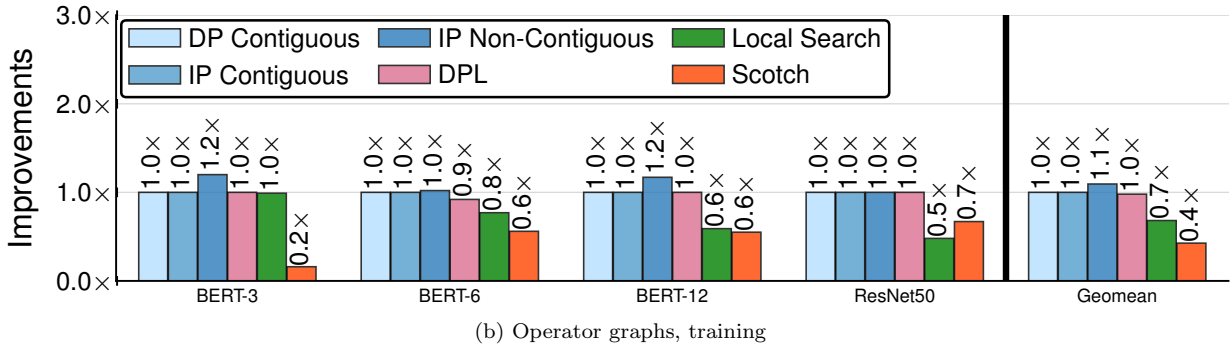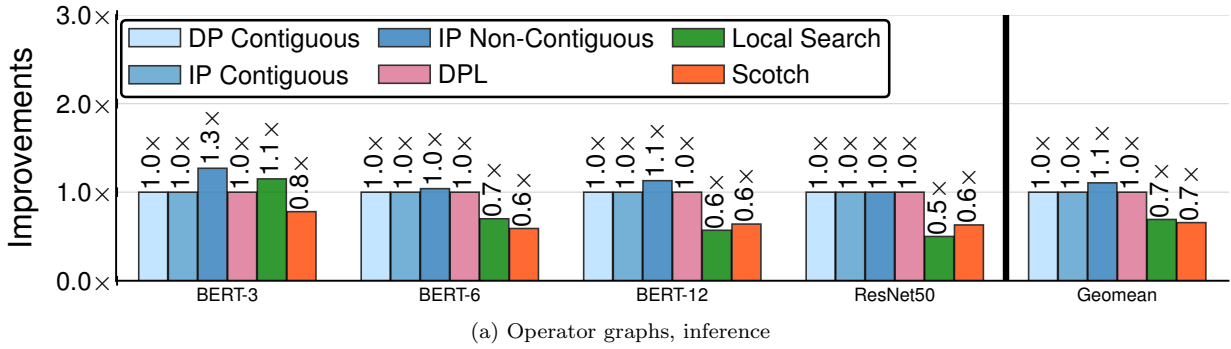(c) Layer graphs, inference

(d) Layer graphs, training

Figure 8: An illustration of throughput maximization results from Table 2, with DP (contiguous) serving as 1×. The blue bars are algorithms from this work, whereas the non-blue-colored bars show baselines. Plots (a) and (b) represent throughput improvements for operator-level graphs, and (c) and (d) for layer-level graphs.
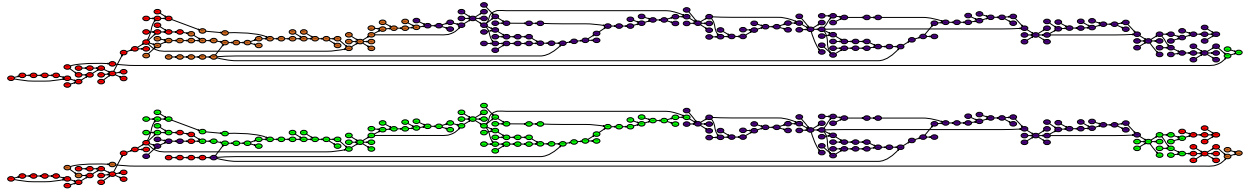
Figure 9: Optimal contiguous (top) and non-contiguous (bottom) splits of the BERT-3 operator-level inference graph onto 3 accelerators and 1 CPU (for throughput maximization). Each node is colored based on its placement – red color indicates CPU placement, and each remaining color indicates a different accelerator. The non-contiguous split achieves a 27% higher throughput. If viewed on a computer, the figures can be zoomed in to an arbitrary degree for better inspection.

in practice the DP runtime is dominated by the $O(\mathcal{I}^2|E|)$ term and does not depend much on the numbers k, ℓ of devices unless these are very large; in contrast, increasing the number of accelerators can have a large impact on the IP runtime (e.g. having 6 rather than 3 accelerators for the BERT-3 inference workload causes the IP runtime to jump from 1s to 27s). Moreover, the DP runtime does not depend on the node weights, whereas the IP runtime does.

DPL (DP with the Linearization heuristic) (see Section 5.1.2). The DPL solution runs in time essentially $O(|V|^2|E|)$, which for our workloads is at most seconds. Crucially, the restricted search space results in a throughput loss of 9% for the BERT-6 training workload, 1% loss for InceptionV3 training, and no loss for all other workloads. Therefore, DPL would be our method of choice for very large graphs; it would be able to process graphs with tens of thousands of nodes within, say, an hour.

Contiguous vs. non-contiguous splits. Our IP solution is able to find optimal non-contiguous splits. To the best of our knowledge, our work is the first one to examine *non-contiguous splits* for pipelined model parallelism; thus we use our experiments to evaluate the potential gains in throughput. We observe that on average, the best non-contiguous splits offer an ∼10% gain over the best contiguous splits; for BERT-3, the gain is as large as 20-27%.

Comparison to other baselines. *As seen in Table 1, our non-contiguous splits outperform all the techniques, with an improvement of up to 2× over **hand-crafted expert** splits (average 1.46×), 2.08× over **local search** (average 1.29×), 1.21× over **PipeDream** (average 1.10×), 7.69× over **Scotch** (average 1.50×).* Hand-crafted expert placements for the layer-based graphs provide 71% and 68% of the throughput in comparison to contiguous and non-contiguous splits, respectively. At the layer granularity, some workloads have a repetitive graph structure, which can be split manually across devices, yet this turns out to be not enough to obtain optimality. Furthermore, performing a reasonable human split over operator graphs is infeasible due to the large branching and number of nodes. Local search fares badly, underscoring the difficult, non-local structure of the optimization problem, which is also resistant to the heuristics used by Scotch. Finally, PipeDream only considers *linear* layer graphs and contracts branchings in the input graph; whereas our technique that does not contract branches is able to explore a larger search space for operator placement and achieve up to 1.21× higher throughput.

6.2 Advantage of operator vs. layer graphs

In this section we measure the throughput advantage that can be obtained by using finer-granularity operator graphs in lieu of layer graphs. No conclusions on this matter can be drawn from the experimental results

Workload	DP (run on original operator graph)	DP (run on contracted layer graph)	Gain
Operator-granularity graphs, pipelined inference			
BERT-3	27.92	27.92	0%
BERT-6	29.58	29.58	0%
BERT-12	147.48	159.43	8%
ResNet50	124.35	129.15	4%
Operator-granularity graphs, pipelined training			
BERT-3	65.30	65.30	0%
BERT-6	72.86	72.86	0%
BERT-12	438.00	465.41	6%
ResNet50	255.19	269.63	6%

Table 3: Throughput maximization; throughput advantage of optimization on the operator-granularity level vs. the layer-granularity level (see Section 6.2), for optimal contiguous splits. The numbers shown are TPS (time-per-sample).

of Section 6 or Section 7 alone, as our operator-graph and layer-graph workloads are disjoint.[6] Therefore we proceed as follows: for each operator-graph workload, we manually annotate all nodes to group them into corresponding layers. Then we contract each layer and run the DP algorithm on the layer-graph thus obtained.

We present the results of this experiment in Table 3. We compare the optimal contiguous splits. The results show that finding the best split on the more precise operator level results in a throughput advantage of up to 8%.

7   Experiments – Latency Minimization

In this section we evaluate our Integer Programming (IP) based algorithm for latency minimization. We consider the most relevant deployment scenario: single-sample inference with memory-bound accelerators (that is, when the entire model does not fit on one accelerator). We run our algorithm for the same inference workloads as in Section 6. As before, we use Gurobi to solve our IP formulation. The code and workloads used for evaluations are available at `https://github.com/msr-fiddle/dnn-partitioning`.

Devices, implementation, experimental setup.   We run experiments on the same inference workloads as in Section 6. However, to model a memory-bound deployment scenario where splits are necessary to fit the DNN, we assume an accelerator DRAM size of either 600 MB (for smaller DNNs, of size at most 3.6 GB) or 2 GB (for larger DNNs, of size at least 9 GB), and a number of accelerators such that the total accelerator memory is 1.4–1.8 times the size of the DNN. Note that this implies, in particular, that a single-accelerator split is not feasible for any of our workloads. In keeping with the mild assumption made at the beginning of Section 4, we assume 8 CPU cores. We use our IP solution to optimize for the best contiguous split. Other implementation details are similar as in Section 6.

Baselines.   We compare our IP algorithm against four baseline solutions. The **first** is the following **greedy** algorithm:

- contract colocated nodes and any strongly connected components that arise (as in Appendix B),

- fix a topological ordering of the nodes,

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[6]Even though the ResNet50 DNN architecture appears in both lists, these input graphs come from different sources; the layer-graph ResNet50 has runtimes profiled on a GPU, while the operator-graph ResNet50 has runtimes estimated for a non-GPU hardware accelerator. Thus the corresponding results are incomparable.

Workload	Nodes	Greedy	Max-load DP	Scotch	Expert	IP			
		Latency	Latency	Latency	Latency	Latency	Runtime	MIP Gap	Gain
Operator-granularity graphs, single-query inference									
BERT-3	235	416.20	415.90	497.75	-	**408.47**	3m (6s*)	<1%	1.8%
BERT-6	418	494.13	445.48	564.61	-	**438.06**	>1h (1m*)	12.6%	1.7%
BERT-12	783	867.84	1327.03	1755.41	-	**729.56**	>1h (10m*)	93.8%	19.0%
ResNet50	604	839.54	1123.65	857.73	-	**672.06**	>1h (7m*)	54.0%	24.9%
Layer-granularity graphs, single-query inference									
BERT-24	32	**100.22**	108.03	108.03	111.94	**100.22**	14s (1s*)	<1%	0.0%
ResNet50	354	4197.06	1443.79	3610.87†	OOM	**1191.02**	>1h (19m*)	93.1%	21.2%
InceptionV3	652	2485.24	1621.74	3068.00†	OOM	**1318.08**	>1h (43m*)	93.5%	23.0%
GNMT	192	268.50	244.33	636.91†	293.40†	**225.6**	3m (1m*)	<1%	8.3%

Table 4: Single-sample inference workloads for latency minimization. We run the IP optimizer until it guarantees a solution within 1% of the optimum, but no longer than 60 minutes. Where the optimization was terminated after 60 minutes, we report the optimality gap that the solver was able to certify at that time. The parenthesized times with asterisks denote the time it took the optimizer to find a solution within 2% of the final value (though it could not yet guarantee its near-optimality). We also report the latencies obtained by the four baselines described in Section 7; their running times are always under 0.5s (Greedy, Scotch) or the same as reported in Section 6 (Max-load DP). Daggers† denote a slight (between 20% and 34%) violation of the memory constraints, and "OOM" denotes a major violation (more than a factor 3×). The best latency for each workload is given in bold. In the column "Gain" we report the advantage of our IP algorithm's solution over the best baseline.

- for every available accelerator, place as many nodes (in the topological order above) as will fit on the accelerator,

- place any remaining nodes on the CPU.

The greedy algorithm returns a contiguous split that is feasible (i.e. satisfies the memory size constraints). For all our test workloads, it is able to place all nodes on accelerators (thus it does not use the CPU). However, it does not take processing times or communication costs into account when selecting the split. The runtimes of this baseline are under 0.5s.

Our **second** baseline is meant to answer the following question: *If we obtain splits by optimizing the max-load objective, as we would for the throughput maximization task (that pertains to the pipelined setting), are they "good" in terms of minimizing latency as well?* Therefore, we obtain contiguous splits by running the **max-load DP** algorithm of Section 5.1.1, and then we report the single-sample latency that they obtain. The runtimes of this baseline are essentially the same as those of the max-load DP reported in Section 6 for the corresponding DNNs.

The **third** baseline is **Scotch** [Pel09], a graph partitioning software used for mapping computation graphs onto devices in a balanced way, taking communication costs between dependent nodes into account (used also in Section 6). It produces non-contiguous splits.

The **fourth** baseline are **human-expert** placements, the same as used in Section 6.

We do not compare against a local search heuristic, as it is not clear how to design one that satisfies the memory bounds.

7.1 Results

Table 4 shows each workload, the number of nodes (operators or layers) in the graph, and the latencies found by our IP algorithm and by the baselines. We also report running times.

As we remarked in Section 5, the latency minimization task is significantly harder than throughput maximization as it contains a scheduling component. This is reflected in the performance of our IP algorithm:

for five out of eight workloads used, the IP solver did not converge to certified (near-)optimality within 1 hour. However, it still comes out far ahead:

- The IP, even where it could not prove that it has found an optimal solution, does no worse than the baselines. In fact, it outperforms the best of them by a margin of around 20% in terms of the solution value (latency) for half of the considered workloads.

- Similarly as for max-load minimization (Section 6), we note that the solution quality improves slowly over time, and most of the runtime is often spent on certifying the near-optimality of the found solution; it would therefore be reasonable to cut the computation much sooner, still obtaining high-quality solutions.

- In particular, for each workload it took the IP solver at most 7 minutes to match the solution quality of the best baseline.

Comparison to baselines.

- **Greedy**: our algorithm achieves latency lower by up to 72% (i.e., over 3× faster inference; 23% lower latency on average).

- **Max-load DP**: the latency-IP achieves lower by up to 42% (17% on average). This shows that the best splits for latency minimization are, indeed, different from the best splits for max-load minimization (throughput maximization for pipelined settings). Still, the max-load DP turns out to be the best baseline in 5 out of the 8 cases, showing some degree of compatibility between the two objectives.

- **Scotch**: our algorithm achieves latency lower by up to 67% (40% on average). In fact, Scotch never does better than the greedy heuristic. Furthermore, as it does not balance devices with respect to memory usage, it violates the memory constraints by up to 34% in some cases.

- **Human expert** splits: as in Section 6, we provide them for layer graphs only, due to the large node counts and high branching of operator graphs. As the expert splits were not designed with our strictly memory-bound scenario in mind, two of them are unbalanced with respect to memory usage, violating the size constraints by more than a factor 3×. For the other two, our algorithm achieves latency lower by up to 23% (17% on average).

8   Conclusions

In this paper we give algorithms for the problem of model partitioning of DNN workloads. They target both inference and training, and optimize the objectives of either minimizing latency or maximizing throughput. Our work follows a principled algorithmic approach, in which we identify the "right" combinatorial optimization problem to solve, and find *provably optimal* splits. While other approaches struggle to capture long-term dependencies in the graph and require trying large numbers of placements on the target system, we solve the global, end-to-end joint placement and scheduling problem in one shot. Our algorithms are efficient and can be run on arbitrary DAGs, including operator-granularity graphs, and are hardware-platform agnostic. Experiments show that they outperform human experts and significantly improve over state-of-the-art methods.

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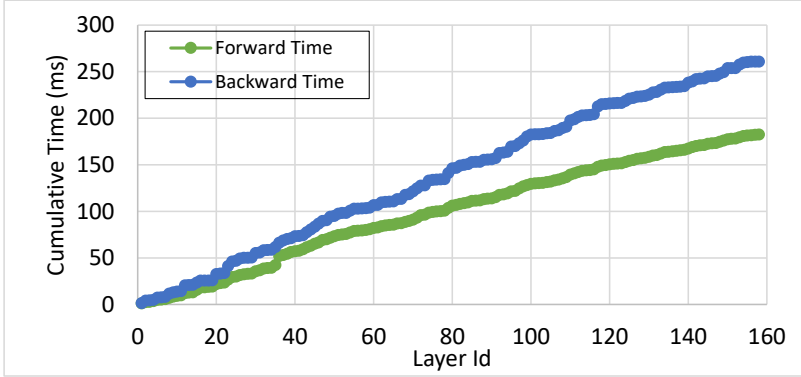
Figure 10: Cumulative training time for forward and backward layers of ResNet50 (layer graph). The time accumulates with each layer progressively, that is, the i-th entry is the sum of processing times of layers from 1 to i.

A Objective Functions Across Schedules

In Section 5.3 we have argued that for PipeDream schedules, the objective function that accurately reflects the quality of any split, that is, the average time taken per sample (inverse throughput), is $\max_i(\mathrm{FW}_i + \mathrm{BW}_i)$, where FW_i and BW_i are the respective loads/costs of the forward and the backward subgraph associated with device i. This is the objective function that we minimize in both our IP and DP solutions.

In the case of GPipe schedules, we have argued that the objective function can be formulated as $\max_i \mathrm{FW}_i + \max_i \mathrm{BW}_i$. This is equal to the former if the maximizing i's are the same – that is, if the bottleneck device is the same for the pipelined forward pass (the first seven columns in Fig. 7a) as for the pipelined backward pass (the next seven columns).

This usually holds true for real-world DNN workloads due to three factors described below:

- For any device, its forward subgraph S and its backward subgraph S' contain paired nodes; that is, most nodes in the backward subgraph S' have a corresponding forward node, which, due to colocation constraints, will be in S, and vice versa. For instance, most forward nodes operate on a set of weights, for which the backward pass then computes gradients and weight updates.

- The processing and communication times of such corresponding/colocated nodes are correlated; for example, if the forward node corresponds to a matrix multiplication, then the processing times of both forward and backward nodes will grow with the size of the matrix.

- In fact, GPipe uses a re-materialization technique [CXZG16] to save memory: it discards stashed activations generated in the forward pass (needed later in the backward pass), and instead reruns the forward pass operators in the backward pass to re-materialize the required stashed activations for the backward operators. If this is reflected in the DNN workload operator-graph or layer-graph, then it further increases the aforementioned correlation between forward and backward times.

In Fig. 10 we plot cumulative forward and backward times for an example training workload (that does not use re-materialization), which grow at a similar pace. These runtimes have been profiled on a GPU.

The above discussion motivates the use of our objective $\max_i(\mathrm{FW}_i + \mathrm{BW}_i)$ as a proxy for the objective $\max_i \mathrm{FW}_i + \max_i \mathrm{BW}_i$ also in the case of GPipe schedules. Nonetheless, our IP solution can also be adjusted to optimize the latter objective. Unsurprisingly, we empirically find that splits found by optimizing either objective differ by at most 6% when using re-materialization.

B DP Preprocessing and Reductions

DP preprocessing. In our Dynamic Programming solution we need to handle colocation constraints given in the input: certain pairs of nodes operate on the same state and thus they are required to be on the same device. A common scenario where this arises concerns forward and backward nodes that operate on the same set of weights, but pairs of forward nodes (or pairs of backward nodes) can also be colocated. In the input files this is expressed via the `colorClass` field: nodes of the same color class must be placed on the same device.

Moreover, for training workloads, the DP can natively find only contiguous splits, but now most devices need to be assigned two contiguous subgraphs (backward and forward). Therefore we run the DP only on the forward part, but we take the corresponding backward nodes together with every considered contiguous subgraph. However, some care is required to make sure that we assign those backward nodes that do not have a corresponding forward node; we call these backward nodes *orphaned*.

For the reasons outlined above, our solution needs to run a series of preprocessing steps before the core DP method can be applied:

- For every color class $C \subseteq V$, i.e., a set of nodes that must be colocated, let C_{FW} and C_{BW} be the forward and backward nodes in C, respectively (so that $C = C_{\mathrm{FW}} \cup C_{\mathrm{BW}}$). We *contract* each set C_{FW} and each set C_{BW} (that is, we compress each of them into a single node; this new node will be forward for C_{FW} and backward for C_{BW}).

- The input graph was guaranteed to be acyclic at the beginning, but the new contracted graph may no longer be acyclic. For instance, there could be a path u, v, w where u and w are colocated (but not v); then the contracted graph will have edges in both directions between v and the new node corresponding to $\{u, w\}$. In the original graph, any colocation-respecting contiguous split would need to contain all of u, v, w in a single subgraph; more generally, every strongly connected component in the contracted graph needs to be colocated. Therefore, we contract all strongly connected components. Now the contracted graph is again acyclic.

- Later, when we run the DP, while considering a subgraph S of forward nodes we will consider the subgraph S' of their corresponding backward nodes at the same time, and take the total computation and communication cost of $S \cup S'$ into account. Thus, when we have assigned all forward nodes, we will have also assigned all backward nodes that are not orphaned. However, orphaned nodes would not be assigned to any subgraph/device.

  To prevent this behavior, we introduce new artificial forward nodes, to be images of the orphaned backward nodes. When the DP decides where to place these new forward nodes, it will also have decided the placement of the orphaned backward nodes. (At the end we will remove the artificial nodes from the final split.)

  However, if the new nodes are isolated (have no adjacent edges), then the number of ideals grows exponentially[7]; furthermore, as the placement of the new forward and orphaned backward nodes is arbitrary, we may end up with non-contiguous splits on the backward side.

  To deal with these issues, we also add new artificial edges adjacent to the new artificial nodes. Since backward nodes and edges mostly resemble a mirror image of their corresponding forward nodes and edges, we add the new edges in such a way as to also build such a mirror image. Namely, for a backward edge (u', v') where at least one of u', v' is orphaned, we add a forward edge (v, u), where u and v are the forward images of u' and v' respectively (note that at least one of u, v is a new artificial node).

After these preprocessing steps, we can use our core DP method on the contracted graph. Once this is done, we map the resulting splits back to the original graph and return the result. For more details on implementation, see the attached code and the comments therein.

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[7]Suppose we have introduced r such new nodes; since each of them is free to be or not be in an ideal, the number of ideals grows by a factor 2^r, and the DP runtime, which depends on the number of ideal pairs I', I with $I' \subseteq I$, grows by a factor 3^r.

We remark that due to our preprocessing steps, the number of ideals may sometimes be smaller than the number of nodes in the initial input graph (this happens for several of our workloads in Table 1).

Non-uniform outgoing communication costs. In the case of operator graphs, the input files for our solvers are created based on ONNX computation graphs. There, communication costs are given on edges, rather than on nodes as we require in our model (see Section 3). In the vast majority of cases, all edges going out of the same node u have the same cost, and we can set that cost as parameter c_u. However, sometimes there could be two or more edges with different costs going out of the same node in an ONNX graph; this situation corresponds to e.g. sending different parts of the operator's output to different operators. In this case, we perform the following reduction:

Suppose that u has outgoing edges to nodes $v_1, v_2, ..., v_r$ with possibly different edge costs $d_1, d_2, ..., d_r$. For every outgoing edge (u, v_j), we *subdivide* it: insert a new node w_j in the middle and replace the edge (u, v_j) with two edges (u, w_j) and (w_j, v_j). The new node w_j should have $p_{w_j}^{\text{cpu}} = p_{w_j}^{\text{acc}} = m_{w_j} = 0$ and be colocated with u. We set $c_{w_j} = d_j$. Finally, set c_u to any value, say ∞; this communication cost will never be paid in any feasible solution, as now u is colocated with all of its successors, which are $w_1, w_2, ..., w_r$.

After obtaining a final split, we may remove the artificial nodes w_j from the solution. It is easy to see that the way we have set the outgoing communication costs c on nodes reflects the edge-communication costs given in the input ONNX graph.

C   Extensions

In this section, which deals with throughput maximization (i.e. the pipelined setting), we briefly explain how to adjust our model and solutions so as to account for certain different or more complex deployment scenarios that appear in related work or in practice.

C.1   Interleaving Communication and Computation

Throughout the paper we have assumed that accelerators are invoked when their inputs are ready, at which point they are transferred to the accelerator memory; next, computation takes place; next, outgoing transfers take place (see Section 3). After that, the in-transfer for the subsequent sample/minibatch may begin, and so on. For this reason, the load of a device is defined as the *sum* of the computation cost and the communication cost. However, it is also reasonable to assume that communication (data transfers) may proceed in parallel to computation, at least for different samples. For instance, once we have finished the in-transfer for sample 1, we might simultaneously start the processing of sample 1 and the in-transfer for sample 2. This is the setting considered in the PipeDream paper [HNP+18].

Both of our solutions (DP and IP) can be easily adjusted to this setting: one just needs to define the load of a device as the *maximum* of the computation cost and the communication cost, rather than the sum. In terms of pipeline schedules, one can think of splitting the device into two virtual devices, one holding the communication portion of the load and the other holding the computation portion, that *can* be processing at the same time. Then either virtual device could be a bottleneck in the pipeline.

In fact, one can further assume that the in-transfer and the out-transfer are done over separate channels (full-duplex communication); then a maximum of three quantities (in-transfer cost, computation, out-transfer cost) should be used.

C.2   Replication

An alternative to model parallelism is data parallelism: an approach where the entire model is replicated over multiple devices that process minibatches in parallel. When using this approach, the communication cost associated with synchronizing the parameters of the entire model proves to be very high for many DNN workloads. Nevertheless, it can also yield large gains for other workloads, especially sparser ones (with a small number of parameters relative to computation cost). PipeDream [HNP+18] proposed a hybrid

model-parallel/data-parallel approach, where we form a pipeline, but certain subgraphs in this pipeline can be *replicated* over multiple devices. This allows the automated partitioner to replicate those fragments of the network that will reap the most benefit while keeping synchronization costs low.

We can also introduce this capability into our DP algorithm. When the DP decides whether to place the currently considered subgraph on a CPU or on an accelerator, now it will also decide how many devices to use. That is, in the DP relation, where previously we had $\max{(\mathrm{dp}[I'][k'-1][\ell'], \mathrm{acc}(I \setminus I'))}$, now we write[8]

$$\min_{k''=1}^{k'} \max{(\mathrm{dp}[I'][k'-k''][\ell'], \mathrm{acc}(I \setminus I', k''))},$$

where $\mathrm{acc}(I \setminus I', k'')$ is the average time per sample for this subgraph when replicated over k'' accelerators. In absence of weight synchronization, this average time would be just $\mathrm{acc}(I \setminus I')/k''$. Weight synchronization (assuming efficient AllReduce collective communication) contributes a term $\left((k''-1) \cdot \sum_{v \in I \setminus I'} m_v\right)/(k'' \cdot B)$, where m_v are sizes of weights associated with nodes and B is the communication bandwidth. Thus, $\mathrm{acc}(I \setminus I', k'')$ should be either the sum or maximum of these two terms, depending on our assumption of interleaving communication with computation (see Appendix C.1).

This modification of the DP increases the running time by a factor of $O(\max(k, \ell))$. The memory usage remains unchanged.

C.3   Accelerator Hierarchies

Throughout the paper we have assumed a homogeneous system with k accelerators and ℓ CPU cores (probably a single machine). To more precisely capture a distributed setting, one can consider a hierarchical collection of accelerators, such as clusters of GPUs connected internally with faster interconnects and externally (i.e. between clusters) with slower connections (or over a network). Such a multi-level model is used in PipeDream [HNP+18]. Now, the cost of transferring data over an edge between two nodes depends on whether these nodes are placed on devices in the same or different clusters (or even on different machines). The main new challenge is knowing which cost should be taken into account.

The DP solution in PipeDream handles this by dynamically computing optimal splits not only for prefixes of the input network (that correspond to our ideals), but for every contiguous segment of the network. We remark that we can use the same method, at a cost of an $O(\mathcal{I})$-factor increase in both memory usage (number of DP states) and running time.

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[8]We treat the CPU-related term similarly.